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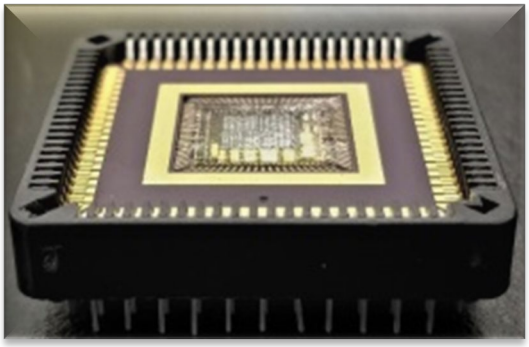
University at Albany, State University of New York
The Ohio State University
SUNY Polytechnic Institute
North Carolina State University

FINAL TECHNICAL REPORT

SMART SiC Power ICs

(Scalable, Manufacturable, and Robust Technology for SiC Power Integrated Circuits)

Award #
DE-AR0001028



Award:	DE-AR0001028
Sponsoring Agency	USDOE, Advanced Research Project Agency-Energy (ARPA-E)
Lead Recipient:	SUNY, University at Albany (Formerly SUNY Polytechnic Institute, Albany)
Project Team Members	Dr. Woongje Sung – University at Albany Dr. Anant Agarwal – OHIO State University Dr. Ayman Fayed – OHIO State University Dr. Bongmook Lee – SUNY Polytechnic Institute
Project Title:	SMART SiC Power ICs (Scalable, Manufacturable, and Robust Technology for SiC Power Integrated Circuits)
Program Director:	Dr. Olga Spahn
Principal Investigator:	Dr. Woongje Sung
Contract Administrator:	Todd Remkus, Associate Director for Award Establishment and Management
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Public Executive Summary

This collaborative project was initiated with the goal of developing Scalable, Manufacturable, and Robust Technology for SiC Power Integrated Circuits (SMART SiC Power ICs). In pursuit of this objective, innovative designs and fabrication processes were implemented, enabling the development of large-scale (>1 cm^2) SiC Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits and high-voltage (400–600 V) lateral power MOSFETs (HV-LDMOS) on 150 mm 4H-SiC substrates. The resulting SMART SiC Power ICs are tailored to support a wide range of applications requiring diverse voltage and power levels, including automotive systems, industrial equipment, electronic data processing, energy harvesting, and power conditioning.

To achieve the proposed 'SMART' technology for SiC ICs, the team focused on 1) the Development of highly scalable CMOS (with high channel mobilities for n-type and p-type MOSFETs), LDMOS (~600V, 10A rated), and IC technologies, 2) Establishment of a manufacturable process baseline in a production-grade-, 150mm, SiC fabrication facility, and 3) Demonstration of SMART SiC ICs.

The project initially comprised of fabricating 5 lots. In lot 1 monolithic integration using a single process was achieved. Here, we were able to successfully accomplish Integrated HV NMOSFET with LV CMOS on N-epi/N+ Substrate. The HV NMOS demonstrated a Breakdown Voltage (BV) more than 600V. Circuit demonstration of CMOS was also another achievement from this lot. In lot 2, priority was in place for isolation and integration. Here we addressed the isolation concerns and integrated the HV NMOS and LV CMOS using the N-epi/P-epi/N+ substrate. Similar to the lot 1, we were able to achieve a BV of 600 V for HV NMOS. Optimized gate oxide process with high channel mobilities, better gate oxide reliability, development of SPICE models, successful ohmic process development, novel wafer area saving design layouts, P+ isolation schemes with channeling implantations and high temperature operational circuits demonstrations are some of the key highlights from lot 1 and lot2. In lot 3, discrete device performances of HV NMOS with a BV ~700V and reliable LV CMOS performances were achieved. Also, novel architectural solutions were successfully implemented to suppress the electric field crowding at the gate oxide for reliable operations. In lot 4, half bridge power driver ICs with a conversion efficiency of (target 90% to 95%) in the 1-5MHz switching frequency range for output power between 25 W to 3 kW have been included in. However, due to the unfortunate events of sudden foundry shutdown (SiCamore Semi) the processing of lot 4 wafers came to a complete stop (January 2024). Arrangements have recently been made to shift the fabrication to another foundry, General Electric Aerospace. The fabrication process now on course (as of December 2024). Characterizations are delayed due to this unfortunate circumstance. The proposed trench architectural-based devices and ICs (lot 5) underwent modifications from the original project proposal. This change was necessitated by limitations in the availability of trench-based processes at commercial production-grade fabrication facilities in the US. Apart from above achievements, a Process Development Kit (PDK) was successfully developed for planar type SiC CMOS/LDMOS.

Acknowledgements

The authors wish to express their sincere gratitude to the Advanced Research Projects Agency-Energy (ARPA-E) for their generous funding and support, which were instrumental in enabling the successful completion of this project. This SMART-IC initiative not only achieved its intended objectives but also contributed significantly to advancing the development of efficient and robust SiC Power ICs, addressing a critical national need.

Special thanks are due to Dr. Isik Kizilyalli, Dr. Olga Spahn, Dr. Eric Carlson, and Dr. Daniel Cunningham of ARPA-E for their steadfast support and dedication, which were pivotal in realizing the shared research goals. The authors also express their heartfelt appreciation to the Co-PIs and their crews: Dr. Anant Agarwal and Dr. Ayman Fayed from The Ohio State University, as well as Dr. Bongmook Lee from SUNY Polytechnic Institute (formerly affiliated with North Carolina State University) who contributed significantly to the success of this project. Their unwavering commitment and expertise were instrumental in accomplishing the research milestones.

Additionally, we would like to acknowledge our fabrication partners, ADI and Sicamore Semi, for their essential contributions. Their expertise and collaboration in providing state-of-the-art fabrication capabilities were critical to achieving the project's research and development milestones.

Accomplishments and Objectives

This award allowed the team to demonstrate several key objectives. The project was primarily aimed to develop a technology platform for SiC-based Integrated Circuits (ICs) tailored for high-power and potentially high-temperature applications, including module process development, process flow definition, discrete device optimization, circuit design and demonstration, packaging and evaluation, and the creation of a Process Design Kit (PDK) for potential users. The actual performance against the stated milestones is summarized here:

Table 1. Key Milestones and Deliverables

Tasks	Milestones and Deliverables
M1.1	**Q1: Go/No-Go: Refine tasks and milestones** Completed (11/30/19). All project teams were in agreement with the present and future targets of the project.
M2.1.1	**Q2: Simulation and process flow design for the planar-type CMOS/ LDMOS/LJBS** Completed (02/29/20). TCAD 2D simulations were conducted to optimize the individual device structure for planar-type CMOS/LDMOS and LJBS. A single process flow was designed to integrate and fabricate the proposed high-voltage and low-voltage mosfets, diodes and other circuits.
M2.1.2	**Q4: Go/No-Go: The 1st lot (Lot 1) fabrication completed and characterized** [Completed Initial due 8/31/20. Revised due: 2/28/21] Due to Fab-out delay (affected by Corona virus pandemic). Subsequent milestone due dates were revised. The fabrication of Lot1 has been completed and the characterization of the Lot1 is complete. The results of the Lateral HV-MOSFET, channel mobilities of NMOS and PMOS, and operation of ring oscillators are reported and presented to the ARPA-E in the Q4 meeting.
M2.1.3	**Q6: The 2nd lot fabrication completed (Lot2) and characterized** [Completed: Initial due 2/28/21 Revised due: 8/31/21]

	The fabrication of Lot2 and the characterization of the Lot2 complete. The results of the Lateral HV-MOSFETs, diodes, test structures, and gate oxide assessment are discussed and reported to ARPA-E in the Q6 meeting and reports.
M2.2.1	**Q10: Simulation and process flow for the trench-type CMOS/ LDMOS/LJBS** [Initial due 2/28/22 Revised due: 8/31/22] (incomplete – obsolete milestone) The proposed trench architectural-based devices and ICs underwent modifications from the original project proposal. This change was necessitated by limitations in the availability of trench-based processes at commercial production-grade fabrication facilities in the US.
M2.2.2	**Q12: The 1st lot of trench devices completed (Lot5) and characterized** [Initial due 8/31/22 Revised due: 2/28/23] (incomplete – obsolete milestone)
M3.1.1	**Q4: High channel mobility for n-ch planar MOSFET demonstrated** [Completed: Initial due 2/28/22 Revised due: 8/31/22 (Pandemic)] NCSU team has demonstrated enhanced mobility (>80 cm2/Vs) with MBE LaO and ALD SiO2. The combination of LaO interfacial passivation layer with the high-quality SiO2 deposited by Atomic Layer Deposition (ALD) effectively removes traps located at SiC/dielectric interface.
M3.1.2	**Q8: High channel mobility for p-ch planar MOSFET demonstrated** [Initial due 8/31/21 Revised due: 02/28/22] (Incomplete – milestone discussed and target revised as the initial mobility target was too high) The second run of p-MOSFET fabrication is complete. There is an enhancement in mobility (78.86%) from the last run, however it is not yet there to meet the milestone.
M3.1.3	**Q12: ALD gate oxide on trench structure evaluated** [Initial due 8/31/22 Revised due: 02/28/23] (Incomplete – obsolete milestone)

M3.2.1	**Q12: Reliability and VT stability for advanced ALD based gate stack evaluated** [Completed: Initial due 8/31/22 Revised due: 02/28/23] NBTI and PBTI were tested and confirmed Vth stability.
M4.1.1	**Q4: SiC CMOS/LDMOS Spice model** [Completed: Initial due 8/31/20 Revised due: 11/30/20] Based on the on-wafer characterizations of Lot1, SPICE models were tweaked to accurately capture the device performances. All the developed SPICE models were presented to the ARPA-E in the Q5 meeting
M4.1.2	**Q5: PDK for planar-type SiC CMOS/LDMOS** [Completed: Initial due 11/30/20 Revised due: 5/31/21] The development of the Process Design Kit (PDK) was completed and was presented to the APRA-E in Q6 report and meeting.
M4.2.1	**Q6: Circuit schematic and layout design of a switched-mode buck converter (IC1)** [Completed: Initial due 2/28/21 Revised due: 8/31/21] The buck converter design was implemented using the SPICE models based on Lot #1 characterizations by OSU.
M4.2.2	**Q8: Circuit schematic and layout design of a half-bridge power driver (IC2)** [Completed: Initial due 8/31/21 Revised due: 2/28/22] The SMART IC team completed this task, and the layout was sent to SiCamore (Foundry).
M4.2.3	**Q10: Circuit schematic and layout design of a high-voltage buck (IC3)** [Completed: Initial due 2/28/22 Revised due: 8/31/22] The SMART IC team has completed this task, and the circuit schematic and layout design were reported in Sections – IV-C of Q11 and Q12 reports. Here, the high voltage buck converter design was implemented using SPICE models based on Lot#2 characterizations.

M4.3.1	**Q9: Go/No-Go: package and characterization of the buck-converter (IC1)** [In Progress: Initial due 11/30/21 Revised due: 05/31/22] The Lot completed the metal 1 process and all the wafers have been sent to SUNY for evaluation. The significant results from the electrical characterizations of the IC1 lot are reported in the reports. The wafers were sent back to SiCamore for further processing of the metal layers. The delay faced in the fabrication process of IC1 at the SiCamore fabrication facility is the major reason that hampered our progress in reaching this milestone. Furthermore, the foundry was shut-down and further processing was halted. The fabrication now continues in a different fab (GE Aerospace) – even though the project has officially ended, SUNY is willing to continue to complete the lot at GE. Results will be reported to Arpa-e when available.
M4.3.2	**Q11: Package and characterization of the half-bridge power driver (IC2)** [In Progress: Initial due 05/31/22 Revised due: 11/30/22] The fabrication of the Lot was started at SiCamore. However, the foundry was shut-down and further processing was halted. The fabrication now continues at GE.
M4.3.3	**Q12: Package and characterization of the high voltage buck converter (IC3)** [In Progress: Initial due 8/31/22 Revised due: 02/28/23] The design was completed, but the fabrication was halted due to shut-down of SiCamore. Fabrication now continues at GE.
M5.1.1	**Q2: Framework of TEA accepted by ARPA-E** [Completed: 2/29/20] The Framework of TEA was drafted and submitted to ARPA-E for review. The framework of TEA focuses on establishing a connection between technical and economic criteria using the story of "Moore's Law for SiC" to develop the case for more functional density and power density at an overall lower system-level cost.
M5.2.1	**Q1: Initial T2M plan and impact sheet drafted** [Completed 12/9/19]

	The initial T2M plan and impact sheet was drafted and submitted to ARPA-E for review. The commercialization trajectory for the SMART SiC Power IC technology involves fab houses of SiC devices incorporating the proposed design process flow into their preexisting portfolio of technologies.
M5.2.2	**Q5: Final T2M plan submitted for ARPA-E acceptance** [Completed: Initial due 11/30/20 Revised due: 5/31/21] The technology to market (T2M) plan was completed and reported in the Q7 report.
M5.3.1	**Q2: IP Strategy** [Completed: 11/4/19] The IP strategy has been drafted and submitted to ARPA-E for review. In summary, the IP landscape pertains to the process recipe for successful fabrication of the integrated high voltage and low voltage SiC devices with desirable characteristics, where the internal semiconductor structure of each SiC device is unique. IP generated will only be known by the fab house.
M5.3.2	**Q4: Analysis of primary markets and competitive analysis** [Completed: Initial due 8/31/20 Revised due: 2/28/21] T2M efforts involved the compilation of a list of industry points of contacts (PoCs) known to the team across a wide range of companies. The SMART SiC Power IC technology summary flyer was sent to PoCs.
M5.4.1	**Q8: Develop of manufacturing capability** [Completed: Initial due 8/31/21 Revised due: 2/28/22] The SMART IC team has completed this task and submitted the report to ARPA-E for review.
M5.5.1	**Q10: Engagement Report** [Completed: Initial due 2/28/22 Revised due: 8/31/22] The engagement report was completed and was reported in Section-V of Q12 report. The report covers the activity towards the next stage of funding, addressing the long-term and near-term market applications, the investment needed to transfer technology, and potential sources of investment.

TCAD simulations were manipulated for development and optimization of the desired SMART-IC devices under different process conditions. Synopsys Sentaurus was employed for all the simulation-based tasks. Appropriate parameter models for Bulk electron

mobility, bulk hole mobility, channel electron mobility, channel mobility degradation, Shockley-Read-Hall (SRH) recombination, impact ionization and interface trap models with relevant coefficient values were manipulated for simulation purposes.

Project Activities

As highlighted in the executive summary, the primary objectives of this project centered on developing highly scalable CMOS technologies with enhanced channel mobilities for both n-type and p-type MOSFETs, along with LDMOS (600V, 10A) and IC technologies. Additionally, the project focused on establishing a manufacturable process baseline in a production-grade 150mm SiC fabrication facility and demonstrating SMART SiC ICs. Here, key highlights should be emphasized. Gate oxidation process was well optimized in which high channel mobilities were achieved for both NMOS and PMOS structures (~20 $cm^2/V{\cdot}s$). Extensive studies were carried out on gate oxide reliability (NBTI, PBTI, Gate Leakage) to develop gate oxide recipes to improve performances along with better reliability. SPICE (Simulation Program with Integrated Circuit Emphasis) Models were successfully developed based on the LV CMOS and HV NMOS data. Ohmic process development focused on achieving better ohmic contacts for N+ and P+ using a single Ni metal process, alongside optimized implant profiles and metal stacks to improve the on-resistance. Furthermore, innovative Edge termination techniques (within the cell and at the periphery) successfully demonstrated better breakdown capabilities. As a result of aforementioned achievements, state of the art performances (better Ron-BV trade-off) were witnessed compared to other reported literature. Also, novel layouts were implemented to save the wafer area and obtain a better yield while maintaining the same current rating (~10A). Additionally, we implemented junction isolation using a deep P+ implant (Al at 380 keV, 2.5 µm) implemented by the novel channeling implantation technique. This also served as an effective and reliable edge termination structure for HV devices. Meanwhile, high-temperature operational circuits were evaluated up to 400°C using a custom measurement setup, employing circuits such as ring oscillators and CMOS inverters. This confirmed that operating frequency over the temperature range is dependent on the peak field effect mobility behavior with temperature. These advancements collectively support the creation of robust and scalable SiC power ICs tailored for diverse applications. In SMART IC lot 3, a novel device architecture was brought in to address some of the issues that was observed in previous lots. This innovative RESURF (Reduced Surface Electric Field) technology ensures the gate is fully shielded from the p-top, rendering it unaffected by the p-top dose and resulting in low leakage during blocking operation. The gate oxide field was significantly suppressed, leading to a substantial reduction in gate-to-source leakage current and, consequently, a decrease in drain-to-source leakage current during blocking mode. Processing of SMART IC lot 4 was halted due to the unfortunate event of the foundry shutdown. The SiCamore Semi foundry at Oregon, USA announced its discontinuation in January, 2024 leading to a complete halt processing of SMART IC lot 4. The team gathered eventually and looked for feasible options to continue the fabrication process. Currently, the wafers are being processed from where it was left off at General Electric's SiC foundry in Niskayuna, NY. During the transition period, Bi-Directional FETs fabricated on lot 3 were characterized.

Project Outputs

A. Journal Articles

- Sundar Babu Isukapati, Hua Zhang, Tianshi Liu, Utsav Gupta, Emran Ashik, Adam J Morgan, Seung Yup Jang, Bongmook Lee, Woongje Sung, Ayman Fayed, Anant K. Agarwal, “Design and experimental demonstration of high-voltage lateral nMOSFETs and high-temperature CMOS ICs, Materials Science in Semiconductor Processing,” Volume 169, 2024, 107921, ISSN 1369-8001, https://doi.org/10.1016/j.mssp.2023.107921.

- Liu, T., Zhang, H., Isukapati, S.B., Ashik, E., Morgan, A.J., Lee, B., Sung, W., Fayed, A., White, M.H. and Agarwal, A.K., 2022. “SPICE Modeling and Circuit Demonstration of a SiC Power IC Technology,” IEEE Journal of the Electron Devices Society.

B. Papers

- S. B. Isukapati, S. Y. Jang and W. Sung, "Enhanced Design Architecture to Suppress Leakage Current of High-Voltage (HV) Lateral nMOSFETs in 4H-SiC," *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hong Kong, 2023, pp. 358-361, doi: 10.1109/ISPSD57135.2023.10147724.

- S. Y. Jang, S. B. Isukapati, D. Kim and W. Sung, "First Demonstration of 600 V 4H-SiC Lateral Bi-Directional Metal-Oxide-Semiconductor Field-Effect Transistor (LBiDMOS)," *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hong Kong, 2023, pp. 5-8, doi: 10.1109/ISPSD57135.2023.10147546.

- Sundar Babu Isukapati, S. Yup Jang, and W. Sung, “Area-Efficient High-Voltage (HV) Lateral MOSFETs for Discrete Device Development and Power IC Integration,” in 2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), Nov. 2022, pp. 122–126. doi: 10.1109/WiPDA56483.2022.9955284.

- Zhang, Hua, Tianshi Liu, Utsav Gupta, Sundar Babu Isukapati, Emran Ashik, Adam J. Morgan, Bongmook Lee, Woongje Sung, Anant K. Agarwal, and Ayman Fayed. “A 600V Half-Bridge Power Stage Fully Integrated with 25V Gate-Drivers in SiC CMOS Technology.” In 2022 IEEE 65th International Midwest Symposium on Circuits and Systems (MWSCAS), 1–4, 2022. https://doi.org/10.1109/MWSCAS54063.2022.9859305.

- Sundar Babu Isukapati, Adam J Morgan, and Woongje Sung. “Edge Termination and Peripheral Designs for SiC High-Voltage (HV) Lateral MOSFETs for Power IC

Technology." In 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 213–16, 2022 https://doi.org/10.1109/ISPSD49238.2022.9813635

- Ashik, Emran K, Sundar Babu Isukapati, Hua Zhang, Tianshi Liu, Utsav Gupta, Adam J Morgan, Veena Misra, et al. "Bias Temperature Instability on SiC N- and p-MOSFETs for High-Temperature CMOS Applications." In 2022 IEEE International Reliability Physics Symposium (IRPS), 3B.4-1-3B.4-8, 2022. https://doi.org/10.1109/IRPS48227.2022.9764565

- Liu, Tianshi, Hua Zhang, Sundar Babu Isukapati, Emaran Ashik, Adam J. Morgan, Bongmook Lee, Woongje Sung, Marvin H. White, Ayman Fayed, and Anant K. Agarwal. "SPICE Modeling and CMOS Circuit Development of a SiC Power IC Technology." In 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 966–69, 2021. https://doi.org/10.1109/MWSCAS47672.2021.9531903

- Sundar Babu Isukapati, Adam J Morgan, Woongje Sung, Hua Zhang, Tianshi Liu, Ayman Fayed, Anant K. Agarwal, Emran Ashik, and Bongmook Lee. "Development of Isolated CMOS and HV MOSFET on an N- Epi/P- Epi/4H-SiC N+ Substrate for Power IC Applications." In 2021 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 118–22, 2021. https://doi.org/10.1109/WiPDA49284.2021.9645134

- Sundar Babu Isukapati, Hua Zhang, Tianshi Liu, Emran Ashik, Bongmook Lee, Adam J Morgan, Woongje Sung, Ayman Fayed, and Anant K. Agarwal. "Monolithic Integration of Lateral HV Power MOSFET with LV CMOS for SiC Power IC Technology." In 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), 267–70, 2021. https://doi.org/10.23919/ISPSD50666.2021.9452235

C. Status Reports

- Quarterly Review Reports submitted to the Arpa-e (Quarter 1 to 19).
- Arpa-e Summit Poster Presentations
- DMEA SBIR Phase I -Manufacturing Platform for High-Temperature CMOS ICs on SiC – Final Report.

D. Media Reports

N/A

E. Invention Disclosures

F. Patent Applications/Issued Patents

U.S. Provisional Patent Application No. 63/451,253, filed Mar. 10, 2023, entitled, "Lateral SIC HV MOSFET Design and Isolation Technique"

(A High Voltage (HV) lateral device is a fundamental component for high voltage power IC (Integrated Circuit). Especially when using 4H-SiC, the maximum power density can be dramatically increased. There have been attempts to demonstrate HV (~200V ~ 1200V) MOSFETs and power diodes. However, the high critical electric field, as the main benefit of using 4H-SiC, could be detrimental to keep a reasonable electric field at the passivation dielectric material, resulting premature breakdown near the surface of semiconductor or within the dielectric material. In this invention, a device architecture to avoid high electric field at the passivation is proposed. As a result, leakage current was reduced and breakdown voltage was improved. In addition to the HV power device with a new architecture described above, it is essential to provide an isolation technique between HV devices and LV (Low Voltage) devices. In this invention, a novel isolation scheme implemented by novel channeling implantation is also proposed.)

G. Licensed Technologies

N/A

H. Networks/Collaborations Fostered

Based on the outcome of this project, the PI has submitted another proposal to Arpa-e (OPEN 2024). The award selection is in process and it is still pending, but the project outcome of this project allowed us to be prepared for more sophisticated applications of CMOS based in SiC.

I. Websites Featuring Project Work Results

https://sunypoly.edu/research/centers-programs/suny-casper/research/smart-sic-power-ics.html

J. Other Products

N/A

K. Awards, Prizes, and Recognition

Best Poster Award –

Sundar Babu Isukapati, Hua Zhang, Tianshi Liu, Emran Ashik, Bongmook Lee, Adam J Morgan, Woongje Sung, Ayman Fayed, and Anant K. Agarwal. "Monolithic Integration of Lateral HV Power MOSFET with LV CMOS for SiC Power IC Technology." In 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), 267–70, 2021. https://doi.org/10.23919/ISPSD50666.2021.9452235

Follow-On Funding

While we were pursuing this project, we were partnered with a SUNY start-up company, NoMIS Power and received an SBIR award from DMEA. This project was to evaluate SiC ICs at high temperatures (up to 450 deg. C).