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LANSCE MODERNIZATION PROJECT

MEBT Chopper System: System Design Document (SDD)

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Component Overview

The Medium Energy Beam Transport (MEBT) chopper removes unwanted beam bunches by deflecting them to a targer from a bunched beam transported through the MEBT from RFQ to the Drift-Tube Linac (DTL) entrance. The unchopped bunches propagate through the MEBT to DTL, while the deflected bunches are deposited on a target downstream of chopper. The chopper system consists of a deflecting structure, where the beam-deflecting fields are created, and a pulse generator (pulser) that feeds this structure with voltage pulses having the required time pattern. Ideally, the system should turn deflection on and off in the time interval between the bunches to prevent partially chopped / deflected bunches. This usually requires traveling slow-wave chopper structures where the field propagates with the same velocity as the beam, as illustrated in Fig. 1 [1].

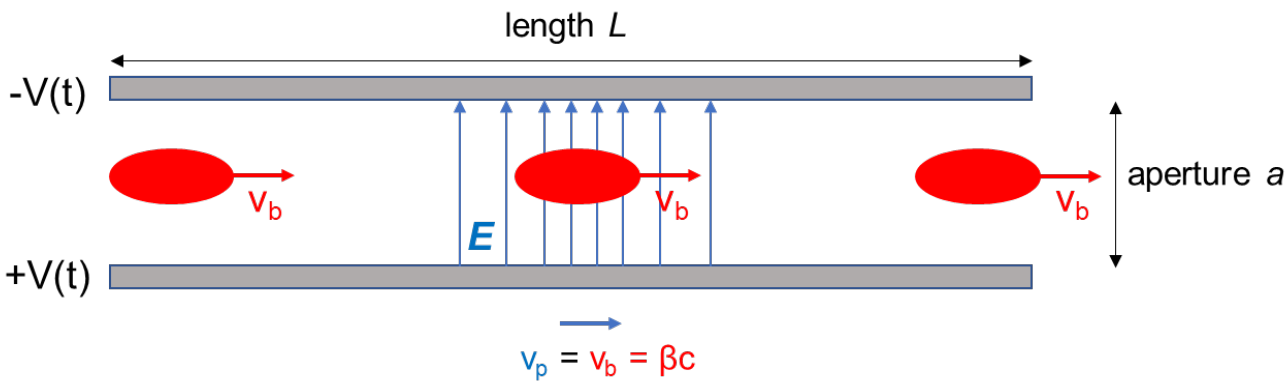


Figure 1: Traveling-wave chopper structure: the region of deflecting electric field travels along the structure with the same velocity as the beam.

The chopper design requirements come from the MEBT beam dynamics design. They include the required transverse kick angle delivered by the chopper to deflected bunches, the aperture available for the beam passing through the chopper, and the maximum chopper length along the beam path, see in Fig. 1. The bunch separation, plus jitter in the bunch arrival time, define the rise and fall times of the chopper deflecting field. The accelerator operation defines the chopping time pattern and which bunches needs to be chopped. From these main parameters, the required amplitude and timing pattern of the voltage provided by the pulse generator are derived. The voltage pulses applied to the two plates in the chopper structure have the same pulse shape but opposite signs, as shown in Fig. 1.

Pulser. Solid-state electronics offer stable and reliable switching performance, making it preferable to older vacuum tubes. High power Silicon Carbide (SiC) and Gallium Nitride (GaN) field effect transistor (FET) technology continues to advance in recent years. However, FET device switching performance is constrained by the physical topology and manufacturing process which creates a complex tradeoff matrix when selecting for devices with high voltage,

fast switching, at high speeds. The burst pulse frequency and power handling required by the LAMP MEBT chopper pulse create a challenging requirement when considering available solid-state technology as seen in Fig. 2.

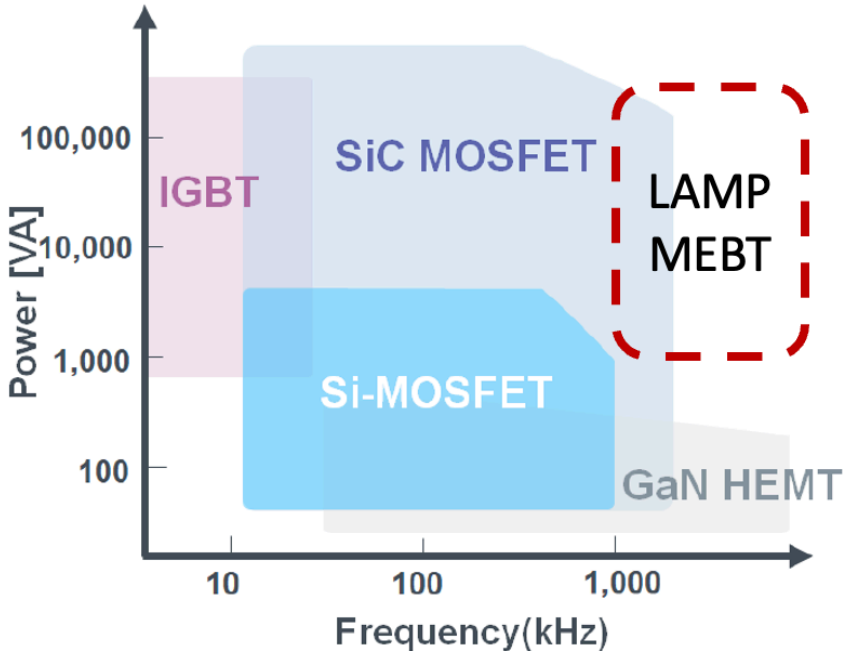


Figure 2: The LAMP MEBT pulser requirements in relation to currently available solid-state electronics [6].

Recent generation SiCFET technology blocks high voltages up to and beyond 2kV, and handles significant drain current, but has large input capacitance that is difficult to charge and discharge rapidly. GaNFETs can typically block around 600V, cannot handle significant drain current, but can switch far more rapidly due to lower capacitance. The higher-power density in SiCFETs devices mostly constrains the topology to transistor outline style packages which have large parasitic lead inductance compared to the typical surface mount style GaNFET chips.

Requirements

The requirements for the LAMP MEBT chopper system are determined mainly by the MEBT beam dynamics design. The main requirements are listed in Table 1 and pulser requirements are listed in Table 2.

Table 1. Main Requirements for the LAMP MEBT Chopper.

Identifier	**Requirement**	**How met**
Deflection angle α	Should be sufficient to deflect the chopped bunches to the target (dump)	Proper beam dynamics design
Chopper field rise / fall time t_c	Deflecting field rise / fall time should be below bunch time separation.	Both chopper structure (s) and pulse generator (p) contribute, which gives $t_c = (t_s^2 + t_p^2)^{1/2}$.
Chopper length L	Should be sufficient to provide the required deflecion while still allowing beam passage	Proper beam dynamics design
Chopper aperture a	Should allow beam to pass without scraping	Proper beam dynamics design

Table 2. Chopper Pulser Requirements

Requirement	Description
Flat Top	Must remain stable within 95% to 120% of 1900 V for full duration of $N \times 5$ ns.
Flat Bottom (Ground)	Must remain stable for at least 2 ns within +/- 1% of Flat Top voltage 0V / GND.
Rise	Must rise from "Flat Bottom" voltage to "Flat Top" Voltage within 3 ns.
Fall	Must fall from "Flat Top" to "Flat Bottom" within 3 ns.
Load Structure	A 200-Ω slow wave structure is proposed to reduce current
Switching Frequency	During 625 μs bursts, which occur every 8.3 ms, the pulser will operate at an approximate frequency of 1.12 MHz
Cooling	The pulser shall operate at an elevation of 7500' (2300 m)

Relevant Parameters

Two well-defined parameters for the LAMP MEBT chopper are the beam energy in MEBT (3 MeV) and the bunch separation of 4.97 ns, which follows from bunch repetition rate of 201.25 MHz. Table 3 lists two sets of parameters: one from the preliminary design outlined in Ref. [2], the other is from the latest iteration of the LAMP conceptual MEBT design [11].

Table 3. Relevant Parameters of the LAMP MEBT Chopper.

Parameter	**Value, units**	**Design**
Deflection angle α	1.14° / 1.16°	Reference [2] / [11]
Chopper length L	36 cm / 55 cm	Reference [2] / [11]
Chopper aperture a	2 cm / 1.8 cm	Reference [2] / [11]
Chopper field rise / fall time t_c	2 ns / 3 ns	Reference [2] / [11]
Pulse repetition frequency	0.56-16.77 MHz*	In bursts, within macro-pulses of 625 µs repeated at 100 Hz

* Typical operation frequency 1.12 MHz: two pulses 5-15 ns separated by 5 ns, repeated at 0.56 MHz (MPEG).

Other parameters of the chopper system are derived based on the main parameters. The deflection angle α is related to the other chopper parameters as follows:

$$\alpha \cong \frac{q}{mc^2\beta^2\gamma}\frac{\eta \Delta V L}{a} \cong \frac{q}{2W}\frac{V_{eff}L}{a}, \quad (1)$$

where q and m are the charge and mass of beam particles (protons or H^-), $\beta = v/c$ is the beam velocity v in units of speed of light c, $\gamma = (1-\beta^2)^{-1/2}$, η is the structure efficiency as defined in [1], ΔV is the voltage between two deflecting

electrodes in the structure, and $V_{\text{eff}} = \eta V$. It is clear from Eq. (1) that choices of L, a, and α from beam dynamics will define the required voltage ΔV to be delivered by the pulse generator. The additional restriction on the pulse rise / fall times and pulse repetition rate can make the pulse generator design challenging, especially if ΔV is too high.

Pulser Parameters.

Figure 3 shows a MOSFET circuit model and the inherent parasitic capacitances which determine the device switching speed and losses.

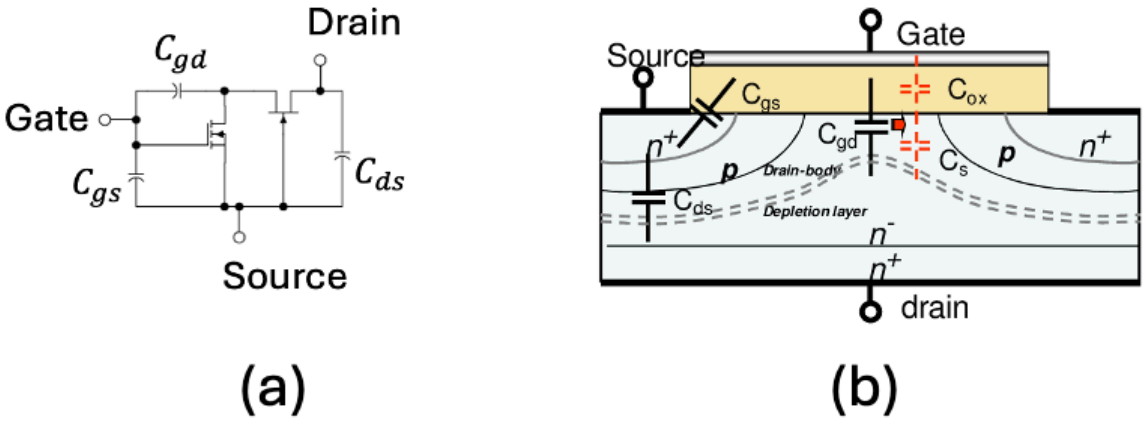


Figure 3. The parasitic capacitance in a MOSFET shown as (a) circuit model (b) physical structure.

In Fig. 3, there are two parasitic input capacitors are C_{gs} and C_{gd}, which sum as C_{iss}. For a FET to 'switch on' and conduct, a gate driver must supply a total amount of charge Q_g to fully charge C_{iss} [6]. During 'switch off', C_{gs} and C_{ds} (which sum as C_{oss}) must discharge. A gate driver must remove a total amount of charge Q_{oss} to fully discharge C_{oss} and turn the FET off [6]. Therefore, fast on/off switching of FET devices heavily depends on the ability of (1) a gate driver to supply Q_g and remove Q_{oss} and (2) the value of Q_g and Q_{oss} which must be transported. Low Q_g, Q_{oss} devices with high blocking voltage is limited by the physical structure and materials of the FET device.

Equations (2) and (3) estimate the fastest possible turn on and turn off times for ideal situations when no other parasitic losses are present.

$$t_{rise} \geq \frac{Q_g}{I_{source}} \tag{2}$$

$$t_{fall} \geq \frac{Qoss}{I_{sink}} \tag{3}$$

Another competing tradeoff space is found at the intersection of input capacitance and drain current handling capability. Faster chips again have less metallization and parasitic capacitance on which directly translates into a weaker structure which cannot handle significant drain current. Further complicating the situation is that high-speed switching introduces losses in the form of heat which must be dissipated to maintain device integrity and performance. During fast switching the user must be aware of heat generated by switching loss, P_{sw}, and loss due to discharge of output capacitance, P_{oss}. Equations for these losses are shown below in (4) and (5).

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_D \times \left(t_R + t_f\right) \times f_{SW} \tag{4}$$

$$P_{OSS} = \frac{1}{2} C_{OSS} \times V_{DS}^2 \times f_{SW} \tag{5}$$

In Eq. (4) V_{IN} is the voltage blocked by a single FET. I_D is the drain current. $t_R + t_f$ is the sum of the rise and fall times. Lastly, f_{SW} is the switching frequency. In Eq. (5) V_{DS} is the voltage blocked by a single FET. f_{SW} is the switching frequency. C_{oss} is the output capacitance, which varies during the switching off, but can be estimated as twice the datasheet value when $V_{DS} = 400$ V.

Design Decisions

Chopper structure.

The required short rise and fall times of the chopper deflecting field can be achieved using traveling-wave chopper structures where the field pulse region propagates along the structure with the same velocity as the beam, as shown in Fig. 1. Fast traveling-wave structures for beam choppers have been implemented in many accelerators, for example, at LANSCE, SNS, CERN, and FNAL, see in [1, 3]. There are various ways to make a slow-wave structure, and it is important to choose a practical design that can be fabricated using established technologies. In Ref. [1], two versions of traveling-wave structures that satisfy the LAMP requirements [2] were developed using 3-D modeling with CST Studio [4]. Both are based on meander-folded 50-Ω line on top of a solid high-purity alumina substrate deposited on a grounded metal plate. The first, a simple meander (S) shown in Fig. 4, provides the field rise / fall time of about 2.5 ns. A faster structure A [1] provides the field rise / fall time of about 1.5 ns. Compared to S, this structure contains grounded separators in substrate cuts between the strip segments to reduce strip-to-strip coupling (see the picture in Table 4). It makes the structure faster but reduces its efficiency.

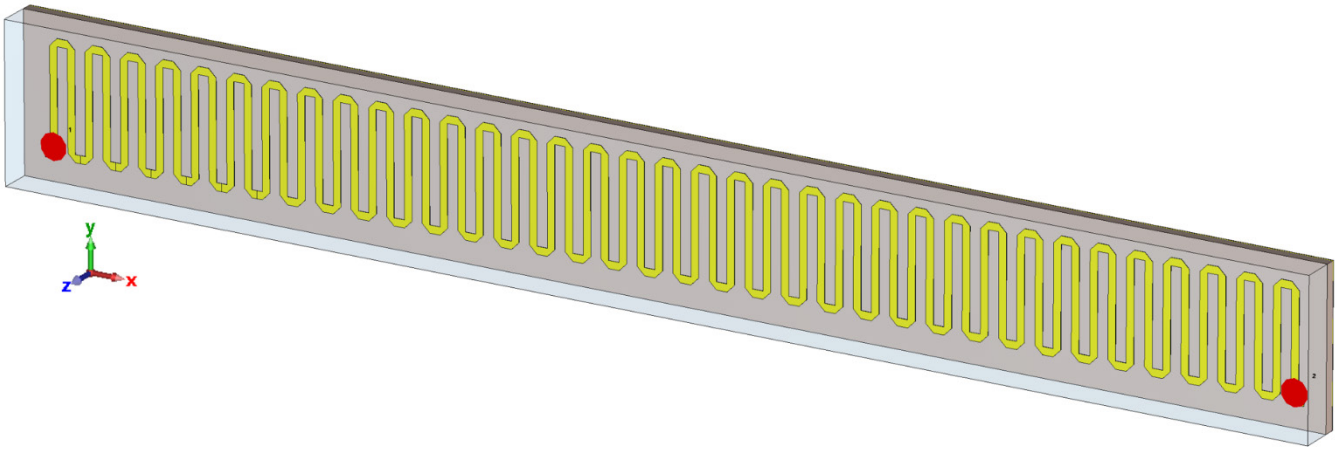
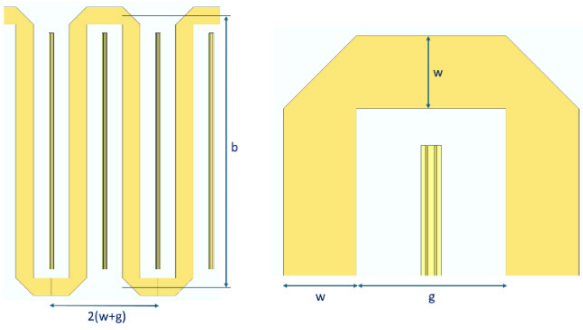


Figure 4: LAMP MEBT chopper structure S (one plate of two): simple 35-cm meander-folded 50-Ω line on solid alumina substrate. Metal is shown in copper color, substrate in gray, and vacuum volume is transparent light blue.

In both structures, the beam velocity $\beta = 0.08$, structure length $L = 35$ cm (/ 55 cm for design [11]), aperture $a = 1.8$ cm, meander period $p = 1$ cm, alumina substrate thickness is 3 mm, and the stripline metal thickness is 0.1 mm. The structure parameters are listed in Table 4 (for MEBT designs [2] / [11]); for more details, see Ref. [1].

Table 4. Parameters of MEBT Chopper Structures.

Parameter	**S**	**A**	**Definition of some geometrical parameters**
Meander pattern width b, mm	29.1	25.41	Meander period $p = 2(w+g)$ 
Stripline metal width w, mm	2.1	1.64	
Substrate dielectric constant	9.9	9.7	
Field rise-fall time, ns	~2.5	~1.5	
Structure efficiency η	0.822	0.581	
Required pulser voltage V_p, kV	±3.77 / ±2.43	±5.34 / ±3.44	

The required voltages from pulse generators to feed the structures above for design [2] are 3.8 kV (S) and 5.3 kV (A). Combined with the required short rise and fall times, below 3 ns, and fast pulse repetition rates up to 5.6 MHz, it makes the pulser requirements very challenging. The required voltages for design [11] are 2.4 kV (S) and 3.4 kV (A), somewhat more relaxed.

One possible way to address the pulser challenges is to adjust the MEBT design aiming to achieve one or more of the following features: (a) reduced deflection angle; (b) increased chopper length; and (c) reduced aperture. All these changes will reduce the required voltage, see in Eq. (1); this is done in design [11]. Note that both structures above are rather narrow (width below 3 cm) and can be placed inside quadrupoles like it was done in the Linac4 at CERN.

Another possible way to address this challenge was developed at FNAL. Their fast chopper system [3, 8] uses a traveling-wave dual-helix structure with 200-Ω impedance to deflect 2.1-MeV ($\beta = 0.067$) beam, see in Fig. 5.

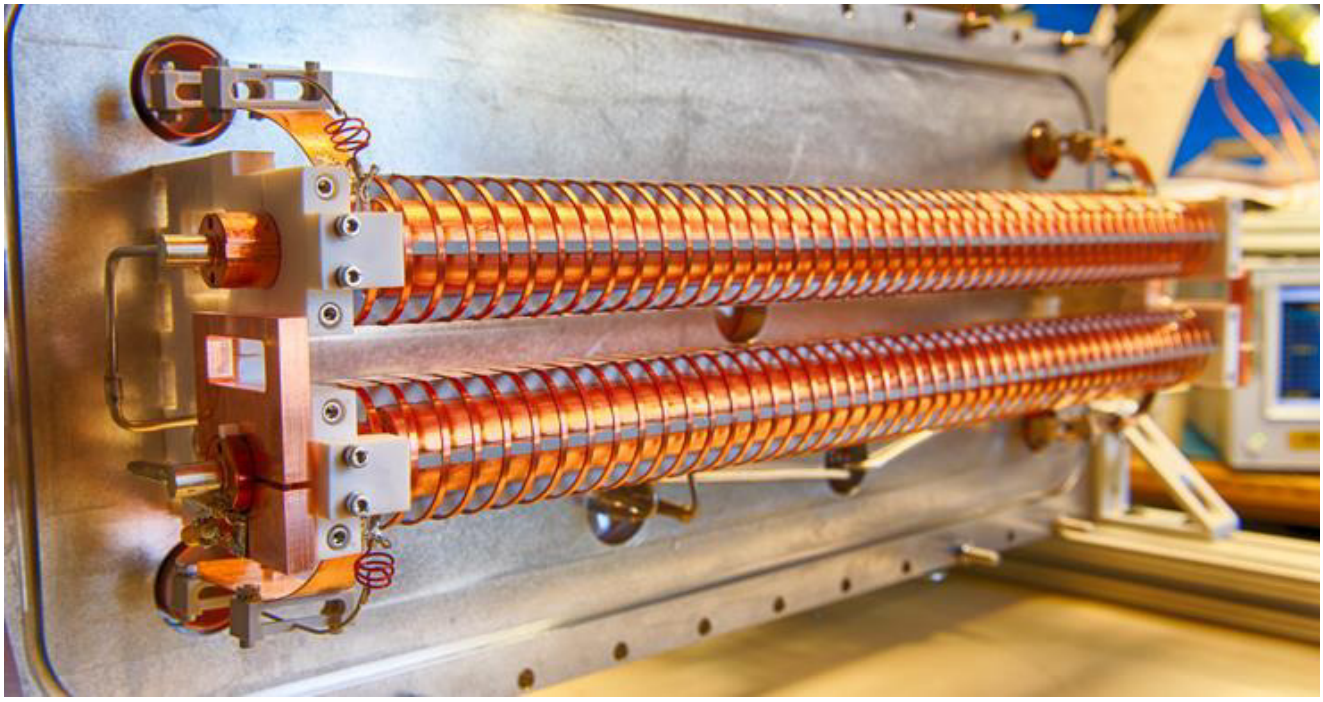


Figure 5: FNAL MEBT chopper dual-helix structure with 200-Ω impedance. Copper plates on the opposite sides from the beam path are attached to the helical windings around grounded copper tubes.

The higher structure impedance reduces the required currents through GaN FETs. Putting 4 FETs in series allows to achieve high pulse repetition rates up to 44 MHz, though at the lower total voltage of 0.5 kV [3, 8] with rise / fall times of about 4 ns. The other structure parameters – smaller kick angle $\alpha = 0.42°$, length $L = 50$ cm, and smaller aperture $a = 1.6$ cm – will need to be adjusted for LAMP MEBT requirements. The FNAL PIP-II MEBT employs two chopper systems to provide the beam deflection required by the MEBT design. The structure efficiency is not quoted and should be evaluated with CST modeling for LAMP parameters. Using Eq. (1) to estimate, the system efficiency is very high, $\eta = 0.996$.

The third option is to develop strip-to-coax helical chopper structures like the existing LANSCE chopper at 750 keV ($\beta = 0.04$) [5]. The structure parameters can be adjusted to the LAMP MEBT requirements. From this design we expect fast rise / fall times of about 2 ns with good structure efficiency.

Based on the available information and simulation results, the dual-helix 200-Ω FNAL chopper structure with parameters adjusted for the LAMP MEBT presents the solution with the highest readiness and lowest risk, mainly because the matching pulser system with a very high rep rate was already demonstrated at FNAL.

Pulse generator.

Based on the available devices and limits, the proposed solution for the LAMP MEBT chopper pulser is a device based on the FNAL PIP-II 2.1-MeV MEBT kicker topology. The FNAL kicker system consists of two simultaneously triggered pulsers of $\pm$ 500 V operating up to 44 MHz on a helical 200 Ω load. Each pulser consists of four GaNFET devices in series.

However, there are three critical areas where the LAMP MEBT chopper must improve upon the FNAL system.

1. The LAMP MEBT chopper demands a faster rise / fall than FNAL operates.
2. The LAMP MEBT pulser voltage is ~4x larger than the FNAL pulser voltage.
3. The LAMP MEBT pulser demands 25% altitude cooling derating compared to FNAL.

The FNAL chopper rise times reach 2 ns, but the fall times are around 4 ns. For the LAMP MEBT chopper the voltage is larger, and both rise and fall must occur in under 3 ns, including ripple. No available GaNFET transistors can block the LAMP full pulser voltage, therefore simultaneous triggering of GaNFETs is critical for both power handling as well as system stability. Whereas in the FNAL kicker, each GaNFET can block the full pulser voltage and the transistors are in series just for power handling. Advances in GaNFET technology will assist in meeting the requirements, especially on the cooling derating, but the combination of these improvements is novel.

The proposed LAMP MEBT chopper pulser topology is shown in Fig. 6. The pulser is composed of four low Q_g GaNFET devices which operate in series such that the drain current will be the same in each device. Each GaNFET will switch about 475 V, with the full stack supporting 1900 V. With a high efficiency (>90%), 200-Ω chopper slow-wave structure the drain current should not exceed 10 A.

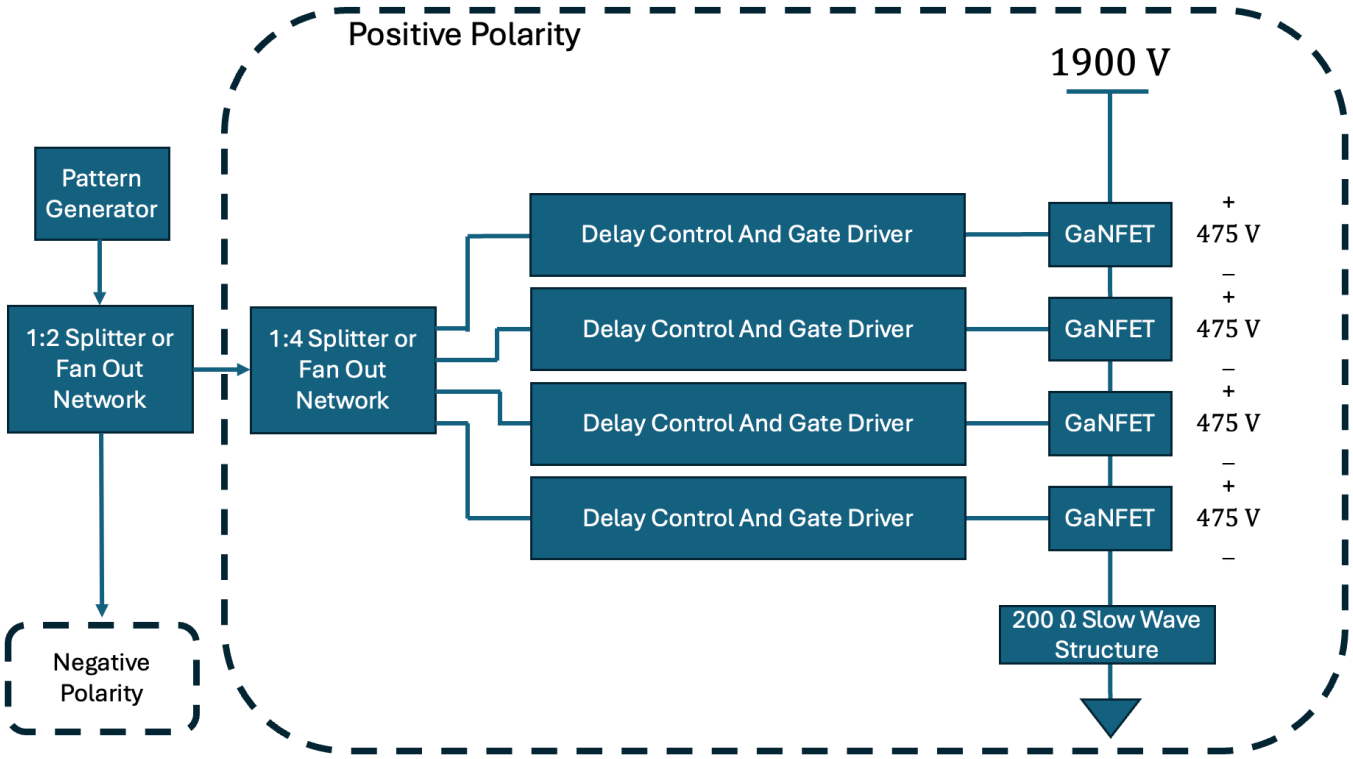


Figure 6. Proposed topology for the LAMP MEBT pulse modulator.

The MEBT physics requires producing two pulses to pass through WNR bunches every 1.8 µs during 625 µs bursts. Although there will be rest time between bursts, this is equivalent to pulsing over 1 MHz and will create a heat

backlog on the chip. However, this is less than the switching speeds (44 MHz) at FNAL, which bursts for similar durations. Therefore, compared to FNAL, the LAMP MEBT solution must have a higher V_{DS} per FET, but f_{SW} is 40x lower. Thus, as shown in equation (4), the power loss for the LAMP solution is dominated by V_{DS} and I_D whereas the FNAL loss is primarily due to the f_{SW} term.

The FNAL kicker used a GaNSystem transistor GS66502B, which could be considered a 3rd generation GaN transistor. The proposed GaNFET for the LAMP MEBT is the Infineon IGLD65R140D2, a 5th generation chip, which has low Q_g but can handle more current than the GS66502B. Newer chips such as IGLD65R140D2 have a similar C_{OSS} as GS66502B but can handle larger drain current.

Gate drive devices which can deliver large currents are limited by available technology and by maximum FET device limits. Existing integrated circuits such as the popular TI LMG 1020 (used in the FNAL kicker) can deliver 7 amps to turn on and 5 amps to turn off [7-8]. Custom gate drive circuits using discrete components produce more current but increase complexity and parasitic losses [9]. All gate drivers are further limited by manufacturer specifications for maximum allowable voltage across the gate to source. The IGLD65R140D2 has a $Q_g = 1.8$ nC and $Q_{oss} = 22$ nC. The IGLD65R140D2 driven by LMG1020 yields a rise/fall under 3 ns based on equation (2) and (3).

There are parallel paths to address challenges for the MEBT chopper pulse generator. First, single SiCFET "gate boosting" exhibits turn on times in the 2-ns range with a very simple topology [9-10]. Although the pulser complexity is significantly reduced, the longevity of such pulsers is unknown and the turn-off time is challenging.

Another possible way to address the pulser challenges is to adjust the MEBT design aiming to achieve one or more of the following features: (a) reduced deflection angle; (b) increased chopper length; and (c) reduced aperture. All these changes will reduce the required voltage, see in Eq. (1).

The pulse generators and their supporting equipment are placed outside the chopper box and connected to the chopper plates by cables or vacuum passthroughs that penetrate the box. For example, red dotes in Fig. 4 indicate the cable connections to the chopper structure through the ground plate and substrate.

Other systems.

Mechanical.

The chopper plates must be placed in an enclosure that is connected to the MEBT beam pipes on both ends. Each plate is supported / suspended on both ends to allow alignment within the box and tilt if needed. The chopper plates need to be protected from stray beam particles by collimators that restrict the chopper entrance aperture (Mo plates). The box should be vacuum-tight and allow penetrations for electrical connectors from the pulse generators to the structure plates. An additional element of the chopper system is the absorber target that absorbs deflected beam particles. The power deposited on the target can be a few kW, so the target needs to be water-cooled.

Several updates will be made from the LANSCE chopper enclosure to reduce leaks. The enclosure will feature conflat flanges to minimize future leaks and avoid o-ring gas diffusion problems. The many electrical, mechanical motion, and water feedthroughs will be specified with metallic seals whenever possible. The up and downstream flanges will be Quick Conflat for a narrow, low-profile metal-sealed joint. One or two 6-inch ID pumping ports will extend from the bottom of the chopper enclosure and connect to vacuum pump(s). The vacuum required is 5×10^{-5} Torr.

The mechanical support of the chopper will be designed to allow fine adjustment in all six degrees of freedom for precise alignment. Additional mechanical work to support the pulser enclosure, load, and related electronics will also be required.

For the high impedance structure, commercial-off-the-shelf options are not readily available. Custom passthroughs for high voltage pulse into the vacuum environment for the chopper structure must be designed. During the pulse burst durations, FET pulsing is likely to exceed manufacturer guidance, leading to heating. Based on FNAL experience and current calculations, it is expected that the LAMP MEBT chopper electronics enclosure will need forced air cooling, or possibly water cooling.

Since the beam energy will be nearly 3MeV at the MEBT chopper pulser electronics will require additional protection from radiation. This can be a mechanical structure which directly shields the pulser. An alternative is custom fabrication of high impedance (200 Ω), low-dispersion transmission lines which can handle voltages to 3kV.

Controls.

The MEBT chopper needs to be synchronized with the accelerator timing system. As such, chopper pattern pulses should only be sent to the MEBT chopper pulser system during the associated beam gate, which is expected to be MPEG. The fine time structure of the MEBT chopper pattern pulses should be synchronized with the LEBT chopper's MPEG pulses and the Low Frequency Buncher. As the expected shape of the MEBT chopper pattern is a rapid double pulse with on time of 5-10 ns, off time of ~5 ns, and on time of 5-10 ns, with the intention for the center to pass micropulses, the center of this structure should be locked up with the timing of the WNR micropulses, see Fig. 7. Adjustments to any of the three possible widths of the MEBT chopper pattern should be made with the center remaining locked up to ease tuning. All synchronization will be handled by the controls interface, with input from LLRF, which will provide the Low Frequency Buncher RF reference.

Due to combinations of beam transit time from LEBT to MEBT choppers, insertion delays through the MEBT chopper pulser equipment and various cable delays, considerations should be made for a phase shift control of the MEBT chopper pattern of up to the WNR micropulse period, typically 1.8 μs. During tune up, the operations team would need to phase shift the MEBT chopper pattern through a full 1.8 μs and watch for a downstream current monitor on a stripchart to dip twice in MPEG current as MEBT pattern passes through the static WNR micropulses. The optimum MEBT chopper pattern phase would be whichever phase command corresponds to the center of this double dip in current on the stripchart.

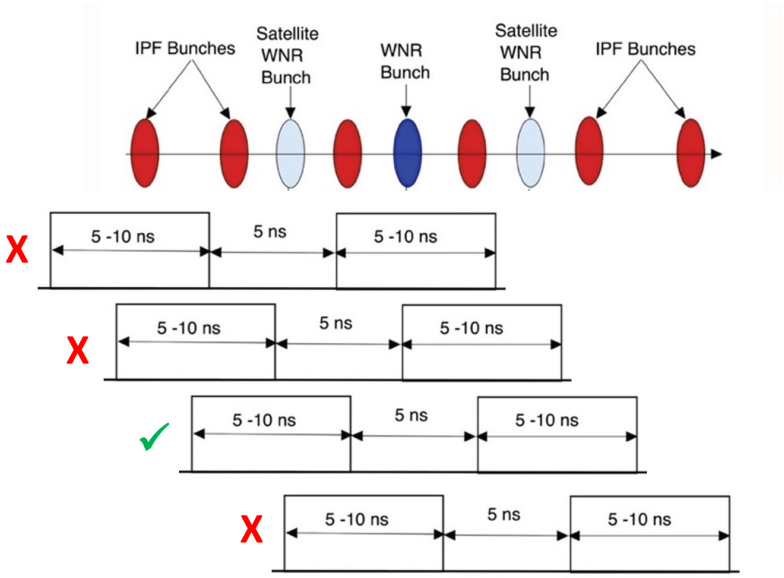


Figure 7: Diagram showcasing how tuning MEBT chopper timing could be tuned, holding upstream chopper timing static, the phase of the MEBT chopper pattern is shifted until the WNR bunch lies directly between the two MEBT chopper pulses.

Readbacks and commands for the chopper pulser and chopper plates shall be provided to the extent necessary to ensure ease of operations.

Protective systems.

It is assumed the MEBT chopper will operate with similar command and return signals of the LEBT chopper. It is also assumed the requirement will be to monitor those signals in a similar way to the LEBT chopper. If those are valid assumptions, the chopper pattern fault device needs to observe the commanded pattern and compare it against

what was chopped. Since rise and fall times are in the single digit ns range, the device should have on the order of 1 ns resolution. As a protective device, this resolution must be realized in hardware, as opposed to ADC digitization of the signals. Allowable tolerances need to be defined and adhered to in the design.

Chopper pattern should be transmitted directly from pattern generator to pulse generator through a modern high speed data link such as LVDS or CML. The legacy pattern fault device is a feed-through, where the digital pattern is converted to fiber optic, transmitted to the pulse generator located far away, then converted back to a digital signal. This design topology introduces variability and adds multiple points of failure and needless error.

All chopper electronics (pattern fault device, pattern generator, and pulse generator) must be mounted in close proximity. This will greatly reduce errors and variability from long distance signal degradation. Ideally all electronics in one RF shielded rack to protect against EMI from the actual chopping. Shielding is critical to precision.

Currently, the chopper pattern fault device outputs a pattern fault and high voltage fault to Fast Protect. Other inputs to Fast Protect include a chopper timing fault (based off gates from IC), chopper guard ring current (from IC), and chopper guard ring self-test (from IC). With the new design, new or differently named inputs to Fast Protect may be determined, but they should maintain the rigor of protection provided by the 5 current inputs.

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