High-Current (390 A) Large Area Vertical GaN PN Diodes with 1600 V Breakdown

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***Abstract*—Due to defects present in gallium nitride (GaN) epitaxial layers, the development of large area devices that are capable of > 100 A current conduction and low leakage breakdown has been challenging. In this work, we will discuss recent efforts to utilize metallic interconnects to allow for the paralleling of vertical GaN diodes that achieve significant pulsed forward conduction while maintaining a low leakage, high voltage breakdown. Forward pulsed conduction of 390 A was achieved for a 13.85 mm^2 vertical GaN PN diode with a 1600 V reverse breakdown.**

Keywords—Gallium Nitride, vertical PN diode, power device, high-current

I. Introduction

While relatively high voltage capabilities of vertical GaN devices have been demonstrated [1, 2], there continues to be challenges in obtaining high current devices. Primarily, the defects present in the epitaxial growth of GaN have resulted in very poor yield when attempting to fabricate devices capable of 100's of amps of current conduction. Previous demonstrations of large area devices have reported up to 400 A pulsed operation for a 16 mm^2 700 V breakdown PN diode device [3]. Isik *et al.* clearly demonstrated the potential of high current GaN devices, however, there have been few reports since, in terms of absolute current. Several published vertical GaN results still rely on relatively small area devices and report out exceptional current densities. In this work we discuss the implications of creating an interconnected device on design and performance through TCAD simulations and report on a method to pre-screen arrays of vertical GaN devices and subsequently create a custom interconnect mask that allows for the parallelization of multiple devices. This allows us to achieve both high current and high breakdown in a vertical GaN PN diode.

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II. Device Modeling

Before attempting to process high-current devices using an interconnected approach, we had to understand how to manage the electric field over the isolation trench. This would create a region where there is a thin dielectric material directly over our n-GaN drift region, essentially resulting in a metal-oxide-semiconductor-capacitor (MOSCAP). One potential solution would be to increase the thickness of the dielectric so that we are well below the critical field during our anticipated blocking voltage. However, for a 1600 V device using SiN, this would require us to double the thickness of our standard passivation from 2 µm to 4 µm to maintain a 4 MV/cm planar electric field in the SiN. An example of this concept is illustrated in Figure 1.

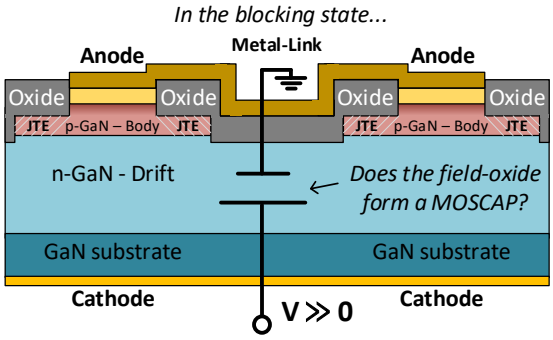

Figure 1: Illustration of how an interconnect metal over an isolation trench may form a MOSCAP.

To better understand the implications of the interconnect design, a TCAD model was developed. Relevant model parameters can be found in our prior work [4, 5]. To verify our initial assumption, we first simulated a case where each device was independently isolated. That is to say that there was no continuous isolation trench between connected devices and the top p-type layer existed between the isolation trenches. The simulation was run until breakdown occurred at 1634 V. As seen in Figure 2, this resulted in a peak electric field of 8.4 MV/cm in the SiN dielectric, which would most likely result in a pre-mature catastrophic breakdown. However, by creating a

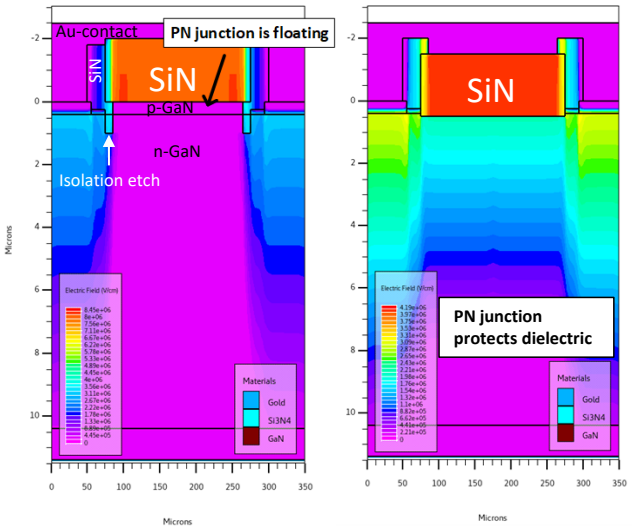

Figure 2: TCAD simulations of a 1600 V PN diode with and without a continues isolation etch between interconnected devices. (left) The simulated devices contain individual isolation trenches resulting in an electric field of 8.4 MV/cm in the SiN during a 1634 V breakdown. (right) The device isolation is connected with a 500 nm etch, resulting a the PN junction partially protecting the SiN above the isolation trench. Electric field scale bars are not the same.

continuous isolation etch between each interconnected device, it was shown from the TCAD simulations that even a 500 nm etch (Figure 2) between devices would result in the PN junction partially protecting the SiN. This is possible because the underlying n-drift region between devices is not directly isolated as a PN junction, rather can aid in spreading out the electric field between connected devices. We further explored how the etch dept impacted the resulting peak electric field in the SiN. The peak field was found to increase linearly, with the etch depth. Figure 3 contains the peak electric field results from four simulations that vary the etch depth. We concluded that a 2 µm etch would result in a 5.6 MV/cm electric field and place us outside of our safe operating region of 4-5 MV/cm. Based on the simulated results, it was determined that a 1 µm continuous etch would be sufficient to protect the 2 µm SiN passivation layer.

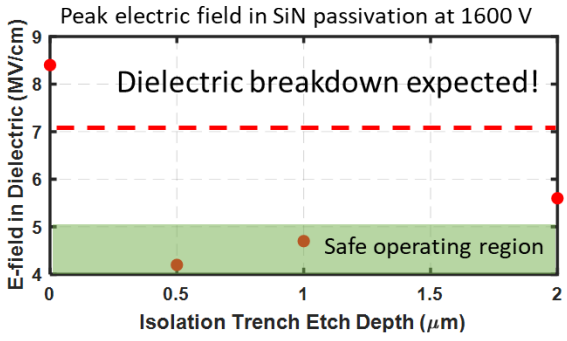

Figure 3: Plot of peak electric field in the SiN vs isolation trench etch depth for a continuous etch between connected devices.

III. Growth and Fabrication

Epitaxial growth of the GaN PN diode was performed via MOCVD in a Taiyo Nippon Sanso Corporation SR4000HT reactor. The growth was performed on a commercially available hydride vapor phase epitaxy (HVPE)-grown laser diode grade 2" GaN substrate with a nominal thickness of 400 µm. The epitaxial structure consisted of a 15 nm p^{++} contact GaN layer (Mg ~ 2 x 10^{18} cm^{-3}), 85 nm p^{+} GaN (Mg ~ 3 x 10^{19} cm^{-3}), 400 nm p^{-} GaN (Mg ~ 1 x 10^{18} cm^{-3}), and a 12 µm n-type (Si ~ 5 x 10^{15} cm^{-3}) drift layer. On device capacitance-voltage measurements verified the carrier concentration in the drift layer. The epitaxial layers were processed into vertical PN diodes using standard lithography techniques. Our junction termination extensions (JTE) followed a similar four-zone design discussed in detail in our previous work [1]. A cross-sectional schematic of the device layout is shown in Figure 4.

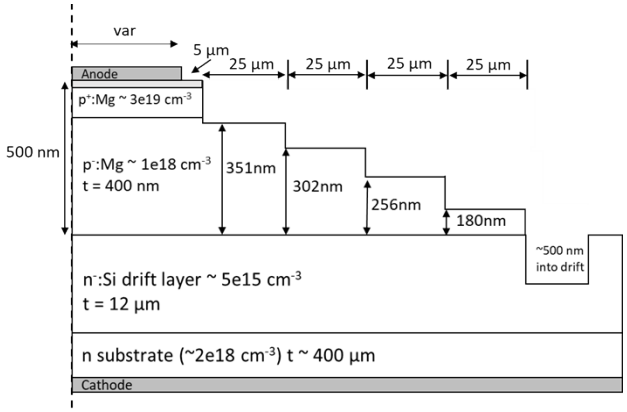

Figure 4: Axisymmetric schematic of the vertical PN diode with a four-zone step-etched JTE.

A full 2" wafer was processed to create four distinct 8 mm x 8 mm cells with varying anode areas of 0. 24 mm^2, 0.48 mm^2, 1.04 mm^2, and 2.77 mm^2. The p-anode contact was deposited via e-beam evaporation and consisted of Pd (20 nm), Au (320 nm), Ti (20 nm), Au (500 nm). A bi-layer passivation of atomic layer deposited Al_2O_3 (100 nm) and PECVD SiN (2 µm) was used. All the devices were then screened and those found to pass our yield criteria of < 1µA/cm^2 at a V_R = 1600 V and a visual inspection of forward IV's were connected within their respective cells with an additional Ti (20 nm) and Au (500 nm) metal deposition that bridged the devices over the bi-layer passivation.

IV. Results and Discussion

The completed wafer after preliminary screening and interconnection is shown in Figure 5. While multiple cells successfully maintained a low leakage and 1600 V breakdown after the interconnection, it was found that the best performing devices generally consisted of those with the 2.77 mm^2 anode areas. The 8 mm x 8 mm cells were then diced out and packaged in TO 254 packages. Twenty 1 x 3 mil Au ribbon bonds were used for the anode contact. Figure 6 shows three of the completed, packaged devices corresponding to different anode contacts. The total effective anode area is displayed on the top of each device image.

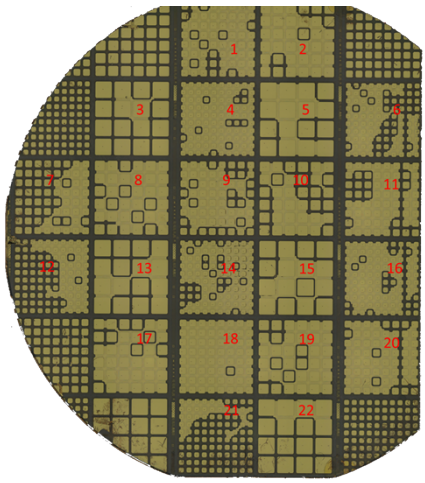

Figure 5: Quad cell array wafer with interconnect metallization. Four cells on the right were diced off prior to metallization.

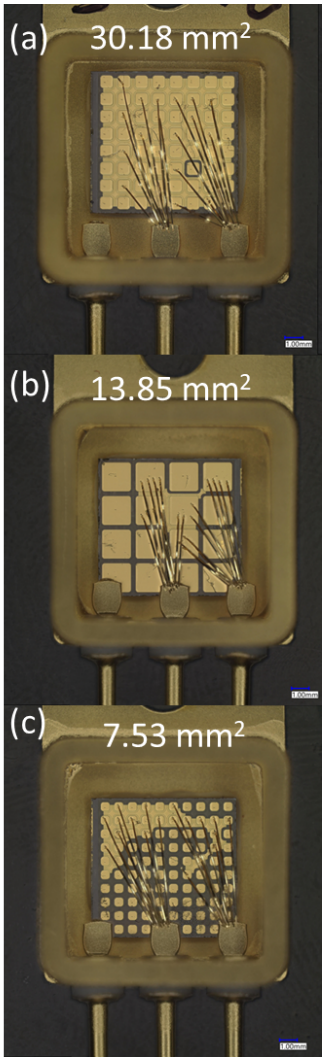

Figure 6: Cell 18, 3, and 21 diced and mounted in a TO 254 packages with 20 ribbon bonds. The total effective anode area is indicated at the top of each image.

No potting compound was used for the initial characterization and the cavity was filled with fluorinert (FC-70) for the high voltage breakdown tests. At each step in the process the devices were evaluated for forward conduction and reverse IV characteristics using a Keysight B1505a Power Device Analyzer. Pulsed current conditions consisted of a 50 µs pulse width and 0.5 % duty cycle. The high current forward and reverse IV characteristics for all three packaged parts are shown in Figure 7. While all three parts demonstrated the capability to conduct > 350 A, the 7.53 mm^2 device exhibited a significantly higher on-resistance and appeared to be limited by the anode area itself, rather than the ribbon bonds. The 13.85 mm^2 and 30.18 mm^2 had similar on-resistance, indicating that the 20 ribbon bonds were now becoming the limiting factor in resistance. As seen in Figure 7, the 7.53 mm^2 and 13.85 mm^2 devices were able to maintain low leakage reverse IV performance up until an ~1600 V breakdown. Unfortunately, the largest area device demonstrated enhanced leakage up to our current compliance (10 µA) at around 1000 V.

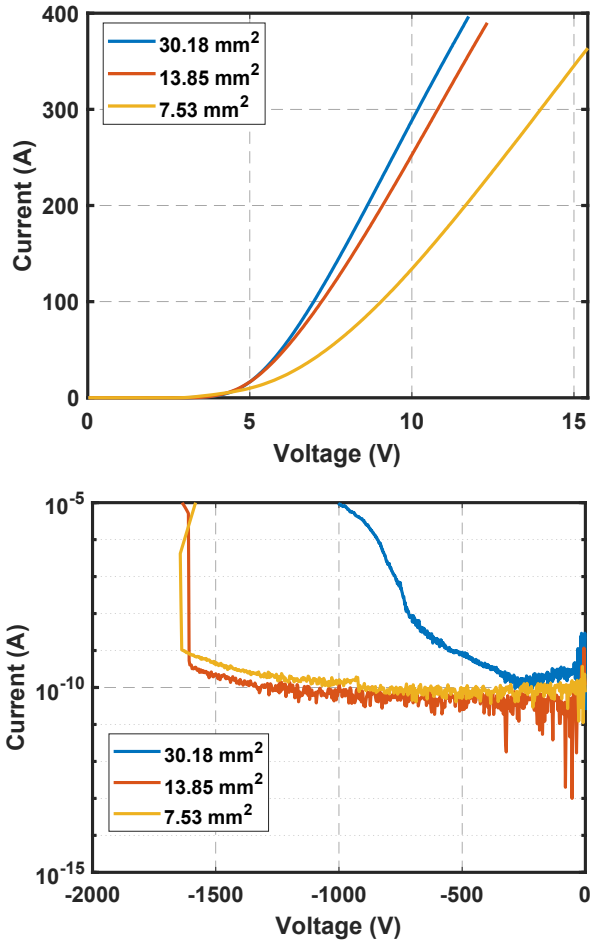

Figure 7: (Top) Forward IV characteristics of the three cells post packaging. (Bottom) Reverse IV characteristics of the three cells post packaging.

If we look at the performance of individual diodes prior to the interconnect process, we can observe changes in reverse IV performance because of the interconnect and packaging process. In Figure 8 we focus on the 13.85 mm^2 device that consisted of five 2.77 mm^2 device connected in parallel with a continuous top metal, we see that a specific on-resistance of ~2.3 mOhm-cm^2 was achieved (assuming the 13.85 mm^2 anode contact area), however, due to the ribbon bonds appearing to be the limiting factor, there is an opportunity to further reduce this resistance. The reverse IV performance did degrade slightly from the five individual diodes before the interconnect metal was applied. The breakdown voltage was reduced from ~1800 V to ~1600 V, and a very slight increase in leakage was observed. This was true for both the 13.85 mm^2 and 7.53 mm^2 device. Interestingly, the 7.53 mm^2 device consisted of a total of 31 of our smallest anode contacts (0.24 mm^2) and the interconnected device was able to achieve similar reverse IV performance as the 13.85 mm^2 device that consisted of our largest (2.77 mm^2) individual anode contacts.

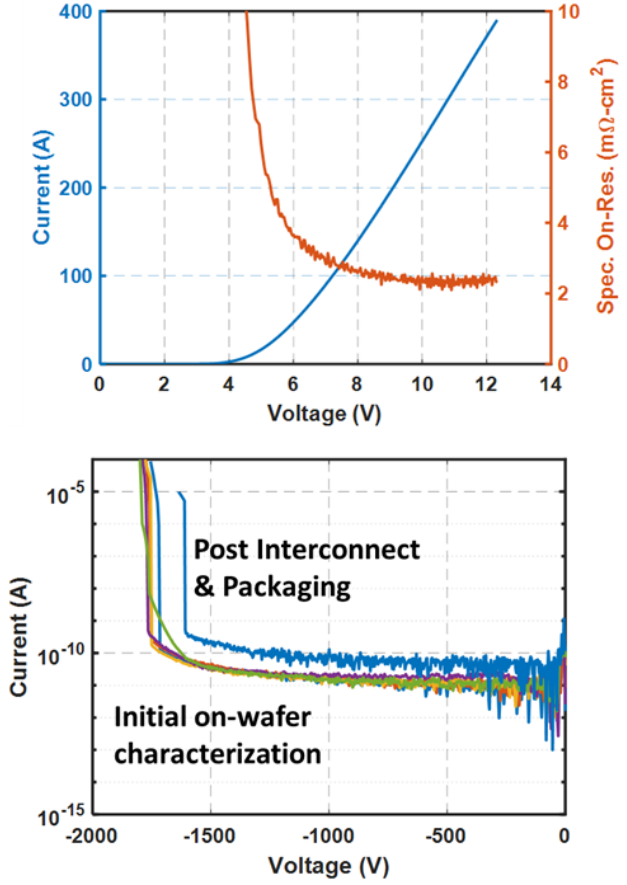

Figure 8: (Top) Forward IV characteristics of the three cells post packaging. (Bottom) Reverse IV characteristics of the three cells post packaging.

V. Conclusions

We have demonstrated the viability of utilizing a custom interconnect metallization scheme to parallel vertical GaN PN diodes. This method was first investigated through TCAD simulations to determine the impact of the interconnect metal over device isolation trenches. It was found that a continuous isolation etch between devices was necessary to allow the electric field to spread between devices in the n-drift region. Additionally, the etch depth of the isolation trench impacted how effective the PN junction was at protecting the passivation dielectric from peak electric fields, with deeper etches reducing the effectiveness. We compared three interconnected and packaged devices with varying individual anode areas. It was found that our ribbon bonds began to limit forward conduction capabilities, indicating a need for additional bonds or an alternative packaging that utilizes the entire contact area. Even with this limitation, we were able to demonstrate a low leakage, high voltage breakdown of 1600 V and a forward pulsed conduction current of 390 A for our best performing device. We saw a slight reduction in breakdown and a slight increase in reverse leakage post interconnect and packaging as compared to the individual device performance.

References

[1] L. Yates, B. P. Gunning, M. H. Crawford, J. Steinfeldt, M. L. Smith, V. M. Abate, J. R. Dickerson, A. M. Armstrong, A. Binder, and A. A. Allerman, "Demonstration of> 6.0-kV breakdown voltage in large area vertical GaN pn diodes with step-etched junction termination extensions," *IEEE Transactions on Electron Devices,* vol. 69, no. 4, pp. 1931-1937, 2022.

[2] H. Ohta, K. Hayashi, F. Horikiri, M. Yoshino, T. Nakamura, and T. Mishima, "5.0 kV breakdown-voltage vertical GaN p–n junction diodes," *Japanese Journal of Applied Physics,* vol. 57, no. 4S, pp. 04FG09, 2018.

[3] I. C. Kizilyalli, A. P. Edwards, H. Nie, P. Bui-Quang, D. Disney, and D. Bour, "400-A (pulsed) vertical GaN pn diode with breakdown voltage of 700 V," *IEEE electron device letters,* vol. 35, no. 6, pp. 654-656, 2014.

[4] A. T. Binder, J. R. Dickerson, M. H. Crawford, G. W. Pickrell, A. A. Allerman, P. Sharps, and R. J. Kaplar, "Bevel edge termination for vertical GaN power diodes." pp. 281-285.

[5] L. Yates, A. Binder, J. R. Dickerson, G. Pickrell, and R. Kaplar, *Electro-thermal Simulation and Performance Comparison of 1.2 kV 10 A Vertical GaN MOSFETs*, Sandia National Lab.(SNL-NM), Albuquerque, NM (United States), 2020.