SAND2024-02541C

Sandia National Laboratories

Exceptional service in the national interest

SCALABLE BENCHMARKING OF QUANTUM CHEMISTRY ALGORITHMS USING CIRCUIT MIRRORING

Aidan Q. Wilber-Gauthier, Stefan K. Seritan, Andrew D. Baczewski, Timothy J. Proctor

APS March Meeting 2024, Session D50

March 4, 2024

U.S. DEPARTMENT OF ENERGY NNSA National Nuclear Security Administration

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc. for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

CURRENT STATE OF QUANTUM BENCHMARKS

- High-level Approaches
  - Scalable, measure general performance of a device
  - E.g., randomized benchmarking, IBM quantum volume benchmark
- Tomographic Approaches
  - Not scalable, but detailed
  - E.g., gate set tomography, process tomography

- What we want from an application-specific benchmark:
  - **Scalable** to many qubits
  - **Representative** of the performance of a specific algorithm
  - **Generalizable** to any algorithm

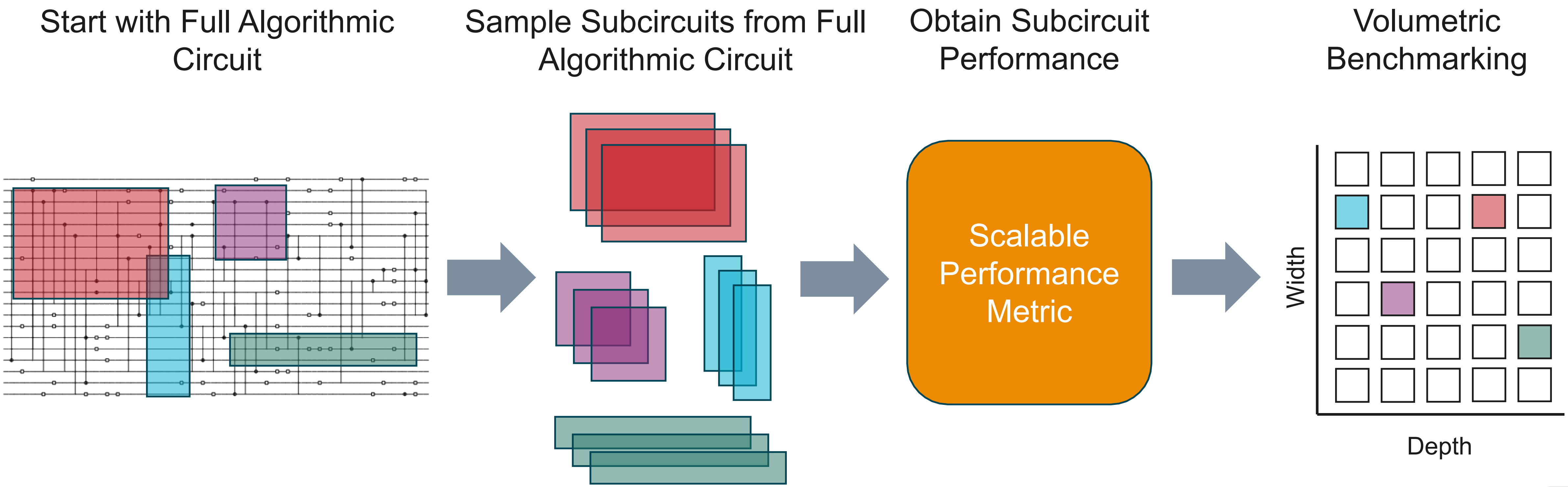
APPLICATION-SPECIFIC BENCHMARKS

- Current application-specific benchmarks typically…
  - Exploit properties of specific problems (i.e., efficiently verifiable circuit outcomes)
  - Lack scalability

- How can we **efficiently** construct benchmarks to measure the performance of **any algorithm**?
  - Use circuit mirroring on subcircuits of an application circuit

SUBCIRCUIT SELECTION

- Randomly sample subcircuits of different shapes from application circuit
- Obtain fidelities using a scalable performance metric
  - We use mirror circuit fidelity estimation (MCFE)



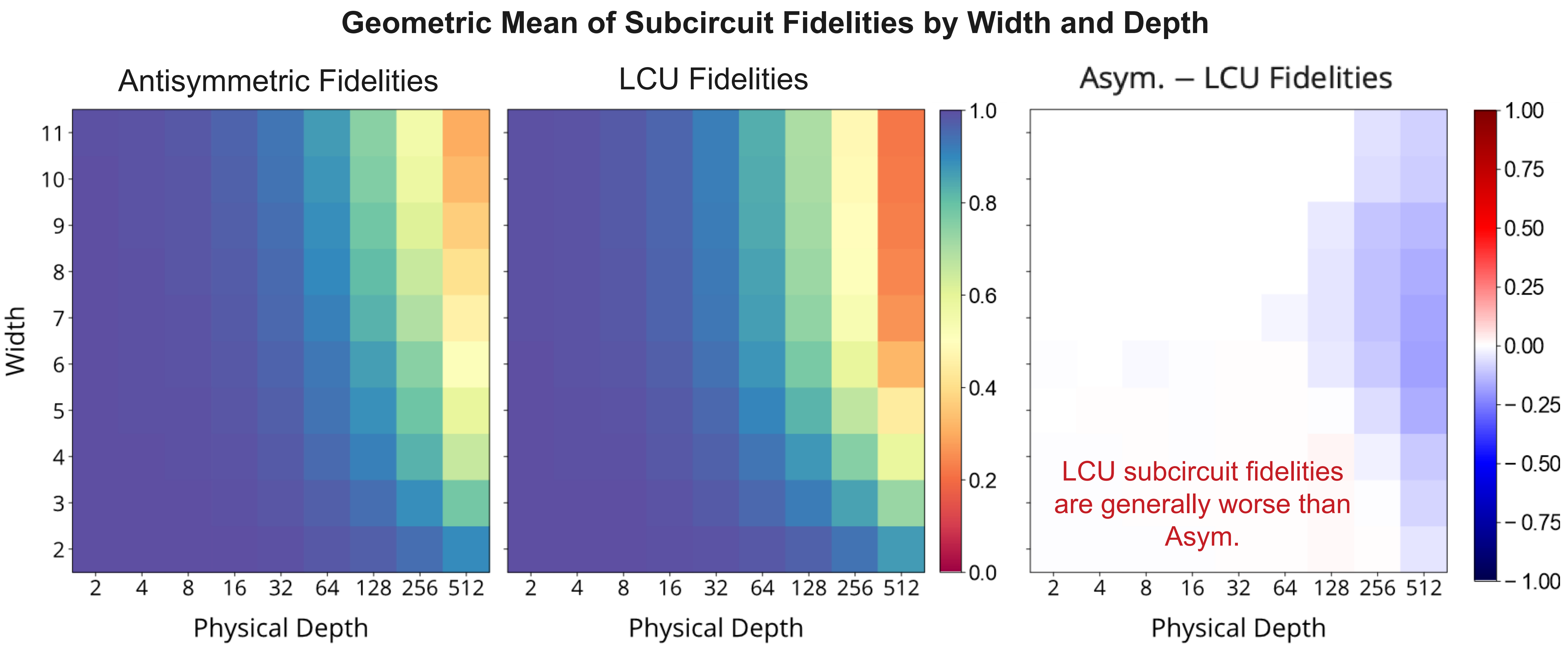
METHODS

- Tested on two different applications
  - Antisymmetrization routine for first-quantized molecular state preparation
    - Uses a bitonic sorting network
  - Block-encoded Hamiltonian for second-quantized state preparation
    - Uses linear combination of unitaries (LCU)

- Used noisy numerical simulations to obtain subcircuit and full circuit fidelities with MCFE
  - 300 subcircuits per width-depth pair
    - MCFE Parameters: 100 mirroring samples per subcircuit, 100 reference experiments per width
  - Widths from 2 to 11 qubits
  - Depths from 2 to 512 (exponentially increasing)
  - Noise model with 1- and 2-qubit Hamiltonian and stochastic error generators
    - Hamiltonian generator strengths of 10^{-3} and 10^{-2} for 1- and 2-qubits
    - Stochastic generator strengths of 4×10^{-4} and 4×10^{-3} for 1- and 2-qubits

VOLUMETRIC BENCHMARKS

- Volumetric benchmarking (VB) plots our benchmark is sensitive to differing performance across algorithms



PREDICTING FULL CIRCUIT FIDELITIES

- Our benchmark is sensitive to differences in performance
- How can we quantify these differences concisely?
  - Use an error rate model
  - Want to use benchmarking results to estimate error rate ε that allows us to predict full circuit fidelity

Compute average fidelity of (w, d) subcircuits

Calculate error rate from average fidelity

Estimate full circuit fidelity from error rate

$$F_{wd} = \mathrm{GeomMean}\{\underbrace{F_{wd,1}, \ldots, F_{wd,n}}\} \longrightarrow \varepsilon_{wd} = 1 - (F_{wd})^{1/wd} \longrightarrow F_{\mathrm{est},wd} = (1 - \varepsilon_{wd})^{WD}$$

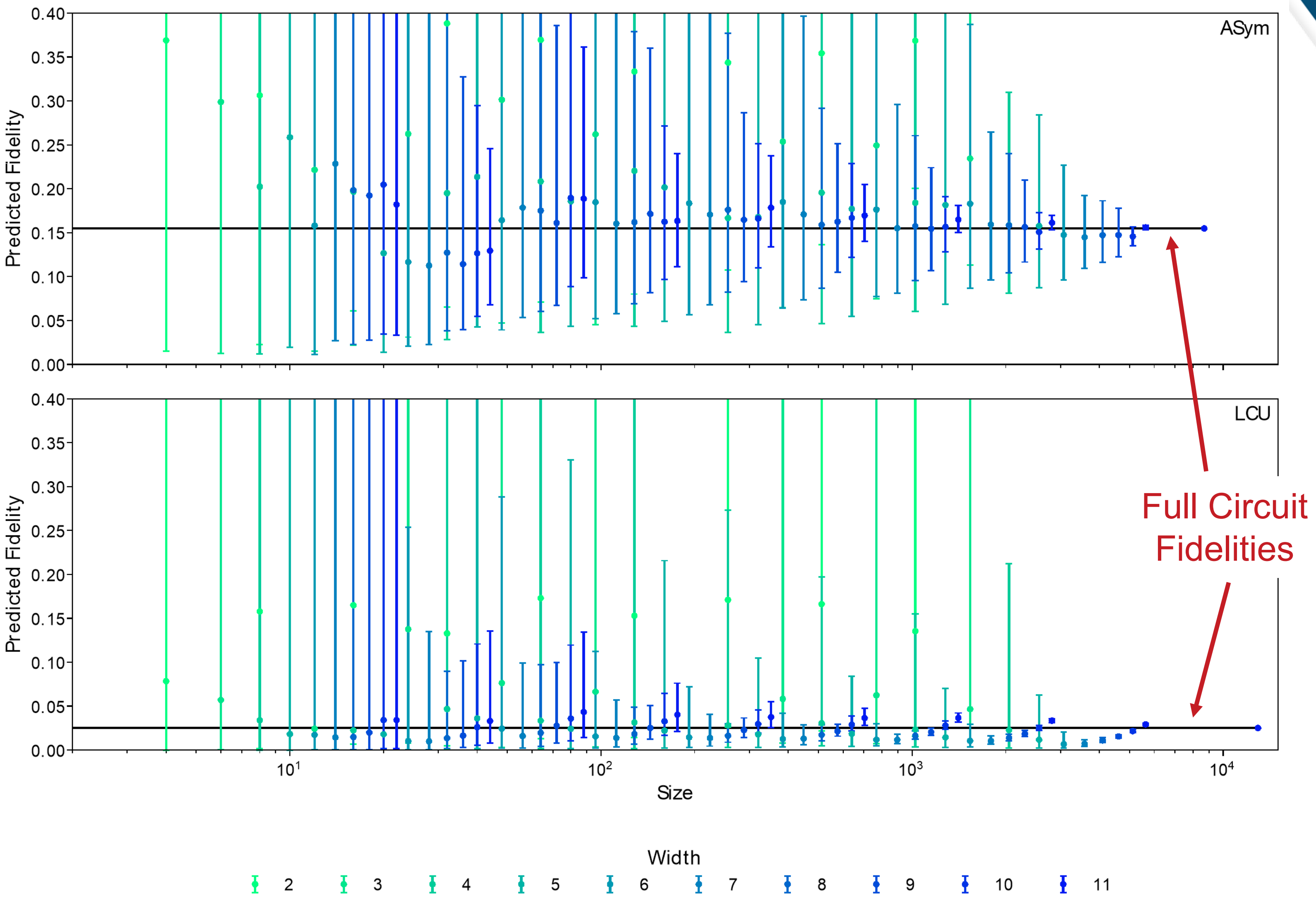
Individual subcircuit fidelities with width w and depth d

Assume fidelity loss occurs equally at each circuit location

Full circuit has width W and depth D

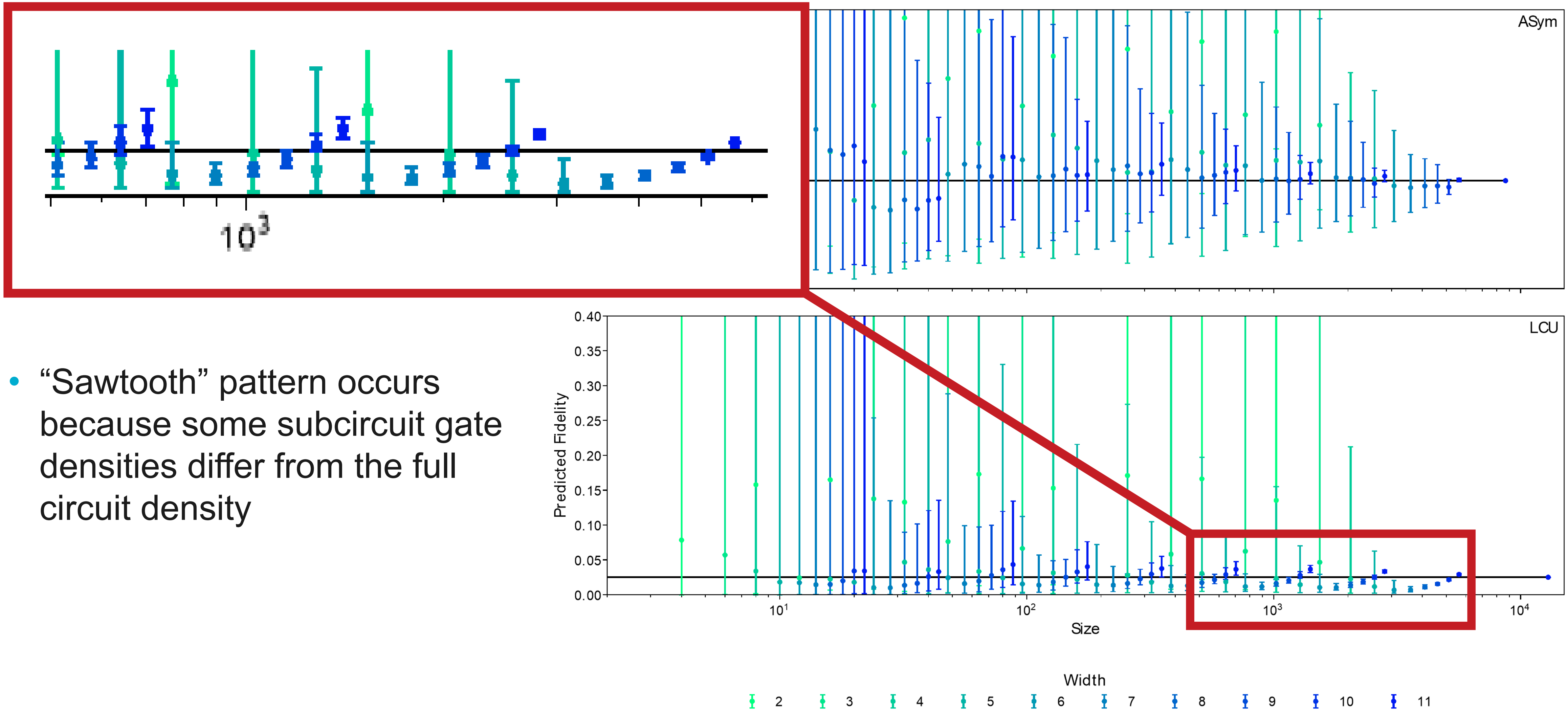
PREDICTING FULL CIRCUIT FIDELITIES

- Low width subcircuits are poor predictors of performance
  - So are 1Q/2Q error rates
- High width subcircuits are generally good predictors of full circuit fidelities, even at lower depths



PREDICTING FULL CIRCUIT FIDELITIES

- “Sawtooth” pattern occurs because some subcircuit gate densities differ from the full circuit density



PREDICTING FULL CIRCUIT FIDELITIES (REVISITED)

- To account for the difference in density between subcircuits and the full circuit, adjust the subcircuit fidelities using:

$$\tilde{F}_{wd,i} = (F_{wd,i})^{\xi/\xi_{wd,i}}$$

"density-adjusted fidelity"

$\xi =$ full circuit density

$\xi_{wd,i} =$ density of (w, d) subcircuit i

Compute average fidelity of (w, d) subcircuits

Calculate error rate from average fidelity

Estimate full circuit fidelity from error rate

$$\tilde{F}_{wd} = \text{GeomMean}\{\tilde{F}_{wd,1}, \ldots, \tilde{F}_{wd,n}\} \longrightarrow \tilde{\varepsilon}_{wd} = 1 - \left(\tilde{F}_{wd}\right)^{1/wd} \longrightarrow \tilde{F}_{\text{est},wd} = (1 - \tilde{\varepsilon}_{wd})^{WD}$$

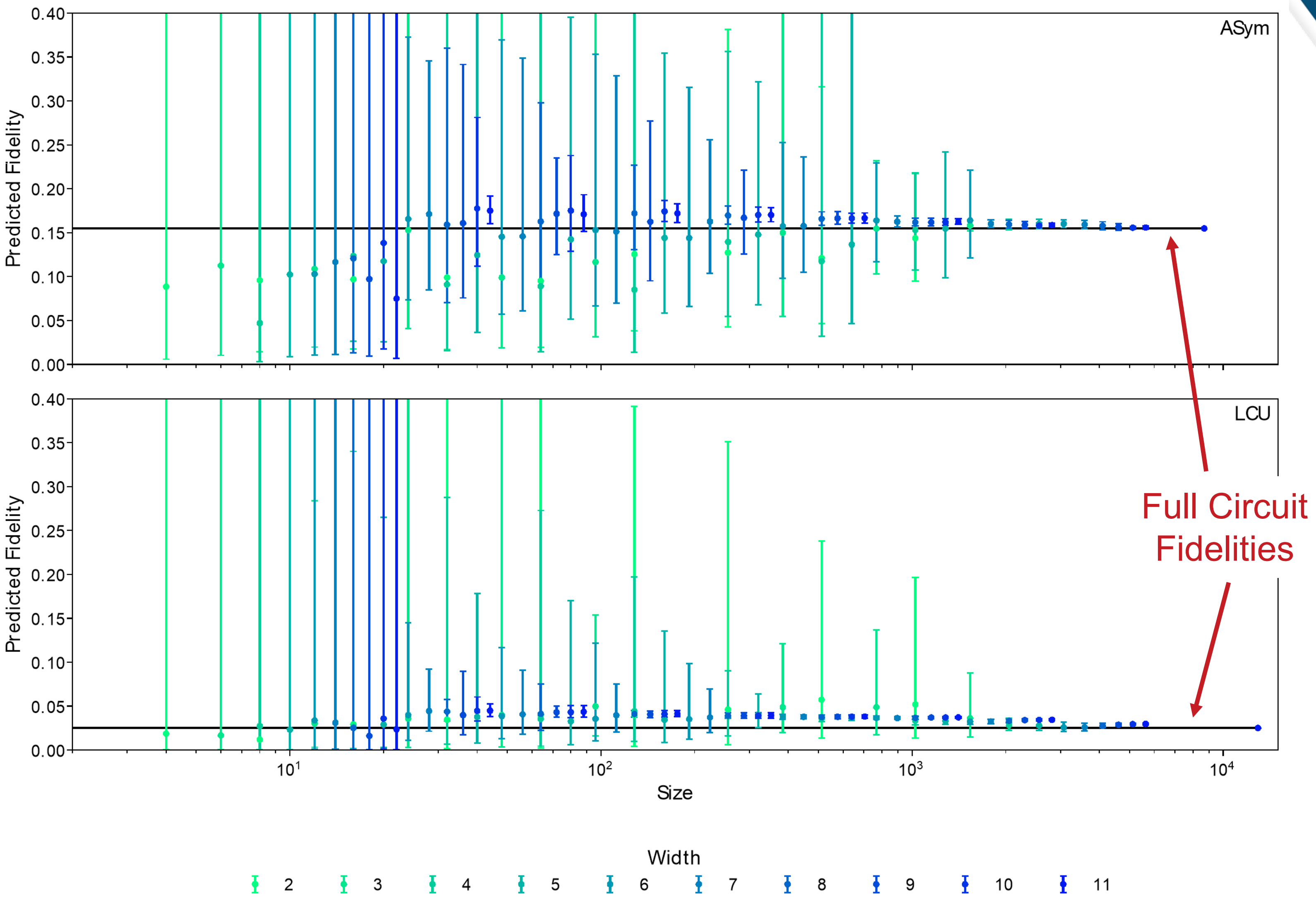
Individual subcircuit fidelities with width w and depth d

Assume fidelity loss occurs equally at each circuit location

Full circuit has width W and depth D

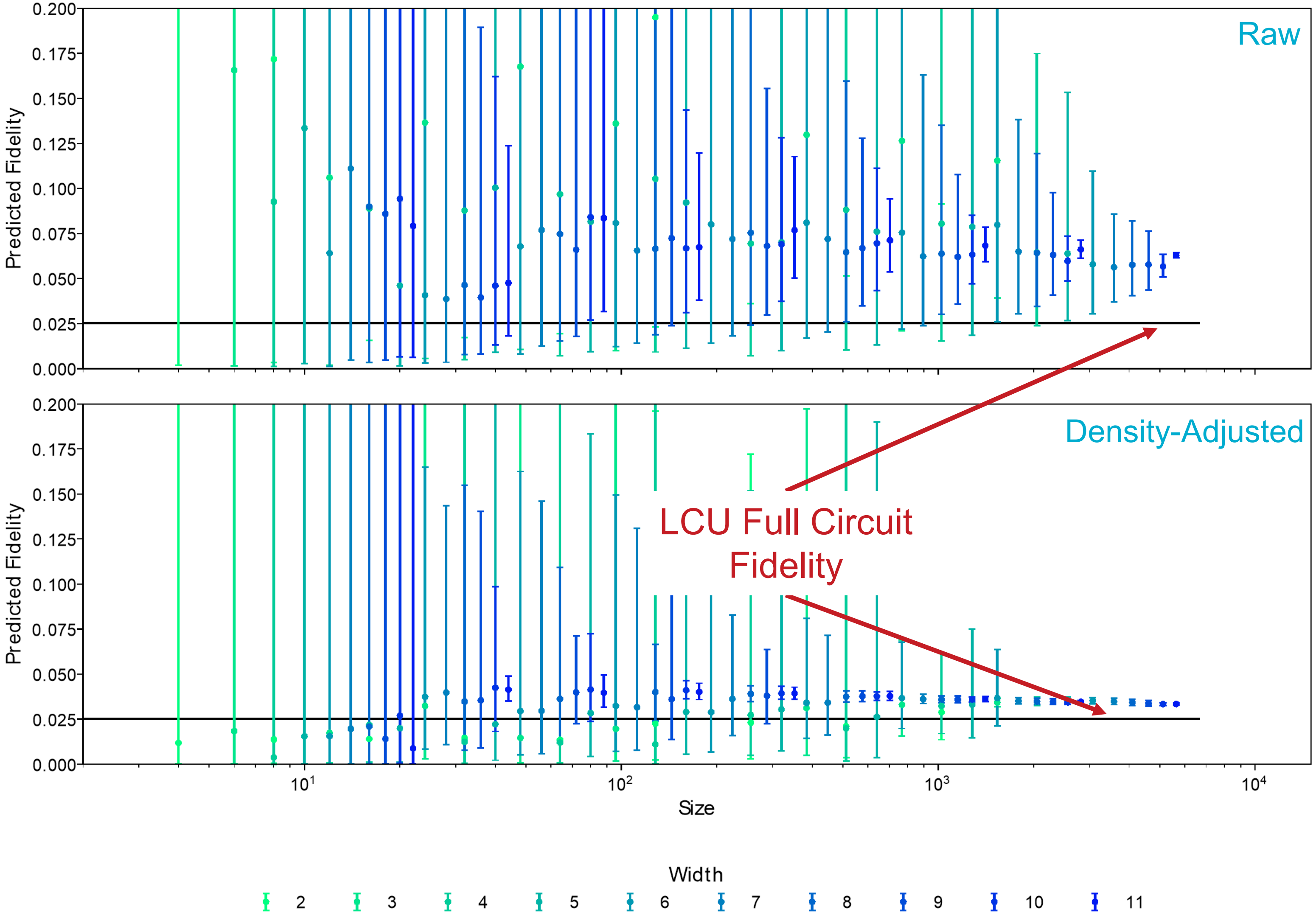
PREDICTING FULL CIRCUIT FIDELITIES (DENSITY-ADJUSTED)

- Accounting for subcircuit density yields more consistent convergence to full circuit fidelity than before



CROSS-PREDICTING CIRCUIT FIDELITIES FAILS

- If we account for circuit width, depth, and density, can we predict the LCU full circuit fidelity from the ASym benchmarking data?
  - No; subcircuit benchmarking data reveals structural differences in performance



CONCLUSIONS

- Application-specific benchmarks using subcircuits can detect differences in performance across applications due to structural differences in the circuits
  - Volumetric benchmarks show performance differences in subcircuits

- Using error rate models, can succinctly quantify algorithmic circuit performance using subcircuit benchmarking data
  - Performance differs even after accounting for width, depth, and density
  - Predicting performance of one algorithmic circuit from benchmarking data for another does not work