

Focus Area: 1

FY23 TRL: 4

FY24 TRL: 4

FY24 Task Goals/Deliverables and status:

- Modelling
- Detector fabrication
- Electronics development
- (deliverable) Detector selection report

PROACTIVE GORs:

**Relevant FA1 topics**

- SNM absence
- Warhead confirmation
- Dismantlement
- (possible) Type identification
- HE absence
- Disposition confirmation

Use Case(s):

Dismantlement confirmation

- Confirm warhead presence before
- Confirm warhead absence after
- Confirm SNM separated from HE

Template initialization

- Confirm that initial item presented for template measurement is a warhead

(possible) Type verification

- Use SNM geometry in a warhead to identify type

Integration Across PROACTIVE:

Participation in venture experiments

Development of information-secure readout and analysis techniques



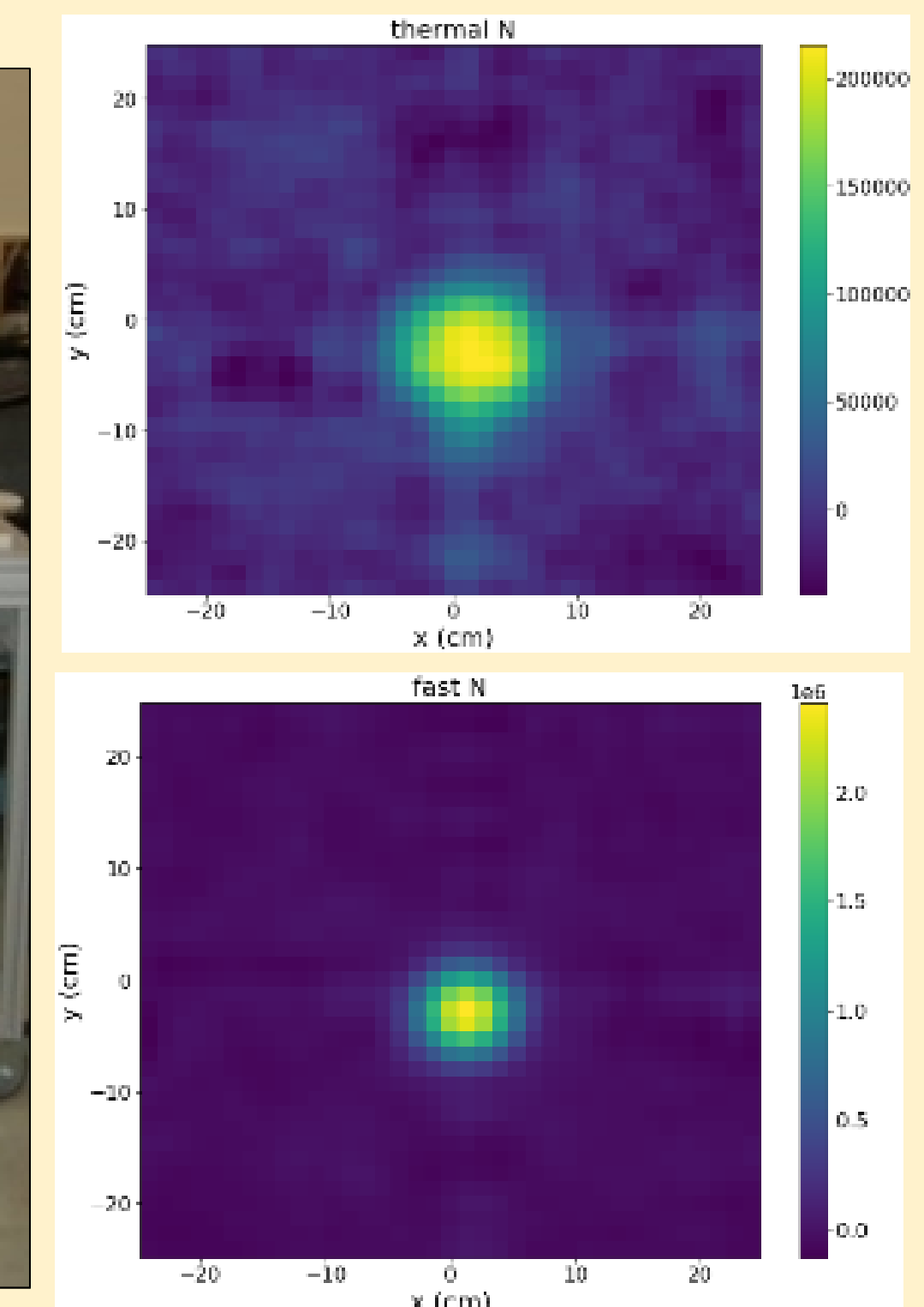
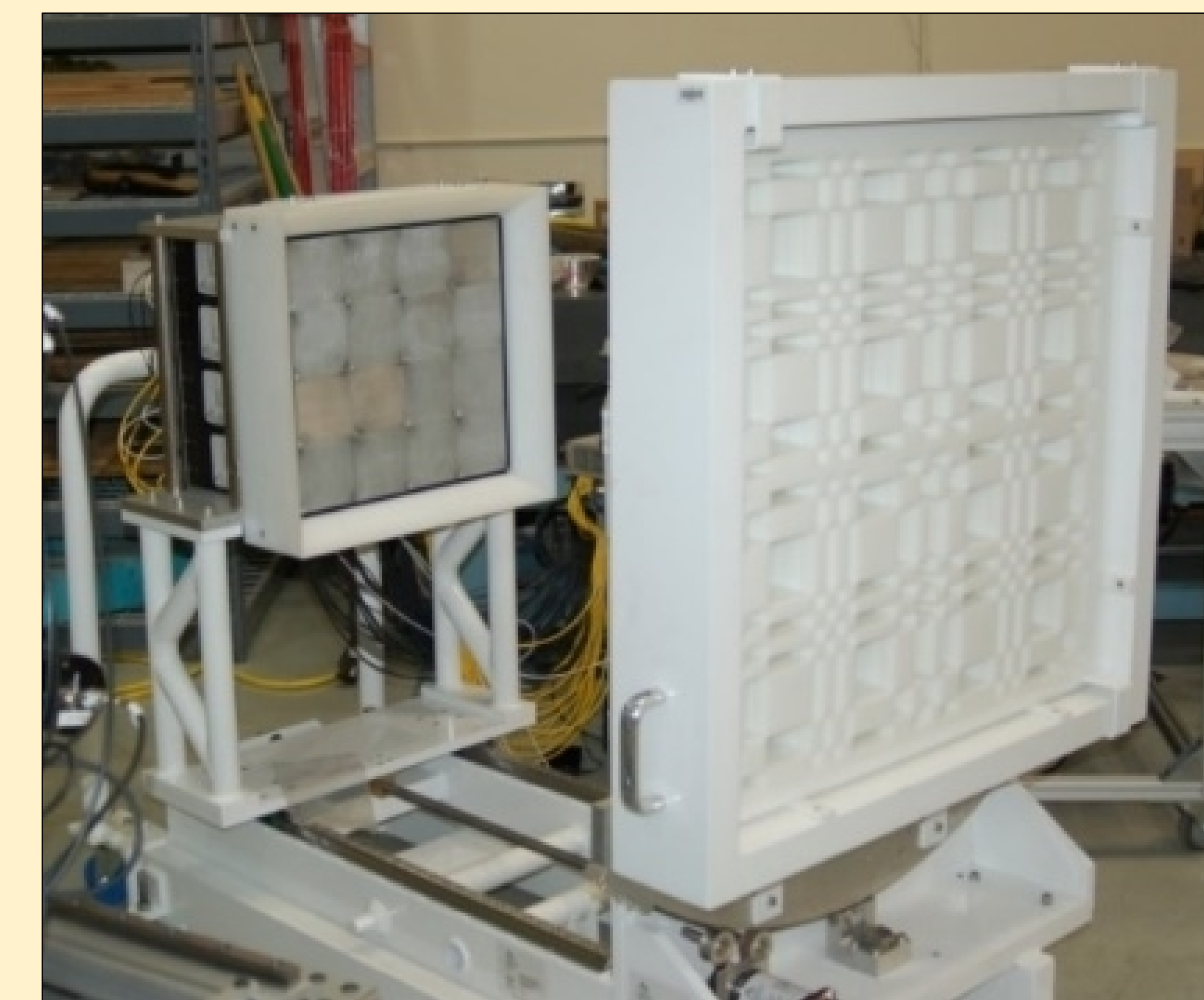
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# Passive Neutron Imaging

## Technical Objectives

Design, fabricate, commission, and field a coded aperture neutron imager for use in an arms control context.

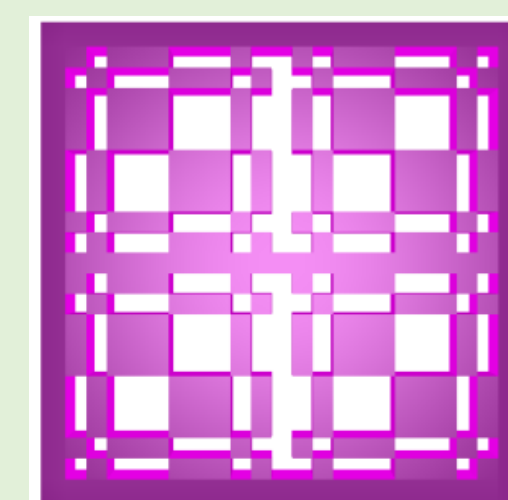
- Modelling to investigate use cases and information at risk
- Production of a 24x24 pixelated neutron detector based on organic glass scintillator and read out be SiPMs
- First-pass electronic readout for participation in venture experiments
- Second-pass electronic readout system for robust information protection



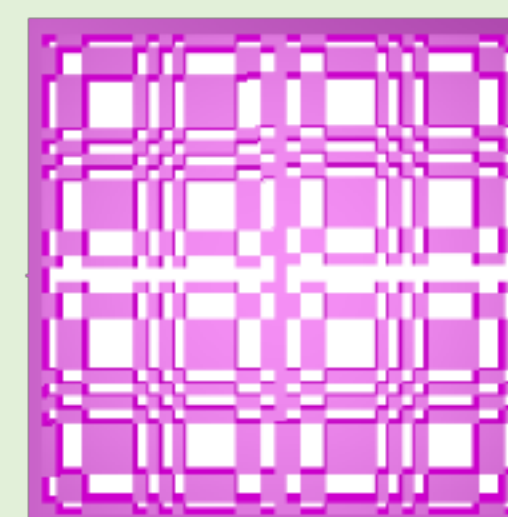
## Modelling

- Mask based on rank 11 Modified Uniformly Redundant Array (MURA)
- Response map generated via ray-tracing and material dependent attenuation
- Image reconstruction via MLEM

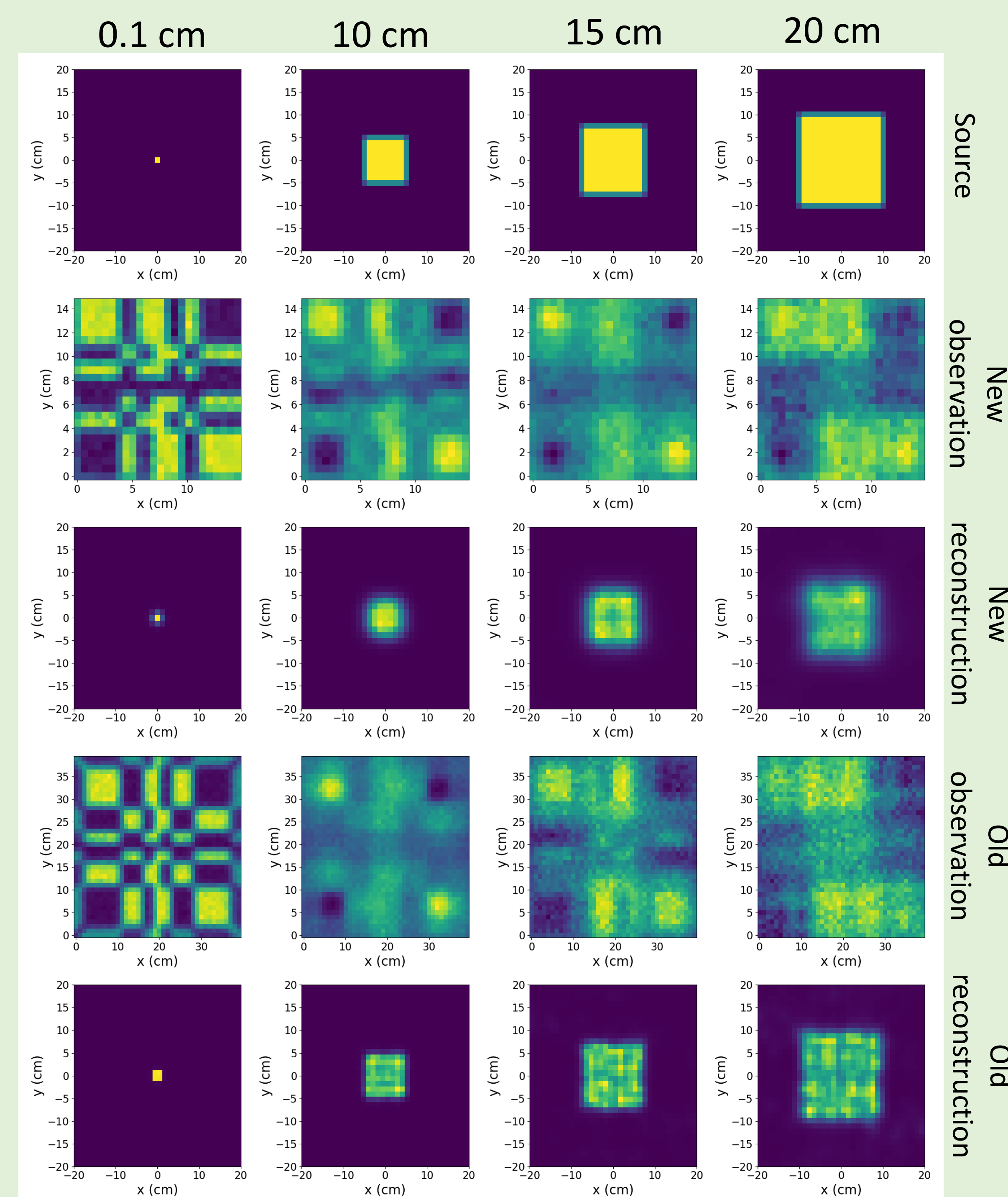
Simulated source:  
centered square



Proposed Detector:  
24x24 6.3mm pixels  
Rank 11 MURA

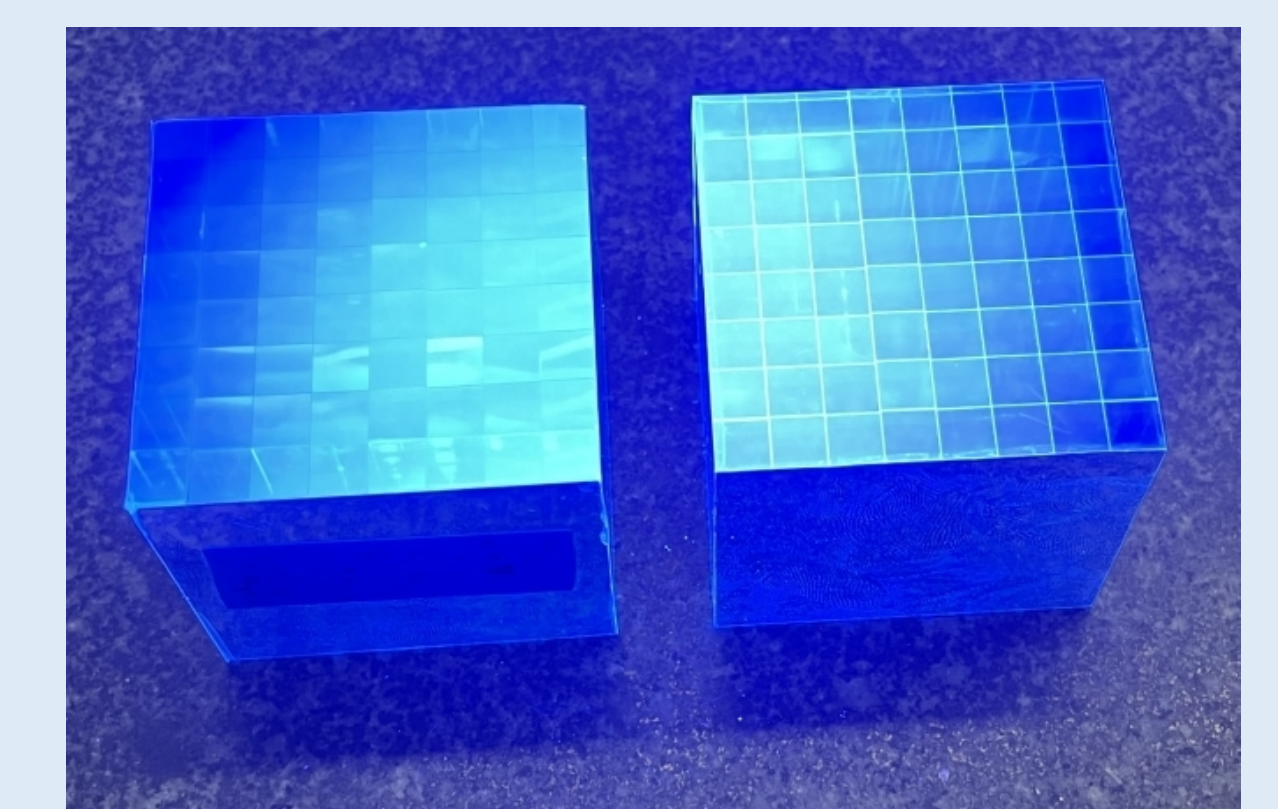
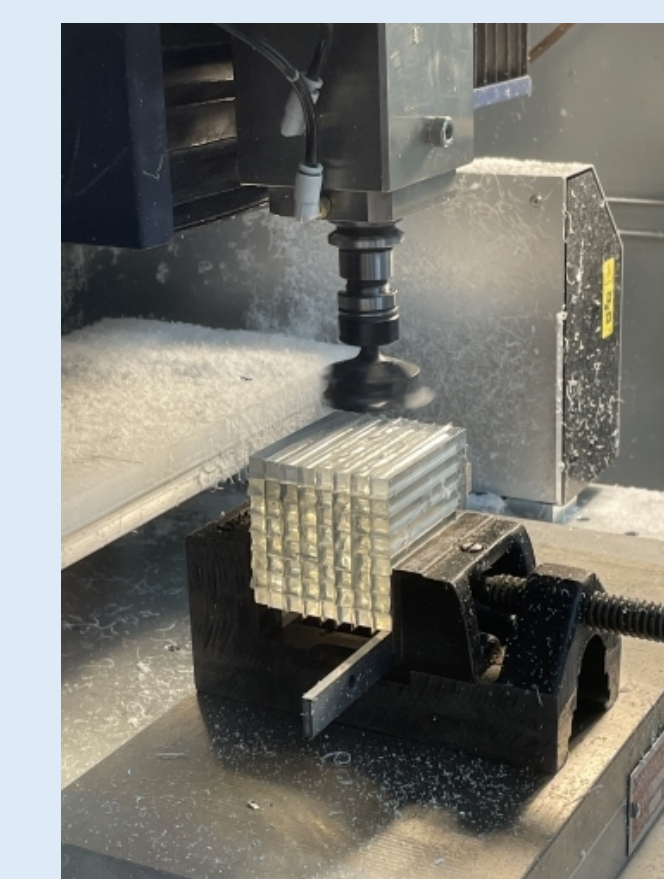


Previous NCA:  
40x40 1cm pixels  
Rank 19 MURA



## Scintillator

- Selected organic glass scintillator (OGS) as fast neutron detector
  - Mixed with PVT for subtractive processing
- OGS produced by Patrick Feng at SNL-CA
- 8x8 blocks fabricated at ORNL
  - Pixels separated with aluminized ESR
- First test blocks with 50% OGS have been assembled



## Electronics

- 3x3 grid of 64-pixel J-series SiPM arrays
- Read out via FSM1 PSD ASICs developed by DTRA
- Motherboard houses FPGA for ASIC readout

