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INTEGRATED DECOUPLING CAPACITORS USING $Pb(Zr,Ti)O_3$ THIN FILMS

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ABSTRACT

Thin-film decoupling capacitors based on ferroelectric (Pb,La)(Zr,Ti)O3 films are being developed for use in advanced packaging applications. The increased integration that can be achieved by replacing surface-mount capacitors should lead to decreased package volume and improved high-speed performance. For this application, chemical solution deposition is an appropriate fabrication technique since it is a low-cost, high-throughput process. The use of relatively thick Pt electrodes (~1 μm) to minimize series resistance and inductance is a unique aspect to fabricating these devices. In addition, the important electrical properties are discussed, with particular emphasis on lifetime measurements, which suggest that resistance degradation will not be a severe limitation on device performance. Finally, some of the work being done to develop methods of integrating these thin-film capacitors with ICs and MCMs is presented.

INTRODUCTION

An important application for ferroelectric/high-permittivity thin films that has received relatively little attention is their potential use as integrated capacitors for advanced packaging applications. For instance, capacitors are required for signal decoupling, signal coupling, filtering, and impedance matching. For these applications, the main motivation for developing thin-film technologies is that they can provide a higher level of integration than could be achieved with discrete components. Integration of capacitors, as well as other passive components, should lead to reductions in system size and improvements in system performance, particularly due to reduced interconnect parasitics.

Of the various applications for capacitors in electronic packages, one of the most important ones for both digital and analog systems is signal decoupling. A decoupling capacitor is inserted in a circuit, as illustrated schematically in Fig. 1, to act as a local source that can supply required charge to the integrated circuit (IC). Since the IC does not get the charge directly from the power supply, the capacitor effectively decouples the IC from the power supply, which speeds up the circuit response and suppresses noise on the power line by reducing the inductance. However, as the clock rates for ICs increase, improvements in signal decoupling will be required since the inductance associated with surface-mount capacitors and their interconnection to the IC will limit operational frequency. Therefore, one strategy for improving signal decoupling in high-speed systems, such as multichip modules (MCMs), is to develop low-inductance, thin-film capacitors that can be highly integrated into packages [1,2].

Replacing multi-layer ceramic decoupling capacitors with thin-film capacitors that can be integrated with ICs and MCMs will generally require the use of thin films with high dielectric constants, since decoupling capacitors typically have values of 10-100 nF. Consequently, the most likely candidate materials for thin-film decoupling capacitors are the perovskites such as $(Ba,Sr)TiO_3$ (BST), $Pb(Zr,Ti)O_3$ (PZT), and $Pb(Mg,Nb)O_3$ (PMN), since these materials have high dielectric permittivities and low losses up to frequencies in excess of 1 GHz [3-5]. Table 1 compares the range of dielectric constants (at room temperature) obtained for these thin-films to the dielectric constants of some lower permittivity materials

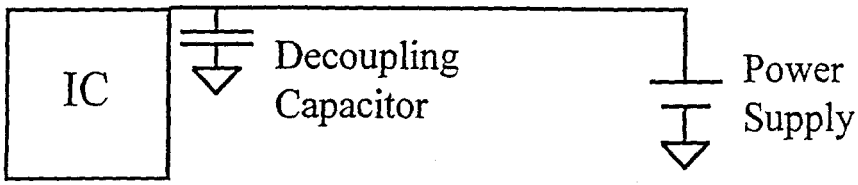

Figure 1. Schematic diagram illustrating a decoupling capacitor which acts as a local source or sink for charge to effectively decouple the IC from the power supply.

being developed for integrated capacitors [6]. It should be noted that the range of dielectric constants for BST and PZT partly reflects the fact that these materials are solid solution systems, where the permittivity is a function of the Ba/Sr and Zr/Ti ratios, respectively.

TABLE I

High-Permittivity (Perovskite) Dielectrics		Low-Permittivity Dielectrics	
$(Ba,Sr)TiO_3$	$\varepsilon = 250\text{-}500$	SiN	$\varepsilon = 7\text{-}9$
$Pb(Zr,Ti)O_3$	$\varepsilon = 400\text{-}1500$	Diamond-like carbon	$\varepsilon = 4\text{-}5$
$Pb(Mg,Nb)O_3$	$\varepsilon > 1500$	Ta_2O_5	$\varepsilon = 20\text{-}25$

Given the various material systems suitable for thin-film decoupling capacitors, we have focused attention on the PZT system due to the high permittivity (>1000) attainable for certain compositions, the inherent flexibility in tailoring properties by adjusting the Zr/Ti ratio and by adding dopants, and the relatively mature state of processing knowledge. In this paper, we discuss the fabrication of PZT thin-film decoupling capacitors, the important electrical properties, and some of the work being done to develop methods of integrating these thin-film capacitors with ICs and MCMs.

FABRICATION OF PZT THIN-FILM DECOUPLING CAPACITORS

A wide variety of fabrication techniques have been shown to be capable of producing high-quality PZT thin films. Therefore, the choice of an optimal fabrication technique can depend on a number of factors. In the case of decoupling capacitors, cost is a particularly harsh driver that dictates which processes may be appropriate. For example, the cost of a typical surface-mount chip capacitor is about $0.01, which means that thin-film decoupling capacitors will have to be very inexpensive to be competitive. Of all the suitable processes, the chemical solution deposition (CSD) approach is probably the most appropriate for passive components, since it offers very low costs. The low cost is due to both the relatively straightforward and inexpensive processing tools required and the fact that the CSD approach is a high-throughput process.

The details of the CSD process we used to fabricate PZT and doped PZT thin films have been described in detail elsewhere [7,8]. Briefly, this method employs alkoxide and carboxylate precursors, along with methanol, acetic acid, and water as solvents. The starting solutions are fabricated by first reacting the appropriate ratio of zirconium butoxide-butanol and titanium isopropoxide. Acetic acid is then added, followed by methanol. Lead (IV) acetate is then added and the solution is heated to ~ 85°C to dissolve the acetate. Preparation is completed with further additions of methanol, acetic acid, and water, to give a 0.4 M solution. The solution

batches were prepared with 10 mol % excess Pb, as compared to the stoichiometric ABO_3 formula, to compensate for Pb loss due to PbO volatilization during the crystallization anneal.

In the case of La-doped films (PLZT), lanthanum acetate or acetylacetonate (acac) is added with the Pb acetate and the composition is adjusted by assuming that charge compensation is due to B-site vacancies. In the case of Nb-doped films (PNZT), niobium ethoxide is added with the Zr and Ti precursors and the composition is adjusted by assuming that charge compensation is due to A-site vacancies. In reality, the exact charge compensation condition may not be critical, since there is a range of Pb excess concentrations for which single-phase perovskite is obtained.

The PZT, PLZT or PNZT films are formed by spin coating the solution onto a substrate. The substrates are Si wafers that have a Pt metallization, including a thin adhesion layer (typically Ti), and a 400-500 nm thick thermal oxide. Each solution-deposited layer is spin cast onto the $Pt/Ti/SiO_2/Si$ substrate at 3000 rpm for 30 seconds and then heat-treated on a hot plate at ~ 300°C for 5 minutes to pyrolyze organic species in the precursor film. The wafers are fired at 650°C in air for 30 minutes using a 50°C/min ramp rate. This technique yields films that are single-phase perovskite and have columnar microstructures, with a lateral grain size of 100-200 nm. Individual, spin-cast layers are 90-100 nm thick after pyrolysis and crystallization; therefore, a multilayering approach is used to obtain thicker films. In this case, a crystallization anneal is done after every four layers are deposited and pyrolyzed to avoid film cracking.

In contrast to many applications for high-permittivity thin films, the performance requirements for decoupling capacitors place more demands on the metallization. Specifically, the electrode sheet resistance must be minimized to reduce the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitor, which for high-performance applications have target values of roughly 100mΩ and 50pH, respectively. Given these target values, approximately 1 μm of Pt would be required ($R_S=\rho/t$; $\rho(Pt)\approx 10\mu\Omega$-cm) the electrodes. However, the use of such thick electrodes is not straightforward, since thick electrodes exhibit more pronounced roughening during thermal processing and weaker adhesion to the substrate (for bottom electrodes) or to the film (for top electrodes). Although alternative metals such as Cu, Au, and Ag would permit thinner metallization layers due to their higher conductivities, they are not suitable, particularly as bottom electrodes, due to their poor stability against oxidation and reaction with the PZT.

To obtain appropriate bottom electrodes, several techniques have been explored. One technique is to sputter deposit the Ti/Pt metallization at ~ 300°C rather than under ambient conditions. The elevated temperature deposition yields a metallization with significantly reduced hillocking, resulting in improved capacitor yield, and improved adhesion to the substrate. The improved adhesion and reduced hillocking are at least partly due to a change in the stress state of the Pt from ambient deposition (~ 300 MPa compressive) to elevated temperature deposition (~ 200 MPa tensile) [9]. Since additional compressive stress is generated in the Pt film during heating, the change from compressive to tensile stress in the as-deposited film is significant.

A further improvement is obtained by using a TiO_x or ZrO_x adhesion layer in combination with the elevated temperature Pt deposition [9]. The TiO_x or ZrO_x are fabricated in-situ by sputtering in an Ar atmsophere and then annealing in the sputtering at 450°C in flowing O_2 and, thus, are not fully oxidized. This approach, which is comparable to that previously reported by Summerfelt et.al. [10], also leads to good adhesion and even smoother films than obtained using the Ti adhesion layer. This further reduction in roughness presumably

occurs by suppressing oxidation of the adhesion layer, which also leads to hillocking. The resistivity of these films also changes less with subsequent annealing than observed for the Ti/Pt metallization, due to reduced diffusion of Ti or Zr from the oxide adhesion layer. An additional improvement in adhesion is obtained with TiO_2 or ZrO_2 adhesion layers that are formed by fully oxidizing thin Ti or Zr films at 750°C in air, prior to depositing Pt at 300°C. The improved adhesion, which is determined by tape testing scribed films, is presumably due to an increase in the roughness of the fully oxidized adhesion layers as opposed to the in-situ formed oxides. Using this approach, we have fabricated substrates with nearly 1 μm thick Pt bottom electrodes that show good adhesion and lead to capacitor films with high yield [9].

For top electrodes, we have had limited success with thick (~ 1 μm) Pt metallizations based on relatively poor adhesion to the perovskite film. Pd exhibits superior adhesion to the PZT, but has a comparable resistance to Pt, which means that thick (~ 1 μm) Pd films are still required. Typical adhesion promoters such as Ti and Cr are not desirable since they tend to form insulating oxides and have been seen to result in premature breakdowns. The lowest resistance metals (Al, Cu, Ag, Au) are also not appropriate top electrodes, since they tend to react even at low temperatures (Al, Cu), diffuse quickly leading to premature failure (Ag), or show poor adhesion (Au). However, a combination of a Pd or Pt layer, which would be in direct contact with the PZT, with a low resistance overcoat of Au or Cu may be a good approach to optimizing adhesion while minimizing sheet resistance.

ELECTRICAL PROPERTIES

Dielectric constant and loss were characterized using an HP 4194 impedance analyzer. A small oscillation voltage (ΔV = 20 mV p-p) was used to minimize domain wall contributions. Leakage resistance was characterized by measuring leakage currents at constant voltage as a function of time using a Keithley source-measurement unit (model 236). The temperature was controlled to ±1°C using a Signatone hot stage with a dc power supply to minimize electrical noise. In general, a steady-state was attained only after extended testing times (> 1 hr) [11,12]. Dielectric breakdown strengths were determined using the Keithley 236 with a voltage staircase program, in which the voltage was incremented by 2V increments and the current was monitored to determine breakdown. A time interval of 5 minutes between voltage increments was used since this time interval was previously shown to minimize the time dependence of the measured breakdown strength [11]. For each test condition, 4 to 10 capacitors were used to obtain a statistically significant value for the average breakdown strength.

For decoupling capacitor applications, the properties that need to be optimized are permittivity, low dissipation factor, low leakage resistance, and good breakdown strength. Since the dielectric constant for PZT films exhibits a peak near the composition $Pb(Zr_{0.5}Ti_{0.5})O_3$ (PZT 50/50) [11, 13], we have focused on PZT 50/50 compositions. The temperature dependence of the dielectric constant for PZT 50/50, PLZT 5/50/50 (5 at. % La), and PZT 30/70 thin films is given in Fig. 2. The PZT 50/50 and PLZT 5/50/50 exhibit a stronger temperature coefficient of capacitance (TCC) than the PZT 30/70. The broad TCC for the PZT 50/50 and PLZT 5/50/50 samples is indicative of the diffuse phase transformation typically exhibited by thin films. However, in this case, La doping results in a lower dielectric constant and smaller TCC since the PLZT 5/50/50 composition is further from the tetragonal-rhombohedral phase boundary than the PZT 50/50 composition [14]. This result is consistent with the fact the La doping suppresses ferroelectric hysteresis [12]. In fact, ε at 5V for the PLZT 5/50/50 film shows only a 6% variation from 20°C to 150°C, which would be consistent

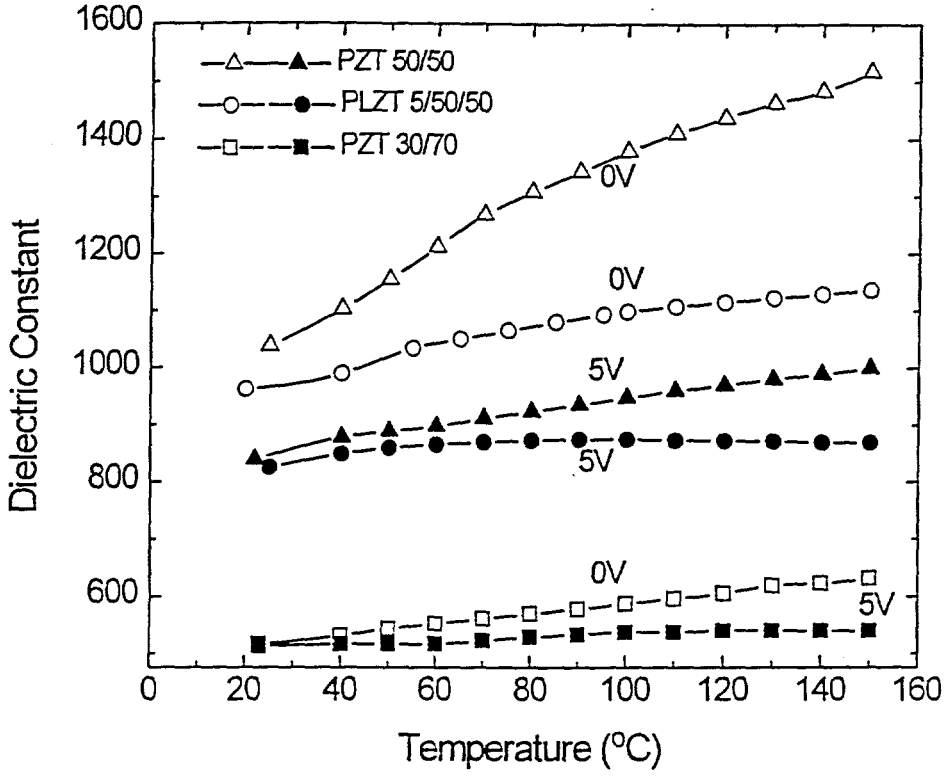

Figure 2. Temperature dependence of the dielectric constant for PZT 50/50, PLZT 5/50/50 and PZT 30/70 films at 0 V and 5 V. All films were roughly 0.8 μm thick.

with an X7R rating. Furthermore, the dissipation factor for these films is typically 0.01-0.02 and remains approximately constant over this same temperature range.

Donor doping has also been found to be critical for obtaining low leakage current densities. The effect of La or Nb concentration on the steady-state leakage resistance of films with Zr/Ti = 1 is shown in Fig. 3. Leakage current densities (at a given electric field) are

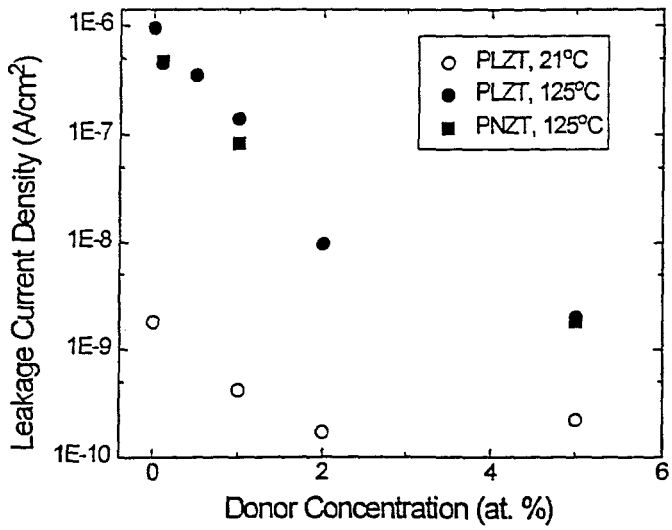

Figure 3. The effect of La and Nb doping on steady-state leakage current density at 125°C and 21°C. All films were approximately 0.8 μm thick and were tested at 5 V.

plotted, rather than the calculated resistivities, since the current-voltage response is not linear. Figure 3 demonstrates that both A-site (La) and B-site (Nb) donor doping is effective in leading to substantial improvements in leakage resistance at elevated temperatures (125°C). In addition, some improvement in the room-temperature leakage resistance has also been obtained. Similar improvements have also been demonstrated for donor-doped films with Zr/Ti ratios of 20/80, 30/70, and 40/60. Figure 3 also shows that leakage resistance continues to improve as the donor concentration increases up to at least 5 at. %, which is much higher than typically required to minimize leakage resistance in PZT ceramics [15]. Although the I-V characteristic is non-linear, an effective value for the film resistivity ($\rho_{eff} = E/J$) can be defined. For example, the 5 at. % La film at 125°C has a value of $\rho_{eff} = 3.5 \times 10^{13}$ Ω-cm, which is higher than the resistivity of comparable ceramic samples [15]. Donor-doped films also retain their high breakdown strengths (~ 1MV/cm) with increasing temperature (up to 125°C), as illustrated in Fig. 4, as compared to lower-resistivity, undoped films [12].

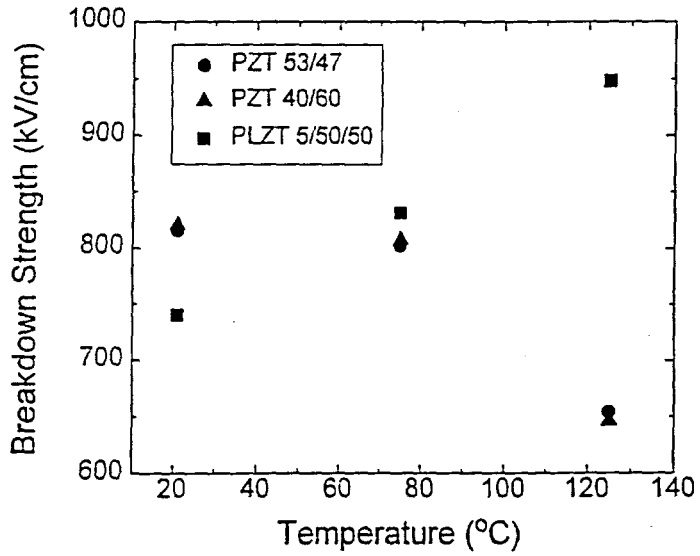

Figure 4. Temperature dependence of the breakdown strength of PZT and PLZT films as a function of temperature. All films were approximately 0.8 μm thick.

The improvement in leakage resistance due to donor doping can be qualitatively accounted for by considering the point defect chemistry. Taking the example of La doping, the charge neutrality equation based on Kroger-Vink notation, considering only the major defects, is given by

$$[La_{Pb}^{\bullet}] + 2[V_O^{\bullet\bullet}] + [h^{\bullet}] = 2[V_{Pb}''] + [A_B'] \quad , \tag{1}$$

where [] denotes concentration, $La_{Pb}^{\bullet}$ is a La^{3+} ion on a Pb^{2+} site, $h^{\bullet}$ is an electron hole, A_B' is an acceptor impurity, such as Fe or Cu, on a B (Ti, Zr) site, and $V_O^{\bullet\bullet}$ and V_{Pb}'' are oxygen and lead vacancies, respectively. Without La additions, Pb loss due to volatility of PbO and/or the unintentional incorporation of impurities generates defects that can increase conductivity, since holes and possibly oxygen vacancies are expected to be mobile over the investigated temperature range [16]. In the case of thin films, V_{Pb}'' appear to be the dominant acceptor

defect [12]. However, $La_{Pb}^{\bullet}$ defects can charge compensate the acceptor defects (V_{Pb}'', A_B'), which results in a dramatic decrease in the concentration of the "mobile" defects ($h^{\bullet}$,$V_O^{\bullet\bullet}$) and, therefore, in the leakage current density. An equation similar to Eq. 1 could be written by substituting $Nb_B^{\bullet}$ for $La_{Pb}^{\bullet}$, where $Nb_B^{\bullet}$ is a Nb^{5+} ion on a B site.

While these PZT-based thin films have excellent characteristics for decoupling capacitors, ultimately, their successful use for this application will probably be determined by lifetime considerations. Typical specifications for decoupling capacitors in accelerated life tests are that they exhibit less than an order of magnitude increase in leakage current density (resistance degradation) after 1) 1000 hrs at 125°C and twice the rated operating voltage, and 2) 1000 hrs at 85°C and 85% relative humidity and four times the rated operating voltage. For most current digital applications, the rated operating voltage is 5V, but this value will keep dropping with new generations of devices. Representative current-time measurements for a 0.8 μm thick PNZT 3/40/60 film at 125°C are plotted in Fig. 5 for two different voltages. For these films, the typical 125°C lifetime determined by resistance degradation at 20 V (4 x rated voltage) is over 250 hrs. If the thin films obeyed a $\tau \alpha V^{-n}$, where $n > 2$, relationship similar to ceramic multilayer capacitors [17], then the extrapolated lifetime at 10 V would be greater 1000 hrs. While these results are very encouraging, more extensive testing will be required.

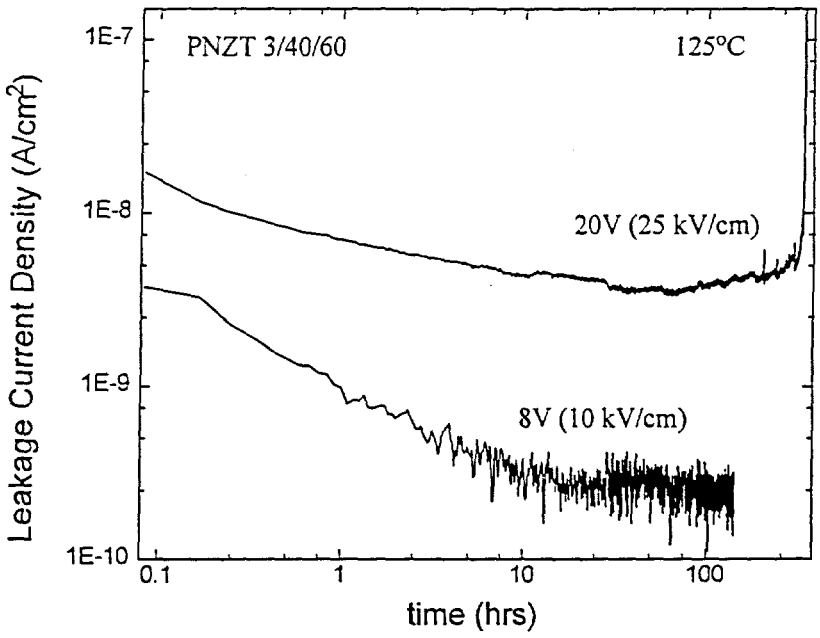

Figure 5. Leakage current density vs time (accelerated life testing) for a PNZT 3/40/60 thin film (0.8 μm thick), indicating a mean time to failure of roughly 250 hrs for 20 V and 125°C.

Increasing the lifetime can also be accomplished by increasing the dielectric thickness, which decreases the applied field on the sample. However, increasing the dielectric thickness decreases the capacitance/area (C/A) of the device. Since the lifetime and the leakage resistance both scale roughly as V^{-n} ($n > 2$) [17, 13], the improvement in lifetime (and leakage resistance) due to an increase in the dielectric thickness can be significantly greater than the resultant loss in C/A ratio. In addition, the capacitor yield increases dramatically with increasing film thickness. For 5V decoupling capacitors, a suitable compromise between C/A ratio, lifetime, leakage resistance, and yield is obtained for a film thickness of ≈ 0.8-1.0 μm.

This thickness leads to C/A(5V) ≈ 10 nF/mm^2 for PLZT 5/50/50. Furthermore, the steady-state leakage current of a 50 nF decoupling capacitor with a thickness of about 0.8 μm, based on Fig. 3, would be < 0.02 nA at 5V and 125°C. However, one drawback of using films > 0.5 μm is that two crystallization anneals at 650°C will probably be required.

INTEGRATION OF THIN-FILM CAPACITORS

Finally, it is important to consider various ways of utilizing and integrating thin-film capacitors. At the simplest level are discrete thin-film decoupling capacitors, such as the ones that have been incorporated in the prototype digital signal processing MCM of Fig. 6. This MCM design, which represents a 10x reduction in size over a comparable circuit board implementation, contains numerous capacitor arrays with either three or six independent decoupling capacitors (~ 40 nF) on each array piece. The inner circle of each capacitor is the Pt top electrode (2.5 mm diameter). The slightly larger dark ring is the PLZT film that extends beyond the top electrode, and the rest of each piece is a continuous Pt bottom electrode. An important reason for using thin-film capacitors in this application is geometrical in that the thickness of the capacitor substrates could be matched to that of the ICs (processors, ASICs, memories) and the capacitor arrays could be sized to fill the space between the different ICs. The result is a space-filling, planar array of ICs and capacitors that is compatible with the Geneal Electric high-density interconnect (HDI) technology.

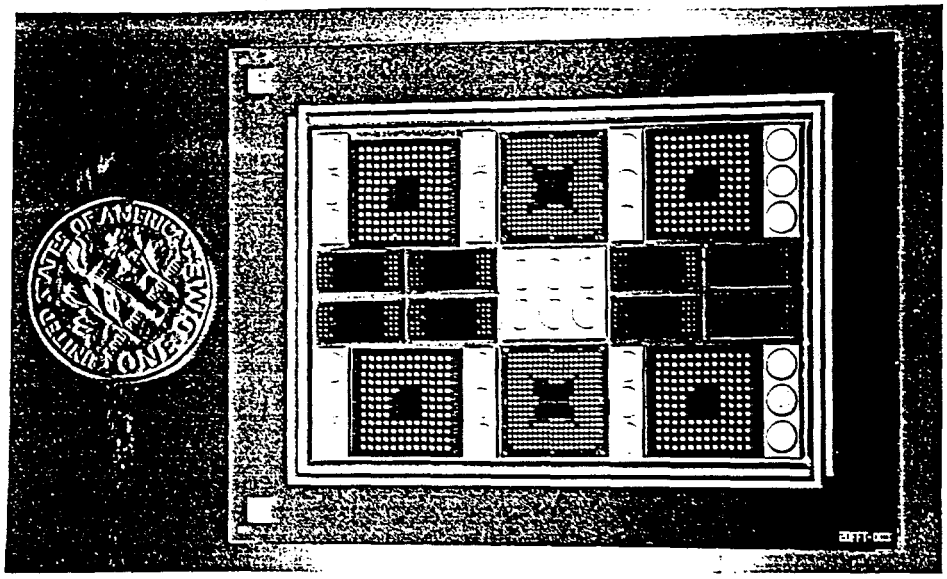

Figure 6. High-density multichip module for 2D-FFT image correlation that incorporates thin-film decoupling capacitors. The dime is to provide a size reference.

Another reason for preferring thin-film decoupling capacitors over ceramic chip capacitors is that single-layer, thin-film devices intrinsically have lower inductance than multilayer capacitors, due to the mutual inductance between the internal counter electrodes. In addition, thin-film capacitors on Si substrates can be handled and mounted like ICs in MCM packages. To make these thin-film capacitors compatible with direct chip attach formats, we have developed a version of discrete thin-film capacitors with solder bump bonds. A spin-on glass layer is used as a nonwetting layer to confine the solder to the exposed Pt pads, as

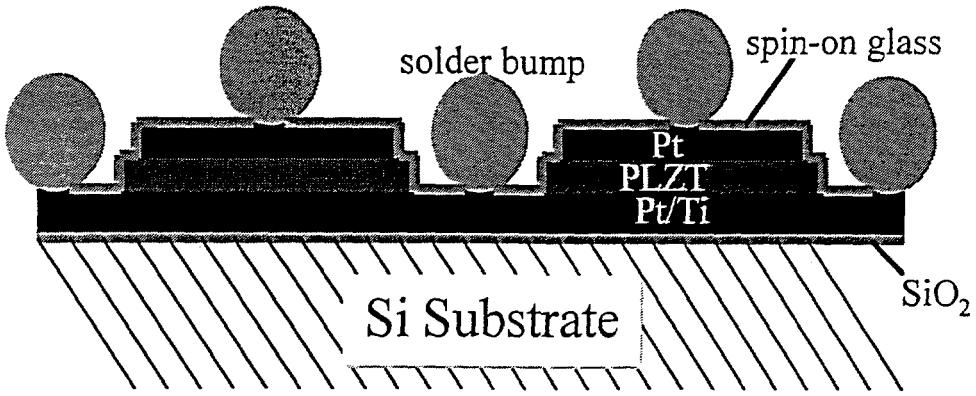

Figure 7. Schematic cross section of part of a solder bump-bonded, thin-film capacitor wafer. The topography of the capacitor is exaggerated with respect to the solder bumps, which are 10 mil high, to emphasize detail.

illustrated in the schematic diagram in Fig. 7. Multiple solder bumps to both the top and bottom electrodes can be patterned to distribute the connection and further minimize the inductance.

While the ability to provide discrete capacitors with low inductance and specific geometries is useful for many applications, the full potential of a thin-film capacitor technology will only be realized by fully integrating the capacitors with the IC or the package. The highest level of integration is obtained by incorporating the thin-film decoupling capacitor into the IC. An example of this approach is the Matsushita GaAs MMICs with integrated BST decoupling capacitors [18]. However, this level of integration, which requires a dedicated IC line, will not be appropriate for most applications. A more general approach is to mount a thin-film capacitor directly on an IC. This approach can be used to provide on-board decoupling capacitors for chip-scale packaging technologies. To be compatible with a mini Ball Grid Array (mBGA) repatterning approach to chip-scale packaging, the capacitor needs to be thin (≤ 5 μm).

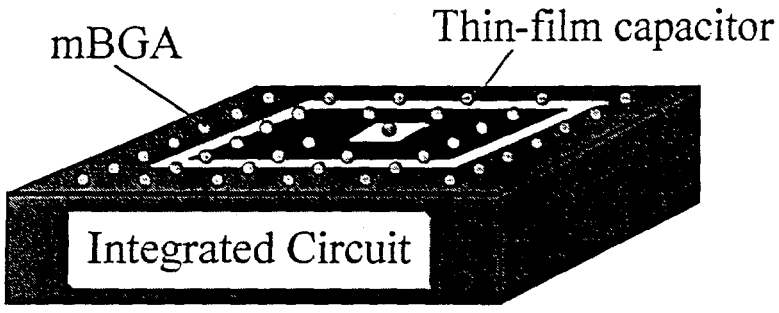

Figure 8. Schematic diagram showing thin-film capacitor integrated into a repatterned IC.

The capacitance/area (C/A) required for on-board decoupling capacitors has been estimated to be ≤ 100 nF/cm^2. This estimate corresponds to a 50 nF decoupling capacitor covering about 50% of the surface area of a 1cm^2 ASIC or a 20 nF capacitor covering about 75% of the area of a 0.25 mm^2 memory. However, a C/A $\sim$ 100 nF/cm^2 may not necessarily require a high-permittivity dielectric film. For example, this C/A value could be obtained with a SiN film 60-80 nm thick or a Ta_2O_5 film 175-200 nm thick. Furthermore, it may be possible to fabricate these low-permittivity films directly onto finished ICs, since these materials can be

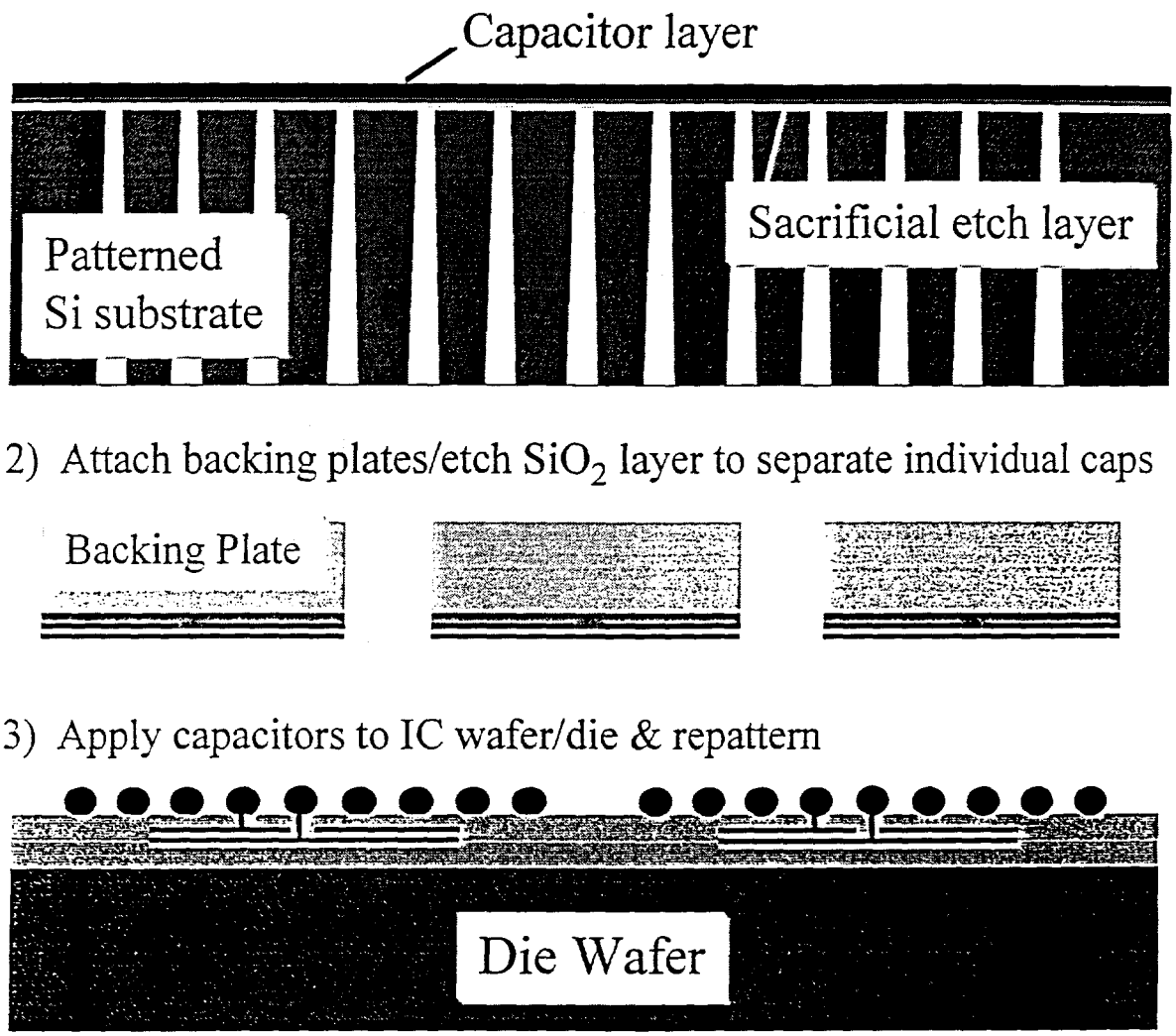

Figure 9. Schematic of the main process steps for an applique capacitor technology.

deposited at temperatures < 400°C, which is about the maximum permissible temperature for a metallized IC.

Nevertheless, high-permittivity films may be necessary if the thicknesses for the low-permittivity films are too thin to meet lifetime/leakage resistance requirements or to provide a high (~ 100%) yield. For this case, the higher processing temperature needed to produce high-quality, perovskite thin films dictates that the capacitor first be fabricated and then mounted onto the IC. To make the capacitor compatible with a chip-scale packaging technology, such as mBGA, we are developing an applique process that permits the thin-film capacitors to be separated from the carrier substrate, creating a "free-standing" thin film that can be reapplied to the IC. Separating the capacitor from the IC can be done using a combination of Si bulk micromachining and a sacrificial (SiO_2) etch, as illustrated in Fig. 9. The substrate is a double-side polished (100) Si wafer with a thin buried oxide (~ 0.5 μm), that is covered by ~ 2 μm of Si and a 0.5μm thermal oxide. After etching channels with KOH from the back side of the substrate to the buried oxide layer, the top capacitor layer can be removed from the substrate by sacrificially etching the buried oxide layer. Prior to the sacrificial etching, the capacitor

structure (with the 2 μm Si and thermal oxide layers) would be bonded to a backing plate to permit easy handling and to protect it during sacrificial etching. The thin capacitor can then be attached to the IC and debonded from the backing plate, allowing the capacitor to be interconnected using a standard wafer repatterning (mBGA) process. The result is a chip-scale package with an integrated decoupling capacitor.

Finally, a potentially very important approach to passive component integration is through the use of thin films to form capacitor, resistor-capacitor (RC), and resistor-capacitor-inductor (RCL) networks. The idea is to fabricate these networks on silicon substrates using mutually compatible thin-film processes. The big advantages of the thin-film approach are that these passive integrated circuits (PICs) can be easily customized and that the PICs can be packaged and assembled like any other IC. In fact, such PICs are already commercially available in limited forms. One of the limitations has been on the capacitance values obtainable, since SiN has been the primary thin-film dielectric. However, this limitation can clearly be overcome by utilizing high-permittivity thin films. For RC networks, conductive oxide films, such as RuO_2 and $(La,Sr)CoO_3$, may also be used for thin-film resistors since they have appropriate resistivities (100-300 μΩ-cm) and are process compatible with the perovskite dielectric thin films.

CONCLUSIONS

High-permittivity, perovskite thin films, particularly donor-doped PZT films, are well suited for developing integrated capacitors for advanced packaging applications. The chemical solution deposition method is probably the optimal processing approach for this application due to its low cost and high throughput. The PZT films have acceptable TCC, dissipation factors, leakage resistances, and breakdown strengths. Initial accelerated life tests for Nb-doped films are also very encouraging. It has also been shown that these thin films are compatible with a variety of integration approaches, which should allow them to impact a wide range of packaging technologies.

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