Packaging a 650V/400A GaN Half-bridge Power Module with Ultra-low Parasitics for Electric Vehicle Drive Applications

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***Abstract*— This paper proposes a compact and efficient half-bridge power module with three 650 V / 150 A GaN dies in parallel. The power module incorporates a main power printed circuit board (PCB), an interface PCB, and a flex PCB to achieve low parasitics in both power loop and gate-side connection, resolving the issue of high parasitics typically encountered with wire bonding in high-current applications. Additionally, the interface PCB decouples the design constraints between the power loop and the gate loops. The proposed design is optimized with a vertical loop configuration to reduce power loop inductance through magnetic flux cancellation. Finite element analysis indicates that the power loop inductance is 0.58 nH at 100 MHz, while the maximum die junction temperature reaches 131 °C under an ambient temperature of 65 °C and a load current of 385 A. The proposed multi-piece PCB structure reduces the inductance of the drive circuit to minimize EMI and to mitigate false triggering. At the same time, it reduces impedance mismatches across different driver circuits, thereby achieving dynamic current sharing in multi-chip parallel configurations. Under simulation conditions of 400 V / 385 A, the current imbalance among chips was limited to 5 A. A 400 V / 385 A double-pulse test was conducted to experimentally validate the performance of the proposed power module.**

Keywords*— *electric vehicle, GaN HEMT, multi-chip power module packaging, planar interconnection

I. INTRODUCTION

THE enhancement-mode (E-mode) gallium nitride (GaN) high-electron-mobility transistor (HEMT) features high switching speed and low conduction loss, enabling high switching frequencies with improved operational efficiency [1][2][3]. Additionally, GaN demonstrates a potential for cost reduction in high-current scenarios within medium-voltage applications, compared to silicon or silicon carbide (SiC) devices. However, in electric vehicle (EV) applications, power devices are often connected in parallel to provide rated currents of up to several hundred amperes for the motor [4]. GaN devices on the market are usually rated at lower current compared to SiC or Si. Therefore, multi-chip parallel configuration is essential to deliver the required high current. On the other hand, the high switching speed of GaN devices also makes them more sensitive to parasitic parameters induced EMI noise [5][6][7]. Therefore, a high-voltage and high-current GaN power module is developed in this paper.

Traditional power module packaging techniques such as wire bonding shown in Fig. 1(a) [8] introduce significant parasitic inductances both in power loop and gate loop, which cause a severe switching oscillation for the drain-source voltage and gate-source voltage during the switching transients. In this case, the planar structure like printed circuit board (PCB) shown in Fig. 1(b) [9] is proposed to mitigate the parasitic inductances. However, it cannot further reduce the inductance due to the external layer of gate loop, which will further extend the thickness of the PCB and power loop. An embedded PCB structure is shown in Fig. 1(c) [10], which decouples the gate loop from power loop by arranging the power loop in external PCB layers and gate loop in internally embedded layers. However, since the GaN device is embedded in the PCB, a large thermal resistance is introduced which limits its application in high current applications. The double sided cooling package with silver sintering technology shown in Fig. 1(d) [11] has been proposed with its good thermal performance and low parasitics in the power loop; however, because the gate driver cannot be integrated in the module, it introduces a large gate impedance and impedance mismatch due to different gate loop lengths in multi-chip applications.

As a result, this paper proposes a GaN power module with multi-pieces PCB, as shown in Fig. 2 to realize both low thermal resistance and small parasitic inductance. Given that multi-chip power module imposes strict requirements for synchronous switching and gate-drive impedance matching, an interface PCB is introduced here to decouple the gate loop and power loop, as well as reduce the gate loop for better dynamic current sharing.

The remainder of this paper is organized as follows. In Section II, the structure of the proposed GaN power module is discussed. The analysis of electrical and thermal

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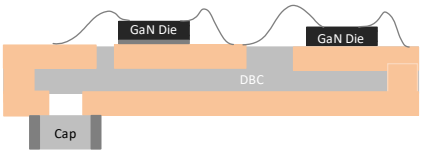
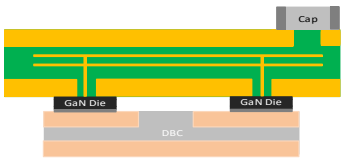
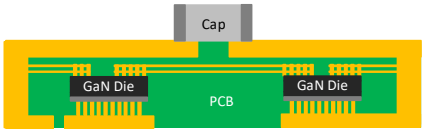
performance is shown in Section III. Power module assembly and experimental results are presented to validate the proposed power module in Section IV and V, followed by the conclusion.



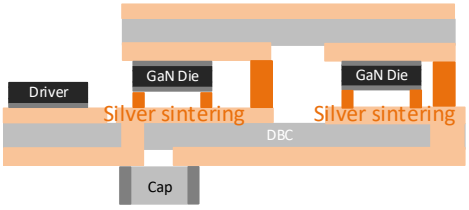
(a) Direct bond copper packaging method. [8]



(b) PCB+DBC hybrid packaging method. [9]



(c) PCB embedded packaging method. [10]



(d) Double sided DBC cooling packaging method. [11]

Fig. 1. Simplified diagrams of different sturctures of GaN power modules.

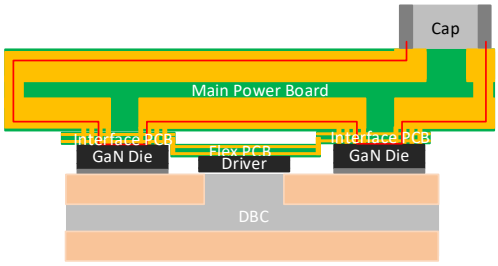


Fig. 2. Cutview diagram of the proposed GaN power module with multi-piece PCBs.

II. Sturcture of the Proposed GaN Half-Bridge Power Module

The power-loop parasitic inductance is one of the most critical parameters for the GaN power module that would cause high voltage overshoot due to the high *di*/*dt* of the GaN device during the switching transient, which can be as large as tens of A/ns [8]. The common method to mitigate the loop inductance is to create a vertical loop to achieve magnetic flux cancellation, as shown in Fig. 3. The inductance can be calculated as [13]

$$L_p = \mu_0 \mu_r \frac{ld}{w} \tag{1}$$

where l, d and w are the length, width, and thickness of the vertical loop, respectively. μ_r is the relative magnetic permeability of the insulating material, and μ_0 is the vacuum permeability. According to (1), L_p is linear with loop thickness, which explains why the method in Fig. 1(b) will increase the power loop inductance due to the thicker copper layer and isolation layer for the gate-drive loop.

The proposed GaN power module introduces a thin interface PCB between the GaN device and main power board for gate and source connection; it does not introduce an extra thickness for the whole board. Fig. 4 shows a comparison between the traditional design and the proposed GaN device and PCB interconnection method. Although the overall height of the GaN power module is the same, the effective thickness, when calculating power loop inductance, can be reduced from 1080 µm to 800 µm, exhibiting a 26% reduction. Also, the proposed GaN power module shows the advantages of simplified mechanical fabrication compared to the PCB interconnection method of the traditional design due to the different fabrication requirements of power loop and gate loop.

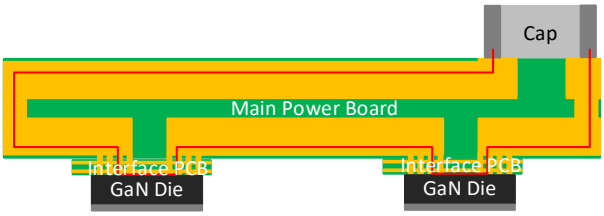
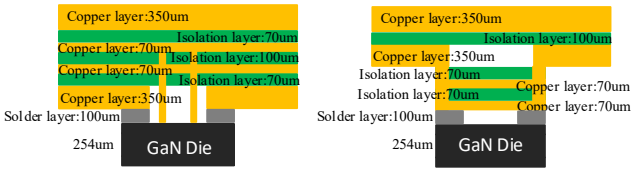


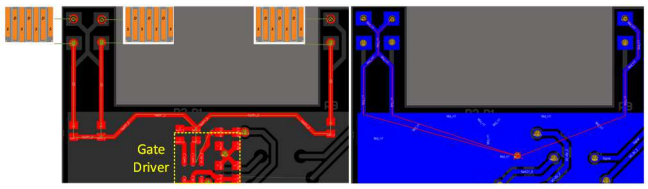
Fig. 3. Current commutating path (red) of the proposed GaN power module.



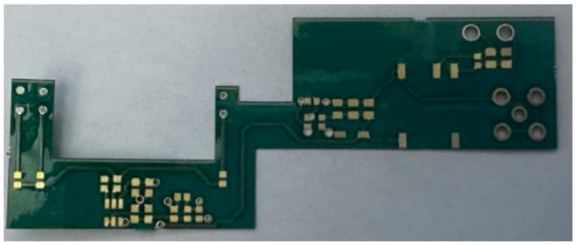
(a) traditional (b) proposed method

Fig. 4. Comparsion of the thickness between (a) the traditional design and (b) the proposed power module.

The gate-drive loop inductance is another critical parameter for the GaN power module. Large gate inductance will increase the risk of switching oscillations and even sustained oscillations. The proposed GaN half-bridge power module introduces a flex PCB and optimizes the gate loop design to realize the low parasitic inductance. The gate driver PCB is shown in Fig. 5. Each gate-drive loop is realized with the optimized vertical loop and approximately equal distance to realize low and identical inductance during switching transients.



(a) Front view (b) Bottom view

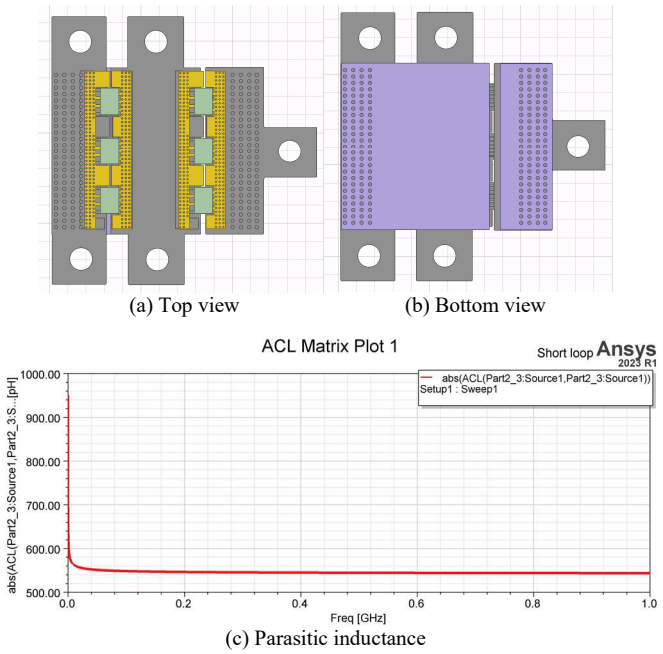


(c) Front view of the flex PCB prototype

Fig. 5. Gate loop path of the flex PCB gate driver.

III. Analysis and Simulation of the Proposed GaN Half-Bridge Power Module

An ANSYS simulation model of the proposed three-die parallel half-bridge power module is shown in Fig. 6. The simulation results show that the parasitic inductance of the power loop of the proposed GaN power module is 0.55 nH. In comparison, the parasitic inductance of the PCB+DBC hybrid structure shown in Fig. 1(b) is 0.70 nH, indicating that the proposed method reduces the parasitic inductance by 21.5 %.



(a) Top view (b) Bottom view

(c) Parasitic inductance

Fig. 6. (a) Top view and (b) bottom view of simplified model of GaN power module in ANSYS Q3D Extractor, (c) simulation results of the inductance of the power loop.

According to the parameters extracted by Q3D Extractor, the gate loop inductance for each die is 7.57 nH, 8.02 nH, and 8.36 nH @ 100 MHz, respectively. The mismatch is ~10%. The LTspice electrical model for a double-pulse-test (DPT) circuit is shown in Fig. 7 with the aforementioned extracted parameters. The turn-on and -off transients are shown in Fig. 8. The maximum dynamic current unbalance is only 2 A during turn-on transient and 5 A during turn-off transient under 400 V / 400 A operation.

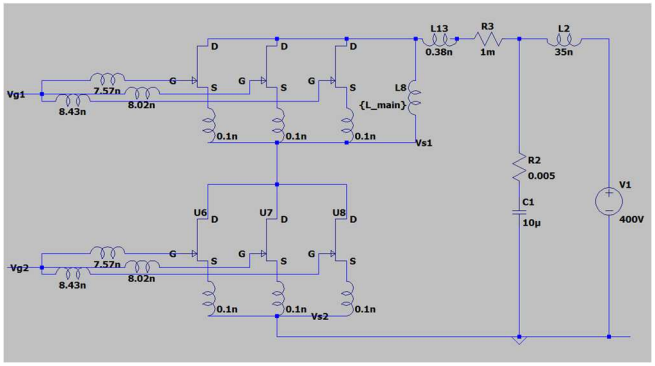
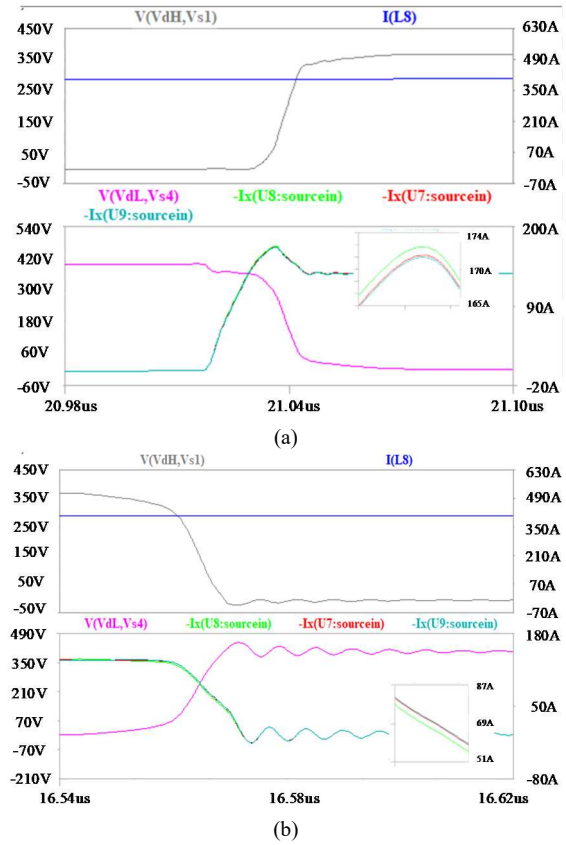


Fig. 7. Circuit simulation model of DPT circuit for the proposed power module in LTspice.

The thermal path is shown in Fig. 9. The thermal simulation result is shown in Fig. 10; with ambient temperature of 65°C, the maximum junction temperature of the paralleled dies in the proposed power module will increase to 131 °C at a load current of 280 Arms. The overall thermal resistance is calculated as 0.84 °C/W.



(a)

(b)

Fig. 8. Waveforms of drain-source voltage and source current during the (a) turn-on transient and (b) turn-off transient under 400 V / 400 A (7 V, 3 Ω on / -2 V, 2 Ω off).

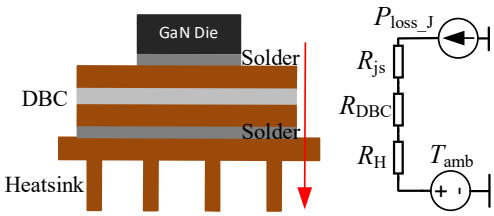


Fig. 9. Simplified diagram of thermal path and thermal model of the proposed power module. (R_{js} is the thermal resitance from junction to substrate. R_{DBC} is thermal resistance of DBC, and R_H is the thermal resistance of heatsink. P_{loss_J} is the power loss of the GaN die, T_{amb} is the ambient temperature). [11]

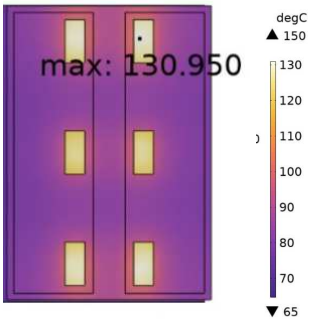


Fig. 10. Thermal simulation of the GaN die junction temperature with the loss of 78 W (per die).

IV. Assembly of the Proposed GaN Half-Bridge Power Module

The laminating process of the proposed GaN half-bridge power module is shown in Fig. 11, which includes multiple steps: 1) 300 °C solder paste (Sn10Pb88Ag2) is used with a hot plate to solder the interface PCB to the main board PCB; 2) 220°C solder paste (Sn96.5/Ag3/Cu0.5) is used with infrared reflow oven or hot plate to solder the dies and flex PCB onto the interface PCB; and 3) 183 °C solder paste (Sn63/Pb37) with hot plate is used to solder dies and DBC. The exploded view of the module is shown in Fig. 12. Key parameters of the proposed GaN power module are summarized in Table I.

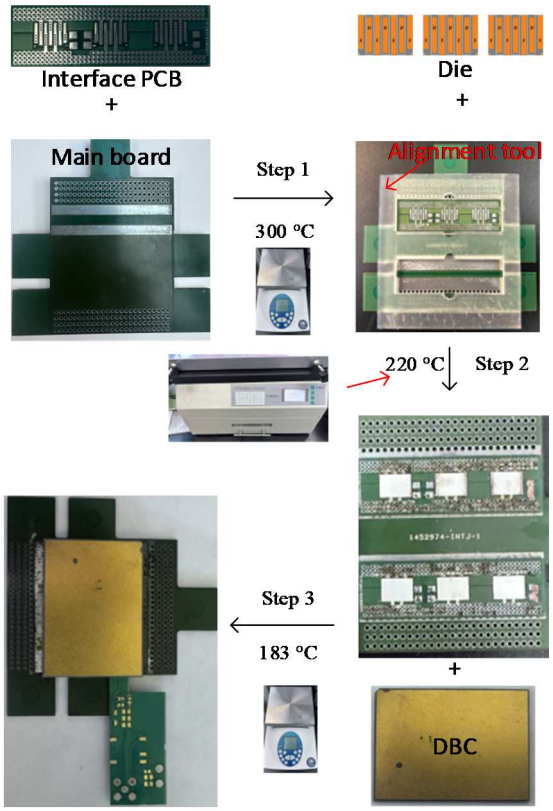


Fig. 11. Lamination steps for the proposed GaN power module.

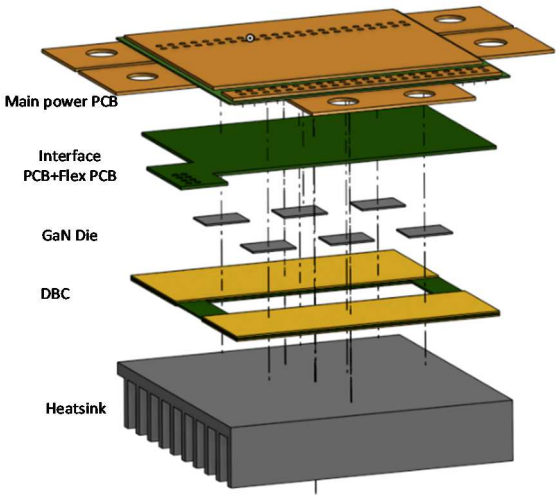


Fig. 12. Exploded view of the proposed GaN power module.

V. Experimental Results of Power Module

The proposed GaN power module is prototyped and tested with a DPT setup shown in Fig. 13. The DPT experiment is realized without DBC attached due to the probe connection. Experimental waveforms are shown in Fig. 14, where I_L is the load current and V_{dsL} (V_{dsH}) is drain-source voltage of low-side (high-side) devices. V_{gsdig_signal} is the signal input of the gate driver. According to the measurement, the voltage spike is only 12 V at 200 V / 115 A and 70 V at 400 V / 385 A. The experimental results validate the performance of the proposed GaN power module.

TABLE I. Key Parameters of the Proposed Power Module

Description	Parameter
DBC thickness	0.63 mm
GaN Die	0.254 mm
Interface PCB thickness	0.5 mm
Main power PCB thickness	0.8 mm
Copper thickness of interface PCB	1 oz
Copper thickness of main-power PCB	10 oz
Overall thickness	2.484 mm
Width of power module	60 mm
Length of power module	75 mm
Power module volume	11.12 cm^3

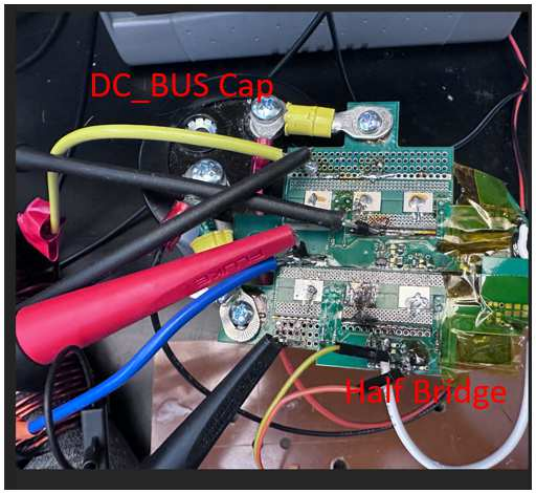
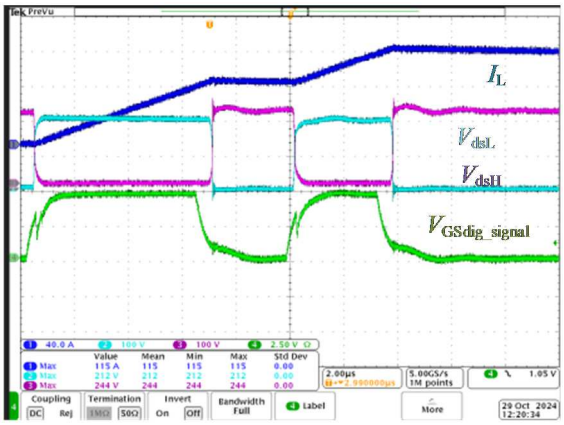


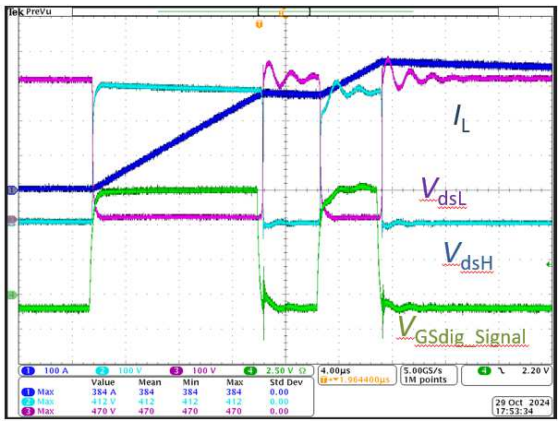
Fig. 13. Prototype of the DPT platform.

VI. Conclusions

This paper proposes a novel GaN power module structure employing multi-piece PCBs. Through simulation analysis, its low parasitic parameters, excellent impedance matching capability, and good dynamic current sharing in paralled dies are verified. Thermal simulation analysis demonstrates that, under a 400 A load and a 65 °C ambient temperature, the temperature rise is 66 °C. The paper further outlines the manufacturing process, highlighting the convenient operability advantages of the power module during production. Finally, a DPT platform is established to validate the reliable switching capability of the power circuit at 400 V / 385 A, with a transient overvoltage of 70 V. The future work includes applying the proposed power module in systems such as motor drive of electric vehicles.



(a)



(b)

Fig. 14. DPT results of different input voltages and currents: (a) 200 V/115 A and (b) 400 V/385 A.

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