

A Compact, Highly Scalable, Low-Power, and Multi-Channel Charge Digitizer for Beam Profile Monitoring

E. M. Muller

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Invited Paper: A Compact, Highly Scalable, Low-Power, and Multi-Channel Charge Digitizer for Beam Profile Monitoring

Trevor Reay^a, Michelle L. Pyle^b, John Carmen^a, Taylor Barton^a, Nina R. Weisse-Bernstein^b, John Smedley^c, Erik M. Muller^d, Ryan Tappero^d, Richard L. Sandberg^a, and Shih-hua Wood Chiang^a
^aBrigham Young University, Provo, UT USA, ^bLos Alamos National Laboratory, Los Alamos, NM USA, ^cSLAC National Accelerator Laboratory, Menlo Park, CA USA, ^dBrookhaven National Laboratory, Brookhaven, NY USA

Abstract—This paper describes a compact, highly scalable, low-power, and multi-channel charge digitizer (MCCD) for particle accelerator beam profile monitoring. The MCCD utilizes charge amplifiers, voltage amplifiers, programmable-gain amplifiers (PGAs), and ADCs to amplify and digitize input signals. The MCCD also demonstrates a novel stackable PCB design to easily reconfigure the channel count. Measurement results show a sample rate of 200 Hz, gain of 6.64×10^{11} V/C, noise of $1.36 \times 10^5 e_{rms}$, and power of 97 mW/channel. The MCCD has been successfully tested at the NSLS-II particle accelerator for beam profile monitoring.

Index Terms—Charge amplifier, transimpedance amplifier, beam profile monitoring, multi-channel readout

I. INTRODUCTION

Beam profile monitoring for particle accelerators measures the profile, position, and intensity of the beam for imaging, spectroscopy, and scattering experiments [1]–[3]. The electronics collect charge from a detector, amplify, filter, and digitize the signals for beam monitoring and data analysis. The detector type and channel count vary widely depending on the application, requiring a highly reconfigurable and scalable electronics for maximum flexibility. In addition, the electronics need to be portable to facilitate easy transportation and setup for the tight experiment schedules at accelerator facilities. Conventional beam profile monitoring utilizes commercial, standalone benchtop systems such as femtoammeters or electrometers [4]–[8]. The FEMTO DDPCA-300 is simple and configurable, but it has only one channel and no analog-to-digital conversion [4]. The Keysight B2985B has high precision, wide input range, and wide bandwidth, but it has only one channel and is bulky [5]. The Keithley 6485 has good precision, a bandwidth of up to 1000 readings/second, and a 2500-point storage buffer, but it also has only one channel

and is bulky [6]. For beam profile monitoring requiring more than a handful of channels, using multiple benchtop instrument pieces is neither scalable nor portable, and the capital expenses can be high. Single-chip solutions such as TI AFE0064 [9] and DDC264 [10] offer 64-channel processing, but they have limited customizability and limited visibility to internal signals for troubleshooting. In addition, the tight proximity of the chip input pins (400- μ m pitch) may suffer from excessive coupling between adjacent channels for sensitive measurements.

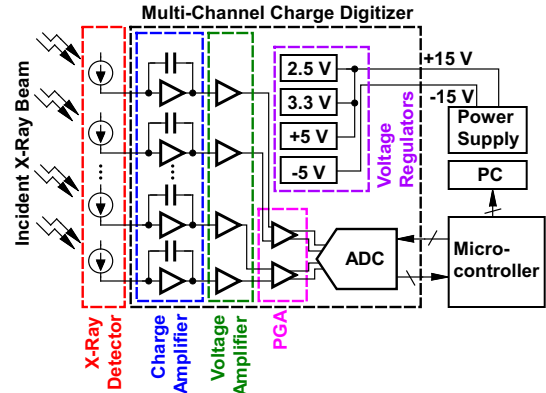


Fig. 1: Proposed multi-channel charge digitizer for beam monitoring in particle accelerators.

In the work, we propose a beam profile monitor that strikes a balance between the existing single-channel benchtop instruments and existing multi-channel single-chip solutions in terms of flexibility, scalability, and performance. The proposed “Multi-Channel Charge Digitizer” (MCCD) (Fig. 1) consists of an array of charge amplifiers for charge integration, voltage amplifiers, programmable-gain amplifiers (PGA), and an analog-to-digital converter (ADC) which communicates with a microcontroller. The MCCD is highly scalable to different numbers of channels by stacking multiple PCBs using a novel system named “staggered through-PCB pins” (STPP). The STPP provides both mechanical support and electrical connectivity between PCBs, making the MCCD modular and easy to reconfigure. The MCCD achieves a sample rate of 200 Hz, gain of 6.64×10^{11} V/C, noise of $1.36 \times 10^5 e_{rms}$, and

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power of 97 mW/channel. The MCCD has been successfully demonstrated in a particle accelerator to monitor high-energy X-ray beams.

II. MULTI-CHANNEL CHARGE DIGITIZER

The MCCD contains 32 channels on 4 stacked PCBs, with each PCB employing 8 channels. Each channel consists of a charge amplifier, a voltage amplifier, an optional level shifter, and a programmable-gain amplifier (Fig. 1). An 8-channel ADC digitizes the channels and communicates with a microcontroller for data transfer. In addition, the microcontroller controls the timing of the circuits in the MCCD. The charge amplifier integrates the charge from the X-ray detector on a feedback capacitor to output a voltage (Fig. 2). The voltage is amplified by an op amp. After the voltage amplifier, a level shifter shifts the common-mode, and a PGA amplifies the signal by a user-selectable gain (1 to 100). The output of each channel is digitized by the 8-channel ADC. The ADC communicates with the microcontroller via an SPI interface.

The gain of the charge amplifier (TI IVC102) is about $1/C_{fb}$ where C_{fb} (10 pF) is the feedback capacitor. Any parasitic capacitance parallel to C_{fb} due to PCB layout effectively increases C_{fb} and reduces the gain. Since the input and output pins of the charge amplifier are close to each other, the trace length between them is kept as small as possible. In addition, each channel has identical routing to reduce gain mismatch between channels. During the reset phase, both S_1 and S_2 switches (Fig. 2) are on, and the charge on the feedback capacitor is cleared. Then, during the integration phase, S_2 turns off, allowing the input charge from the detector to integrate on the capacitor ($T_{int} = 100 \mu s$ in our design). Finally, S_1 turns off to hold the output voltage during the hold phase. Charge injection and clock feedthrough from switches S_1 and S_2 can cause spikes during transitions. Fortunately the charge amplifier has on-chip feedback capacitors and switches, which significantly reduce the aforementioned issues compared to discrete switches and capacitors. The voltage error V_{error} due to charge injection is inversely proportional to C_{fb} . A small C_{fb} results in larger V_{error} , but also larger gain. We choose C_{fb} to be 10 pF, which provides an acceptable gain and adequately small V_{error} . Smaller C_{fb} will incur a higher V_{error} . Furthermore, we adopt the correlated double sampling (CDS) to reject V_{error} . This is illustrated in Fig. 2, where we sample the charge amplifier output V_{out2} just before and after the integration phase to obtain V_1 and V_2 . We then take the difference between the two samples to obtain ΔV which removes V_{error} to the first order. The unit-gain bandwidth of the charge amplifier is 2 MHz [11]. Note that signals at integer multiples of $1/T_{int}$ are nulled by the integrator.

Following the charge amplifier is the voltage amplifier (ADI LT6202CS5), which utilizes an inverting configuration with resistors to provide a gain of 4 to suppress the noise from the subsequent stages. An additional feedback capacitor improves the stability and settling time of the amplifier. The dual supply for the charge amplifier and voltage amplifier allows for the detection of both positive and negative charges. After the

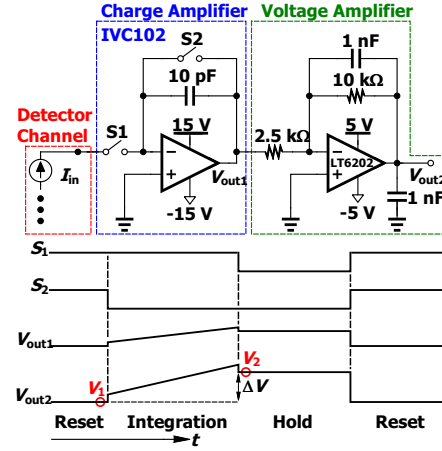


Fig. 2: Charge amplifier and voltage amplifier design and timing diagram. The integration time is $100 \mu s$ in this work.

voltage amplifier, the level shifter (ADI LT6202CS5) with resistor feedback (Fig. 3) shifts the common-mode from 0 V to 2.5 V so as to center the signal at the mid-scale of the ADC. Alternatively, the level shifter can be bypassed using ac-coupling to serve a similar function. Finally, the PGA (ADI LTC6911) amplifies the signal by a programmable gain between 1 and 100 so as to utilize the full scale of the ADC depending on the charge input amplitude. Each PGA chip contains two PGAs, thus only 4 chips are needed per PCB. The bandwidth of the amplifier stages can be limited to limit noise.

An 8-channel, 12-bit ADC (AD7928BRUZ) digitizes the PGA outputs and transmits them to the microcontroller (Arduino Uno A000066) via an SPI interface. The ADC operates at 200 Hz and the SPI at 10 MHz. The internal 8:1 mux multiplexes between the 8 PGA outputs so that all 8 channel data are available from one ADC. Since there is one ADC per PCB, if more than 1 PCB is used, the microcontroller multiplexes among the multiple ADCs using the chip select (CS) signal. When CS is low, the selected ADC begins to transmit data on the data bus while the other ADCs are in high-Z mode. In our design, the microcontroller interfaces with 4 ADCs in this manner.

Fig. 4 shows the MCCD PCB containing 8 channels. The layout for the 8 channels are arranged horizontally along one edge of the board for easy input cable installation, and the

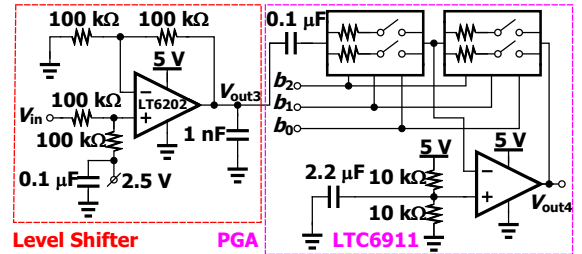


Fig. 3: Level shifter and programmable-gain amplifier design.

layout is identical for the 8 channels to minimize mismatch. The spacing (1.7 cm) between the channels at the frontend offers superior channel isolation compared to a single-chip solution where the channel spacing is small (400 μm in AFE0064) for sensitive measurements. The input utilizes the U.FL coaxial connector for its shielding, small footprint, and flexible cable to interface with the X-ray detector. The connector is placed as close to the charge amplifier as possible to minimize the trace distance for low noise. The ADC is placed on the other side of the board from the sensitive analog circuits to minimize digital noise coupling.

The MCCD utilizes a novel PCB stacking technique to increase the number of channels. Depicted in Fig 5(a), 4 PCBs are stacked to provide 32 channels. To minimize the amount of wiring needed, the MCCD utilizes a proposed “staggered through-PCB pins” (STPP) to share any common signals such as the supply and control among the PCBs (Fig. 5(b)-(d)). This way, only one external wire is needed per signal, and the STPP routes the signal to all the PCBs in the stack. By staggering the pins, all PCBs in the stack can share an identical layout, and utilize the standard male/female header pins to connect to each other. The STPP avoids the otherwise time-consuming installation of cables to connect one PCB to another; it also avoids the problem of the cables coming loose due to the tension on a bent cable between PCBs. In addition, the STPP serves as the mechanical support and spacer for the stack, obviating any standoffs which would need to be set to an exact height to accommodate the header pins. A PCB is fully connected to the power supply and all the necessary control pins as soon as it is plugged into the header pins. With the modular system, the PCBs can be individually tested and verified, then rapidly assembled for operation. Should any part of the system exhibit issues, the system can be quickly disassembled, debugged, and re-assembled. The microcontroller program that controls the timing can be updated for different numbers of channels in the system. Each PCB measures 121 mm $\times$ 167 mm and each layer is 14 mm tall. The physical volume per channel is significantly smaller than the available commercial solutions for charge measurement. The scalability limit will be set by the maximum current that can be carried in the STPP for the supply while the sample rate is currently limited by the microcontroller. An FPGA instead of a microcontroller will allow a higher sample rate.

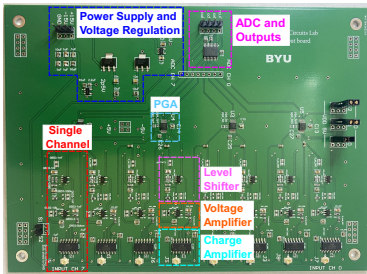


Fig. 4: 8-channel MCCD showing individual components.

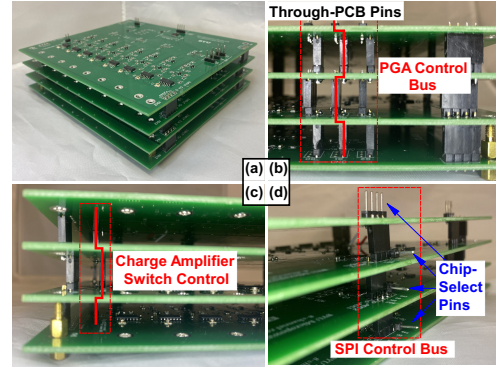


Fig. 5: (a) Stacked 32-channel MCCD and (b) (c) (d) staggered through-PCB pins for various shared signals.

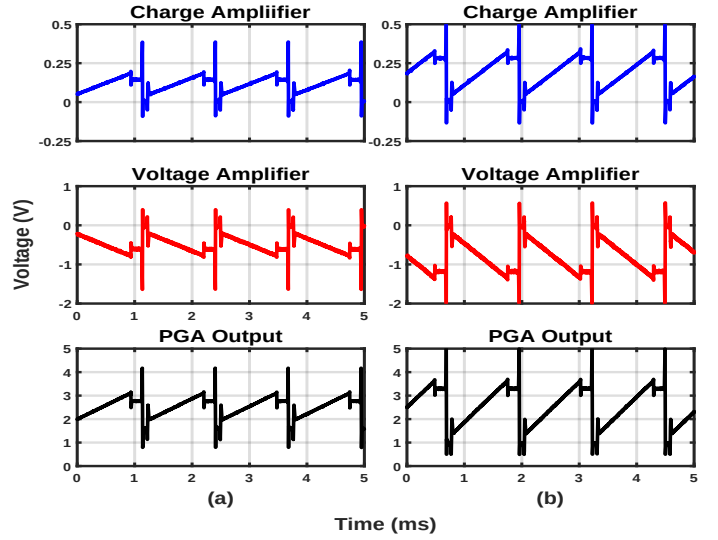


Fig. 6: Measured charge amplifier, voltage amplifier, and programmable-gain amplifier outputs with (a) 15-nA and (b) 30-nA DC input.

III. MEASUREMENT RESULTS

To validate the MCCD, a circuit consisting of an LED and a photodiode generates a tunable current that serves as the test input current I_{test} [12]. I_{test} is measured using a high-precision picoammeter (Keithley 6485) to determine its value. Next, we apply I_{test} to the charge amplifier and measure the amplifier output V_{out} after some integration time T_{int} . We can then calculate the amplifier charge-to-voltage gain $A_{Q-V} \equiv V_{out}/Q_{in} = V_{out}/(I_{test}T_{int})$, which equals $1/C_{fb,equiv}$, where $C_{fb,equiv}$ is the equivalent feedback capacitance of the charge amplifier. From our tests ($T_{int} = 100 \mu\text{s}$), $C_{fb,equiv} = 12.1 \text{ pF}$, suggesting some additional parasitics on top of the nominal capacitance value. Fig. 6 illustrates the measured charge amplifier output, voltage amplifier output ($4\times$ gain), and PGA output ($2\times$ gain) with (a) 15-nA and (b) 30-nA I_{test} . The integration ramps are clearly visible with flat reset and hold regions just before and after. The spikes are from charge injection/clock feedthrough, but they do not

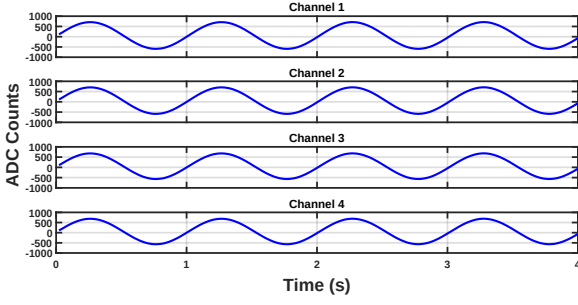


Fig. 7: Measured ADC output from 4 channels with a sinusoidal input after correlated double sampling.

affect our measurement as the ADC samples only in the settled regions. With a higher input current, the ramp in (b) exhibits a larger slope than that in (a) as expected.

We test the dynamic, multi-channel functionality of the MCCD by connecting a sinusoidal voltage source in series with a test resistor placed at the input of each channel. This injects a sinusoidal current simultaneously into the channels to observe their parallel performance and validate our readout hardware and software design. Fig. 7 shows the output from 4 channels. The waveforms are constructed using CDS to reject switch charge injection and clock feedthrough. All channels show the correct waveform with a similar amplitude and offset, suggesting good matching between the channels. Finally, the noise is measured as 12.0 ADC counts RMS, equating to $1.36 \times 10^5 e_{rms}^-$. For our application, we treat the series of fast beam pulses as quasi-continuous over the observation time (near-DC input). Other cases may require actual detection of individual pulses. Fig. 8(a) shows the MCCD test setup at 4-BM beamline of NSLS-II particle accelerator. The detector (RMD Inc., MA) converts the high-energy X-ray beam into free charges collected by the MCCD. The stepped motor slowly scans the detector position to produce the signals shown in Fig. 8(b) which is expected based on the detector pixel design. Table I summarizes the MCCD performance and compares to other existing solutions. Note that our work is charge-amplifier-based with $T_{int} = 100 \mu s$ while the others are transimpedance-amplifier-based. Our gain is programmable and the gain here is specified for PGA gain = 4. The MCCD offers an attractive volume/channel, power/channel, and cost/channel compared to existing standalone systems.

TABLE I: Performance Summary and Comparison

	This Work	DDPCA-300 [4]	B2985B [5]	6485 [6]	5015A 1010 [7]	DLPCA-200 [8]
No. of Channels	32	32	1	1	1	1
Volume (cm ³)	1128	354	6440	7106*	3772*	137
Volume per Channel (cm ³)	35	354	6440	7106*	3772*	137
Supply	±15 V	±12 V	±15 V	Wall Power	Wall Power	15 V
Speed	200 S/s	10 Hz	20 kHz	10 kHz	200 kHz	2 kHz
Gain	6.64e11 V/C	10e13 V/A	N/A	N/A	N/A	10e13 V/A
Noise	1.36e5 e_{rms}^-	2 fA_{pp}	1.4 μV_{rms}	100 nA _{rms}	N/A	0.18 $fA/\sqrt{Hz}$
Power/Channel	0.097 W	1.05 W	1 W	30 W	20 W	0.225 W
Cost/Channel	\$28**	\$300	\$13,508	\$2,890	\$7,049	\$379

*Includes power supply **Excludes NRE

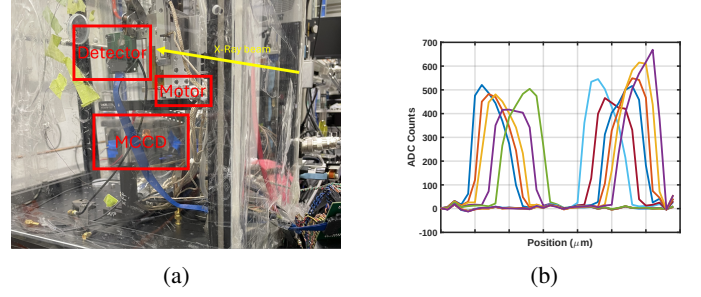


Fig. 8: (a) MCCD test setup at 4-BM of NSLS-II particle accelerator. (b) Measured beam signal versus scan position.

IV. CONCLUSION

A multi-channel charge digitizer (MCCD) is proposed for beam profile monitoring. The MCCD utilizes a charge amplifier, voltage amplifier, level shifter, programmable-gain amplifier, and ADC to amplify and digitize input signals. The MCCD consists of multiple PCBs stacked using a novel system and it can be easily scaled to up to 32 channels. Measurement results show a sample rate of 200 Hz, gain of 6.64×10^{11} V/C, noise of $1.36 \times 10^5 e_{rms}^-$, and power of 97 mW/channel. The MCCD has been successfully tested at the NSLS-II particle accelerator for beam profile monitoring.

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