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ABSTRACT

Experimental observations of dopant diffusion and defect formation are reported as a function of ion energy and implant temperature in Si implanted GaAs. In higher energy implants (>100 keV), little or no diffusion occurs, while at energies less than 100 keV, the amount of dopant redistribution is inversely proportional to energy. The extended defect density shows the opposite trend, increasing with increasing ion energy. Similarly, the diffusion of Si during post implant annealing decreases by a factor of 2.5 as the implant temperature increases from -2 to 40°C. In this same temperature range, the maximum depth and density of extrinsic dislocation loops increases by factors of 3 and 4, respectively. Rutherford Backscattering (RBS) channeling measurements indicate that Si implanted GaAs undergoes an amorphous to crystalline transition at Si implant temperatures between -51 and 40°C. A unified explanation of the effects of ion energy and implant temperature on both diffusion and dislocation formation is proposed based on the known differences in sputter yields between low and high energy ions and crystalline and amorphous semiconductors. The model assumes that the sputter yield is enhanced at low implant energies and by amorphization, thus increasing the excess vacancy concentration. Estimates of excess vacancy concentration are obtained by simulations of the diffusion profiles and are quantitatively consistent with a realistic sputter yield enhancement. Removal of the vacancy rich surface by etching prior to annealing completely suppresses the Si diffusion and increases the dislocation density, lending further experimental support to the model.

INTRODUCTION

Increasing the reliability and yields of Si, GaAs and other semiconductor devices requires accurate knowledge and control of doping profiles. As device dimensions shrink, increasingly shallower junction depths and tighter control of channel doping will be required, necessitating precise placement of dopant atoms. Of particular concern in recent years has been transient enhanced diffusion (TED) of annealed shallow implants, leading to anomalously deep junction depths.[1,2] This enhanced diffusion is a observed in many ion/target systems including B implanted Si, which has received the most attention, and Be, Mg, Zn, and Si implanted GaAs. By focusing on understanding fundamental mechanisms, knowledge gained from studying TED in one system should be applicable to modeling other ion/target combinations.

The most widely used n-type dopant for fabricating GaAs devices is ion-implanted silicon. Unfortunately, the diffusion of silicon has been found to vary over a large range of values, depending on processing conditions.[3-7] These process conditions are often not well controlled, leading to large variations in reported diffusivities and anomalous diffusion behavior.[6] Recently, Haynes and Holland reported dramatic variations in implant damage as a function of temperature

for Si implanted GaAs.[8] For example, in 6×10^{14} cm^{-2} Si implants, the effective fraction of displaced atoms at the peak of the damage profile (from Rutherford Backscattering (RBS) channeling measurements) decreased from 95 to 15% as the temperature was increased from 20 to 30°C. For this reason, the as-implanted defect morphologies of nominal "room temperature" Si implants into GaAs can vary dramatically. Moreover, the diffusion of implanted Si has been found to increase with decreasing implant energy, making shallow implants potentially more sensitive to implant temperature variations.[9,10] This variation in damage density with implant temperature and energy may be responsible for much of the discrepancy in previous studies of implanted Si diffusion.

Another factor that has not been well understood is the effect, if any, of extended defects, primarily dislocation loops, on dopant diffusion. Allen, et.al., speculated that dislocation loops might be responsible for the variation in their diffusion data.[6] In a previous paper, we reported correlations between loop density and Si diffusion and concluded that the loops were reacting to the same source of vacancies that were assisting the diffusion, although the source of the additional vacancies was not identified.[9] In this paper, we report on the effects of well controlled implant temperature and energy variations on Si diffusion and defect morphology. A relationship between defect morphology, as given by RBS channeling and transmission electron microscopy (TEM), and Si redistribution is demonstrated. We estimate the excess vacancy concentration that is needed to explain the enhanced diffusion and show that sputtering, enhanced at lower ion energies and by amorphization at the lower implant temperatures, provides a plausible source for the required number of extra vacancies. The results of this work provide a better understanding of the relationship between dopant redistribution and implant damage, and should improve the reliability and reproducibility of Si implants into GaAs and the simulation of TED in all ion/target systems.

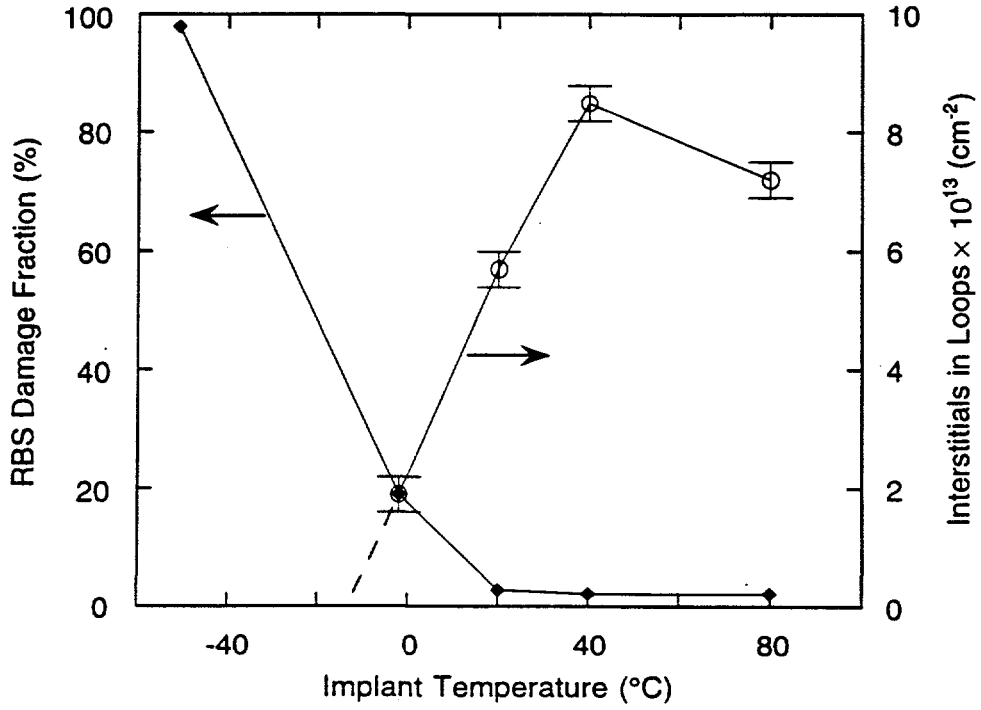

Figure 1. Concentration of interstitials bound by type I dislocation loops and RBS damage fractions vs. implant temperature. The bound interstitial concentrations were measured from PTEM micrographs.

RESULTS AND DISCUSSION

Implant Temperature

The redistribution of implanted Si during short time annealing has been found to depend strongly on the implant temperature.[9,11] As the implant temperature is decreased from 40 to -2°C, the amount of diffusion decreases by a factor of 2.5 for 900°C, 5 min anneals. Since Si diffusion in GaAs occurs via a vacancy-assisted mechanism,[6,12] the increase in diffusivity with decreasing implant temperature implies that the vacancy concentration is higher at lower implant temperatures. When the implant temperature decreases to -51°C, amorphization occurs and no dopant redistribution is observed.

The RBS channeling yield of the as-implanted samples is also a strong function of temperature, as seen in Figure 1. At temperatures above 40°C, the yield is low, indicative of a crystalline lattice with minimal damage. As the temperature decreases from 40 to -2°C, the damage fraction increases as isolated, amorphous pockets form in the GaAs. At an implant temperature of -51°C, the crystal forms a continuous amorphous layer with an average thickness of 450 Å. Also shown in Figure 1 is the change with temperature of interstitials in extrinsic, type I dislocation loops in post-implant annealed samples. The interstitial density rises sharply as the implant temperature increases. A possible mechanism for this increase, which is consistent with the diffusion data, would be a reduction in the vacancy concentration as the implant temperature rises. The maximum depth of the type I loops also increases with implant temperature, indicating that ion and recoil channeling is greater in the higher temperature implants.

Ion Energy

In a parallel set of experiments, the energy of the Si ion was varied for room temperature implants.[10] The maximum diffusivity (8×10^{-13} cm^2/sec) was found for the lowest energy (20 keV) implant. As the implant energy increased to 200 keV, the diffusivity decreased sharply, with no discernible Si redistribution observed in the higher energy (>150 keV) implants. As with the variable temperature results, the loop density was inversely proportional to the amount of Si diffusion, increasing sharply with implant energy. The increase in Si redistribution in lower energy implants suggests that near surface phenomena can affect the Si diffusivity. The nature of these surface effects is discussed in the next section.

Effect of Sputtering on Vacancy Concentration

Because Si is a vacancy diffuser in GaAs, the increase in Si diffusion at low implant energies has led to the hypothesis that excess vacancies from sputtering might be responsible for the variation in diffusion and extended defect data.[10,13] Subsurface atoms ejected form the sample would leave behind vacancies which could then recombine with interstitials, reducing the extended defect density, and couple with Si atoms, enhancing the dopant diffusion. This hypothesis appears to be supported by the literature. In a recently published paper by Malherbe, the sputter yield for Ar implanted GaAs was seen to reach a relatively sharp maximum at an energy between 10 and 40 keV.[14] The maximum sputter yield was approximately three GaAs molecules per incident Ar ion, decreasing to approximately 2 molecules/ion at an energy of 200 keV.

Variations in the sputter yield are also consistent with the changes in Si diffusion and defect morphology in the variable temperature experiments. For semiconductor targets, several studies have shown that the sputtering yield increases significantly when the wafer temperature is lowered through the crystalline to amorphous transition.[15-18] For (111) implants of 16 keV Ar into GaAs,

Farren and Scaife found the sputtering yield to abruptly decrease from 3 to 1.5 molecules/ion at a temperature of 130°C.[16] This behavior has been explained on the basis of channeling in crystals; i.e. ions and recoils which can obtain channeling trajectories in crystalline targets are less likely to suffer momentum reversing collisions.

The RBS damage fractions (Figure 1) and TEM micrographs of the as-implanted samples indicate that GaAs undergoes an amorphous to crystalline transition at around room temperature for the dose rate used in these experiments. The sputtering yield should thus decrease significantly as the temperature is increased through this transition, leading to lower surface vacancy concentrations. To evaluate the possibility that sputtering is also responsible for changes in vacancy concentration required to affect Si diffusion by the amounts found in the variable temperature experiments, computer simulations using SUPREM-IV.GS,[19] a general purpose GaAs process modeling program and TRIM89,[20] a Monte Carlo ion implantation simulator, were performed. The TRIM simulations were used primarily to determine the depth range in which excess vacancies and interstitials are produced during Si implantation. Parameters used in the simulations have been previously reported.[11] A TRIM simulation of 100,000 Si ions implanted at 40 keV into GaAs at 7° off axis was made. After adding the ion and Ga interstitial distributions (since most of the Si is believed to reside on the Ga sublattice), the excess vacancy and interstitial profiles were calculated by subtracting the total point defect profiles from one another. This results in a Ga vacancy rich surface layer to a depth of 200Å, followed by a buried interstitial rich layer. In the SUPREM simulation, both the excess Ga vacancy and interstitial profiles were read into the simulator, along with the as-implanted Si profile from SIMS. The diffusivity of silicon was chosen to correspond to the implanted value used in SUPREM-IV.GS at 900°C,[19,21] but with an electron squared dependence. This diffusivity is sufficiently small that no Si redistribution would occur during 5 minute, 900°C anneals in the absence of vacancy injection. The SIMS profile for each implant temperature was fit by adjusting the excess vacancy distribution until the simulated and experimental dopant profiles overlayed one another. The effective vacancy "doses" needed to fit the -2, 20, and 40°C annealed profiles were 2.3, 2.0, and 1.7×10^{14} cm^{-2} respectively. The decrease in diffusivity in going from a -2 to a 40°C implant is therefore caused by a 35% decrease in vacancies. The approximate 6×10^{13} cm^{-2} increase in vacancies at -2°C as compared to 40°C is the same to the number needed to dissolve the interstitial loops to the extent observed (see Figure 1), lending quantitative evidence to the conclusion that the same source of vacancies is affecting both the diffusion and change in loop density.

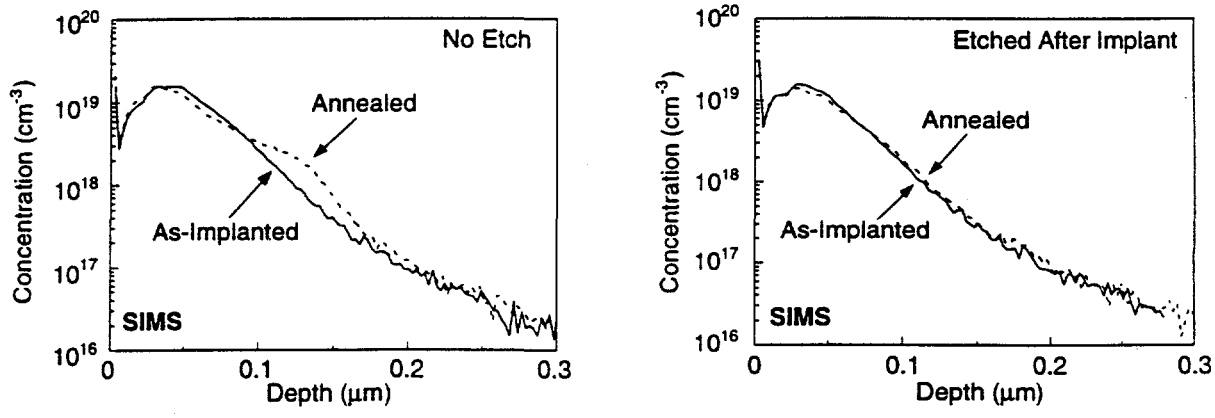

Figure 2: SIMS profiles showing the effect on Si redistribution of removing the surface vacancy layer by etching off 100Å of the substrate prior to annealing for 1 hour at 800°C.

Removal of Sputter Damage by Etching

To further confirm that surface vacancies created by sputtering are responsible for the transient diffusion observed in low energy silicon implants, 100Å of the surface was etched off after the implant but prior to annealing. A <100> semi-insulating LEC GaAs wafer was implanted at 7° off normal with 40 keV, $1 \times 10^{14}/cm^2$ $^{29}Si^+$. Before implantation, the wafer was solvent cleaned and etched to remove polishing damage. After implantation, one set of samples was etched for twenty seconds in a solution of (1:1:400) H_2O_2:NH_4OH:H_2O to remove approximately 100Å of material. Another set of samples received no etch and both groups of samples were capped with a 1000Å layer of silicon nitride using plasma enhanced chemical vapor deposition. Furnace anneals were performed at 800°C and 900°C for one hour in flowing forming gas. After etching the silicon nitride in concentrated HF, the Si concentration profiles were determined with SIMS. Plan-view TEM samples were also made using a bromine-methanol solution to jet etch the back side of the wafer. A JEOL 200CS or a JEOL 4000FX instrument was used to take bright-field micrographs with a g_{220} two-beam condition.

As seen in Figure 2, the unetched sample exhibited significant amounts of transient diffusion upon annealing. In the etched sample, however, the diffusion was suppressed. Clearly the point defects responsible for the transient diffusion were removed by the etch. Further evidence that sputtering creates an excess vacancy layer at the surface is seen in the TEM images of the etched and unetched samples (Figure 3). The etched sample contains approximately 25% more trapped interstitials than the unetched one, indicating that removal of the vacancy rich layer allows more interstitials to coalesce into dislocation loops. These results have been confirmed by TRIM and SUPREM simulations in which no diffusion occurs when the top 100Å of the surface is removed.[22]

SUMMARY

In conclusion, the amount of Si redistribution is found to decrease with increasing ion energy and implant temperature. Concomitantly, the area bound by extrinsic, type I dislocation loops increases. These observations result from an increase in vacancy concentration caused by a higher sputter yield at low implant temperatures and energies. The data has been successfully simulated by accounting for the change excess vacancies in SUPREM simulations. Removal of the surface

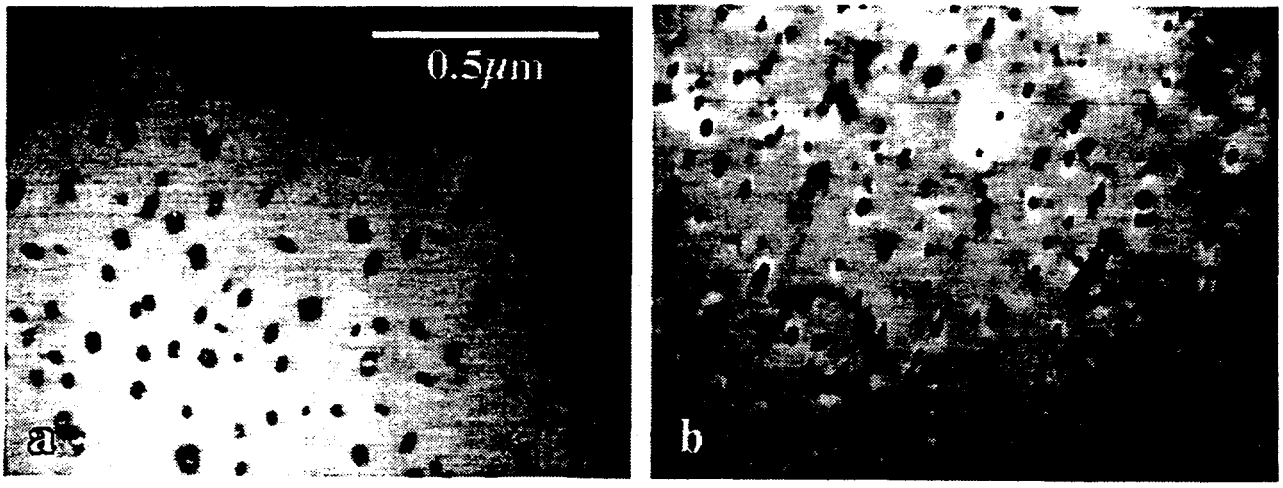

Figure 3: TEM micrographs of the annealed samples shown in Figure 2. The etched sample (b) has approximately 25% more dislocations than the unetched sample.

layer reduces the excess vacancy concentration and retards the transient diffusion while increasing the extended defect density. These results reinforce the fact that careful choice and control of implant conditions are essential for obtaining reproducible and reliable electronic devices. Accurate simulation of transient enhanced diffusion from implantation must account for sputter induced changes in the point defect concentrations.

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