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LDRD PROJECT TITLE: SIREN: Scaling Ion-Traps by REquiring iNnovative Heterogenous Integration
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ABSTRACT:

The SIREN (Scaling Ion Traps by Requiring iNnovative heterogenous integration) project explores the feasibility of heterogeneous integration (HI) as a transformative approach to scaling ion traps, a critical technology for advancing quantum computers and atomic clocks. Traditional ion trap architectures face significant challenges in scalability due to limitations in optical access, fabrication techniques, and material constraints. SIREN addresses these challenges by leveraging HI, which combines different materials and fabrication processes to create more complex and efficient ion trap structures. HI integrated structures can be manufactured without compromising the process to maintain compatibility to ion traps.

This project focuses on integrating a separately fabricated waveguide with a fully functional ion trap. The respective alignment between the pieces needs to be accurate to less than 2 μm to ensure that the light from the waveguide can overlap with the trapping region. The fine alignment must also be maintained through an ultra-high vacuum bake, a critical step in preparing an ion trap experiment.

The project's outcomes suggest that heterogeneous integration is a promising pathway for overcoming current scalability barriers, paving the way for the next generation of quantum technologies. SIREN's findings contribute significantly to the field, offering a scalable solution that could accelerate the development of practical quantum computers and highly accurate atomic clocks.

INTRODUCTION AND EXECUTIVE SUMMARY OF RESULTS:

The scalability of trapped ion technology is currently constrained by limited optical access. Trapped ions are crucial for quantum computers and atomic clocks, but to miniaturize these systems or increase the number of ions, we need to greatly increase the number of lasers into the system and reduce the space the imaging systems take. Traditional ion trap setups often face restricted optical access due to the vacuum chambers and using large lenses to collect as much light as possible. To develop systems with thousands to millions of ions, we must significantly improve the optical access. The need for increased laser access requires innovative ion trap designs and integration methods that enable more efficient and scalable optical pathways for precise ion control and measurement.

Towards these goals, the current state of the art has been to incorporate the necessary lasers directly into the ion trap surface [1-4]. This monolithic incorporation of light allows for individual sites on

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an ion trap to each have their own laser addressing without occupying large amounts of a vacuum window. These approaches have the particular benefit of lithographic alignment. By integrating the waveguides and output coupler directly into the trap, the output alignment location never changes and is determined by the lithography during fabrication. Additionally, the light and the ion are now interacting with the same surface meaning that vibrations in the ion trap are now common mode with the lasers and should not lead to increased decoherence on the signal. However, the photonic technology needed for scaling goes beyond grating couplers to include splitters, modulators, and detectors.

Combining several of these integrated technologies into a single ion trap has been challenging due to the compatibility of different fabrication methods and the sensitivity of ions. To achieve integration, some components often need to be sacrificed. From the ion trap, a gold metal coating to reduce charging and improve surface quality cannot be added. While the photonics require iterating on layer thicknesses, that may not be achieved over the entire wafer due to stresses from the trapping layers. Ultimately, each technology is compromised slightly to fabricate them together. Given the ultimate goal of high-fidelity quantum operations when millions of ions need to be stable, these trade-offs seem a little high.

Alternatively, this project studied the potential of leveraging heterogenous integration (HI) of ion traps. By showing that two different chips can be aligned at the packaging level to the necessary precision (< 1 μm) we reintroduce the possibility of making separately optimized components that are packaged together much like the quantum information's classical counterparts. These separate pieces could be fabricated in parallel and even designed for interchangeability which would reduce turn-around time on large advancements. The alignment of a photonic waveguide with grating output coupler to the ion location requires tighter accuracy due to the small beam waist of the light as compared to detectors, for example. We will show that this alignment is possible using a waveguide designed for 355 nm light (the typical 2-photon transition laser used for ytterbium) and demonstrate that the alignment is maintained through a vacuum back.

The SIREN trap is assembled by attaching a waveguide to the back of an ion trap from a previous project (the Phoenix trap). This trap was not designed for HI and needed to be modified by machining a hole in the side for light to pass through to reach the waveguide. After machining the ion trap, the waveguide is attached and then the entire assembly is packaged onto a ceramic land grid array for installation into a vacuum chamber. The device is characterized using the ion trapping experiment and initial traps were able to trap an ion. After preliminary measurements of the waveguide location, the entire vacuum chamber undergoes a vacuum bake to achieve ultra-high vacuum. The chamber is then reinstalled on the experiment table to determine how much the waveguide shifted. Our first test showed that using just solder to attach the chip led to a relative shift of 2.5±0.5 μm tangential to the trap axis. We developed a new approach for attaching the waveguide to reduce the shift during the bake leveraging knowledge from HI in other fields. This approach involved adding an adhesive after the solder to help support the solder at high

temperatures. This combined attach had a measured shift at the surface of 0.0±0.5 µm. Though the position stayed constant, we were unable to trap an ion in the second trap due to surface contamination from the method of applying the adhesive and the machining. Despite not showing laser addressing through the waveguide, we believe this accurate alignment and stability through a vacuum bake shows promising application for a full 3D HI implementation of ion traps.

Quantum computers are working to scale from the current 10's of ions to millions. In this regime, the resources for trapping and manipulating the ions will need to scale as well. The current approaches face fabrication challenges, thermal dissipation challenges, and resource scaling limits. By separating the ion trap from the supporting chip, we can start to address some of the immediate barriers to scaling while opening the doors to including more exotic technology by adding additional chips. This demonstration shows we can consider an ion trap package to include more technology than what is integrated into the chip directly and that a 3D ion trap stack is possible.

DETAILED DESCRIPTION OF RESEARCH AND DEVELOPMENT AND METHODOLOGY:

Current ion trap fabrication is focused on overcoming limitations in scaling by integrating all needed technology directly into the ion trap. This approach allows for the advantages of lithographic alignment between the ion trap and light from output coupling gratings, for example. However, it requires that each technology compromise in fabrication strategy to be compatible. This compromise can lead to higher loss, higher noise, and generally lower performance metrics which are hard to overcome given the goal of a high-performance quantum computer or atomic clock. In this project, we show that the necessary alignment can be achieved without lithography, but by leveraging advanced packaging techniques. We use a separately fabricated ion trap chip and wave guide chip and attach them at the packaging level to within 2 µm and maintain that alignment through a vacuum bake.

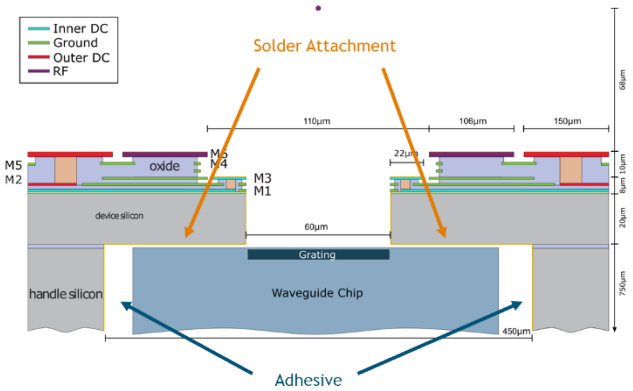

Figure 1: Cross section (not to scale) of the Phoenix trap in the slot region. The ion sits 68 µm above the top of the trap. The hole in the metal layers of the trap is only 60 µm to limit the ion exposure to the handle material. However, to keep the NA of the path large, the hole in the backside is 450 µm. This is large enough for a small optical chip (blue) to be placed and soldered to the back of the Phoenix.

The ion trap is a Phoenix trap [5] which is a long linear trap with a large slot in the center of the trapping region for allowing atomic flux and light to pass through from the backside. **Error! Reference source not found.** shows a cross section of the Phoenix trap in the slot region. We made custom waveguide chips to sit within the backside slot of the Phoenix. These chips are standard wafer thickness 700 µm, 350 µm wide, and 2 mm long. Our packaging tool can place pieces this small due to a custom

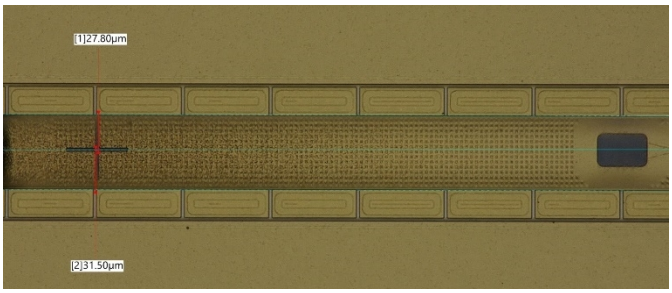

Figure 2: Measurement of the centering of the left alignmnet mark. On the right side of the image, the grey square is a hole in the metal coating on the waveguide to allow for light to exit the grating coupler. The left side shows the crosshair alignment mark used by the packaging tool to center the waveguide chip. In this case, the crosshair is 1.9(4) µm above center due to an offset in the gold layer.

attachment arm made for trench capacitor modules which are a similar size and typically added to the package of traps that do not have integrated capacitors.

In preliminary tests, solder appeared to survive a bake test with minimal movement during a 24-hour 200 degree C bake. Thus, the first attempt at integration used Au80Sn20 solder to attach the waveguide chip to the back of the Phoenix trap. The waveguide chip we used was initially fabricated for a different program, but for this work, we modified a gold top metal layer to have solder pads and alignment marks where necessary. The entire center line of the waveguide was gold coated to minimize the impact to an ion and alignment marks were added for the tool at each end (crosshairs). Additional marks were placed (3 triangles) at the center of the chip aligned to the input coupler so the 355 nm laser can be aligned to the input location while looking at the trap surface with the experimental imaging system. The waveguide has small solder pads for solder spheres (see Figure 3) which can be re-flowed to allow for precise alignment to the trap. After re-flowing, the variation in the solder height is < 1 µm, the solder bumps are then gently pushed into the backside of the Phoenix to identify a common reference frame. Then, the tool carefully reflows the solder and pulls the waveguide away from the Phoenix until the intended spacing is reached, in this case 105 µm. Alignment marks on the waveguide are used to calibrate the position of the waveguide with respect to the trap to minimize position errors orthogonal to the trap. These alignment marks are measured after chip placement to determine the approximate location (shown in Figure 2).

After the waveguide is placed, the trap is installed into an ion trapping vacuum chamber. Typically, a new trap would be baked immediately. However, to characterize the movement during a bake, the waveguide was measured before baking. Once installed in the ion trapping experiment, 355

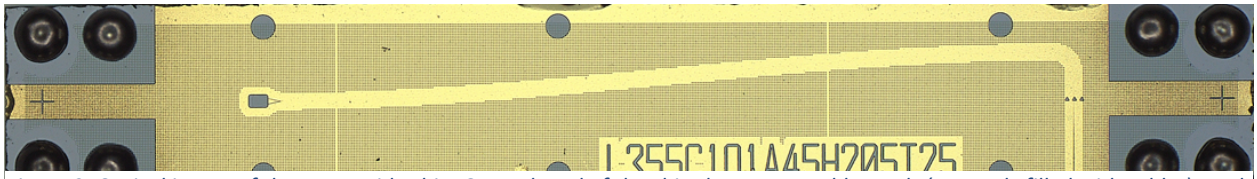

Figure 3: Optical image of the waveguide chip. On each end of the chip there are 4 solder pads (currently filled with solder) used for both registering the chip to the trap die and for attaching the waveguide chip to the trap. The input coupler of the chip is on the bottom right designed for free space coupling into the edge of the chip. The two alignment crosshairs are at the optical center of the chip at opposing ends.

nm light was coupled into the waveguide and detected using the imaging system. This system

(described in Ref. [6]) has a magnification of about 28 and a reimaged pixel size of 0.28 µm. Additionally, we can measure the propagation of the light from the waveguide and compare it to the ion location. We have focused our interpretation on when the system is focused on the ion trap surface which is > 120 um from the waveguide surface. Small tilts between the waveguide and the trap would be obvious at this height. Images are captured which have 355 nm light both coming out of the waveguide and incident on the ion trap surface as shown in Figure 4. From these images, we can determine the location of the edge of the ion trap and thus the relative location of the center of the waveguide light.

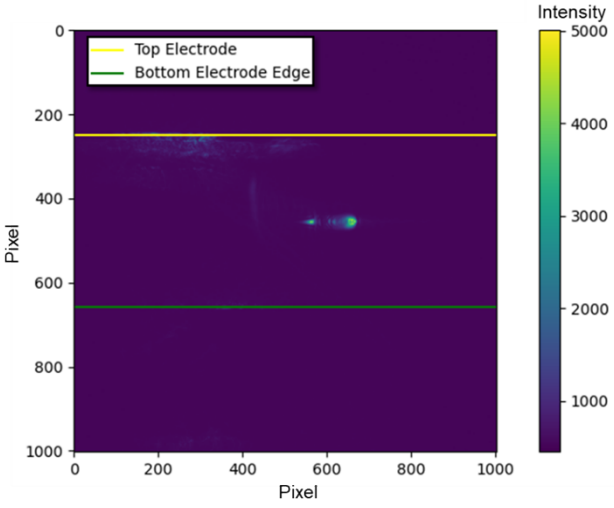

Figure 4: Result from the ion trap imaging system in false color. The bright teal spot in the center of the image is the light out of the waveguide. The complex structure is likely due to the gold coating on the waveguide. The right spot is the main diffracted order. The lines are fit to the inner edges of the slot, not visible as they are covered by the fits.

After measuring the initial waveguide location, the vacuum chamber underwent a standard 5 day 150°C bake. The chamber was then reinstalled in the experiment and the propagation of light from the waveguide was remeasured. Discussed further in the results section, our first measurements indicated that the solder creeped during the vacuum bake [7]. While the overall movement was small, it resulted in a shift that was larger than the trapping region and thus we developed a second approach.

Rather than only use solder, a typical packaging approach in other HI applications is to employ an epoxy adhesive underfill where voids between solder are filled with adhesive to improve reliability. Thus, we added MB600 adhesive to the sidewalls of the trap assembly (locations are noted in Figure 1). The new trap with the solder adhesive combination attach was installed into the vacuum chamber and the position measure pre- and post-bake.

RESULTS AND DISCUSSION:

To determine if the waveguide moved at all during the high temperature bake, we measured any y, or z shifts by capturing the images of the 355 nm light out of the waveguide as a function of the imaging focal plane both before and after undergoing the bake. We denote the x direction as lying along the trap axis, the y direction perpendicular to x along the trap plane, and the z direction as

being in and out of plane. After finding the correct z needed to bring the surface into focus, we moved the imaging focus towards the direction of the waveguide and then took measurements

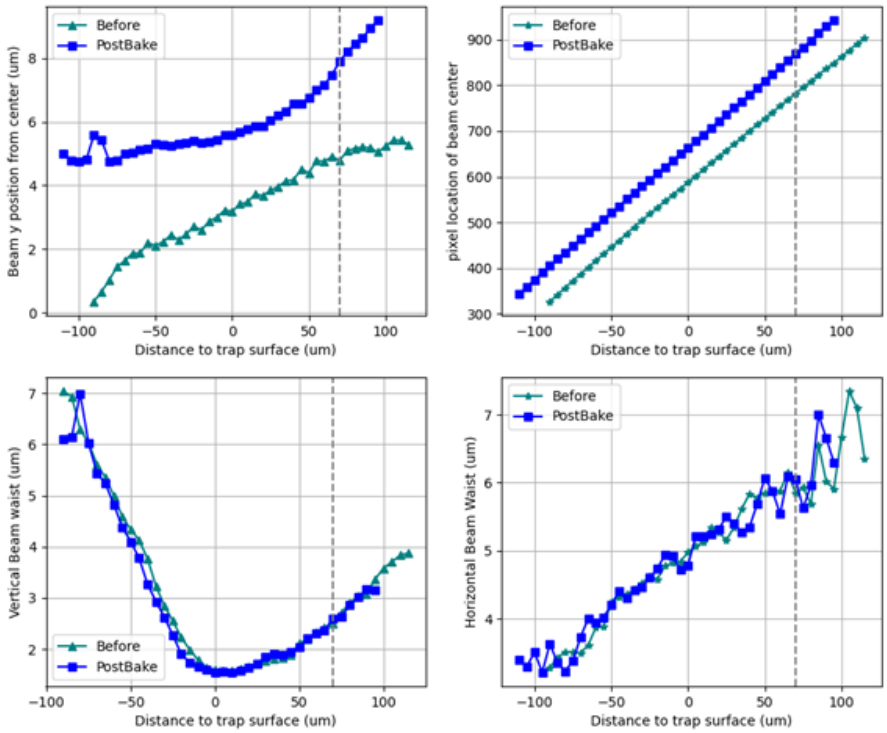

Figure 5: The top left image shows the 2.5 um shift from center of the light exiting the waveguide after the bake. Though there are some slight hysteresis effects which add to the curvature of the measurements, the direct comparison can be made at the trap surface focus, 0 um. The dotted line represents the ion height. The horizontal and vertical beam waist measurements show otherwise good overlap. The position in the horizontal direction is monitored to verify that the fit is accurate tracking the beam propagation but otherwise does not have an absolute position reference to the trap hence the units are left in pixels. However, the ion is free to move along the trap axis, so small shifts (which are unlikely to occur in only a single access) are acceptable in the x direction.

every 5 µm in the negative z direction towards the direction of where the ion would be. We compared the directionality of the measurements by repeating measurements in the positive versus negative directions and found that moving in the negative direction minimized hysteresis effects of the imaging stage.

For the preliminary tests using solder attachments to the solder pads, we found that the waveguide shifted along the y direction by 2.5 µm during the bake, though it held steady in the z direction. These results are shown in Figure 5, where we see that though the vertical and horizontal beam waist directions did not shift from one another, the beam's position in the y direction saw a shift from center. Though there some slight curvature differences between the measurements due to some residual effects of stage hysteresis, the direct comparison is made at the trap focus, which, in these plots, is 0 um from the trap surface. During the experiment, we became concerned that

aberrations could play a role in how well the edges are calculated, which could in turn influence the measured shift from center. Error bars are not plotted, but we calculate a 0.5 µm error in the y direction that could arise from lack of precision with edge finding on the trap surface image. This was calculated by comparing the edges in the measurements taken +/- 5 µm away from the surface image. Therefore, the actual shift could have been between 2.0 – 3.0 µm. A shift in this direction is detrimental to waveguide output alignment to the ion position. The ion would be trapped in the region along the center of the trap, and this amount of shift would cause the light to miss the ion completely. We attributed this shift to a process known as solder creep [7], which is a phenomenon that occurs due to stress that is applied on the solder pads during the high temperature bake. After this set of measurements, we developed some preliminary stress models that suggest the solder pads and thermal expansion are high enough at 150°C to induce shifts on this order.

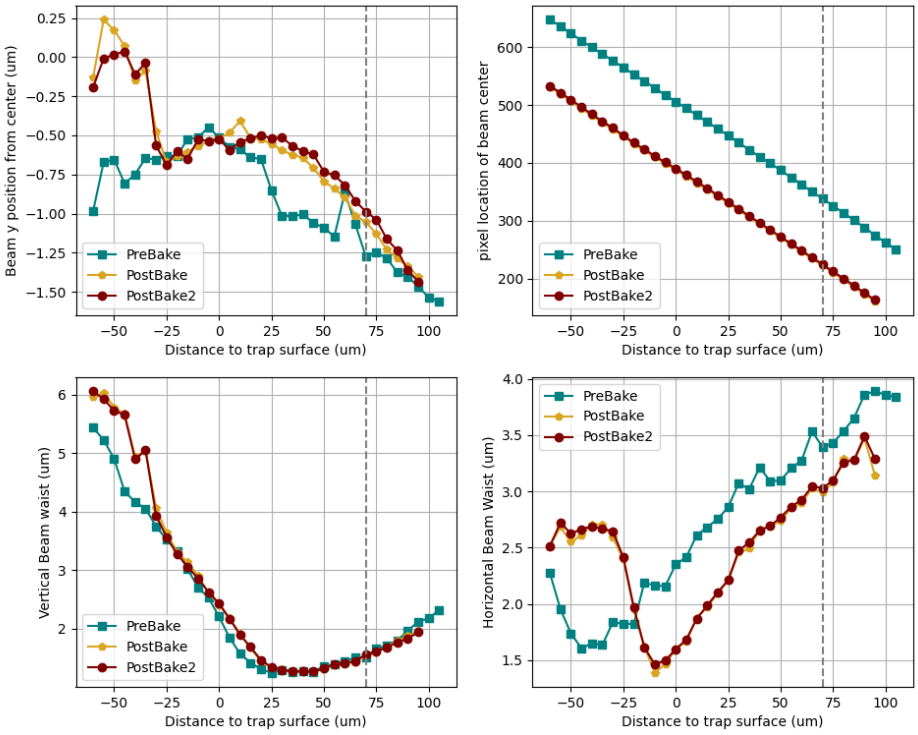

Figure 6: The top left image shows there was no shift in the waveguide output of light in the y direction post bake. Likewise, the vertical beam waist offset shows good overlap. The bottom right image depicts a 0.7 um shift in the horizontal beam waist, which we attribute to imaging aberrations based off subsequent measurements taken where we intentionally introduced a tip and tilt offset in imaging alignment.

We needed more stability in our waveguide at higher temperatures, so the next thing we tried was the ceramic adhesive (MB600) underfill. After this application, we did find we had reduced surface quality on our trap due to either the epoxy outgassing glass onto the surface or the epoxy wicking up to the trap surface during the curing process. This made aligning the imaging system more

difficult, and our imaging focal range was more limited as we became more sensitive to scattering along the surface. We were still able to image efficiently along the region of largest interest, however, and we repeated the same types of measurements before and after the bake. These results are shown in Figure 6. Unlike before, at the surface focus, we see no shift of the beam's position in y after the bake. We repeated this measurement again after the bake to confirm reproducibility in our results. In this case, we did see a 0.7 µm shift in the horizontal beam waist for the second set of measurements. Not only is this close to our 0.5 µm error due to a lack of precision in edge finding, we also note through subsequent measurements that an intentional introduction of imaging aberration can induce this shift. Because our imaging system was not realigned in a satisfactory way due to the poorer surface quality, there were likely some imaging aberrations in this set of measurements that affected these measurements in the horizontal direction. These measurements otherwise show little to no movement in the waveguide from before to after the bake using this application technique. In our measurements to induce aberrations, there was no measurable shift in the y focus likely due to the improved beam shape in y versus x. Grating shape plays a larger role in the x direction making the complex shape more sensitive to optical alignment.

Ultimately, this final measurement shows that the beam was aligned to the center of the trap (at the trap surface) to -0.5±0.5 µm and suggests we are similarly close at the ion height.

ANTICIPATED OUTCOMES AND IMPACTS:

Room temperature ion traps must be maintained at ultra-high vacuum (UHV) pressure to ensure ion stability and prevent ion loss. Achieving UHV conditions typically requires a high temperature bake to remove water and other contaminants from all vacuum components. One of the most significant challenges in the heterogeneous integration (HI) of ion traps is ensuring precise position alignment and stability through these temperature fluctuations. This work demonstrates that these barriers can be overcome with the right approach.

To fully mitigate the effects of vibrations on the trap, light should not be coupled into the waveguide chip through free space. Although initial post-mortem investigations did not reveal any damage from focusing light into the waveguide, there are potential concerns with using free space optics for on-chip light guidance. Additionally, the ion trap should not be mechanically modified, such as by machining, to allow light to reach the chip. The next critical question is whether a trap and chip can be co-designed to facilitate easier alignment, apply adhesive without creeping or outgassing onto the trap surface, and avoid mechanical modifications after fabrication. With the advanced fabrication facilities at Sandia National Laboratories, we believe these goals are achievable. A comprehensive demonstration should involve using multiple wavelengths in the photonics chip and attaching it to an ion trap in a more refined manner.

This work on ion trap HI was presented at an international conference on trapped ions, an AMO (Atomic, Molecular, and Optical) physics conference, and several internal workshops and meetings at Sandia. From these interactions, we identified the next steps: developing a new packaging method for trapped ions, focusing on improving alignment accuracy, and advancing

chip-to-chip registration and attachment techniques. We also need to test new adhesives near an ion trap surface and explore new methods for applying adhesive to minimize its impact on the trap. These efforts should be part of a new trap/photonics chip design specifically tailored for this purpose.

Scaling the support technology for quantum systems is essential for scaling the quantum technology itself. Moving towards heterogeneous integration for ion traps will also enable the inclusion of more advanced photonics and additional technologies. By separating components into distinct chips, we can implement otherwise incompatible technologies and shield them from the ion using the trap itself. Demonstrating this approach with a trapped ion addressed by light from an HI photonics chip is the next step in this research. As the advancement of quantum technologies cannot be confined to a single platform or architecture, supporting this approach aligns with national interests by accommodating a broader range of technologies beyond just ion traps.

Leveraging HI in ion traps has the potential to increase throughput, not only in trap manufacturing but also in all fabricated technologies relevant to trapped ions. This initial demonstration can support the integration of more technology into other quantum devices. The alignment tolerances for trapped ions are among the most stringent, as ions have minimal room for radial movement within an ion trap. However, photonic devices can benefit any quantum technology requiring light. For example, neutral atom quantum computing efforts have begun integrating photonic modulators to improve scaling [8]. Lasers are used across various fields of quantum research, and demonstrating a robust method for coupling technologies across chip boundaries allows for their integration into cryogenic and UHV systems.

In summary, maintaining room temperature ion traps at UHV pressure is crucial for ion stability and preventing ion loss, necessitating high-temperature bakes to eliminate contaminants. Overcoming the challenges of position alignment and stability through temperature fluctuations is essential for the heterogeneous integration of ion traps. This work shows that these barriers can be addressed with the right approach, including avoiding free space coupling of light into waveguide chips and co-designing traps and chips for easier alignment and adhesive application. Presentations at various conferences and workshops have highlighted the need for new packaging methods, improved alignment accuracy, and advanced chip-to-chip registration and attachment techniques. Scaling quantum support technology is vital for scaling quantum technology itself, and heterogeneous integration of ion traps will enable the inclusion of more advanced photonics and additional technologies. This approach aligns with national interests by supporting a broader range of quantum technologies and has the potential to increase throughput in trap manufacturing and other fabricated technologies.

CONCLUSION:

The scalability of trapped ion technology, crucial for advancing quantum computers and atomic clocks, is currently limited by restricted optical access. Traditional ion trap setups face significant

challenges due to the constraints imposed by vacuum chambers and the need for large lenses to collect light. As quantum computers scale from tens to millions of ions, the resources required for trapping and manipulating the ions must also scale. Current approaches encounter significant challenges related to fabrication, thermal dissipation, and resource scaling.

By separating the ion trap from the supporting chip, we can address some immediate barriers to scaling and incorporate more advanced technologies. This work demonstrates the feasibility of aligning two separate chips in packaging to achieve the same goals as monolithic integration, effectively bringing photonics to the chip level. This approach allows for parallel fabrication and interchangeability, reducing turnaround time for advancements. Initial experiments with the SIREN trap, which involved attaching a waveguide to an existing ion trap using solder and adhesive, showed promising alignment precision and stability through a vacuum bake, although surface contamination issues need to be resolved.

Moving away from monolithic integration enables us to tackle immediate scaling barriers and incorporate more advanced technologies. This demonstration suggests that a 3D ion trap stack is feasible, paving the way for more sophisticated and scalable quantum computing systems. By confidently designing and assembling separate pieces into an ion trap processor, we can integrate all necessary supporting technology into a single packaged device, marking a significant step towards the future of quantum computing.

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