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LDRD PROJECT NUMBER: 233544
LDRD PROJECT TITLE: Microfabricated Ion Traps on Sapphire for Larger Trap Areas and Higher Qubit Count
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Abstract
Surface ion traps are a promising platform for quantum computing due to their potential to store large numbers of ions that can be addressed by electrical and optical control signals in order to implement quantum algorithms. Increasing the power of the quantum computer requires increasing the number of ions, but this poses a significant challenge in that it leads to a non-linear increase in on-chip power dissipation. The primary contributor to this power scaling in current devices is the capacitance between the radio frequency (RF) electrode and the metal plane that shields the silicon substrate from the RF signals applied to it. Silicon has traditionally been chosen for the substrate material for compatibility with the processing required for multi-metal-level traps. In this work, we address these capacitance and fabrication challenges by replacing the commonly used silicon substrate with an insulating sapphire substrate to fabricate a multi-metal-level ion trap, while still employing common semiconductor manufacturing techniques. This change in substrate allows the design to remove the metal shielding from the device design, reducing the capacitance of the RF electrode. The electrical characteristics of these traps were measured, specifically trap impedance, capacitance, and voltage breakdown, and compared to nearly identical silicon trap devices. Finally, we used laser cutting techniques to shape a sapphire wafer into bowtie shapes matching silicon traps previously fabricated at Sandia National Labs to explore solutions for integrating sapphire substrates into non-rectangular ion trap designs.

Introduction
Ion traps use a combination of radio frequency (RF) and direct current (DC) electric fields from trap electrodes to form harmonic potentials above the trap surface to confine ions. Since each ion requires a certain number of electrodes, increasing the total number of trapped ions requires proportionally increasing the size of the RF electrode. This correspondingly increases the total RF power dissipation, with the power roughly scaling with the cube of the number of ions.[1] The two major sources of RF power loss are ohmic power dissipation, which is caused by the currents flowing through the RF electrode (which has non-zero resistance), and dielectric power dissipation, which is due to loss in the insulating dielectric between metal layers.

The primary objective of this LDRD was to reduce the RF power dissipation on the device. To achieve that goal, we replaced the silicon substrate on which the multi-metal level trap (MMLT) was fabricated with a sapphire substrate. This substitution is beneficial because the sapphire has much lower RF loss, and therefore does not require a ground plane to screen the RF electrode's field from the underlying substrate, as in the case when using relatively lossy

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silicon. This reduces the capacitance of the RF electrode, which subsequently results in lower RF currents (and therefore lower ohmic power dissipation) as well as lower electric fields in the dielectric insulators (and therefore lower dielectric loss). The impact of these parameters towards the power dissipation of the ion trap is summarized in (Equation 1) and (Equation 2). It is important to note that in this research we retain important features like sub-surface DC routing.

The current state-of-the-art ion trap devices have been fabricated on silicon-on-insulator substrates and incorporate four or more metal interconnect layers defined for routing and ground planes[2,3,4]. The motivation for using silicon instead of insulating substrates, like sapphire or fused silica, is their compatibility with complimentary metal-oxide-semiconductor (CMOS) fabrication techniques, like photolithography, thin-film deposition, and etching processes[5]. Specifically, silicon wafers are opaque, which allows optical sensing systems in semiconductor processing toolsets to perform automated wafer handling tasks that enable high-volume manufacturing. Also, modern ion traps use processes that etch completely through the substrate, which is extremely challenging on sapphire substrates. These fabrication capabilities have allowed more complex trap designs to be fabricated, including multi-level metal routing layer designs, RF traces that tunnel under DC electrodes, on-chip trench capacitors, loading holes, and monolithically integrated photonic devices[6,7].

Another obstacle to integrating sapphire substrates into future ion trap fabrication is the singulation of devices from the substrate wafer. For rectangular trap designs, a mechanical dicing process is used to remove individual die from the wafers. However, some ion trap designs require bowtie shapes to support optical access from the sides, where the narrow trap region reduces laser scattering from the die edges[7]. These irregular shapes cannot be made using dicing, but can be achieved for silicon substrates by using through-substrate etching techniques to define the bowtie shapes. This cannot be done with sapphire due to the material's high resistance to etching techniques[8]. Therefore this LDRD also included research in laser machining to singulate the die.

In this research effort, we fabricated an MMLT with a c-plane sapphire wafer substrate using a CMOS compatible process and copper damascene vias. The ohmic and dielectric RF power dissipation values were measured and directly compared to traps with similar layouts fabricated by Sandia using tungsten vias and silicon substrates. These results showed a 7× reduction in trap capacitance (with an expected 25× reduction in ohmic power dissipation and a 7× reduction in dielectric loss) and an 8% increase in breakdown RF voltage compared to the equivalent design fabricated on a semiconductor. Finally, using unprocessed sapphire wafers, with the same size and crystalline orientation as those used for the sapphire traps in this research, we developed a laser cutting process to singulate bowtie pieces and optically inspected their compatibility with ion trap requirements. A summary of the goals, achievements, and potential impacts of this research effort can be found on the end-of-year summary in Figure 5.

R&D Approach and Methodology

The trap was designed to maximize the benefits of the sapphire substrate but minimize design differences not directly caused by the sapphire. The design chosen was previously used for a silicon-substrate trap with on-chip optical modulators homogeneously integrated on the device[9]. This conveniently provided a silicon version with the same electrode layout and two-metal layer stack as the sapphire trap for directly comparing the power dissipation. The silicon version of this trap designated the first metal layer exclusively as a ground plane to shield the RF rail from the high-loss semiconductor surface. The top metal layer is where all the traces, bondpads, RF and DC electrodes reside.

Some design changes were needed for the sapphire trap to properly benefit from the insulating substrate. First, the regions of the first metal layer directly underneath the RF lead were removed through plasma etching, exposing the sapphire underneath. This design change is key to removing the primary source of power dissipation in the trap, the parallel plate capacitor structures formed when there is a large ground plane directly underneath the RF rail. The two types of power dissipation in these devices, ohmic (Equation 1) and dielectric (Equation 2), both scale with increasing capacitance. A cross section of the sapphire trap with the removed aluminum can be seen in Figure 1a. In the silicon trap, an aluminum ground plane spans across the entire M1 level.

$$P_{Ohmic} = \frac{1}{6} V^2 \Omega^2 C^2 R \qquad \text{(Equation 1)}$$

$$P_{Dielectric} = \frac{1}{2} V^2 \Omega C tan\delta \qquad \text{(Equation 2)}$$

Here, V is the voltage amplitude, Ω is the drive frequency, R is the resistance of the RF lead, C is the device capacitance, and $tan\delta$ is the dielectric loss tangent. In the silicon dioxide used in the fabrication the loss tangent is 10^{-3}. For both the sapphire and silicon traps, the input voltage, drive frequency, and loss tangent are the same. The resistance is slightly different between the two devices, but minimal compared to the expected change in device capacitance.

Another difference is that the first metal layer of the sapphire trap was patterned to be a routing layer for the DC electrodes and demonstrate the process for making vias on the sapphire. Regions of the first metal layer that are sufficiently far from the trap region retain their aluminum. These large regions of unetched aluminum allowed optical metrology processes, such as radius of curvature measurements, to be performed to check in-process device health. Without these regions, the translucent surface would interfere with ellipsometer measurements.

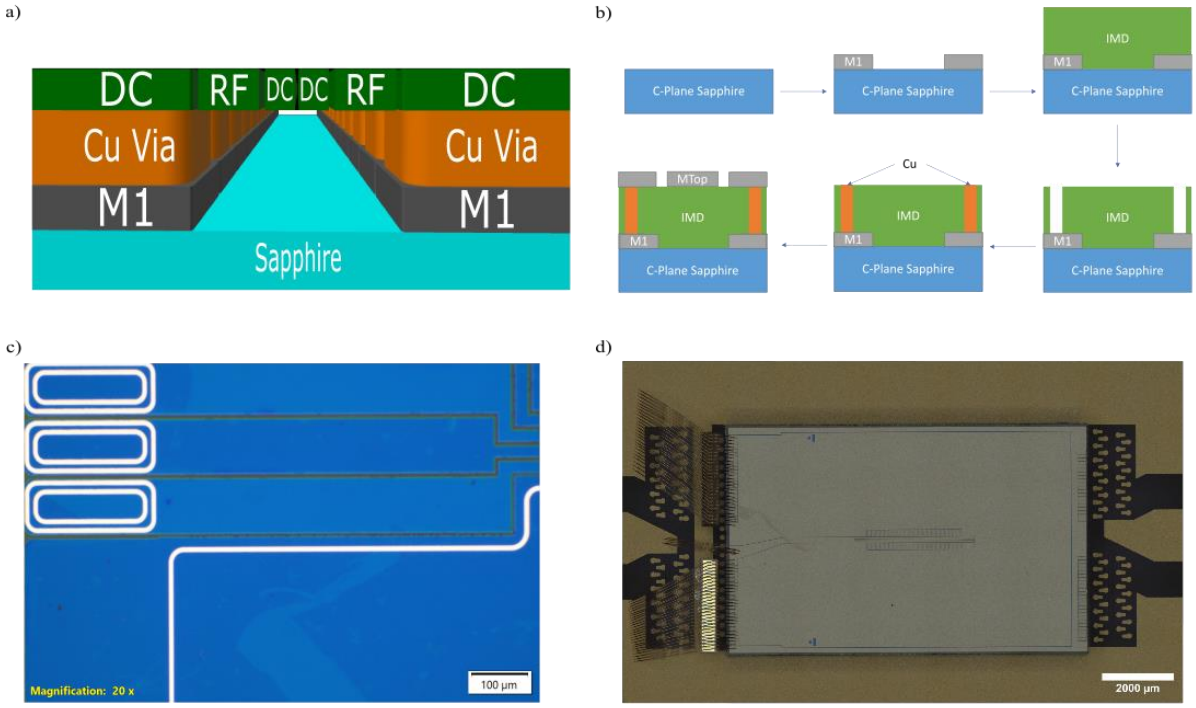

Figure 1: a). A 2.5D view of trap region on the sapphire trap. Both the M1 (gray) and the M2 (Green) layers are comprised of film stacks detailed in the Design and Fabrication section. The RF rail and inner DC electrodes are directly above the sapphire surface to reduce the leakage capacitance in the device. b). A schematic of the single damascene process used to deposit and define the two aluminum metal layers and copper vias. c). An optical image of the first metal layer, inter-metal dielectric oxide, and copper vias before the top metal was deposited. d). An optical image of the sapphire ion trap device in the 100-pin CPGA package with gold wirebonds.

When the RF lead is directly above the insulating surface, the only remaining source of capacitance results from the co-planar geometry of the RF rail and neighboring DC electrodes, which are capacitively grounded. The fringe-field capacitance values were not calculated, but the co-planar lead capacitance between the DC electrodes and RF rail were calculated to be 0.14 pF. Both of these sources contribute significantly less to the total power dissipation than the parallel-plate structure created by the ground metal layer in silicon devices. These coplanar and fringe field capacitance sources are identical to silicon traps tested in this effort because of the design choices detailed before, so they do not contribute any differences in voltage amplitude or voltage breakdown results observed during testing.

The process flow for the manufacture of the sapphire traps was designed to be as similar to the fabrication of the silicon traps as possible. The first film on top of the sapphire is a metal layer comprised of 100 nm titanium nitride (TiN) layers that sandwich a 1.2 µm aluminum layer. Both the TiN and aluminum were deposited with a metal sputtering process. After

deposition, this metal stack is selectively etched to form the DC electrode routing using an ultraviolet lithography and plasma etching process. Next, a 3.5 µm inter-metal dielectric (IMD) layer of silicon dioxide is deposited with a chemical vapor deposition (CVD) process and a chemical-mechanical polishing (CMP) process is used to planarize the oxide surface. Metal vias are formed in the IMD layer using a copper single damascene process to form 5.0 µm wide trench structures, seen in Figure 1c. This process involves patterning and etching the oxide IMD down to the metal layer underneath, then depositing a seed layer of 20 nm tantalum/200 nm copper. Afterwards, electroplating is used to deposit copper to fill the trench vias and a copper CMP process is used to remove the residual material above the oxide surface. Finally, the top metal layer is a film stack of 100 nm TiN and 1.2 µm aluminum deposited with the same processes as the bottom metal layer. The thickness values of the metal layers and IMD were chosen to match the corresponding film thicknesses of the silicon devices to keep the routing resistance and capacitance values as equal as possible.

Sandia National Labs has two primary semiconductor manufacturing facilities as part of its Microsystems, Engineering, Science and Applications (MESA) complex. The first is the SiliconFab, which is a Class 1 production facility designed to process 8" silicon wafers. This facility is the primary area where ion traps made by Sandia National Labs are fabricated. The second fabrication area is the MicroFab, which is a class 10 facility that can process compound semiconductors and insulating substrates as well as silicon wafer post-processing. The fabrication process of the sapphire trap is different in two primary ways from the production of silicon substrate traps. First, the copper interconnect layers differ from the silicon devices that use tungsten vias. This process change was made to take advantage of the copper electroplating capabilities in Sandia National Lab's MicroFab facility, a capability not provided in the SiliconFab. This makes it possible to use a copper damascene process used in silicon foundries for their metal interconnect layers. An advantage to these copper interconnects is their significantly lower resistances. A similar process was used to fabricate a copper mesh ground plane for an ion trap device on silicon[10]. The known resistivity values for copper vias is ~70% lower than their tungsten counterparts. In this design, the copper vias connect the DC electrodes and bondpads on the top metal layer to the traces in the first metal layer. Due to the rapid and unmitigated oxidation of copper films, aluminum was used for the trapping surface. However, if a design of three or more metal layers was fabricated, copper electroplating could be used to fabricate both the vias and metal layers simultaneously using a dual damascene process.

The other difference in fabrication parameters is the deposition processes used for the metal stacks. The sapphire trap used metal sputtering to deposit the titanium nitride and aluminum where the silicon trap used a physical vapor deposition (PVD) process. Similar to the copper damascene process, this change was necessary due to capability differences between the fabrication facilities used to produce the two traps. The major difference observed between these devices due to this change is the measured resistivity of the TiN film. For the metal evaporation process, the resistivity, measured with a four-point probe, was 3000 µΩ-cm.The PVD process yields a TiN resistivity of 200 µΩ-cm which is 93% lower than its counterpart. The total resistance for the RF rail on the sapphire trap is 6.56 Ω, which is 3.2% higher than

the silicon device with an RF trace resistance of 6.35 Ω. From (Equation 1), this difference in resistance should result in a 3.2% increase in ohmic power dissipation and no change in dielectric power loss.

Both the silicon devices and sapphire devices were packaged on 100 pin ceramic packages for power dissipation tests and 16 pin dual in-line packages (DIPs) for voltage breakdown testing. Trench capacitor chiplets, containing 25 capacitor structures each, were attached and wire bonded between the 100-pin package's ground plane and the trap's DC bondpads in series to shunt RF pickup from the DC electrodes. This heterogeneous integration method avoids the obstacles of etching into the sapphire substrate to fabricate chip-level capacitor structures. In the DIP packaging, each DC electrode is tied together, and wire bonded to the package ground. Capacitors were not used for breakdown testing due to their ±30 V safe operating limit. For the one-port probe testing, bare die were tested in an electrically grounded test setup.

To electrically test and characterize the silicon and sapphire traps, multiple test setups were used. The power dissipation was measured in a turbo-pumped vacuum chamber (at a pressure of 10^{-6} Torr) with a signal generator, gain amplifier, and a solid-state resonator to supply the RF power to the trap. Once the resonant frequency of the resonator was tuned, the voltage amplitude between the RF rail and ground was recorded as the input power was increased. We then compared the trend of measured voltages over that input power scale.

The voltage breakdown for each device was measured using the same setup as previous voltage breakdown tests performed at Sandia National Labs[11], except the vacuum chamber was baked out for four days to allow it to reach a pressure 10^{-9} Torr. A helical resonator was used to supply the increasing high-voltage to the trap at a filtered-down frequency. A breakdown event is recorded when there is a sudden shift in impedance, showing that an arc bridged a gap somewhere on the device.

The capacitance and resistance values of each trap were characterized using one port s-parameter measurements. The probe tips were placed between the RF rail bondpad and the adjacent ground pad for each device. Capacitance values for both traps were also measured using a multi-meter during the previously mentioned power dissipation characterization. In this case, the multi-meter probes were placed at the RF and GND pins of the CPGA socket for both traps and with the socket exclusively. Since the capacitance sources can be equated to parallel capacitors in a circuit model, the capacitance of the socket was subtracted from the total capacitance values of each trap to attain their individual contributions. The results from these tests are discussed in the next section.

Results

The electrical characterization of the sapphire and silicon traps was performed with three testing methodologies. First, the capacitance and DC resistance of each trap substrate was measured using one port s-parameter measurements with frequencies ranging from 300 kHz to 2 GHz. The capacitance values were extracted from these s-parameter results where the

DC resistance was obtained using a data matched circuit for both trap devices on the RF rail. For this test, frequencies of 100 MHz and 140 MHz were isolated for capacitance measurements due to their relevance to ion trapping parameters. Multiple sapphire devices were measured using these one-port measurements and device variation of <1.2% was observed. For this test, only one silicon device was available. These tests were performed across multiple sites of the silicon substrate device and a similar variation was observed for this trap. The results of these tests can be found in Table 1:. From these one-port probe results, the capacitance values of the sapphire trap, at both 100 MHz and 140 MHz, was 85% lower than the comparable silicon trap. The resistance values for the sapphire trap were 90% higher than the silicon trap at 2.1 Ω. This can be attributed to the thin-film differences between the aluminum processed in the SiliconFab and the MicroFab facilities. The copper vias did not affect the resistance measurements since the RF rail was not connected to a lower metal layer with vias. From (Equation 1) and (Equation 2). these results, with constant voltage amplitude, drive frequency, and dielectric loss tangent, result in a reduction in ohmic power dissipation of 96% and a reduction in dielectric power dissipation of 85%. The calculated RF power dissipation values can be found in Table 2.

For the voltage breakdown testing, both the sapphire and silicon devices were placed in a vacuum chamber and pumped down and baked until the pressure was measured at 10^{-9} torr. The resonator used to introduce the high voltage signal to the trap was tuned before the experiment to minimize internal loss and determine the system's resonant frequency. Also, all cables and components were mechanically secured to the optical table setup before the procedure started to prevent any mechanical disturbances to the testing apparatus during the experiment. With these initial conditions, each trap has a voltage applied to it that increases every 20 minutes. This holding pattern between voltage steps allows the system to stabilize and limits the effect of outgassing at lower voltage levels. Also, the chamber pressure is monitored throughout the testing due to possible breakdown voltage limitations due to vacuum levels in the system. For all of these tests, the pressure in the vacuum chamber ranged from 10^{-9} to 4×10^{-9} Torr for both traps. During the testing, an oscilloscope is used to monitor the coupled back-reflection voltage of the system. An instance where there is a spontaneous impedance mismatch in the back-reflected voltage is a triggering event that determines when a breakdown event has occurred somewhere in the device. An impedance mismatch signal, as seen on the oscilloscope, can be seen in Figure 2 and the voltage values where breakdown events were seen for both traps are tabulated in Table 1:.

Substrate	Capacitance (pf) @100 MHz	Capacitance (pf) @140 MHz	DC Resistance (Ω)	Breakdown Voltage (V)
Sapphire	2.04	2.02	2.1	250±20
Silicon	14.24	14.20	1.1	230±20

Table 1: Measured electrical parameters using one port s-parametric measurements, including capacitance, DC resistance, and RF voltage breakdown of the devices.

Substrate	Ohmic Power Dissipation (mW)	Dielectric Power Dissipation (mW)	Total Power Dissipation (mW)
Sapphire	5.75	6.41	12.16
Silicon	146.76	44.74	191.50

Table 2: Calculated power dissipation values for the sapphire and silicon trap devices. For these calculations, capacitance and resistance were taken from Table 1:, V is set to 100 V, Ω is set to 100 MHz, and tanδ is set to 10^{-3}

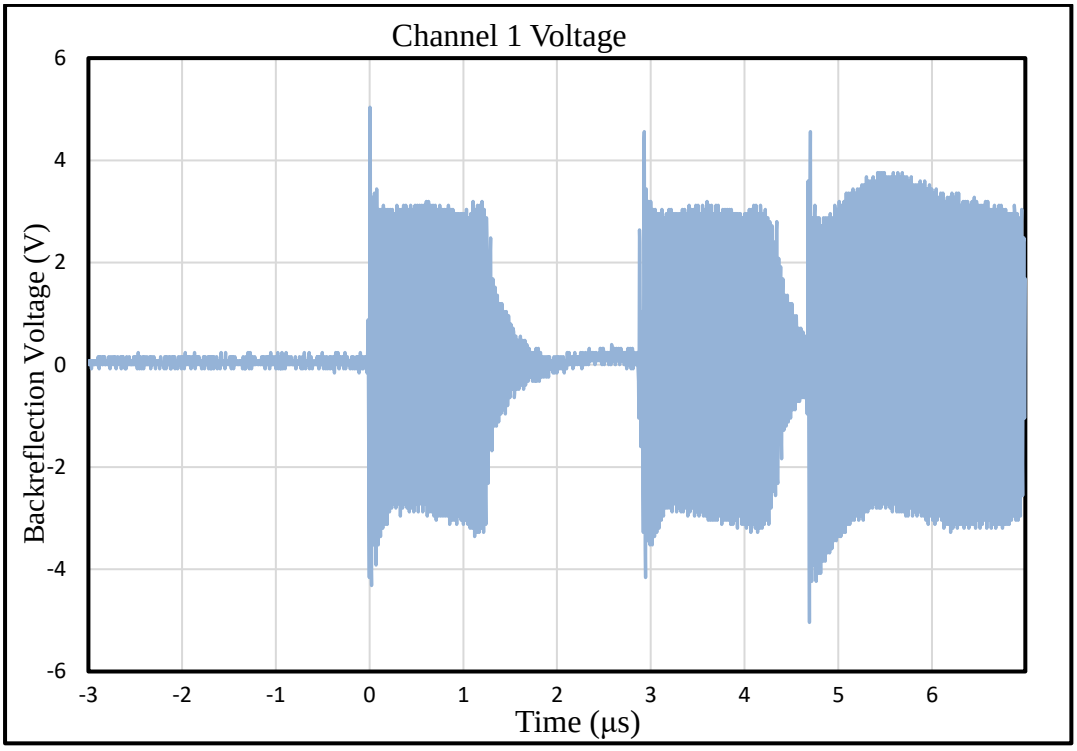

Figure 2: An oscilloscope chart detailing back-reflection voltage vs time showing a voltage breakdown event on the sapphire trap at 250 volts.

The final characterization test performed was the measurement of voltage from the RF rail to ground at increasing applied power values. The traps used in this testing were assembled onto 100 pin CPGA packages, then installed into a vacuum chamber pumped down to 10^{-6} torr. Then, power was applied to these traps with a solid-state resonator at the resonant frequency. This applied power was increased from 10 dBm to 35 dBm (10 mW to 3.16 W) in 5 dBm steps as the voltage across the RF rail to ground pins was measured using an RF analyzer. The results from this testing are shown in Figure 3. From this data, the sapphire trap showed a 21% increase in measured voltage at the highest power value than the silicon trap. This increase in voltage ranged from 17% to 22% across the entire range of applied power levels.

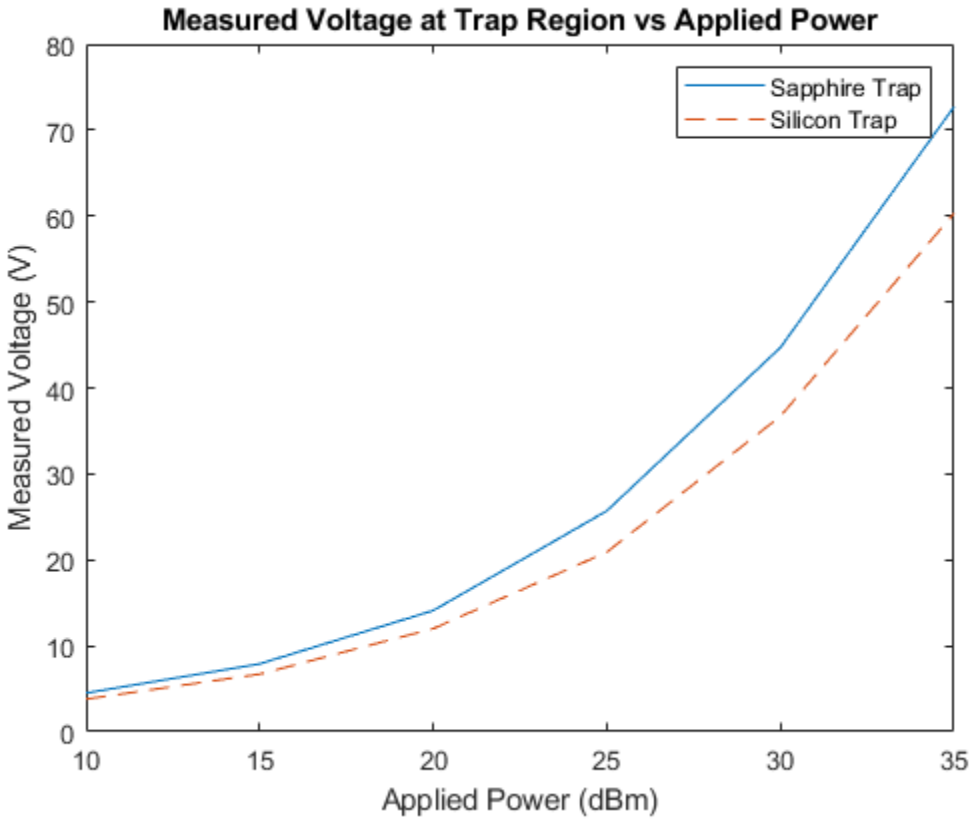

Figure 3: A plot comparing the measured voltage between the RF rail and GND versus the input power. Here, the sapphire shows a 20% increase in observed voltage at 35 dBm (3.16 W)

Lastly, laser cutting techniques were used to singulate bowtie shapes out of unprocessed sapphire wafers to demonstrate the capability of fabricating non-rectangular ion trap devices on insulating substrates resistant to standard etching techniques used in cleanroom manufacturing. Figure 4 shows our demonstration, where a bowtie was cut out of a 6" C-Plane sapphire, with a 650 µm thickness, using a LPKF Protolaser U4 laser micromachining tool at the Center for Integrated Nanotechnologies (CINT). This instrument has a 384 nm femtosecond laser and was designed by LPKF to prototype printed circuit boards. At CINT, a cutting process was developed with this tool to laser cut 500 µm thick sapphire, but the extra thickness of our target material in this project required additional tuning of our standing laser parameters. These recipe changes can be applied to future devices that use these larger sapphire wafers.

Figure 4: A bowtie shape cut out of a 6" C-Plane sapphire wafer to demonstrate the capability of fabricating non-rectangular ion traps from a sapphire substrate. Multiple passes and adjustments were needed to singulate this shape, which can be seen in the additional dicing mark near the bottom of the isthmus.

Anticipated Outcomes and Impacts

This research showed that a multi-metal-level trap on sapphire can be successfully fabricated and achieve significantly lower RF power dissipation than its silicon alternative. With these results, we will be submitting a manuscript for publication, detailing the research methods and results we acquired with this Exploratory Express LDRD. The immediate next steps to take advantage of these findings is seeking out future funding opportunities for processing sapphire wafers in the SiliconFab and testing the feasibility of high-voltage ion trapping with the newly fabricated sapphire trap devices. There are also plans to work with the Quantum Systems Accelerator program, a research center created by the Department of Energy's Office of Science, to continue breakdown testing of ion traps to compare with these sapphire devices, which will also add more data to use for the publication.

From the results gathered during this project, there are multiple future research directions and development efforts that can follow on or use this project as evidence for feasibility. The primary application is to scale up trap architectures that support more ions, when otherwise they would have been limited by power losses. These large traps require multiple metal layers to accommodate the routing of electrical signals to control electrodes. The successful fabrication of the sapphire device provides strong evidence that a multi-metal-layer trap can be created using sapphire wafers. The process detailed before can be repeated to incorporate more than two metal layers, including the six or more metal layers used in some current traps.

Another of this LDRD's accomplishments is the successful demonstration of a copper damascene process on a transparent substrate to fabricate a device for quantum physics research. The single copper damascene process used in this fabrication is commonly used in high-volume semiconductor manufacturing for creating vias with a different metal composition than the metal interconnect layer above it. Copper has the benefit of significantly lower resistivity compared to previously used tungsten via structures. A path forward that uses these results would be to pair the aforementioned scaling efforts, where more metal layers are added to the device stack, with copper vias and metal layers. Another common processing technique in the semiconductor industry is the dual damascene process. Dual damascene is a method of depositing the copper for both a metal layer and the via underneath simultaneously. This comes with both process time saving and lower resistance metal layers. The time savings are derived from cutting the number of electroplating steps in half to define the two features. One caveat of this path forward is that any copper layer must be completely encased in dielectric material due to rapid oxidation of exposed copper surfaces. Future efforts in the MicroFab can use a dual damascene process to fabricate ion traps, or other quantum physics devices, with copper vias and copper metal layers. In this case, there is a strong case for defining the first metal layer as both DC and RF routing, then using the copper via structures to connect the RF rail at the first metal layer to the top metal layer in regions directly surrounding the trap structures. From (Equation 1), the lower resistance in this section of RF rail can reduce the power dissipation further since the ohmic power loss scales linearly with the resistance of the trace.

Finally, a sapphire wafer was micromachined with a laser dicing tool to create a bowtie shape routinely used in state-of-the-art ion trap devices. Although a single bowtie was singulated in this research effort, this process can be scaled to fabricate many devices on the same wafer. We would simply need to have global alignment markers to align our bowtie cutting pattern to each device, which could be incorporated into future designs.

These results will help Sandia National Labs support future projects in trapped-ion quantum computing that focus on scaling the number of qubits, and by doing so positively impact the national security and DOE mission applications associated with quantum computing.

Conclusion

The Microfabricated Ion Trap LDRD concluded with the following accomplishments:

- Ion Trap devices were successfully fabricated on an insulating substrate and processed with CMOS manufacturing techniques.
- Copper vias were formed on these devices using a damascene process on a sapphire substrate, a first use of this method for quantum devices.
- Electrical benefits, including a 7× reduction in device capacitance, a 23% increase in measured voltage between the trap and ground with identical input power, and an 8% increase breakdown voltage value, were observed between sapphire and silicon substrates.
- Bowtie shapes were singulated from unprocessed 6” sapphire wafers to allow non-rectangular trap designs to be integrated onto the transparent substrate.

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Addendum

Microfabricated Ion Traps on Sapphire LDRD #233544

Zach Meinelt, Matt Bahr, Patrick Finnegan, Ray Haltli, Matt Jordan, Tyler Liebsch, Scott Weatherred, Daniel Stick

- ***Goal:*** *Fabricate and characterize a multi-metal-level ion trap, for quantum computing, on a sapphire substrate.*
- ***Hypothesis:*** *Sapphire ion traps can be fabricated with multiple metal levels and will demonstrate lower power dissipation and higher voltage breakdown values*
- ***Success Criteria:*** *Fabricate Ion Traps in the MicroFab with sapphire wafers* ***AND*** *demonstrate lower RF power loss and higher voltage breakdown*
- ***Motivation:*** *Increase the qubit count capability of trapped ion quantum computing by significantly reducing RF power losses*

- *RF power dissipation increases as the cube of the number of qubits. Sapphire significantly reduces capacitance (C)*
- *Ohmic power dissipation scales with C^2, dielectric loss scales with C*
- *Addresses multiple investment areas for LDRDs*
- *Sandia can make larger ion traps for future customers*
- ***Future Work:*** *Sapphire wafer fabrication in SiFab and attempt to trap ions on new devices*

- ***Did we meet success criteria?:*** ***Yes!***
  - *We demonstrated that multi-metal-layer traps (MMLT) were fabricable.*
  - *We also demonstrated electrical benefits to using the sapphire substrate.*

Major change:

Copper damascene process to fabricate metal layer interconnects (vias). This added another novel aspect to this process.

Biggest Discovery: Complimentary metal-oxide-semiconductor (CMOS) fabrication techniques can be utilized on insulating substrates for producing quantum physics nanodevices

Publications & staff developments, and new capabilities

- Manuscript to be submitted to AVS Quantum
- First PI opportunity for Zach M.
- Process learnings on how to operate CMOS processes with Sapphire for Scott W.

Figure 5 A quad chart from the end-of-project summary presentation summarizing the goal, methods, and achievements of this LDRD