# Final Technical Report (FTR)

## Cover Page

| | | |
|---|---|---|
| ***a.*** *Federal Agency* | Department of Energy | |
| ***b.*** *Award Number* | DE-EE0010239 | |
| ***c.*** *Project Title* | Planar Transformer Systems for Modular Power Electronics in Long-Haul, Low-Cost PV Systems | |
| ***d.*** *Recipient Organization* | Arizona State University | |
| ***e.*** *Project Period* | *Start:* Oct. 1, 2022 | *End: March 31, 2024* |
| ***f.*** *Principal Investigator (PI)* | Name: Mike K. Ranjram<br>Title: Assistant Professor<br>Email address: mike.ranjram@asu.edu<br>Phone number: (857) 445-6676 | |
| ***g.*** *Business Contact (BC)* | Name: Heather Clark<br>Title: Assistant VP – Research Operations<br>Email address: heather.christina.clark@asu.edu<br>Phone number: (408) 965-1427 | |

*Signature of Certifying Official*

2024.07.23

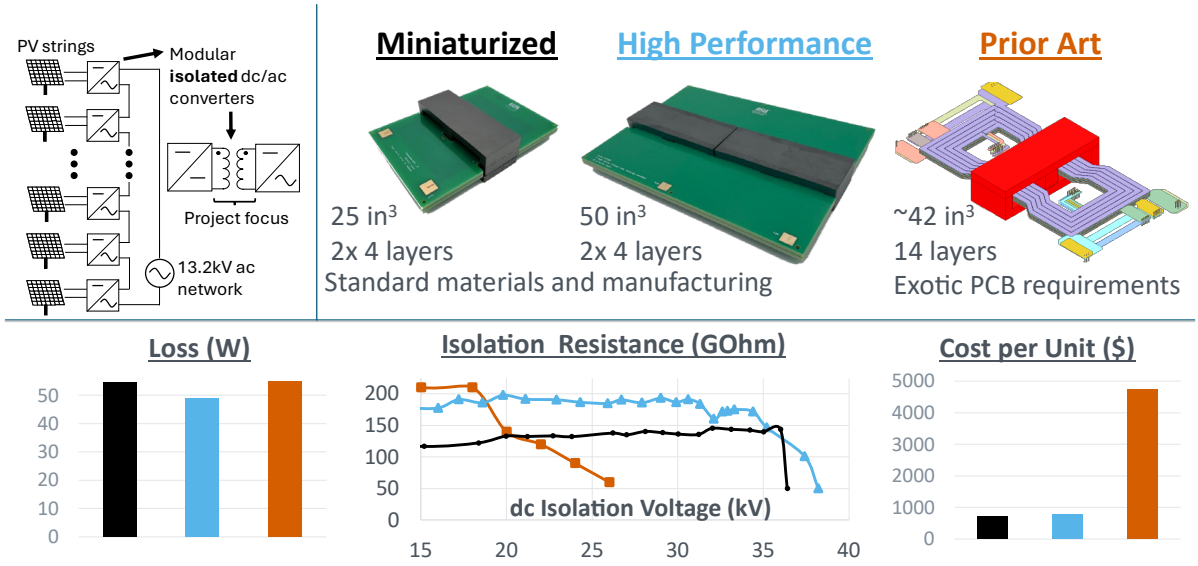
*Date*

*By signing this report, I certify to the best of my knowledge and belief that the report is true, complete, and accurate. I am aware that any false, fictitious, or fraudulent information, misrepresentations, half-truths, or the omission of any material fact, may subject me to criminal, civil or administrative penalties for fraud, false statements, false claims or otherwise. (U.S. Code Title 18, Section 1001, Section 287 and Title 31, Sections 3729-3730). I further understand and agree that the information contained in this report are material to Federal agency's funding decisions and I have any ongoing responsibility to promptly update the report within the time frames stated in the terms and conditions of the above referenced Award, to ensure that my responses remain accurate and complete.*

**Acknowledgement:** "This material is based upon work supported by the U.S. Department of Energy's Office of Energy Efficiency and Renewable Energy (EERE) Solar Energy Technologies Office (SETO) under the DE-FOA-0002606 Award Number DE-EE0010239.

## Executive Summary

This project successfully developed and verified a new approach for medium voltage (MV) planar transformers for use in emerging, utility-scale, modular PV systems. This approach simplifies their manufacture, improves their isolation capability, lowers their cost, and reduces their volume and loss, while also creating flexibility in the materials that can be used. These key outcomes are summarized in the figure below.




In contrast to prior work, our approach targets the simplest possible winding arrangements in these transformers to minimize the number of MV isolation barriers. In other words, we prioritize meeting the critical isolation requirements of these systems. In so doing, we greatly expand the feasible PCB dielectrics and other insulation barrier concepts that can be considered for these systems, thereby mitigating sensitivity to supply chain changes in any particular material. This isolation barrier prioritization can be done without affecting a dramatic increase in copper loss compared to the prior art owing to an improved understanding developed in this project of the isolation design and spacing requirements of the windings and connecting vias in these transformers. We also show that multi-core design optimizations can employ series-connected transformers to trade-off core and copper losses to minimize overall losses.

In addition to a technology demonstration which verifies the proposed design approach, this project advances a PCB cost model for improved cost assessment of planar magnetic components which is especially relevant for LCOE-constrained solar PV systems. We also develop an automated core loss data collection testbed to accurately verify transformer losses. These cost and loss data comprise a design framework for planar transformers which elucidate trade-offs between efficiency, volume, and cost, and enable planar transformer designs for emerging utility-scale modular PV systems which produce best-in-class results in these three metrics. Such innovations are integral to developing the next generation of high-performance, low-cost utility-scale solar PV systems.

## Table of Contents

1. Background ..... 5
1.1 Utility-scale PV Systems and Their Isolation Transformers ..... 5
1.2 Medium-Voltage Planar Transformers and Limitations of the Prior Art ..... 6
1.3 Planar Transformer Costs ..... 8
1.4 Assessing Magnetic Core Loss ..... 9
2. Project Objectives ..... 10
2.1 Project Goals and Outcomes ..... 10
2.2 Significance, Innovation, and Fundamental Advancements ..... 11
2.3 Summary of SOPO Tasks ..... 11
3. Project Results and Discussion ..... 14
3.1 Achievement of Milestones, Deliverables and Metrics ..... 14
4. Significant Accomplishments and Conclusions ..... 29
5. Path Forward ..... 30
6. Products ..... 31
7. Project Team and Roles ..... 32
8. References ..... 32

# 1. Background

The aim of this project is to develop and verify a new approach to designing medium-voltage (MV) planar transformers for emerging, utility-scale, modular PV systems. This approach considers these MV planar transformers as *systems* rather than as *components*. This means they can comprise multiple individual magnetic cores and printed circuit boards (PCBs) which can be distinctly organized both electrically and physically to achieve maximum performance. Central to this approach is that low-complexity winding stack-ups are leveraged which simplify primary-to-secondary insulation requirements, mitigate the need for interleaved windings, and aid in streamlining manufacturing and greatly reducing cost. Additionally, these systems dramatically expand the available material choices for the PCB by significantly reducing their required dielectric strength. This is a key driver of low-cost PCBs and mitigates sensitivity to supply chain changes in any particular material.

The three key aspects of a medium voltage planar transformer in a solar PV application are its: (1) isolation capability, (2) cost, and (3) loss. This project comprehensively explores each of these three facets and we ultimately advance planar transformers having higher isolation capability, much lower cost, and lower loss than the state-of-the-art, at a comparable and lower volume. In this section, we provide background on each of these three key facets of the design.

## 1.1 Utility-scale PV Systems and Their Isolation Transformers

Modular isolated power converters are attractive solutions due to their flexibility, scalability, efficiency, and ease of maintenance making them well-suited for a wide range of applications- including utility-scale renewable energy systems, industrial power supplies, and electric vehicles. This project focuses on utility-scale PV systems and the modular string inverter architecture shown in Fig. 1 in which multiple isolated dc/ac inverters are connected in a series-output configuration. The inputs of these inverters each connect to a PV string. The outputs are connected in series such that they directly synthesize a 60Hz MV (e.g., 13.2kV line-to-line). These systems dramatically reduce balance of system costs (and correspondingly LCOE) via simpler maintenance, heightened reliability, increased efficiency, and economical wiring [1].

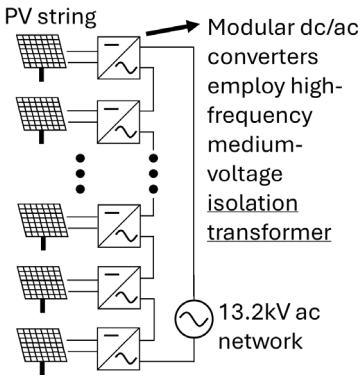



**Figure 1**. Multiple-input, series-output utility-scale PV conversion architecture. Two additional identical structures would implement the additional ac voltage phases in a three-phase system.

Today's utility-scale PV systems often employ string inverters which similarly interface to a set of PV strings at their input, but output an ac voltage around 800$V_{ac}$ [2]. This value is limited by the voltage blocking capability of today's high-performance semiconductors. Thus, a bulky and expensive 60Hz transformer is employed in these systems to provide isolation and to step up this voltage to MV for interfacing with the local distribution system. A highly attractive feature of modular architectures is that this bulky transformer is replaced by a miniaturized transformer within each isolated power converter module. This transformer experiences much higher frequencies within the power converter (e.g., in this project, 200kHz is the target) and this is a substantial driver of miniaturization as it enables much lower flux densities within the magnetic core of the transformer, and enables the use of high-

performance, low-loss MnZn ferrites. A further advantage in the architecture in Fig. 1 is that each transformer can be designed for a simple 1:1 conversion ratio since the MV is derived from series-stacking the converter modules. Each transformer in the converter modules only needs to provide isolation, with no voltage gain, which greatly simplifies their design. In the example traditional system, the transformer provides isolation and a voltage gain of ~60x.

Fundamental to these systems and gains is that the commonly employed grid-interfaced MV transformer is replaced with high-frequency miniaturized MV transformers in each module. However, transformers are inherently difficult to miniaturize owing to fundamental scaling constraints [3], and they bottleneck the power processing capability, size, and efficiency of proposed modular solutions. It is imperative that as cutting-edge modular architectures are proposed and developed, the low-cost, simple-to-manufacture, and high-performance magnetics required to enable them are advanced in kind.

## 1.2 Medium-Voltage Planar Transformers and Limitations of the Prior Art

Planar magnetics are inductors and transformers with windings that are implemented directly on printed circuit boards (PCBs). They represent an active area of research in high performance and miniaturized power conversion, owing to numerous advantages such as high repeatability, simplicity for manufacture, and improved thermals [4]. This technology has enabled strong improvements in power conversion applications with low isolation voltage requirements [1], [4], [5], but these benefits have not yet been realized in applications requiring medium voltage isolation.

To date, virtually all MV high-frequency transformers employ wire-wound constructions. These are much more expensive and complicated to manufacture than planar constructions, typically employing Litz wire and requiring bobbins and coil formers in their construction [6] and manufacture. However, they also greatly simplify meeting insulation requirements since the entire construction is controlled. In being much simpler to manufacture, planar transformers are also much more restrictive. The planar transformer design approach proposed in this project is foundational to maximally leveraging this technology in this and other MV applications (such as electric vehicle charging stations), and creates a basis to fundamentally consider the transformer bottleneck in ideating future low-cost, miniaturized modular MV architectures.

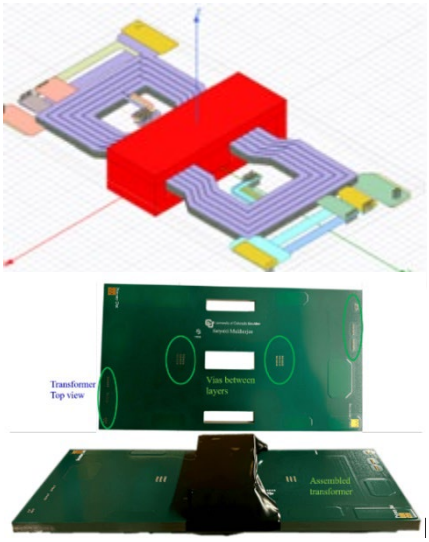



Figure 2. Illustration of planar transformer and corresponding hardware prototype from prior work [6].

One previous study has explored fully-PCB-based MV planar transformers [7]. In that work, the authors developed a transformer for the converter architecture in Fig. 1 with transformer ratings of 1kV:1kV, 7.5kW, 200kHz switching frequency under dual active bridge-type (DAB) excitations. This work achieved a dc isolation capability of 26kV for a 13.2kVac grid interface application, lower than the designed expectation of 35kV. Their design is shown in Fig. 2 and employs interleaved, 12-layer windings (although the PCB comprises 14 layers, as discussed in Section 2). Interleaving refers to a transformer construction in which the turns of the primary and secondary windings

are arranged in an alternating pattern in the PCB stack-up (e.g., in a four-layer board, fully interleaved windings would be arranged as layer 1: primary, layer 2: secondary, layer 3: primary, layer 4: secondary). Doing this can reduce the ac resistance associated with high layer counts [8]. However, a 12-layer interleaved winding arrangement imposes 11 isolation barriers between the windings and forces the use of an uncommon very-high-breakdown-voltage (276kV/mm) polyimide film dielectric (RF775) in the PCB, which dramatically increases its cost and compromises manufacturability.

Through our project, we identified three discrepancies with the approach in prior art, which we include here as background as it is the best place to contextualize prior work. However, we emphasize that these represent key findings of this project and they are addressed again in Sections 3 and 4.

First, the prior approach uses ANSYS Electrostatic simulations to design the transformer's insulation. The difficulty is that this software cannot simulate dielectric breakdown, and so its results are ambiguous if the simulated electric field strength exceeds the dielectric's rating. In [7], and reproduced in Fig. 3, an ANSYS electrostatic simulation result is interpreted as verifying a safe isolation distance because full breakdown of the air is not observed. However, the 3kV/mm dielectric rating of dry air at standard temperature and pressure is exceeded around the windings, and so this results in simulation ambiguity. An example simulation tool that can model dielectric breakdown is ANSYS EMA3D Charge Plus.

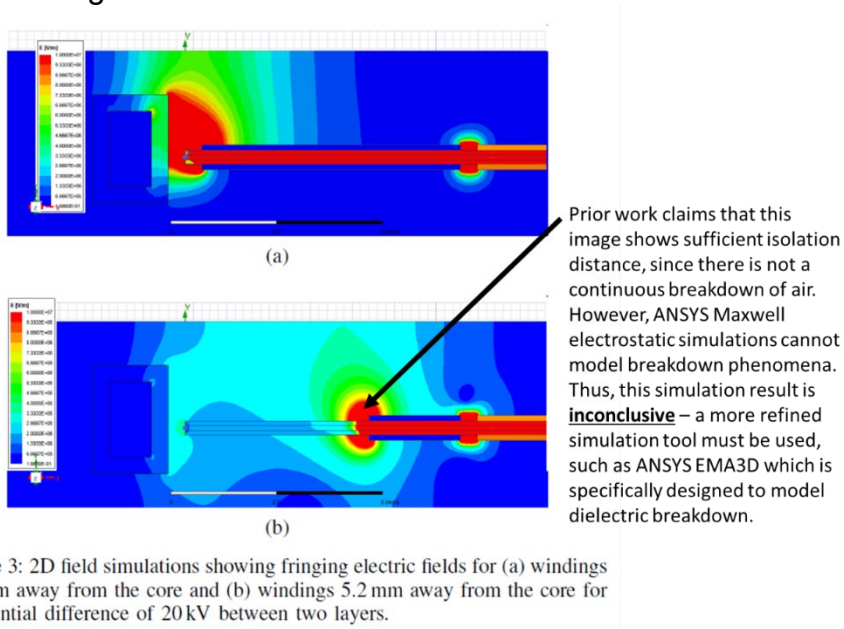



Figure 3: 2D field simulations showing fringing electric fields for (a) windings 1.2 mm away from the core and (b) windings 5.2 mm away from the core for a potential difference of 20 kV between two layers.

**Figure 3.** Figure from prior work [7] suggesting how ANSYS electrostatic simulations can be used to design the isolation spacing between windings and the transformer core. In this project, we show that this is an inappropriate use of this software owing to its inability to propagate the effects of dielectric breakdown. The true results of this simulation are ambiguous, and our in-lab tests confirm breakdown through the air in this arrangement closer to 14kV rather than better than 20kV.

Second, the prior design employs through-hole vias to connect its interleaved winding layers, as seen in Fig. 2. This is a key trade-off of interleaved windings: since the windings are interlaced, interconnecting the turns on the different layers becomes more difficult (these vertical connections must not connect to the turns of the other winding). In

the prior design, significant volume is devoted to isolation spacing between the through-hole vias and the windings and this also dramatically increases the winding length of each turn. This large spacing is designed assuming dry air separates the windings from the vias, but the inner layers of the PCB are surrounded by the high-dielectric-strength PCB dielectric and so this large spacing is unnecessary. Furthermore, our simulations of this design indicate that the top and bottom winding layers *cannot* be exposed to air owing to breakdown conditions occurring between the turns on these layers. This means that the top and bottom layers must also be enveloped by an insulator. Notably, this additional insulation requirement is implied but not explicitly discussed by the prior work -- the fabricated design, shown in Fig. 2 includes additional top and bottom PCB dielectric layers encapsulating the identified 12 winding layers. This effectively results in a 14-layer board with 12 “inner” winding layers. Given that all the winding layers are actually enveloped by PCB dielectric, the detrimental spacing requirement imposed by the prior design is unnecessary.

Finally, the prior design encapsulates the transformer core in a high insulation epoxy material to prevent dielectric breakdown between the windings and the core. However, because the windings *must* be fully encapsulated by PCB dielectric, the only remaining breakdown path through air is between the through-hole vias and the core. This suggests that a small amount of epoxy can be used to insulate the vias, rather than a large amount of epoxy being used to insulate the core, greatly simplifying manufacture.

In this project, the focus is on employing non-interleaved windings to greatly simplify the isolation design, which represents the biggest burden on the design of these transformers. We reduce the number of winding layers from 12 to 4 to minimize the number of isolation barriers and minimize the ac resistance penalty of non-interleaved windings, and we maintain a similar copper loss owing to the elimination of the winding excursion in the prior design. Furthermore, the planar transformer system concept allows a fine-tuned trade-off between core loss and copper loss and can further help to minimize the copper loss penalty in a non-interleaved design.

Our original vision was to employ a single four-layer PCB for both the primary and secondary windings, with blind vias interfacing L1-L2 and L3-L4. However, the discovery of the need for winding encapsulation changed this to a focus on each winding being implemented by its own PCB with encapsulation. We determined the best solution to be a 4-layer board where only the two inner layers are used, rather than seeking encapsulation with an alternative material (such as insulating epoxy). Our approach to targeting the most insulation-favorable designs resulted in demonstrating planar transformers having a fraction of the cost, tremendous flexibility in dielectric material selection, lower loss, and lower volume than the prior art, while achieving 1.5x higher isolation capability.

## 1.3 Planar Transformer Costs[1]

A widely touted feature of planar magnetics is their cost savings compared to wire-wound alternatives. This benefit is typically assessed qualitatively, for example, by noting the simpler manufacturing of printing the windings and slotting in a planar core compared to using a coil former to wind turns on a bobbin, mounting that bobbin on a core, and then installing the magnetic unit onto a PCB. Similarly, the cost impact of certain planar design

[1] This section includes direct excerpts from the introduction of the paper we published on this topic [9].

choices, such as the number of layers, is also typically assessed qualitatively (e.g., by the reasonable assumption that a board with fewer layers will be less costly [5], [10], [11] or that some designs are complex to fabricate than others [12]). Cost is an important metric in the trade-offs of considering a planar magnetic design. While the quotation from PCB manufacturers determines specific final costs, the ability to understand cost trends and estimate cost impacts in a planar magnetic design is useful.

In utility-scale solar PV applications, planar transformer cost estimates are necessary to compute the levelized cost of electricity (LCOE) and is thus fundamental to assessing the benefit of a new approach. However, because the literature does not contain a clear assessment of planar magnetic costs, existing LCOE optimizations have relied on conventional volume-scaled cost models which are poorly suited for planar magnetics [7]. Furthermore, the work in [7] has identified the transformer cost as critically impacting LCOE, emphasizing the importance of being able to identify it accurately.

Typical wire-wound magnetic components have costs that scale reasonably with volume since the primary materials that comprise the component, such as silicon steel and copper in a power transformer, are priced by weight (and by proxy, volume)[2]. In contrast, two planar magnetic components having similar volumes may have dramatically different costs, depending on the details and complexity of their manufacturing requirements.

The literature on cost considerations in planar magnetics is sparse. The most relevant study is in [13] which formulates a cost-benefit analysis comparison between a planar and conventional transformer for a specific 100kHz power supply. However, this study does not provide a basis to compare two different planar magnetic components, and it does not consider constructions wound directly on a PCB (instead, it considers the historically more common implementation of planar magnetics in which the windings are implemented by multiple separate PCBs)[3]. Similarly, [14] offers a clear description of the process by which a manufacturer develops a PCB cost quote but does not offer quantitative insight into modern cost trends for planar magnetic windings.

In this project, we clarify and quantify the key factors affecting the cost of planar magnetic windings to enable their cost-informed design. In doing so, we acknowledge that assessments of cost can be tenuous, as it is inherently affected by a multitude of economic factors which are difficult to control, including the local cost of labor, the impact of economies of scale, purchasing power of an entity (e.g., of an academic laboratory versus a multinational corporation), and the current state of the relevant supply chains. However, a clear, well-justified assessment of the relative cost impacts is a useful tool for researchers and designers who are exploring new planar magnetic architectures and configurations or who wish to leverage these components in cost-constrained systems. Our intent is not to provide exact price models for planar magnetics but to create a model allowing cost to *inform* their design and compare between designs.

## 1.4 Assessing Magnetic Core Loss

Transformers have two loss mechanisms: conduction loss in the windings (called “copper loss”) and losses in the magnetic core (called “core loss”). The former is

[2] Modifications to cost owing to specialized windings (e.g., Litz wire) or insulation materials can also be readily estimated from manufacturer catalogues.
[3] Importantly, this study also indicates that the planar magnetic winding cost can be dominant, further emphasizing the importance of modeling it well.

straightforward to assess from small-signal measurements and can be extracted from standard in-lab equipment, such as an impedance analyzer. The latter cannot be extracted from a small-signal measurement. To support the optimized design of planar transformers, especially for the planar transformer systems explored in this work which involve a careful trade-off between core loss and copper loss, we developed an in-house core loss tester. This tester generates square wave voltages which drive flux densities that are representative of their true deployment in a dual-active-bridge-style converter.

During our testing, we automated this tester. This was both convenient but also critical for ensuring repeatable measurements. We used this automated tester to report the core loss of our developed transformer and confirm the accuracy of our loss modeling. We also validated it against the MagNet dataset, which is the first open-source large-scale core loss dataset [15]. In performing this validation, we recognized a challenge: this representative dataset was originated by one research group on one experimental test bed, and there are inherent errors associated with this testbed which are likely to be different from the data produced by our testbed. Thus, we proposed simple error characterization methods for new contributions to these kinds of datasets, and to better contextualize errors between our data and the MagNet dataset.

# 2. Project Objectives

Numerous recent SETO-supported projects target modular conversion for utility-scale PV as a pathway towards industry and SETO goals of higher reliability, repairability, and efficiency to enable long-haul systems that meet SETO's LCOE target of $0.02/kWh by 2030 [1], [16]. This project greatly improves the ability for this suite of emerging converter concepts to meet these goals as it targets cost-optimized, high-isolation-strength, low-loss design of the high-frequency transformer they ubiquitously require. Thus, it greatly strengthens LCOE gains of these architectures while also simplifying their manufacture. The proposed framework can also be directly employed within existing foundational efforts to optimize the LCOE of modular PV systems [17].

## 2.1 Project Goals and Outcomes

The overall objective of this project is to develop and experimentally demonstrate a framework for designing these planar transformer systems to elucidate trade-offs between efficiency, volume, and cost, and to enable planar transformer designs for emerging utility-scale modular PV systems which produce best-in-class results in these three metrics while supporting MV isolation requirements.

The project goal was that a planar transformer would be demonstrated with a loss less than 55W (i.e., lower than the state-of-the-art [7]) and/or a volume better than 30in$^3$ (i.e., much lower than the state-of-the-art at ~42in$^3$ box volume) while having lower cost than a 12-layer board using Panasonic Felios RF775 dielectric and using industry-standard PCB construction materials and layer counts to yield significant cost reductions. This last metric, developed at the start of the project, did not account for the prior art's true deployment as a 14-layer board as discussed in Section 1.2. A demonstrated isolation voltage better than 26kV was targeted to meet or exceed the isolation capability of the prior art.

It is important to note that no standard yet exists which defines the isolation requirement of transformers embedded in power electronics. Recognizing this, PI Ranjram joined the P3105 IEEE working group which is developing recommendations for

such standards. In the absence of a standard, the focus in this project is an isolation metric relative to the prior work (>26kV).

## 2.2 Significance, Innovation, and Fundamental Advancements

This project pursued six technology innovations to achieve the project goal:

1. Develop non-interleaved low-layer-count PCB planar transformers to reduce the number of MV isolation barriers to one, dramatically reducing the dielectric strength requirement of this barrier compared to prior art, and greatly expanding the possible PCB materials that can be used for MV isolation applications.
2. Advance the implementation of these transformers as systems which comprise multiple series connections of transformers to optimize the trade-off between core loss and copper loss.
3. Develop a design framework to design these planar transformer systems to minimize their loss within a desired box volume.
4. Develop a planar magnetic winding cost model which captures the impacts of PCB complexity to replace previously proposed volume-scaled approaches.
5. Develop a square-wave core loss tester to accurately characterize the core loss of the developed transformers, and to verify the core loss estimation.
6. Establish high voltage isolation test capability to experimentally validate the isolation voltages of the developed transformers.
7. Correct the design discrepancies in designing the MV isolation barrier proposed in prior art.

## 2.3 Summary of SOPO Tasks

The technical tasks of this project were partitioned into five categories:

1. **PCB manufacturer cost surveying** (explicitly via direct correspondence and implicitly via quotation of exemplar transformers) and the **development of an empirical cost model** (in contrast to the state-of-the-art, which assumes linear scaling of cost with overall volume and does not account for pricing effects of non-standard dielectrics or board complexity).
2. **Design framework scope reduction** via evaluation of material availability, grounding requirements, creepage/clearance distances, transformer excitation type, and viable transformer system configurations.
3. **Design framework development and verification,** which employs simple loss models (Dowell's equation for copper loss [18] and the improved General Steinmetz Equation for core loss [19]). An output produced by this framework is compared to Finite Element Analysis simulations to ensure sufficient matching in predicted and simulated loss and insulation capability.
4. **Experimental development and measurement** of at least three planar transformer systems produced by the design framework. This includes the in-house development of a core loss tester capable of square-wave excitations reflecting the transformer excitation type, resistance measurements to characterize the conduction loss characteristics, and hi-pot dc isolation testing of the fabricated systems.
5. **Knowledge transfer** of the innovations gained in the project.

The specific SOPO subtasks are specified in the table below, including their end of project status. Highlighted tasks in this table correspond to milestones. There were no Go/No-Go decision points. All tasks were successfully completed, with augmentations occurring during the project to 2.7, 3.1, and 5.4 as discussed below.

| Task Number | | Comment |
|---|---|---|
| 1 | **1.1:** Obtain PCB cost data | Complete. |
| | **1.2:** Develop empirical cost model | |
| 2 | **2.1:** Select representative ferrite core material and coreset options | Complete. |
| | **2.2:** Evaluate transformer core grounding requirements and corresponding insulating potting options | Complete. |
| | **2.3:** Perform electrostatic FEA to determine transformer creepage and clearance to meet isolation requirements | Complete. This task was planned according to the design procedure in the prior art. It was determined during the project that this approach was not viable, and this was confirmed in subtask 2.7. |
| | **2.4:** Down-select transformer excitation type | Complete. |
| | **2.5:** Down-select viable planar transformer configurations | Complete. |
| | **2.6**: Create a report on the down-selection process | Complete. EOP Deliverable. |
| | **2.7:** Isolation measurement of exemplar transformers | Complete. This was an additional task added after Q1 of the project. Once we discovered the design inconsistencies in the prior art, we pivoted to an “experiment-in-the-loop” design approach. |
| 3 | **3.1:** Merge developed cost model with existing simplified transformer loss models | Augmented. The loss and cost model frameworks were both successfully developed. It was decided to keep them as separate tools rather than merge them as the planar winding cost model can be used in many other applications. The developed instructions are sufficient to use both. |
| | **3.2:** Verify a design output by the model in FEA simulation | Complete. |
| 4 | **4.1:** Design the core-loss tester circuit and verify in simulation | Complete. |
| | **4.2:** Fabricate and verify operation of the developed core loss circuit | Complete. |

| | | |
|---|---|---|
| | **4.3:** Experimental confirmation of core loss tester accuracy | Complete. |
| | **4.4:** Fabricate planar transformer systems | Complete. |
| | **4.5:** Obtain core loss, resistance measurements, and insulation results of transformer systems | Complete. |
| **5** | **5.1:** Research dissemination | Complete and in progress. One published peer reviewed conference paper, and two more peer reviewed conference papers accepted. Plans to submit journal manuscripts post EOP. |
| | **5.2:** Lecture development | Complete. EOP deliverable. |
| | **5.3:** Framework dissemination | Augmented. We have drafted detailed instructional documents in lieu of companion videos. EOP deliverable. |
| | **5.4:** Industry feedback | Augmented. PI Ranjram joined the IEEE P3105 working group, which kicked-off during this project. This group is drafting recommendations for a future standard on the isolation requirements of grid-connected power electronic converters with embedded high frequency isolation transformers. This participation established two final gaps towards the commercial deployment of our planar transformers as discussed in Section 5. |

# 3. Project Results and Discussion

All project milestones were achieved. We demonstrated medium voltage planar transformers with 1.5x greater isolation capability, >4x lower cost, and both lower volume and lower loss compared to the state of the art. Fig.4 summarizes the high-level achievement of the project.

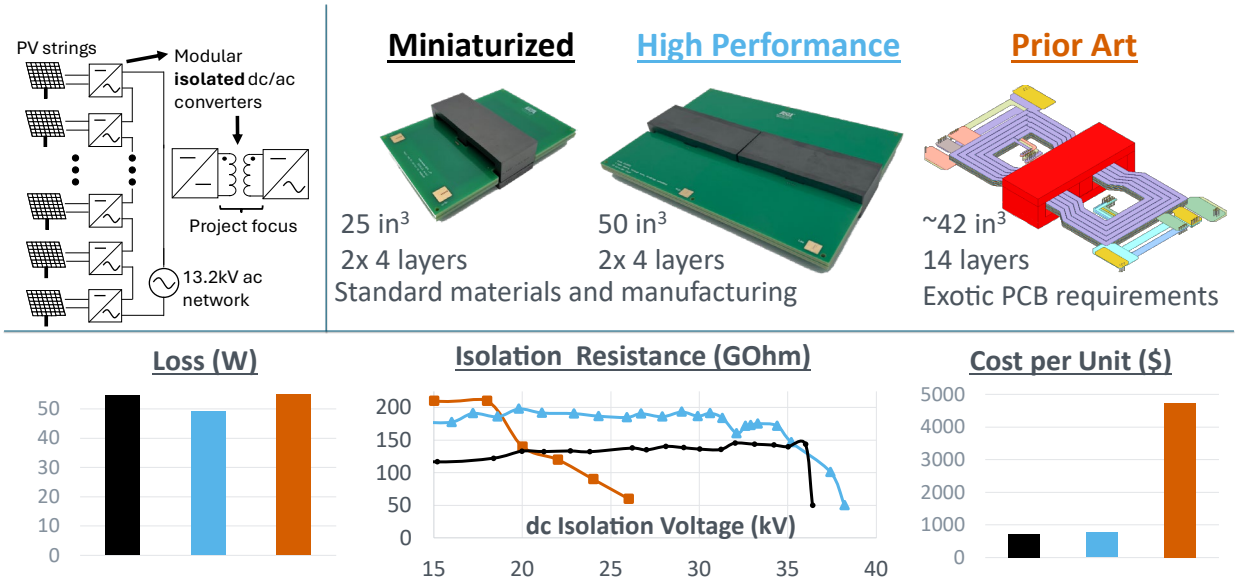



**Figure 4**. High-level summary of the project's achievement. The planar transformers developed in this project are smaller, lower loss, have higher isolation capability, and have much lower cost than the prior art.

## 3.1 Achievement of Milestones, Deliverables and Metrics

The project tasks, subtasks and milestones are summarized in Section 2.3. First, we describe the specific achievement of the milestones and their metrics. Then, we address the deliverables.

### Milestone 1.1.1

This milestone relates to the successful completion of Task 1.1 in which representative PCB cost data is collected to develop the cost model. The performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| PCB manufacturer responses<br>AND<br>planar transformer quotations | Similar cost estimates in responses from two PCB manufacturers<br>AND<br>>13 planar transformer quotations | Cost estimates within 20% from two manufacturers.<br><br>AND<br><br>Number of quotations obtained. | Verification of responses by DOE. |

A cost survey was prepared and sent out to 18 US PCB manufacturing houses to obtain explicit responses on cost impacts of key PCB design choices. Five detailed responses

were received, as well as three more general ones. The cost-impact estimates provided in these responses were within 20% across more than two manufacturers, meeting the first requirement of milestone 1.1.1. These qualitative cost impacts are summarized in the table below, with Fig. 5 showing how these parameters relate to planar PCB windings.

| **Feature** | **% increase in cost** | **Connection to planar winding design** |
|---|---|---|
| Layer count | 35-40% for every additional layer pair (e.g., 4 to 6 layers) | Key driver of copper loss – affects the number of turns per layer, ability to interleave |
| Via configuration | 20-30% increase for every additional via set | Strongly related to layer count and interleaving structure |
| PCB area | Scales with number of panels used (100% cost increase) | Board area is defined by the planar magnetic footprint |
| Copper thickness | 10-20% for increasing from 1oz to 2oz | Related to winding loss |
| Board thickness and stack-up | Non-standard stack-ups cost more, too variable to generalize | Typically specified to achieve a certain isolation requirement or to control interwinding capacitances |
| Dielectric material | 10-60% depending on the material | Related to isolation requirements, loss, and board thickness |
| Board milling | 0% | Related to core shape and isolation requirements. Stated to weakly affect cost. |

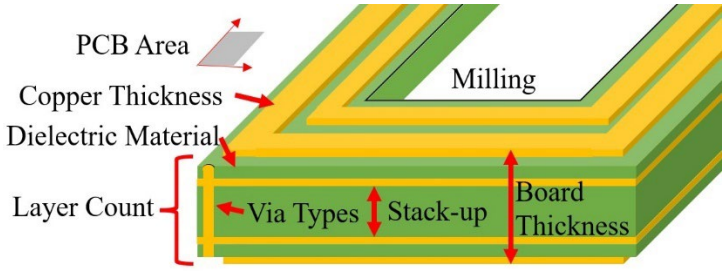



**Figure 5**. Key planar magnetic winding features are considered in the cost assessment.

The second performance metric was also met, with 81 PCB quotations obtained for 10 exemplar designs. These data are summarized in Fig. 6.

| Design | PCB dim. | Spacing | Man. 1 [Q: $ cost] | Man. 2 [Q: $ cost] | Man. 3 [Q: $ cost] | Man. 4 [Q: $ cost] |
|---|---|---|---|---|---|---|
| 1 | 4.57x5.01" | L2-L3: 52 mils | **5:** 4,112.9 **10:** 4,127.3 **20:** 4,714.6 **50:** 6,387.5 | **5:** 1,135.0 **10:** 1,582.0 **20:** 2,207.6 **50:** 3,573.5 | **5:** 3,450 **10:** 3,580 **20:** 3,875 **50:** 4,765 | - |
| 2 | | L2-L3: 70 mils | **5:** 4,112.9 **10:** 4,127.3 **20:** 4,714.6 **50:** 6,387.5 | **5:** 1,145.0 **10:** 1,595.0 **20:** 2,237.6 **50:** 3,648.5 | **5:** 3,431 **10:** 3,580 **20:** 3,877 **50:** 4,767 | - |
| 3 | | L2-L3: 96 mils | **5:** 3,434.8 **10:** 3,434.8 **20:** 4,160.6 **50:** 6,116.0 | **5:** 1,165.2 **10:** 1,502.3 **20:** 2,172.6 **50:** 3,673.5 | **5:** 3,450 **10:** 3,600 **20:** 3,950 **50:** 4,950 | - |
| 4 | 8.62x5.01" | L2-L3: 52 mils | **5:** 4,127.3 **10:** 4,714.5 **20:** 5,844.8 **50:** 9,667.5 | **5:** 1,457.3 **10:** 2,082.6 **20:** 2,823.2 **50:** 5,094.5 | **5:** 3,565 **10:** 3,850 **20:** 4,400 **50:** 6,150 | - |
| 5 | | L2-L3: 70 mils | **5:** 3,573.3 **10:** 4,160.5 **20:** 5,290.6 **50:** 8,559.5 | **5:** 1,472.3 **10:** 2,112.6 **20:** 2,883.2 **50:** 5,229.5 | **5:** 3,565 **10:** 3,850 **20:** 4,400 **50:** 6,150 | - |
| 6 | | L2-L3: 96 mils | **5:** 4542.8 **10:** 5,268.5 **20:** 6609.2 **50:** 10,792 | **5:** 1,502.3 **10:** 2,172.6 **20:** 3,003.2 **50:** 5,499.5 | **5:** 3,600 **10:** 3,900 **20:** 4,500 **50:** 6,400 | - |
| 7 | 4.57x8.71" | 10 layers; 5 mil b/w layers | - | - | **5:** 3,579 | - |
| 8 | | | - | - | **5:** 19,800 | - |
| 9 | 4.57x8.21" | 12 layers; 5 mil b/w layers | - | - | **5:** 4,500 | **4:** 3,473 **10:** 4,982 |
| 10 | | | - | - | **5:** 23,600 | **2:** 26,675 **10:** 69,245 **4:** 39,107 |

**Figure 6**. Obtained PCB cost data. All quotes use 2oz copper on all layers. Designs 1-6 employ stock FR-4, four layers, two sets of blind vias while designs 8 and 10 use RF775 and only through-hole vias. Designs 7 and 9 are identical to designs 8 and 10, respectively, except they were quoted with FR-4 dielectric (to isolate dielectric cost).

Critically, the obtained quotations confirmed one of the driving aspects of this project which is that the multi-layer construction of prior work which leverages a special, non-stock dielectric is substantially more costly than the simpler 4-layer constructions being pursued in this project. In particular, these PCBs were too costly for prototyping in this project, and so designs of this nature were not developed. However, this confirms the immense cost savings associated with targeting commonly stocked manufacturer PCB dielectrics.

### Milestone 1.1.2[4]

This milestone relates to the successful completion of Task 1.2 in which an empirical PCB winding cost model was developed. The performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| Planar PCB winding cost prediction matching to obtained data | <25% variation in predicted vs manufacturer reported costs across variations AND Correct trend prediction (i.e., that features predicted by the model to yield higher cost are consistent with the data obtained in 1.1.1.) | Aggregate manufacturer trends and create cost versus variation correlations for reported quotations. All manufacturer data is combined into the dataset to smoothen effect of possible manufacturer cost differences. | Cost model reported to DOE including plot of reported trends or empirical data points versus prediction of the model. Plot shows required matching tolerance of 25%. |

We proposed a "cost index" approach for modeling the total cost (TC) of a quantity Q of PCB windings:

$$TC = GFC \times DFI_d \times MFCI_m + Q \times (DIVC + BA \times DI_d \times LI_l \times GVC \times MVCI_m)$$

[4] This section includes excerpts from our work in [9].

In this model, there are fixed cost indices related to:

1. General fixed costs (GFC), such as the labor and overhead required to manufacture a $\mathrm{PCB}$ separate from the quantity that is produced or the specific design parameters. The model fits a single value of GFC on all the data it is trained on to extract a single "general" fixed cost associated with manufacturing a PCB.
2. Choice of dielectric material $(\mathrm{DFI_d})$. For example, if a material is not typically stocked, then there may be an upfront cost in stocking that material which the customer incurs separate from the number of units that are ordered. Every material that is part of the training data is assigned its own value of DFI (and labeled with a unique numerical subscript $\mathrm{d}$ ), with $\mathrm{DFI_1}$ assigned to 1. This indicates the relative fixed cost of using a different dielectric.
3. Choice of manufacturer $(\mathrm{MFCI_m})$, which modulates the above costs (e.g. different manufacturers may have different labor or overhead costs, or different ability to source dielectrics). Every manufacturer that is part of the training data is assigned its own value of MFCI (and labeled with a unique numerical subscript $\mathrm{m}$ ), $\mathrm{MFCI_1}$ assigned to 1. This indicates the relative fixed cost of using a different manufacturer.

There are also costs related to the quantity of PCBs which are being manufactured, which we term "variable costs". Specifically, we consider:

1. Choice of dielectric material $(\mathrm{DI_d})$. Every material that is part of the training data (labeled with numerical subscript d) is assigned its own value of DI, with $\mathrm{DI_1}$ assigned to 1.
2. Number of layers $(\mathrm{LI_l})$. One LI value is produced for each layer configuration in the data that is being fitted (labeled with numerical subscript $\mathrm{l}$ which is equal to the number of layers), with one layer count assigned to 1. For example, if the data has 4-,10-, and 12-layer information, then three LI indices are produced which indicates the relative cost of moving between these layer configurations.
3. General variable costs (GVC). The model fits a single value of GVC on all the data it is trained on to extract a single indicator of variable costs that can be impacted by board area. For example, it can capture scrap and copper weight effects.
4. Design-independent variable costs (DIVC), such as the labor and overhead required to manufacture a given PCB design which scale with the number of units that must be produced but are independent of the design details, including board area. In principle this can always be set to zero and its impacts absorbed by GVC, but its inclusion is a reasonable generalization (separating quantity-dependent effects from quantity- and area-dependent effects).
5. The choice of manufacturer $(\mathrm{MVCI_m})$ which modulates the above costs. Each manufacturer is assigned a value of MVCI (labeled with numerical subscript $\mathrm{m}$), with $\mathrm{MFCI_1}$ assigned to 1.

The indices of the model can be interpreted as relative cost factors for the feature captured by each index. For example, the quantitative data contains designs having 4, 10, and 12 layers. We choose four layers to have $\mathrm{LI} = 1$, and the fitted model will produce index values for 10 layers and 12 layers (for example, $\mathrm{LI}_4 = 1, \mathrm{LI}_{10} = 2.6,\ \mathrm{LI}_{12} = 3.0$ ). This indicates the relative cost penalty of a design changing between these layer counts which is separated from the other index factors. Thus, the cost indices approach has the advantage that cost trends or comparisons of two designs can be made by eliminating the manufacturer's parameter and quantity parameters to compare the cost of designs.

Note that there are no indices for via configuration or copper weight. In the former case, this is because the quotations have a direct coupling between via configuration and layer count - the four-layer boards use two sets of blind vias while the higher layer boards use only through hole vias. So, these two features are combined into the layer count. In the latter case, there is only one copper weight to be fit from the data and so the model does not require an index for this parameter. The model can be modularly extended to add additional features and this is discussed in detail in [9]. The indices derived for the collected data are shown in Fig. 7.

| Feature/Index | Value |
|---|---|
| **Design-independent / General** | |
| GFC / GVC / DIVC | 3304 / 2.72 / 0.0 |
| **Dielectric and Layers** | |
| FR-4[8] | $\mathrm{DFI}_1$=$\mathrm{DI}_1$ = 1.0 |
| Felios RF775 | $\mathrm{DFI}_2$= 19.3; $\mathrm{DI}_2$ = 4.1 |
| Layers | $\mathrm{LI}_4$=1.0; $\mathrm{LI}_{10}$=2.6; $\mathrm{LI}_{12}$=3.0 |
| **Manufacturers** | |
| Manufacturer 1 | $\mathrm{MFCI}_1$ = 1.00; $\mathrm{MVCI}_1$ = 1.00 |
| Manufacturer 2 | $\mathrm{MFCI}_2$ = 0.32; $\mathrm{MVCI}_2$ = 0.75 |
| Manufacturer 3 | $\mathrm{MFCI}_3$ = 1.04; $\mathrm{MVCI}_3$ = 0.34 |
| Manufacturer 4 | $\mathrm{MFCI}_4$ = 0.75; $\mathrm{MVCI}_4$ = 0.99 |

**Figure 7**. Cost model indices derived from the obtained PCB quotations.

The SOPO plot is shown in Fig. 8. The model achieves a 6.53% mean absolute percentage error with a standard deviation of 4.65% between the predicted and quoted values of the cost data, better than the 25% milestone requirement. The trend prediction is also correct (e.g., exotic dielectrics are much more costly, as are increasing layer counts). The model was also tested on a new set of cost data and shown to have good predictive power for cost features included in the training data. For example, the cost of a new 4 layer, 2oz board having a smaller area of 2.61x5.21” was predicted with 13% error. The index-basis of the model also ensures that trends are well predicted, as the penalty for adding increased cost components is clearly captured by the index method, as described above. For example, the relative cost of a 12, 10, and 4 layer board is extracted by the model.

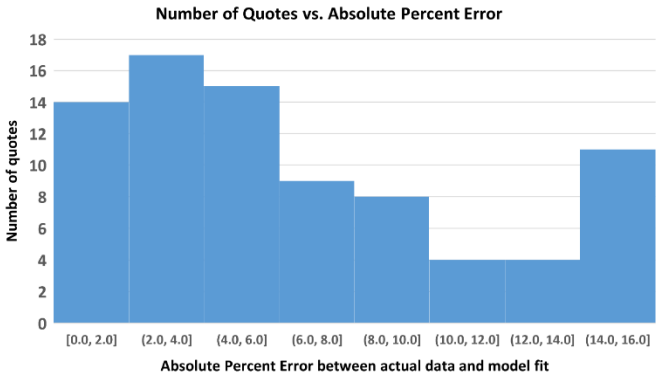



**Figure 8**. Summary of the cost index model error.

## Milestone 1.2.5

This milestone relates to the successful completion of Task 2.5, in which viable planar transformer configurations are selected which can achieve the EOP goals. The

performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| Viability | At least 3 different systems have a volume less than 45in$^3$, with at least one less than or equal to 30in$^3$. | Volume estimate based on coreset sizes and configurations. | Verification of volume assessments and methodology by DOE. |

Completing this milestone relied on completing a new task (Task 2.7) which was introduced after Q1 of the project. For completeness, we first begin by describing the work completed on this task.

After learning that prior work was not a 12-layer design as reported, but rather a 14-layer one (employing two additional PCB dielectric layers on the top and bottom of the board) [7], it was decided to pursue and experiment-in-the-loop approach to self-verify the isolation characteristics of possible transformer structures. A custom safety enclosure was designed and fabricated to ensure user safety during the high voltage testing in this project, as shown in Fig. 9. High voltage personal protective equipment (PPE) was also purchased (insulation blanket, insulation gloves, and glove protectors), as was a thermo-hygrometer for recording temperature and relative humidity. A safety procedure was devised for using the high voltage tester (PTS-75) with this enclosure and PPE.

**Figure 9**. High voltage test enclosure for multi-kV isolation testing of planar transformers in this project. The 0.09” aluminum enclosure is 5' x 3' x 2' and is solidly connected to earth. The viewing window is 0.25” Lexan.

A two-layer board with one turn for each winding and 2.4mm of FR-4 between the two copper layers was fabricated having 4.8mm clearance between the edge of the windings and the cutouts for the core, as shown in Fig. 10. The primary winding and secondary winding were each short-circuited, and the high voltage from the PTS-75 was applied between these two short-circuits. A smartphone on a tripod was used to record all isolation tests. This winding arrangement was only able to support 14kV before failing. The video recording confirmed that it was not the FR-4 dielectric of the PCB which failed, but rather that arcing occurred through the air. A screenshot from this video is shown in Fig. 11. Critically, an ANSYS Maxwell Finite Element Analysis (FEA) simulation of this setup in Fig. 12 shows that only

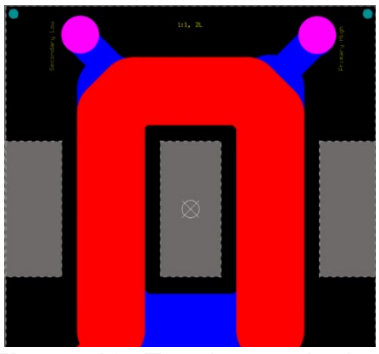


**Figure 10**. Two-layer, single-turn design for PCB isolation testing. This matches the spacings selected through the tasks completed in Q1 of the project. The red trace is the primary, the blue trace is the secondary.

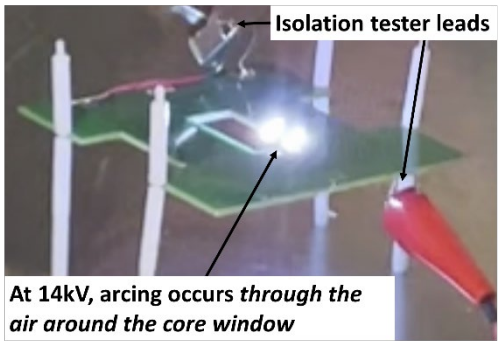



**Figure 111**. Screenshot from isolation testing recording of 2L board in air.

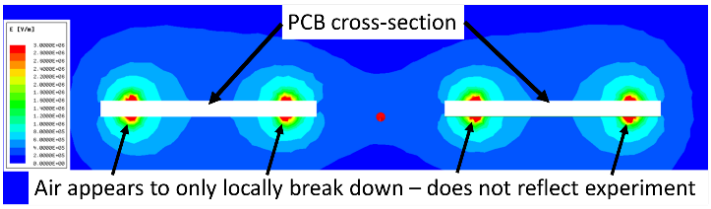
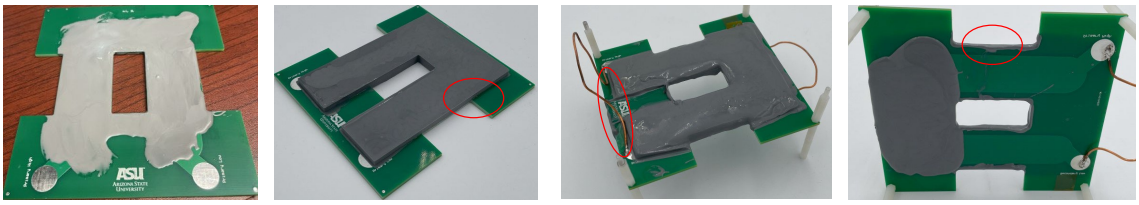



**Figure 12**. ANSYS Maxwell FEA simulation result for the experimental condition in Figure 11. Air breakdown is indicated in red.

"partial" breakdown of the air occurs, which is not sufficient for breakdown according to prior work [7]. This confirms that ANSYS simulations do not correlate to experimental results of isolation testing. ANSYS Maxwell cannot model dielectric breakdown propagation. While breakdown is likely occurring where Maxwell suggests it is in Fig. 12, the software is incapable of propagating that breakdown.

This experimental result confirms the importance of the additional top- and bottom-layer isolation layers used but not discussed in prior work [7]. Critically, the FR-4 dielectric is not the bottleneck on isolation in this experiment – it is the breakdown of air around the PCB which causes isolation failure. To confirm this, Sylgard 164 isolation material was applied to different copies of the same PCB design in Fig. 10. This material has a dielectric rating of 19kV/mm, and a number of different applications were explored (ref. Fig. 13) including: (1) a thin layer applied by hand to the primary, (2) a 4mm mold applied using a 2-part applicator gun to the primary, (3) the previous design, but with the mold removed during curing, (4) the previous design, but with Sylgard 164 also applied to part of the secondary winding.



Thin application, 22kV
24°C, 36% Relative Humidity

4mm mold, <10kV
24°C, 60% Relative Humidity

+ unmolded cure, <20kV
24°C, 61% Relative Humidity

+ secondary cast, >26kV
24°C, 62% Relative Humidity

**Figure 12.** Example applications of 19kV/mm Sylgard 164 insulation material. The red circles indicate points of failure observed in experiment.

The 4mm mold failed at a relatively low voltage (arcing at 19kV). It was cured in a 3D mold, and when that mold was removed the isolation was also slightly "peeled" off the board. An air-channel was formed at the location highlighted in Fig. 13 which likely concentrated the electric field and yielded the much lower resistance. To avoid peeling, this method was revised by pouring the Sylgard 164 into the developed mold, but removing the mold during curing, so that it would adhere to the PCB. This increased the measured resistance but failed at 20kV due to arcing from the primary winding connection, emphasizing the importance of considering how the primary winding is

connected to the rest of the system. Isolation was further added to the secondary winding and improved the breakdown to >26kV, with the failure occurring outside of the isolated section of the secondary.

It is emphasized that dielectric failure of the PCB was not observed during any testing. Failure always occurred through the Sylgard 164 material through the air. For example, one failure observed at 30kV for the unmolded cure with secondary insulation is shown in Fig. 14. This suggests a thickness of approximately 1.5mm in the region of failure, which is consistent with a visual observation of the application there. This emphasizes that the PCB dielectric is only part of the design requirement, and very careful consideration must be made for how the windings exposed to air, and to the core, achieve the required isolation. The design procedure proposed in prior work to use ANSYS Maxwell electrostatic simulations is insufficient.

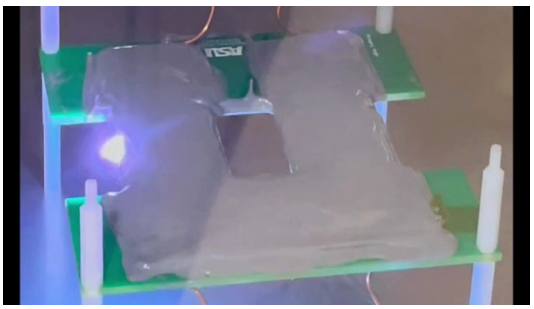


**Figure 13**. Isolation breakdown during experimental testing always occurred through the air.

Based on these results, new constraints are imposed on the developed transformer systems. Namely, there must be a solution for fully isolating the primary winding of the core. The following options were considered:

1. Top and bottom isolation is achieved entirely through the PCB's construction. In this case, through-hole vias cannot be used because it interrupts the primary-to-secondary isolation and increases the winding length of each winding (since they must be routed to avoid these through-hole vias). Thus, the only feasible method is to implement each winding on its own PCB. These can both be 4-layer boards with the windings applied on the two internal layers and connected with through-hole vias or buried vias. Thus, the PCB's dielectric serves as the top- and bottom-layer isolation for the winding, as in the prior work. If through-hole vias are used, a small amount of Sylgard 164 isolation material is applied to isolate them.

2. Top and bottom isolation is achieved via Sylgard 164 isolation material (or similar material). This was not pursued owing to the manufacturing inconvenience, cost, and poor repeatability of employing the molded winding concept illustrated in Fig. 13.

Based on the isolation results of Task 2.7, four core-to-winding spacings were considered in Task 2.5: 3, 5, 7.5 and 10mm. The larger this is, the simpler it becomes to achieve the required isolation (giving more separation through the dielectric that will be applied to shield the windings) but the worse the losses are (as less of the winding window is available for the transformer windings). A separation of at least the same amount in the vertical direction of the core window is also required for isolation between the primary windings and the core, which is nominally at the same potential as the secondary winding. This limits the coresets under consideration to: EILP102, ELP102, and ELP64, having core window heights of 20.3, 26.6, and 10.2mm, respectively. Three copper thickness arrangements are considered: 3/3/3/3oz, 3/2/2/3 oz, and 2/2/2/2 oz copper for layers 1/2/3/4, respectively. Owing to the severity of the isolation requirement, only series

connected transformer systems are considered. This greatly simplifies connection of the primary windings to the circuit it interfaces to, which we have seen is a critical element for isolation design. Milestone 1.2.5 requires the selection of three planar transformer configurations having less than 45in$^3$, with at least one having less than or equal to 30in$^3$. These are:

1. EILP102 core, 3/3/3/3oz copper, 3mm core-trace spacing, standalone, 28 turns on both primary and secondary. Estimated volume: 17.6in$^3$, estimated loss: 38W.
2. ELP64 core, 3/3/3/3oz copper, 3 mm core-trace spacing, 2 in series, 32 total turns on both primary and secondary. Estimated volume: 14in$^3$, estimated loss: 39W.
3. ELP102 core, 3/3/3/3oz copper, 10mm core-trace spacing, 2 in series, 34 total turns on both primary and secondary. Estimated volume: 45in$^3$, estimated loss: 55W.

These are the lowest loss design, the lowest volume design, and a design which supports a large 10mm core-trace spacing with a large core window, respectively. Note that the first two model results exceed the minimum requirement of better-than 55W and/or better than 30in$^3$ volume. The details of the loss estimates are explained in the Milestone 1.3.2 description.

The volume is assessed as the box volume of the transformer including its windings. For example, Fig. 15 shows an example back-to-back ELP core, the box volume is

$$V_{box} = A \times (2B) \times (C + E - F - 2s_{ct})$$

For transformer system arrangements, it is assumed that the cores are side-by-side and touching, so that no volume is lost to spacing between the cores. In this case, the volume of a two-transformer system is simply twice the volume of one of the transformers.

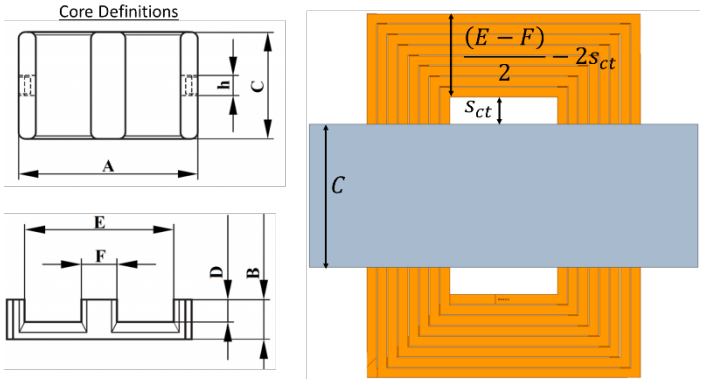



**Figure 14**. Planar transformer volume estimate parameters.

## Milestone 1.3.2

This milestone relates to the successful completion of Task 3.2, in which the developed loss estimation models are verified against an FEA simulation. The performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| Loss matching | Better than 15% matching in copper loss and 15% matching core loss between a design output by the framework and FEA, with justification for error. | FEA eddy current simulation for copper loss; FEA transient simulation for core loss. | Loss comparison verified by DOE. |

The design framework requires estimation of the core and copper loss of a given transformer system construction, and Milestone 1.3.2 requires better than 15% matching

between the estimated loss and a FEA simulation of loss. To estimate copper loss, Dowell's equation is used [18]. Namely

$$R_{ac} = F_R R_{dc}$$

where $R_{dc}$ is the dc resistance of the winding and $F_R$ is the "ac resistance factor" which quantifies the resistance-increasing, frequency-dependent skin and proximity effects. Dowell's equation is accurate for planar transformer systems with no gap in the core path. The total loss is computed as

$$P_{copper} = \frac{1}{2}\sum_{n=1}^{11} I_{n,pk}^2 R_{ac}(nf)$$

Where $I_{n,pk}$ is the $n_{th}$ harmonic of the current through the transformer and $f$ is the fundamental frequency (200kHz). This Fourier decomposition is required since the currents in the transformer are trapezoidal, as shown in **.**

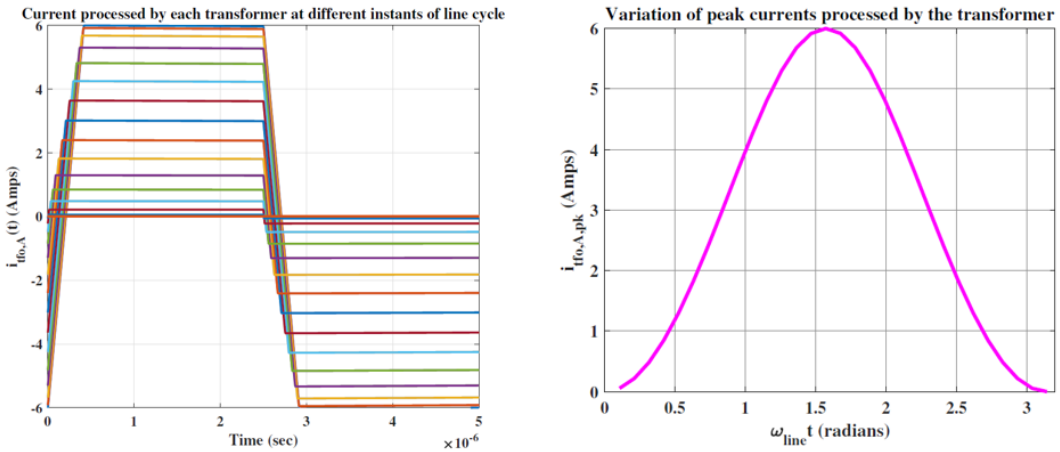



**Figure 15**. The transformers carry trapezoidal currents, with the peak of these currents changing during one 60Hz line cycle as shown in [7].

The first 11 harmonics are chosen because these well capture the frequency content of a symmetric trapezoid. The copper loss associated with 31 different peak currents are computed and then averaged to compute the net effective copper loss. Note, for example, that while the transformer must be rated to carry 7.55A$_{pk}$ at 200kHz (associated with the first harmonic of the trapezoid with peak 6A), it only operates here for a fraction of the overall line cycle. The average of the loss across the line cycle is the actual indicator of average loss and is consistent with the reporting in [7].

The core loss is computed using the improved General Steinmetz Equation [19], with the Steinmetz parameters extracted from [20]. The corresponding equation is

$$P_{core} = k_{iGSE} \cdot \left(\frac{V}{NA_c}\right)^{\beta} \cdot (2f)^{\alpha-\beta} \cdot V_e$$

Where $k_{iGSE}$, $\alpha$ and $\beta$ are the Steinmetz coefficients in the iGSE framework, $V$ is the peak square voltage applied to the core (1000V), $N$ is the total number of turns which support this voltage on each winding, $A_c$ is the cross sectional area of the centerpost of the core ($F \times C$ in Fig. 15), $f$ is the switching frequency (200kHz), and $V_e$ is the volume of the core which carries flux (initially assumed to be the full core volume).

An example design featuring 16 primary and secondary turns and an EILP102 core is input into ANSYS Maxwell, with 500V applied to the secondary winding, mimicking the voltage across it if it was in a two-transformer system. This simulation predicts 25.8W of copper loss for a $6A_{pk}$ trapezoidal current, and 10.3W core loss in this 16-turn transformer. The model predicts 24.7W of copper loss and 12.8W of core loss. The error in the copper loss prediction is within bounds (5%, less than the 15% requirement). The core loss prediction is too high (24%). This is attributed to the fact that the simulation properly accounts for the flow of core flux, and the "outer edges" of the core carry almost no flux, as shown in Fig. 17. On a total cross-sectional area of $1827mm^2$, the estimated zero loss regions are approximately $208.3mm^2$. This suggests that the core loss estimate should be reduced by 11.4%. Doing so yields 11.3W, which is within 10% of the prediction of the model, as required.

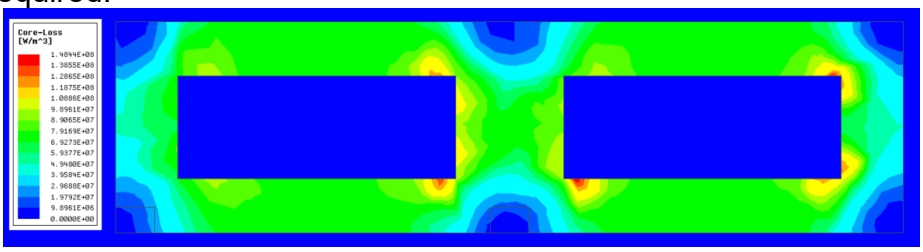



**Figure 16.** Simulation showing the core loss locations in a cross-section of the simulated core. The preference for flux to avoid corners of the core is clear (blue indicates zero loss). Thus, the effective volume for estimating core loss is lower than the actual core's volume by approximately 11.4%.

### Milestone 1.4.3

This milestone relates to the successful completion of Task 4.3, in which the developed core loss tester's measurement accuracy is validated to publicly available core loss data. The performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| Measured core loss match to publicly available core loss data | Better than 30% matching in measured and publicly available core loss measurements on at least three different core materials. At least 20 points of varying flux densities and frequencies will be tested for each core material. The average of these 20 points must have better than 30% matching for each core that is tested. | Performed on in-house core loss tester developed during project. | Core loss test waveforms and measurement data comparison reviewed by DOE. |

To ensure consistent data measurements, an automated test setup was developed using the core loss tester. A schematic block diagram of the tester is shown in Fig. 18. The setup comprises an oscilloscope, which records voltage and current measurements on the device under test, a dc power supply with powers the tester, a gate driver power supply, a DSP controller which transmits gating commands to the switches of the square wave inverter, and a temperature sensor for recording the temperature of the core under test. The core is wound with two sets of windings, the first connected to the exciting square wave generator and the second used to measure the voltage on the core. By

measuring the current through the first winding and the voltage on the second winding, taking their product, and then computing the average of this product (all done on the system oscilloscope), the power loss in the core can be measured. The frequency and flux density of the core is settable by controlling the switching frequency of the inverter and the voltage of the dc power supply, respectively. This control is all commanded through a central computer to ensure consistency in system measurements. The tester can produce waveforms up to 400kHz.

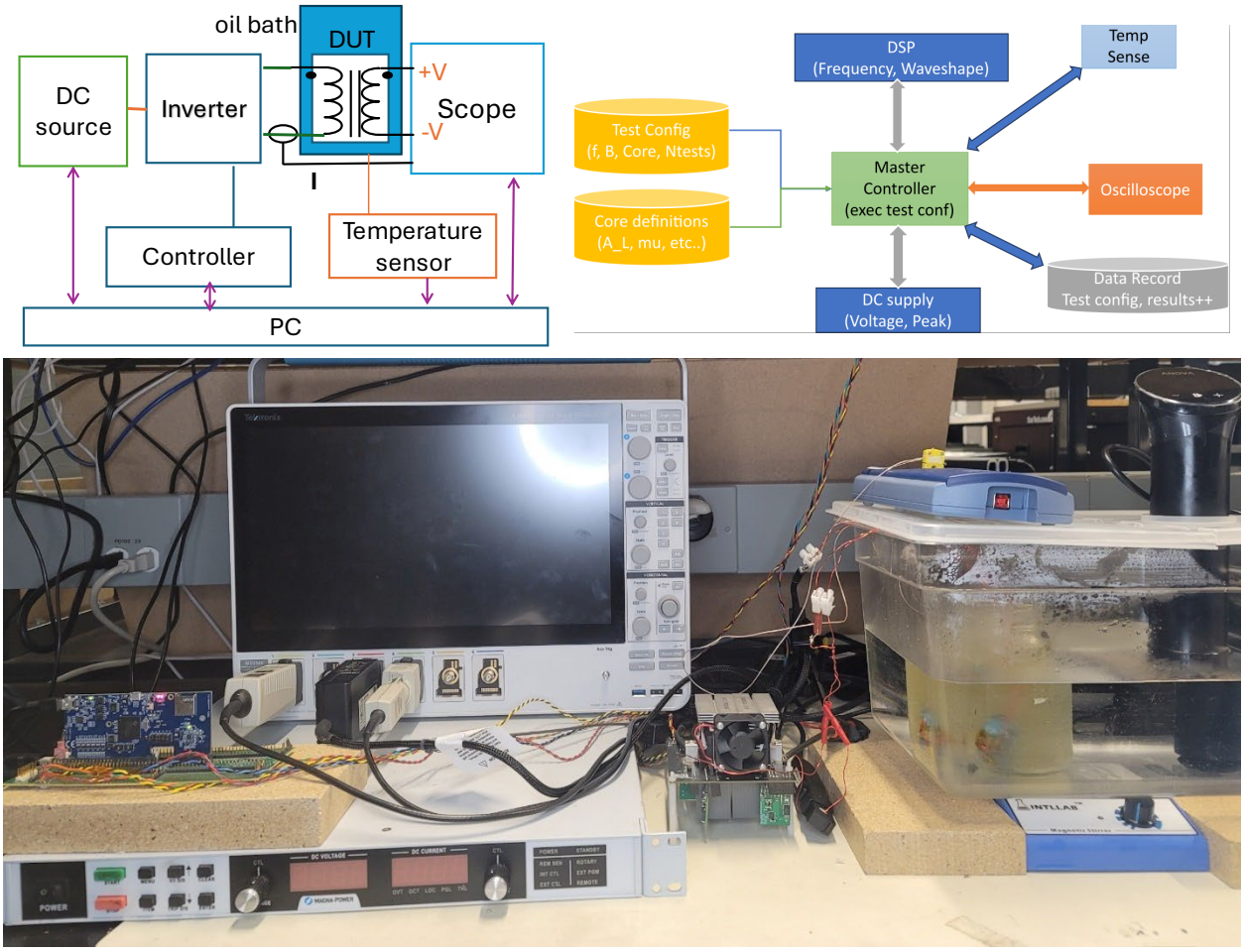



**Figure 17.** Automated core loss tester. Top left: overall measurement schematic. Top right: automation structure. Bottom: Hardware image showing oscilloscope, dc power supply, custom full-bridge inverter, inverter control card, Anova precision temperature controller, and Pico Technology thermocouple logger.

A “self-validity” check on the tester is included by measuring two additional powers in the system. First, the input power is measured (reported directly by the in-built voltage and current readings of the dc power supply). Second, the power output from the inverter is measured (by adding an additional voltage measurement at the output of the inverter; the corresponding current is the same as what drives the core under test and is already measured). It is known that the core loss must be less than the power output by the inverter, and this power must itself be lower than the power output by the dc supply. The validity of a given measurement can be checked by ensuring this consistency with the

power measurements. If a reading does not satisfy these rules, the reading is ignored. This tends to happen primarily in conditions of very low power loss.

To evaluate the accuracy of our tester, we tested three core materials that are included in the MagNet dataset [15]: TDK/Lambda N87, Fair-rite 77, and Ferroxcube 3C90. MagNet includes a machine-learning based statistical model built from the loss data they collected, which also enables efficient querying of their data. Our measurements had better than 30% average error across all three materials taken over at least 20 samples of varying frequency and flux density, satisfying the SOPO requirements. The statistics of these measurements is shown in Fig. 19.

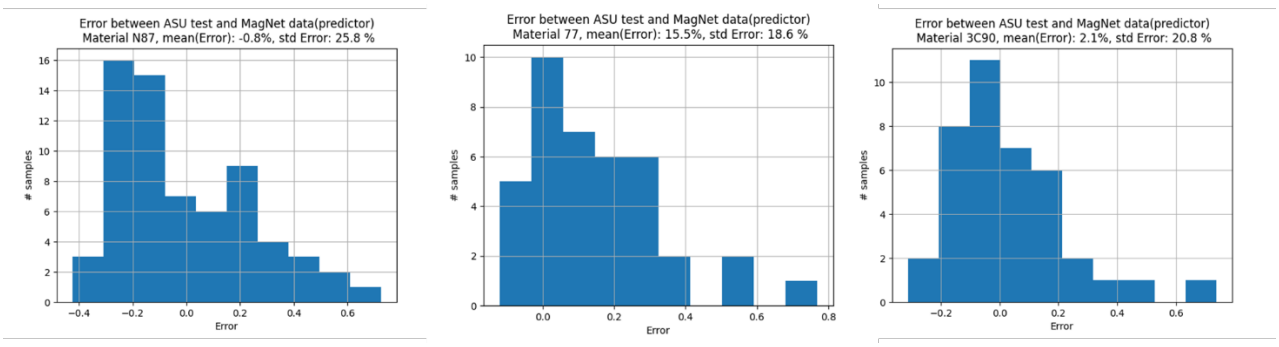



**Figure 18**. Error analysis comparing collected data to MagNet dataset. The maximum mean error is in the FR77 material, at 15.5%, well within the SOPO requirement of 30% matching.

Error information in a large scale dataset is critical because it affects one's ability to compare a new core loss tester to this dataset, as well as making it difficult for a user to attempt to aggregate multiple large-scale datasets (e.g., aggregate the MagNet data with the data generated in this project). We formulated metrics for assessing and publishing the error of one's own core loss tester, rooted in measuring the tester's repeatability variance (i.e., the loss it reports for the same datapoint taken in different measurements). A peer-reviewed conference paper has been accepted on this topic.

## EOP-A

This first end-of-project milestone relates to demonstrating the performance gains of the approach developed in this project. The performance metric, success value, assessment, and verification process are summarized in the table below.

| Performance Metric | Success Value | Assessment Tool / Method of Measuring Success Value | Verification Process |
|---|---|---|---|
| Loss, volume, and cost of developed planar transformer systems | Better than 20% matching between estimated and measured loss, volume, and cost.<br>AND<br>The trends in relative cost, volume, and loss of the planar transformer systems must be correctly predicted by the design framework. For example, the model should correctly predict which of the three systems | Volume and cost are directly reportable without measurement. Core loss is measured via the developed in-house core loss tester. Resistance measurements are obtained via impedance analyzer measurements which directly relate to copper loss. Insulation results are obtained using the hi-pot tester equipment specified in the budget. | Framework results, loss data, and any refinements in the design framework are reported to DOE. |

| | | | |
|---|---|---|---|
| | has the highest cost, separate from the quantitative accuracy of that prediction.<br>AND<br>A transformer is demonstrated with loss less than 55W and/or volume better than 30in$^3$ while having lower cost than a 12-layer board using Panasonic Felios RF775 dielectric. | | |

As shown in Fig. 4, we demonstrated two planar transformers which exceed the main metric of the EOP-A goal. One design, using one EILP102 core, has a 25 in$^3$ box volume, 54.6W loss, >4x lower cost compared to the state of the art. The other design, using a 2xEILP102 planar transformer system has a 50 in$^3$ box volume, 49W loss, and a similarly lower cost to the state of the art. Both meet the EOP-A goal. Critically, though not identified as a metric in EOP-A, these designs also have much higher isolation voltages, reaching the 60GΩ failure point identified by the prior art at 36kV and 38kV, respectively, compared to the 26kV of prior art. Notably, the 2xEILP102 design also achieved better than 60kV withstand voltage (i.e., we tested up to this value without achieving breakdown, and reducing from this value resulted in the isolation resistance recovering). Thus, the developed designs are lower cost, lower volume, lower loss, and have much better isolation performance.

The remaining metrics relate to the developed design framework which produced the three planar transformer windings in Fig. 20.


**Figure 19**. The winding structures of the three planar transformer systems built for EOP-A.

First, we discuss the cost modelling results. This model was developed based on surveying US manufacturers, but we encountered quality-control difficulties during the project. Namely, a design manufactured by a US manufacturer had a 1.5x higher dc resistance than expected. In contrast, the same design manufactured in China had a 1.2x higher dc resistance. This higher performance led us to manufacture the final designs by this manufacturer. Because the model was not trained on this manufacturer's data, there

is a higher likelihood for cost errors. Nevertheless, a strength of the approach is that it is possible to define manufacturer indices MFCI=0.18 and MVCI=0.24 for this new manufacturer by comparing the costs of this single design. The results are shown below.

| Winding Type | EILP102 | 2x EILP102 | ELP64 |
|---|---|---|---|
| Estimated Cost [Quantity:20] | $908 | $1212 | $761 |
| Purchased Cost [Quantity:20] | $843 | $812 | $673 |
| Error | +8% | +50% | +13% |

Two of these designs are within the 20% expectation. This showcases the strength of the approach, since **only one quote** was used to create estimates for this new manufacturer, while still accurately estimating cost. In contrast, the 2xEILP102 board was greatly overestimated. This suggests that this manufacturer has different board area impacts compared to the US-based manufacturer it was scaled from. The accuracy of the model for this manufacturer would be improved by re-training the model to incorporate more quotes from this manufacturer, and would likely result in a different MVCI to better capture board area impacts. Another possibility is that, even though the area of the 2xEILP102 board is similar, it occupies a similar panel burden on this manufacturer, and suggests they may be less susceptible to PCB area variation. Nevertheless, these results highlight the strength of the cost modeling approach and represent excellent matching in the context of updating it from only one additional quote.

The core loss is well predicted, as summarized in the table below. The results meet the performance metrics.

| Winding Type | EILP102 | 2x EILP102 | ELP64 |
|---|---|---|---|
| Estimated Core Loss | 15.5 | 14 | 7.6 |
| Measured Core Loss | 15 | 12.5 | 7.2 |
| Error | +3% | +13% | +6% |

The winding loss comparisons for the three designs is shown in the table below.

| Winding Type | EILP102 | 2x EILP102 | ELP64 |
|---|---|---|---|
| Estimated 200kHz resistance (Ω) | 1.3 | 1.3 | 3.2 |
| Measured 200kHz resistance (Ω) | 2 | 2 | 4.2 |
| Error | -54% | -54% | -31% |

These have significant errors, but the right trend loss. These errors are attributable to: (1) the inherent dc resistance error in the manufactured prototypes (20%, 20%, and 27%, respectively) – this is related to manufacturing imperfections; (2) the impedance analyzer used for these measurements has an inherent error of approximately 9% in these measurements; (3) the short-circuit applied in experiment further increases measured resistance and is not considered in the design framework. The takeaway is that the design framework as-is may underestimate ac resistance by ~25%. However, it is important to emphasize that this did not impede the development or demonstration of high performance prototypes in this project.

### EOP-B

This second end-of-project milestone relates to the final deliverables. They are related to four subtasks:

1. **Task 5.1: Research dissemination.** We have published one peer-reviewed conference paper related to the cost model [9], and have submitted two more related to the core loss tester and the planar transformer design concepts.
2. **Task 2.6: Down-selection process report.** This report explains how we arrived at the candidate planar transformer systems. This information is being integrated into Htat Min's recently accepted ECCE 2024 paper entitled "Improved High-Frequency, Medium-Voltage Isolation Planar Transformers". A pre-print copy of this paper will be made available on our research website to ensure appropriate dissemination. Integration of the contents of this report into this paper enables the full context of the issues identified in Subtask 2.3 to be incorporated into that discussion, which is critical for understanding the design selections that were made.
3. **Task 5.2: Sustainable Energy lecture material.** The project's ideas and results have been integrated into a set of lecture slides for integration into a lecture series on Sustainable Energy in development by our team.
4. **Task 5.3: Publish framework code and companion video.** We have attached the cost model and the planar transformer design models to this report. Detailed instruction documents have been drafted which we feel communicate using these tools more clearly and succinctly than a hosted video would. These files and instructions will be hosted on our website for public download.

# 4. Significant Accomplishments and Conclusions

This section summarizes the project's significant accomplishments, challenges encountered, and lessons learned.

## 4.1 Significant Accomplishments

In the 18-month period of performance in this project, we achieved several significant accomplishments.

### Met and Exceeded Originally Proposed Performance

At the start of the project, the estimated performance was demonstration of a 2x cost reduction in a similar volume and loss using standard materials and an easier to manufacture PCB winding process, while meeting the 26kV isolation performance of prior art. At the project's end (ref. Fig. 4), we experimentally demonstrated designs with >4x cost reduction having 38kV isolation voltages and demonstrated both lower loss and lower volume constructions.

### Identified and Corrected Design Inconsistences in Prior Art

This project originally contained tasks which built on the design procedure proposed in the prior art. We identified several design inconsistencies in this previously proposed approach:

1. Prior work incorrectly interpreted ANSYS Electrostatic simulations for defining the insulation design of planar magnetic transformers.
2. Prior work employed a *14-layer* PCB, though only 12-layers are used in the planar windings. These additional two layers allow encapsulation of the windings in PCB dielectric and are *fundamental* to the correct isolation performance of the design.
3. Given the requirement for additional layers which encapsulate the windings, prior art's design requirement for a large spacing between through-hole vias and the windings is not required. Eliminating this spacing dramatically reduces the winding length and thus the copper loss.
4. With this corrected understanding of the insulation limitations, it also becomes apparent that the core need not be encapsulated in a high isolation strength potting material as required in prior art. Instead, the limited portions of the windings which extend to the surface (owing to vias) can be potted with a fraction of the required material in prior art.

It is a significant achievement that we were able to exceed the original design outcomes even though significant and unplanned project time had to be devoted to understanding, confirming, and correcting these issues in the prior art.

### Developed an Effective PCB Cost Modeling Framework

We published the first framework for assessing cost of planar magnetic windings which can be incorporated into improved LCOE estimates which include PCB-based magnetic components. This also has utility in other cost-constrained applications.

### Developed an Automated Core Loss Tester for Accurate Loss Assessments

We developed an in-house core loss tester to experimentally validate transformer losses in this project. We automated this measurement to ensure repeatability, and are using this as a critical example of how data from "new testers" can be integrated into existing large-scale core loss datasets.

## 5. Path Forward

This project was a success in demonstrating dramatically simpler, lower cost, and higher performance planar transformers with medium-voltage isolation capability. However, two critical gaps were identified during this project through PI Ranjram's participation in the P3105 Working Group. These also represent gaps in prior art, and filling these gaps is a critical next step toward practical deployment of the developed technology.

First, this project, and prior art, do not address the impact of temperature on the isolation performance of the developed transformers, nor characterize their partial discharge (PD). PD is a measure of the degree of localized/internal discharge within an insulation material – this discharge typically occurs in the imperfections/voids of this material and will degrade its insulation capability over time. A PD measurement is an indicator of the long-term health of an isolation barrier and is considered by some

members of industry to be the most important metric for assessing the isolation performance of a transformer. In our initial conversations with PCB manufacturers, knowledge of PD capability is lacking, though several options have been provided that may have acceptable PD. A key benefit of our proposed technology is that is greatly widens the available isolation materials which can be considered, since it does not impose an extreme isolation requirement between each layer. It is also critical to understand what such an acceptable level is – i.e., what kind of insulation degradation results from long-term partial discharge? Because these transformers are distributed within many hot-swappable modules, extreme lifetimes are not necessarily required for a productive and functional system. A related research need is to develop a design procedure that does not require in-the-loop experimental characterization and instead leverages either the correct simulation tools for assessing dielectric breakdown or simple, experimentally verified design *principles* that can be applied ubiquitously to these designs.

It is also relevant that work to-date has focused exclusively on dc isolation capability. This is a reasonable starting point, as it simplifies testing during these early understanding phases and is representative of their ac isolation capability. However, in utility-scale solar PV applications, the voltage that must be isolated is an ac one, and future measurements should apply such voltages exactly. Temperature is a similarly important feature, especially under temperature cycling which can degrade the isolation barrier. While prior work includes discussions of the isolation impact of temperature cycling PCBs [21], more relevant data is needed for deployment in a PV system, which is distinct from the applications considered in this earlier work.

A second critical gap to fill is to demonstrate these miniaturized transformers within a converter module. All work to-date has been at the component level. Incorrect or inappropriate converter designs built around these transformers can compromise their isolation capability.

The team has strong interest in exploring these questions and we are actively seeking collaborators to participate in and support this work.

## 6. Products

Three peer-reviewed conference publications have been produced to-date:

1. E. Havugimana, S. Ahmed, and M. K. Ranjram, “Assessment of Cost Factors Impacting Planar Magnetic Windings,” in *2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2023, pp. 1–8. doi: 10.1109/COMPEL52896.2023.10221106.
2. Htat Min and M. K. Ranjram, “Improved High-Frequency, Medium-Voltage Isolation Planar Transformers,” in *2024 IEEE Energy Conversion Congress and Expo (ECCE)*, Oct. 2024, *accepted.*
3. E. Havugimana and M. K. Ranjram, “Automated Core Loss Tester Error Characterization for New Contributions to Large-Scale Datasets,” in *2024 IEEE Energy Conversion Congress and Expo (ECCE)*, Oct. 2024, *accepted.*

## 7. Project Team and Roles

The project team and roles are listed below.

| Name | Role | Contribution |
|---|---|---|
| Dr. Mike K. Ranjram | Principal Investigator | Led and directed the project. |
| Htat "Ted" Min | Doctoral Student | Simulated, fabricated, and tested all the planar transformer systems in the project. Oct. 2023-EOP. |
| Emmanuel Havugimana | Doctoral Student | Developed the planar transformer winding cost model. Developed the automated core loss testbed and collected and analyzed core loss data. Jan.2023-EOP. |
| Sakib Ahmed | Doctoral Student | Performed initial ANSYS Maxwell electrostatic simulations. Oct. 2022-May 2023. |

## 8. References

[1] "Solar Energy Technologies Office Fiscal Year 2021 Systems Integration and Hardware Incubator Funding Program," Energy.gov. Accessed: May 15, 2024. [Online]. Available: https://www.energy.gov/eere/solar/solar-energy-technologies-office-fiscal-year-2021-systems-integration-and-hardware

[2] "SG350HX of High Quality - Sungrow." Accessed: May 15, 2024. [Online]. Available: https://en.sungrowpower.com/productDetail/2305/string-inverter-sg350hx

[3] C. R. Sullivan, B. A. Reese, A. L. F. Stein, and P. A. Kyaw, "On size and magnetics: Why small efficient power inductors are rare," in *2016 International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, Raleigh, NC, USA: IEEE, Jun. 2016, pp. 1–23. doi: 10.1109/3DPEIM.2016.7570571.

[4] Z. Ouyang and M. A. E. Andersen, "Overview of Planar Magnetic Technology—Fundamental Properties," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014, doi: 10.1109/TPEL.2013.2283263.

[5] M. K. Ranjram and D. J. Perreault, "A 380-12 V, 1-kW, 1-MHz Converter Using a Miniaturized Split-Phase, Fractional-Turn Planar Transformer," *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1666–1681, Feb. 2022, doi: 10.1109/TPEL.2021.3103434.

[6] Z. Li, Y.-H. Hsieh, Q. Li, F. C. Lee, and M. H. Ahmed, "High-Frequency Transformer Design with High-Voltage Insulation for Modular Power Conversion from Medium-Voltage AC to 400-V DC," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2020, pp. 5053–5060. doi: 10.1109/ECCE44975.2020.9236384.

[7] S. Mukherjee *et al.*, "A High-Frequency Planar Transformer with Medium-Voltage Isolation," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix, AZ, USA: IEEE, Jun. 2021, pp. 2065–2070. doi: 10.1109/APEC42165.2021.9487061.

[8] J. G. Kassakian, D. J. Perreault, G. C. Verghese, and M. F. Schlecht, "Principles of Power Electronics," Higher Education from Cambridge University Press. Accessed: Jul. 19, 2023. [Online]. Available:

https://www.cambridge.org/highereducation/books/principles-of-power-electronics/D8B559E0FE5AC2949F5446C54C33BFF3
[9] E. Havugimana, S. Ahmed, and M. K. Ranjram, “Assessment of Cost Factors Impacting Planar Magnetic Windings,” in *2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2023, pp. 1–8. doi: 10.1109/COMPEL52896.2023.10221106.
[10] D. Fu, S. Wang, P. Kong, F. C. Lee, and D. Huang, “Novel Techniques to Suppress the Common-Mode EMI Noise Caused by Transformer Parasitic Capacitances in DC–DC Converters,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013, doi: 10.1109/TIE.2012.2224071.
[11] D. Huang, S. Ji, and F. C. Lee, “LLC Resonant Converter With Matrix Transformer,” *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4339–4347, Aug. 2014, doi: 10.1109/TPEL.2013.2292676.
[12] Z. Zhou, Y. Gao, X. Zhang, and H. Ma, “A Design Principle Ensuring Uniform Flux Density Distribution of the Two Middle Legs Planar Core for LLC Converter,” in *2022 IEEE 1st Industrial Electronics Society Annual On-Line Conference (ONCON)*, kharagpur, India: IEEE, Dec. 2022, pp. 1–5. doi: 10.1109/ONCON56984.2022.10126629.
[13] A. I. Maswood and L. K. Song, “Design aspects of planar and conventional SMPS transformer: a cost benefit analysis,” *IEEE Transactions on Industrial Electronics*, vol. 50, no. 3, pp. 571–577, Jun. 2003, doi: 10.1109/TIE.2003.812469.
[14] R. P. Hedden, *Cost engineering in printed circuit board manufacturing*. in Cost engineering, no. 11. New York: M. Dekker, 1987.
[15] H. Li *et al.*, “MagNet: An Open-Source Database for Data-Driven Magnetic Core Loss Modeling,” in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2022, pp. 588–595. doi: 10.1109/APEC43599.2022.9773372.
[16] “Advanced Power Electronics Design for Solar Applications (Power Electronics),” Energy.gov. Accessed: May 15, 2024. [Online]. Available: https://www.energy.gov/eere/solar/advanced-power-electronics-design-solar-applications-power-electronics
[17] G.-S. Seo *et al.*, “Levelized-Cost-of-Electricity-Driven Design Optimization for Medium-Voltage Transformerless Photovoltaic Converters,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 6973–6980. doi: 10.1109/ECCE.2019.8913063.
[18] P. L. Dowell, “Effects of eddy currents in transformer windings,” *Proc. Inst. Electr. Eng. UK*, vol. 113, no. 8, p. 1387, 1966, doi: 10.1049/piee.1966.0236.
[19] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters,” in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, Jun. 2002, pp. 36–41. doi: 10.1109/CIPE.2002.1196712.
[20] “Ferrites and accessories - SIFERRIT material N97”.
[21] R. Tarzwell and K. Bahl, “High Voltage Printed Circuit Design & Manufacturing Notebook”.