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GALLIUM NITRIDE JUNCTION FIELD EFFECT TRANSISTORS FOR HIGH-TEMPERATURE OPERATION

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Abstract

GaN is an attractive material for use in high-temperature or high-power electronic devices due to its high bandgap (3.39 eV), high breakdown field (~5×10^6 V/cm), high saturation drift velocity (2.7×10^7 cm/s), and chemical inertness (Morkoc 1994; Chow 1994). To this end, Metal Semiconductor FETs (MESFETs), High Electron Mobility Transistors (HEMTs), Heterostructure FETs (HFETs), and Metal Insulator Semiconductor FETs (MISFETs) have all been reported based on epitaxial AlN/GaN structures (Khan 1993a,b; Binari 1994 and 1995). GaN Junction Field Effect Transistors (JFETs), however, had not been reported until recently (Zolper 1996b). JFETs are attractive for high-temperature operation due to the inherently higher thermal stability of the p/n junction gate of a JFET as compared to the Schottky barrier gate of a MESFET or HFET. In this paper we present the first results for elevated temperature performance of a GaN JFET. Although the forward gate properties are well behaved at higher temperatures, the reverse characteristics show increased leakage at elevated temperature. However, the increased gate leakage alone does not explain the observed increased in drain current with temperature. Therefore, we believe this first device is limited by temperature activated substrate conduction.

INTRODUCTION:

As mentioned above, GaN based electronics are being developed for high-temperature operation. GaN MESFETs, HFETs, and MISFETs have all been reported, and recently GaN junction field effect transistors (JFETs) have also been demonstrated (Zolper 1996b). The advantages of a JFET structure, which have been clearly demonstrated for GaAs-based devices (Zolper 1994a,b), result from the higher gate turn-on voltage compared to a MESFET due its p/n junction gate. For high-temperature

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operation, a JFET will have less gate leakage current than a Schottky gate device due to the higher built-in voltage of the p/n junction. Furthermore, the gate of a JFET will be metallurgically more stable than a Schottky gate MESFET or HFET since gate rectification does not rely on a metal/semiconductor interface, as in a Schottky gate, but rather a buried p/n junction that will withstand higher temperature operation. In addition, since the channel of a JFET is effectively buried below the surface, this structure should be more environmentally robust (Zipperian 1986). For all the above reasons, a JFET should be able to operate at higher temperatures than a Schottky barrier device such as a MESFET or HFET.

As has been shown for GaAs-based JFETs (Zolper 1994a,b), ion implantation is an attractive technology for forming the selectively doped regions and for minimizing the JFET parasitic capacitance's. With the demonstration of n- and p-type ion implantation doping of GaN using Si and Mg (Pearton 1995) or Ca (Zolper 1996a) respectively, fabrication of an all ion implanted GaN JFET has now been reported (Zolper 1996b). After reviewing the fabrication of the GaN JFET and presenting its room temperature performance, we present the first elevated temperature results for this device.

JFET FABRICATION:

The GaN layers used in the experiments were 1.5 to 2.0 μm thick grown on c-plane sapphire substrates by metalorganic chemical vapor deposition (MOCVD) in a multiwafer rotating disk reactor at 1040 °C with a ~20 nm GaN buffer layer grown at 530 °C (Yuan 1995). The GaN layers were semi-insulating with background n-type carrier concentration $\leq 1x10^{16}$ cm^{-3}. The as-grown layers had featureless surfaces and were transparent with a strong bandedge luminescence at 3.484 eV at 14 K.

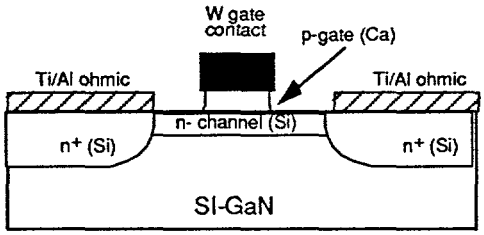

FIG 1. Schematic of ion implanted GaN JFET (Drawing not to scale).

Figure 1 shows a schematic of the ion implanted GaN JFET structure. The key processing steps are as follows: 1) selective area ion implantation of the n-channel (^{28}Si: 100 keV, $2x10^{14}$ cm^{-2}) and p-gate ^{40}Ca (40 keV, $5x10^{14}$ cm^{-2}), 2) sputter deposition of 300 nm of W gate contact metal, 3) RIE gate contact patterning using an SF_6/Ar plasma, 4) selective area, non-self-aligned ^{28}Si ion implantation of the source and drain regions, 5) a 1150 °C, 15 s rapid thermal anneal to activate the implanted dopants, 6) ECR-plasma etching of ~50 nm of p-GaN from the source and drain regions using a $BCl_3/H_2/Ar$ chemistry (Shul 1995) 7) deposition of Ti/Al (20 nm/ 200 nm) ohmic metal, and 8) 500 °C, 15 s ohmic alloy. This structure minimizes the gate capacitance often associated with JFETs by self-aligning the p-type gate to the gate contact metal. In addition, since the doping was done in selective areas, device isolation was realized via the semi-insulating properties of the GaN substrate. That is, no implant isolation or mesa etch isolation was required to isolate these devices.

An important feature of this device structure is that the W-gate contact is in-place during the high temperature implant activation anneal. This will allow for self-aligned source-and-drain implants as has been demonstrated in GaAs JFETs (Zolper 1994a,b). However, this approach also requires that the W not spike down through the p/n junction

during the anneal. Figure 2 shows Auger depth profiles for W on GaN either as deposited or after a 1100 °C, 15 s anneal. By comparing the two profiles, we estimate that after annealing the W has diffused into the GaN by only ~100 Å while Ga and N are diffusing out into the W over a distance of ~300 Å. Therefore, the Auger data demonstrates that the W/GaN interface is sufficiently stable during the implant activation anneal since the junction depth is expected to be near 450 Å and it is the indiffusion of W that could short the junction. This annealing data also demonstrates the extreme thermal stability of this gate structure for high temperature device operation.

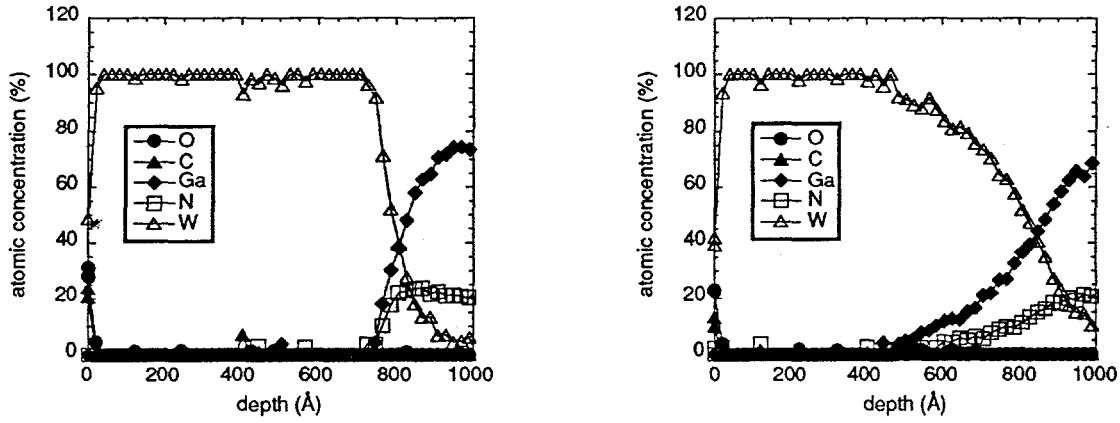

FIG 2. Auger depth profiled of W on GaN either a) as deposited or b) after a 15s, 1100 °C anneal. W indiffusion is estimated to be 100 Å after annealing.

DEVICE RESULTS

Figure 3 shows the room temperature I_{DS} versus V_{DS} curves for varied gate biases for a ~1.7 μm x 50 μm GaN JFET with a 4 μm source-to-drain spacing. The JFET demonstrates good modulation characteristics with nearly complete pinch-off at a threshold voltage of approximately -6 V for V_{DS} = ~7V. For V_{DS} = 25 V, a maximum transconductance of 7 mS/mm was measured at V_{GS} = -2.0 V with a saturation current of 33 mA/mm at V_{GS} = 0 V. The reverse breakdown voltage of the gate junction is estimated to be ~ 35 V. Four-probe measurements of the source resistance gave $R_S \approx 500$ Ω. Although this value of R_S is extremely large, it only accounts for a 20% reduction in the external transconductance with respect to a corrected internal transconductance of 8.5 mS/mm. This high resistance is attributed to the region between the ohmic contact and the channel since transmission line method (TLM) test structures using the same source and drain implants on GaN witness pieces gave a value of the specific contact resistance of ~1×10^{-5} Ω-cm^2 (Zolper 1995). This access resistance can be substantially reduced by optimizing the source and drain implant conditions and by self-aligning these implants to the gate contact metal. A second possible cause of the low transconductance is low electron mobility in the implanted channel region. If this is the case, optimization of the implant activation process should lead to improved mobilities. In addition, optimization of the epitaxial GaN layers for maximum electron mobility, as has been done for epitaxial FETs, should result in improved JFET performance. At room temperature this device demonstrated a unity gain cut-off frequency of 2.7 GHz and a maximum oscillation frequency of 9.4 GHz. These frequency metrics are comparable to similar dimension epitaxial GaN MESFETs (Binari 1995).

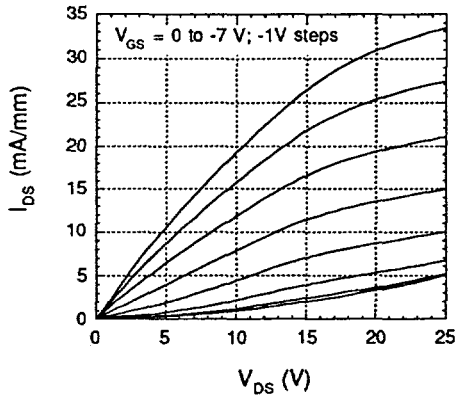

FIG 3. Room temperature I_{DS} versus V_{DS} curves for the first GaN JFET (V_{GS} starts at 0 V with -1 V steps). The JFET is 1.7 μm x 50 μm.

Figure 4 shows the forward and reverse gate diode characteristics of a ~1.7 μm x 50 μm GaN JFET between 25 and 175 °C. The diode demonstrates room a temperature (RT) gate turn-on voltage [V_{GS}(on)] of 1.84 V at 1 mA/mm of gate current. This voltage is roughly 55% of the bandgap of GaN (0.55E_g) which is slightly lower than that seen in GaAs JFETs where a gate turn-on voltage of 0.67E_g or ~0.95 V at 1 mA/mm of gate current has been reported (Sherwin 1995). This reduction in V_{GS}(on) can be explained if the W-gate contact is not completely ohmic and therefore causes band bending at the surface that will reduce the diode turn-on voltage as in a Shannon contact (Shannon 1972). This effect has been demonstrated in GaAs JFETs (Zolper 1994). This reduction in V_{GS}(on) can be overcome by increasing the p-type doping level or by employing an improved gate contact scheme to the p-region. At 175 °C the gate diode's forward turn-on voltage decreases to 0.9 V while still displaying very good rectification characteristics but with an increase in the reverse leakage current.

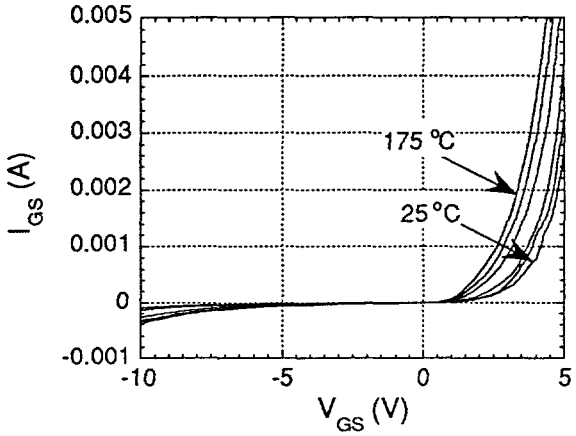

FIG 4. Temperature dependence of I_{GS} versus V_{GS} of a 1.7 μm x 50 μm GaN JFET. The temperature starts at 25 °C and steps by 25 °C to 175 °C.

Figure 5 shows I_{DS} versus V_{DS} curves for varying gate bias at temperatures of 25, 75 and 125 °C. The gate bias swing was limited to -5 to 0 V and the drain sweep was only taken to 15 V for these measurements to avoid catastrophic breakdown of the gate at

elevated temperature. As seen in fig 5, the source/drain pinch-off and breakdown characteristics quickly degrade with increasing temperature. For V_{GS} = -5 V and V_{DS} = 15V, I_{DS} increases from 1.3 mA at 25 °C, to 2.3 mA at 75 °C, and then dramatically to 6.7 mA at 125 °C where the start of enhanced breakdown is becoming evident. This phenomena may either be due to an increase in substrate conduction or defect assisted tunneling conduction of the gate diode in reverse bias. Reverse gate leakage alone does not explain the drain current seen in Fig 5c. From Fig 4 the gate current at -10 V and 125 °C is ~ 0.3 mA while the drain current in fig 5c at V_{GS} = -5 V and V_{DS} = 5 V(an effective gate bias of -10 V) is ~1 mA. Further work is needed to understand the mechanism, however, variable temperature Hall measurements on the starting GaN material shows temperature activated conduction with an estimated activation energy of 335 meV (Zolper 1996a). This may be due to compensating impurities in the MOCVD GaN. Therefore, although further study of the gate properties is needed, substrate conduction is certain to play a significant role in these first GaN JFETs at elevated temperature.

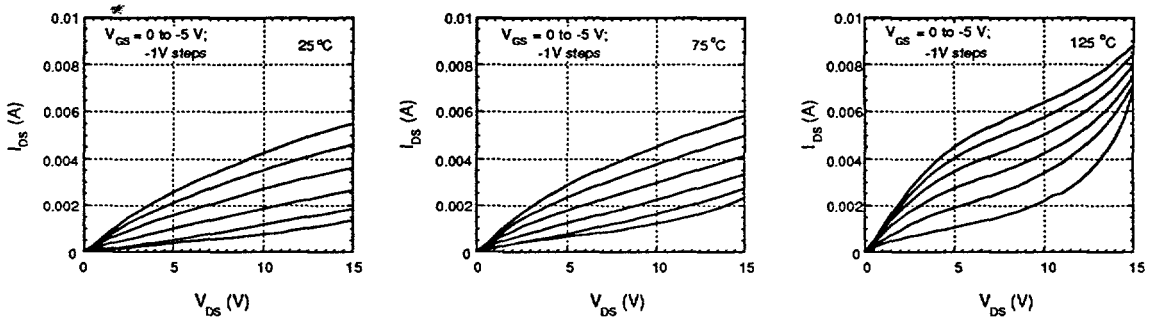

FIG 5. I_{DS} versus V_{DS} for 1.7 μm x 60 μm GaN JFET for V_{GS} starting at 0 V and stepping by -1V to -5V. The test temperatures are a) 25 °C, b) 75 °C, c) and 125 °C.

CONCLUSION

Selective area ion implantation doping has been used to fabricate the first GaN JFETs. P-type and n-type doping was achieved with Ca- and Si-implantation, respectively, followed by a 1150 °C rapid thermal anneal. A refractory W gate contact was employed that allows the p-gate region to be self-aligned to the gate contact. This contact was in-place during the 1150 °C implant activation anneal and will therefore be extremely stable for lower temperature (~600 °C) device operation. Although the gate diode demonstrated good forward rectification properties to 175 °C, the JFET's pinch-off characteristics are markedly degraded even at 125 °C. At this point we attribute the temperature degradation to increased conduction in the GaN buffer. Although these first GaN JFETs do not display good high-temperature operation, the basic device structure with a self-aligned W gate contact, coupled with the attractive material properties of GaN, should perform well at high temperature once improved GaN buffer layers are employed.

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