A Multi-functional Double Pulse Tester for Cascode GaN Devices

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***Abstract*—Gallium Nitride (GaN) power devices with low switching and conduction losses can lead to superior power density in numerous power conversion applications. Their fast switching speeds, however, pose challenges in dynamic device characterization. The large parasitic inductances and contact impedances in conventional double pulse testers (DPTs) meant for Si devices, make them unsuitable for GaN characterization. GaN devices are directly soldered on to testers for minimizing parasitic effects. Furthermore, currently different testers are used for different types of device characterization, requiring the device under test (DUT) to be repeatedly soldered to different boards. This paper proposes a multi-functional tester well-suited for GaN devices and capable of completing all the dynamic characterization on the same board. The proposed tester is able to characterize: device turn on and off transition under hard and soft switching, dynamic Rdson, diode reverse recovery and device reverse conduction voltage drop. The proposed tester has been implemented in hardware and the functions are validated with tests on a cascode GaN device. Some special properties of the cascode GaN device seen from these tests are highlighted. Detailed design procedures for selecting the critical components of the double pulse tester are presented.**

***Index Terms*—Gallium Nitride, power device, WBG, cascode device, double pulse tester, dynamic Rdson, reverse recovery**

I. Introduction

FOR conventional silicon (Si) device dynamic characterization, the double pulse tester (DPT) shown in Fig. 1 is used. The tester characterizes the device inductive load switching loss, voltage and current slew rates, and the switching times. The device being tested then needs to be ported to a different tester setup in order to extract the body diode parameters such as reverse recovery time and charge. Beyond these dynamic parameters, Gallium Nitride (GaN) devices also have the issue of dynamic Rdson (dRdson) which relates to larger resistance at the turrn on instant progressively reducing with time till it reaches the steady-state Rdson value. This effect is due to AlGaN electron trapping [1] [2] [3]. The higher the blocking voltage, and the longer the blocking time, deeper are the electrons trapped in AlGaN layer [2]. After the device is turned on, the trapped electrons are released in finite time with fast and slow release effects [3]. For power electronics applications, this phenomenon is seen as the device on resistance being higher than its steady state value measured in curve tracer. As the switching frequency increases, the effect of dRdson on conduction loss will be larger. Hence, for accurate evaluation of a GaN device for high frequency applications, precise measurement of dRdson is needed, and a tester is expected to support this measurement. The sequence for measuring the dRdson by pulsed drain source voltage is the similar to DPT. References [4] [5] and [6] have reviewed five different schemes for measuring dRdson.

GaN switches have low input capacitance and low turn off switching loss [7]. The inherent low turn off loss makes the device suitable for zero voltage transition (ZVT) circuits. For Si devices, usually an output capacitor is added to achieve very low turn off losses while the ZVT circuit ensures zero turn on losses. The added output capacitor increases the resonant current used for achieving ZVS turn on, thereby increasing the conduction loss in the circuit. As soft switching with very high switching frequencies is a good application for GaN devices, a circuit for evaluating dynamic dRdson at soft switching conditions is needed. One such circuit has been proposed in [8]. However, this scheme only evaluates the full resonant switching scheme. With full resonant scheme, the voltage applied to the device before turn on is a sinusoidal waveform. Different to that, this paper proposes a circuit for measuring dRdson with ZVT scheme. In the ZVT circuit here, the voltage applied to the device is close to a square waveform. Therefore, in the new tester, the off state voltage and the voltage stress time are more precisely controlled for dRdson test.

The diode D_T or a top side switch shown in Fig. 1 does not experience switching loss. All the energy stored in the output capacitor or junction capacitor during diode turn off is released during diode turn on. However, this is not always true for switching pole formed by cascode devices. In a cascode device, there is a phenomenon called capacitance mismatch [9]. It leads to switching loss during soft turn on. Therefore, a diode turn on and off characterization is needed to capture the switching loss in half bridge configuration applications.

With the dRdson under hard and soft switching, and mismatch scenarios considered, a new DPT setup is proposed. The new tester circuit can evaluate GaN device hard switching loss, soft switching loss, forward conduction loss and reverse conduction loss with dRdson measurement. The operating

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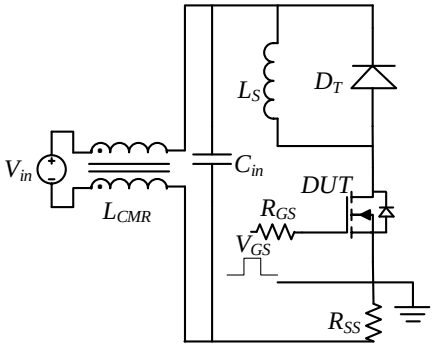


Fig. 1. Conventional double pulse tester

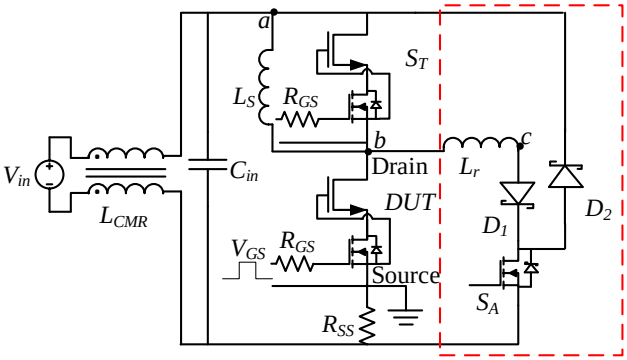


Fig. 2. ZVT double pulse tester circuit

principle of the proposed tester is explained in Section II. And the design concerns and design methods are described in Sections III and IV. The test results with a cascode GaN device are shown and analyzed in Section V, with the conclusions presented in Section VI.

II. Circuit Operation Principles

A. Active switching characterization

The proposed circuit for dynamic characterization builds on the DPT which has been studied in detail in [10] [11] [12] [13] [14] and [15]. Reference [16] shows a DPT with auxiliary circuit for ZVT, similar to the one shown in Fig. 2. Different to the circuit in [16], the top switch is connected to a gate drive with isolated gate signal. The other different feature of the circuit, shown in Fig. 3, is the dRdson voltage clamping circuit proposed in [4]. This circuit uses diodes clamping the voltage between T_1 and T_2 to less than 10 V. The voltage difference between the two nodes can be measured with a low voltage differential probe. When the DUT is on, the probe is connected to the drain source of the DUT by the current mirror circuit. This method has two advantages: fast response after the DUT turn on and low voltage spikes at DUT turn off. Also with current mirror, the effect of clamping diode voltage drop can be minimized. By combining the two elements with modifications, the proposed tester is able to do much more than each of them individually. Especially, the DUT dRdson at soft switching, diode dynamic and forward voltage drop can be measured with the same setup.

For characterizing DUT under hard switching, the main circuit operation is identical to that of the conventional DPT

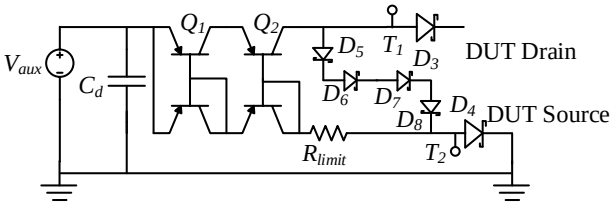


Fig. 3. Current mirror circuit for dRdson measurement

with the top switch S_T kept off. The conventional DPT operation is well documented in [10] and not repeated here. The clamping circuit operation is explained in [5]. Only the case of ZVT characterization is explained here. Before the DUT turn on, the voltage clamping circuit diode D_3 is off blocking the dc link voltage V_{in}. The current mirror forces current through D_5 to D_8 and D_4. T_2 is at the potential lifted by D_4 forward voltage drop. The voltage between node T_1 and T_2 is clamped to the sum of the forward voltage drops of D_5 to D_8. Before the DUT turn-on for measurement, the auxiliary switch S_A turns on. Once S_A turns on, current through L_r is increased by V_{in}. As L_r is much smaller than L_S, the current through L_r rises to that through L_S within a short time. When current through L_r is equal to the current through L_S, the top device S_T turns off. Then L_r resonates with the output capacitance of S_T and DUT. When DUT voltage resonates to zero, its gate voltage V_{GS} goes high and achieves ZVS turn on. For the voltage clamping circuit in Fig. 3, when the DUT drain source voltage resonates below the clamped voltage, D_3 turns on. The current through clamping diodes D_5 to D_8 is commutated to D_3, and D_5 to D_8 turn off. The current mirror works as a constant current source forcing current through D_3. Also, it guarantees the current through D_3 and D_4 are the same. The low voltage probe is connected to the drain source of DUT through D_3 and D_4, and the voltage drop across the device during device on time can be measured accurately. With the shunt resistor in series with DUT, the current through the device channel can be measured also, from which the channel resistor can be derived. After DUT is on, the auxiliary switch S_A needs to be turned off. The resonant inductor L_r is connected to $-V_{in}$ through D_1 and D_2. And the current through L_r is decreased fast. When current through L_r goes to zero, diodes D_1 and D_2 turn off.

B. Passive switching characterization

For the body diode characterization, conventional double pulse tester approach will need to move DUT to another test setup [17]. An advantage of the proposed tester is that it can complete the diode characterization in the same setup with L_S replacing L_r connected between nodes b and c shown in Fig. 2. These inductors are not in the high frequency loop. Therefore screw terminals or relays can be used for connection. And the interchange of the inductors can be done easily without soldering. The circuit operating principles are illustrated in Fig. 4 and the ideal waveforms are shown in Fig. 5. In Fig. 5, from top to bottom, gate source voltage of auxiliary switch S_A, top switch S_T, and DUT are plotted followed by load inductor current and voltage I_L_S, V_L_S, auxiliary switch drain source current and voltage $I_{DS}\_S_A$, $V_{DS}\_S_A$, top switch

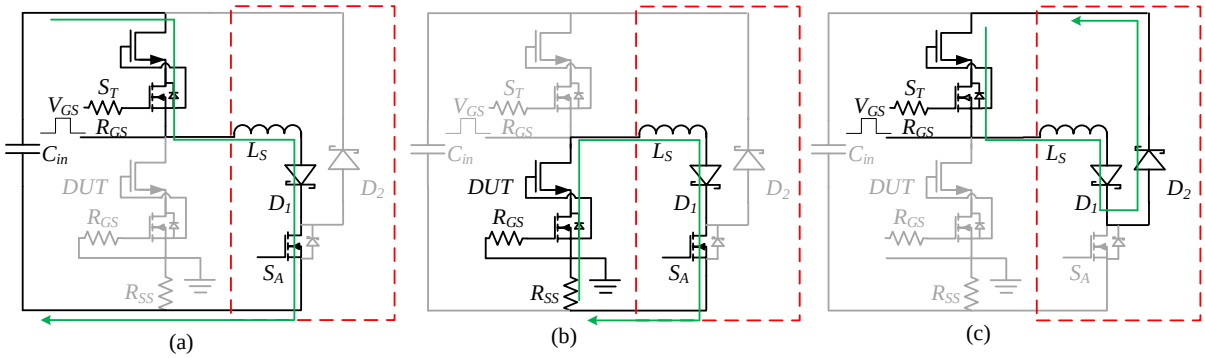


Fig. 4. Testing scheme for diode characterization

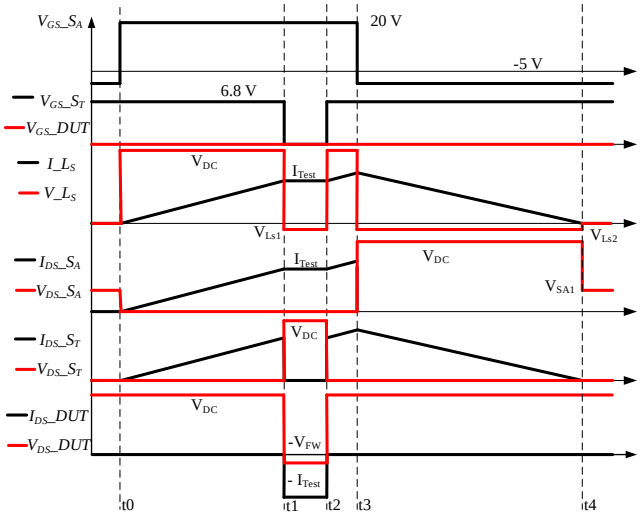


Fig. 5. Ideal waveform of passive switching characterization

drain source current and voltage $I_{DS}\_S_T$, $V_{DS}\_S_T$, and DUT drain source current and voltage I_{DS}_DUT, V_{DS}_DUT. From t0 to t1, the circuit is as shown in Fig. 4a, the top switch S_T is kept on and the auxiliary switch S_A is turned on. The current increases in the inductor L_S linearly to the desired testing current I_{Test}. Then from t1 to t2, top switch S_T is turned off. The current in the load inductor forces DUT to be turned on in the reverse direction. At this turn on transition, the amount of energy released from the output capacitor is measured as E_{Don}. Then the current mirror clamping circuit D_3 is turned on to measure DUT reverse voltage drop. After the transition, the circuit is shown in Fig. 4b. A small negative voltage V_{Ls1}, majorly contributed by DUT reverse voltage drop V_{FW} and $D1$ forward voltage drop, is applied to the load inductor decreasing the current through it. Since V_{Ls1} is much smaller than V_{DC} and the time duration is short, the current through the DUT can be considered constant. And the DUT reverse voltage drop V_{FW} can be accurately measured for a certain current I_{Test}. After the data is captured, the top switch S_T is turned on again at time t2. The current in the DUT is forced to commutate out of the DUT. The DUT drain source voltage starts rising and the voltage clamping circuit blocking diode D_3 is turned off. The reverse recovery time and charge can be measured as E_{Doff}. After the transition, the circuit state goes back to the one shown in Fig. 4a with the waveform shown in t2 to t3. Then the auxiliary switch S_A is turned off pushing the current through diode D_2. And the current circulates in the path highlighted till the current dies down in Fig. 4c. The energy left in the load inductor is dissipated in the top device S_T, D_1 and D_2. The waveform is plotted in Fig. 5 t3 to t4. This interval is much longer than that of t0 to t3. Then the circuit waits for the next cycle of test.

For a conventional diode, when the junction capacitor has not been fully discharged, there will be no current through the P-N junction. Therefore, the released energy E_{Don} should be the same as the stored energy E_{Doff}. But ,in a cascode device, if the Si MOSFET output capacitor voltage is discharged to the threshold voltage of the GaN device before its output capacitor is fully discharged, then part of the stored energy will be dissipated in the GaN device channel [9]. In this case E_{Don} will be less than E_{Doff}. And the difference will be the switching loss during device passive turn on.

III. Key Components Selection

A. Resonant inductor

Compared to conventional DPT, the ZVT DPT has the issue of diode current clamping ringing. This phenomenon is observed when the current through resonant inductor L_r goes to zero. At this moment, D_1 and D_2 are turned off. It becomes a voltage excited LC resonant circuit through the path of DUT channel, L_r, and D_1 and D_2 junction capacitors. The resonant current can be described by (1). In (1), i_{Lr} is the current through the resonant inductor after D_1 and D_2 turn off, Z_r is the resonant impedance shown in (2), ω_r is the resonant frequency, I_{rr} is the reverse recovery current of D_1 and D_2. In (2), C_{jD} is the diode junction capacitance. In order to limit the current ringing in the DUT channel, the resonant impedance Z_r needs to be high and diode reverse recovery current I_{rr} needs to be small. This suggests that D_1 and D_2 need to be Schottky diodes, and their junction capacitance C_{jD} should be small. L_r needs to be maximized. However for fast measurement of dRdson, the smaller the resonant inductor L_r the shorter is the blank time of measurement after the device is turned on. The maximum inductance value L_{rmax} is governed by blank time as shown in (3), where V_{DCmin} is the minimum dc link voltage, I_{Lmax} is the maximum load current, and T_{bmax} is the allowed maximum blank time before reaching the nominal load current.

$$i_{Lr} = \frac{V_{in}}{Z_r}\sin(\omega_r t) - I_{rr}\cos(\omega_r t) \tag{1}$$

where,

$$\begin{cases} Z_r = \sqrt{\frac{2L_r}{C_{jD}}} \\ \omega_r = \sqrt{\frac{2}{L_r C_{jD}}} \end{cases} \tag{2}$$

$$L_{rmax} = \frac{V_{DCmin} T_{bmax}}{I_{Lmax}} \tag{3}$$

On the other hand, the resonant inductor current needs to be controlled. If the auxiliary switch S_A is turned on so late that the current through the resonant inductor L_r cannot reach the current in the main inductor L_S, ZVT cannot be achieved. If S_A is kept on for too long, the dRdson measurement will be delayed. The larger the resonant inductance, the more accurate S_A on time will be. For reliability consideration, a SiC MOSFET is used as auxiliary switch. Considering typical $30\,\mathrm{ns}$ turn-on time of SiC devices, there is a limitation in the minimum inductance value L_{rmin} as shown in (4). V_{DCmax} is the maximum dc link voltage being tested, T_{onmin} is the minimum on time the auxiliary switch can have and I_{Lmin} is the minimum load inductor current being tested.

$$L_{rmin} = \frac{V_{DCmax} T_{onmin}}{I_{Lmin}} \tag{4}$$

Assuming a single resonant inductor, (3) and (4) can be used to derive a relationship between the maximum blank time T_{bmax} and the minimum on time T_{onmin} shown in (5). For conducting the tests from $5\,\mathrm{A}$ to $25\,\mathrm{A}$ and $50\,\mathrm{V}$ to $400\,\mathrm{V}$, T_{bmax} will be 40 times T_{onmin}. For a blank time of $500\,\mathrm{ns}$, the allowed on time should be $12.5\,\mathrm{ns}$. However, the typical turn on time of a SiC switch will take $30\,\mathrm{ns}$, making the time control challenging. Therefore, a single inductor cannot support the whole range of tests. The solution is to use two inductors: one inductor for testing from $50\,\mathrm{V}$ to $100\,\mathrm{V}$ and the other from $200\,\mathrm{V}$ to $400\,\mathrm{V}$. Therefore, the minimum allowed on time is $50\,\mathrm{ns}$. And the desired inductance of resonant inductors are $1\,\mu\mathrm{H}$ and $4\,\mu\mathrm{H}$.

$$T_{onmin} = \frac{V_{DCmin} I_{Lmin}}{V_{DCmax} I_{Lmax}} T_{bmax} \tag{5}$$

For the prototype, two resonant inductors are wired to have indutance of $1.1\,\mu\mathrm{H}$ and $3.2\,\mu\mathrm{H}$ using air core. With *C4D20120A* SiC diodes used for D_1 and D_2, the maximum resonant current peak to peak value is calculated to be $2.13\,\mathrm{A}$ for $100\,\mathrm{V}$ and $3.46\,\mathrm{A}$ for $400\,\mathrm{V}$ by (1).

B. Clamping diodes

The other important component selection is the voltage clamping diodes D_3 to D_8. The transitions during DUT turn-on and turn-off are shown in Fig. 6a and 6b. At DUT turn-on, the junction capacitors of D_5 to D_8 are charged in series while that of D_3 discharged. At the beginning of DUT drain source voltage decreasing, the junction capacitor of D_3 is discharged in parallel with DUT output capacitor. If the induced current in D_3 junction capacitor due to voltage slew rate is higher than the current mirror current, diode chain $D_5 - D_8$ are turned off.

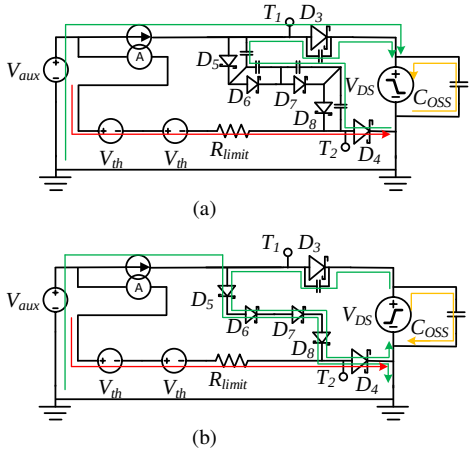


Fig. 6. Transition of the voltage clamping circuit

At this point the diode junction capacitor chain has equivalent capacitance lower than any individual one in series. And the induced current is reduced. If the induced current through the junction capacitor chain goes higher than the current mirror current, then D_4 turns off. To avoid the turn-off of D_4, the diodes $D_5 - D_8$ and D_3 need to have low capacitance so that the current reduction in D_4 during DUT turn on is minimized. And the minimum current from current mirror needs to be set higher than the peak current during transition. The auxiliary supply voltage V_{aux} and current setting resistor R_{limit} has to be selected accordingly. At DUT turn off, the D_3 junction capacitor is charged in parallel with the DUT output capacitor. D_4 to D_8 conduct the charging current in the forward direction. For accurate measurement of switching loss, D_3 needs to have low junction capacitance, as it will increase the amount of stored energy during device turn off (the stored energy is dissipated during device active turn on). Considering that the voltage of the tester can potentially reach $650\,\mathrm{V}$, a $1\,\mathrm{kV}$ rated diode *MUR1100E* is used. Its junction capacitance decreases from around $15\,\mathrm{pF}$ at $0\,\mathrm{V}$ to $2.5\,\mathrm{pF}$ at $50\,\mathrm{V}$. D_3 and D_4 have to be identical as described in [5], for minimizing the measurement error. For increasing the voltage measurement range of the clamping circuit, D_5 to D_8 are preferred to have high forward voltage drop. When the DUT is on, the DUT drain source voltage has to be lower than the serial forward voltage drop of D_5 to D_8. Otherwise, the mirrored current will go through the path of D_5-D_8 and will hold the measured voltage to the clamped voltage. For the prototype, four *1SS355* Schottky diodes are used to obtain a clamping voltage of $2.8\,\mathrm{V}$.

IV. Double Pulse Tester Board Layout

GaN device performance is sensitive to the parasitic inductance and capacitance in the layout of printed circuit board (PCB). The first layout issue is the length of gate drive loop. In order to test the device at the highest switching speed, the parasitic inductance in the gate loop has to be minimized. Otherwise, the gate voltage ringing will be so large that DUT can be mis-triggered to turn on or off. The second issue is the power high frequency loop area. The larger the power

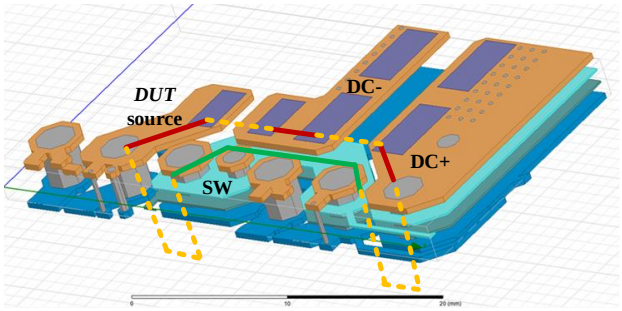


Fig. 7. High frequency loop used for Q3D FEA

high frequency loop the larger is the parasitic inductance [18]. The inductance in the high frequency power loop will induce overshoot on device voltage. The switching node area is also important in layout. If it is close to other nets, the fast potential change in the switching node induces current in other nets through parasitic capacitance. In particular, when the switching node overlaps with positive or negative bus rail, the resulting parasitic capacitance adds to the output capacitance of the devices, impacting the switching characteristics and significantly increasing the switching loss. In this work, the PCB layout is optimized using a finite element analysis (FEA) tool. The *ANSYS Q3D* package is used to extract the loop inductances and parasitic capacitances in the PCB layout. The FEA model used is shown in Fig. 7, where the red line shows the current path in the top layer and the green line shows the current path in the second layer. The yellow dashed line which represents device package inductance is not considered in the analysis. The parasitic inductance of the shunt resistor and the decoupling ceramic capacitor are also not included in the analysis. The analyzed high frequency loop inductance is $2.88\,\mathrm{nH}$. The capacitance of the switching node to negative and positive dc buses are $5.5\,\mathrm{pF}$ and $1.17\,\mathrm{pF}$ respectively.

Another concern is the parasitic capacitance of the load inductor. The change in switching node voltage excites the resonant tank formed by the parasitic capacitance between windings of the load inductor, and the parasitic inductance of the high frequency loop. Therefore, single layer inductor is wired. The last but not the least concern is the common mode current. When the DUT switches, the floating power supply will inject common mode current into the DPT board. This current will affect the drain source current measurement [19]. Therefore, a large common mode choke is wired and inserted between the power supply and the DPT board.

V. Test Results and Analysis

The hardware prototype of the proposed multifunctional DPT is shown in Fig. 8. The components used in this prototype are listed in Table I. The DUT current is measured by a $0.1004\,\Omega$ non-inductive shunt resistor R_{SS}.

A. DUT active switching characterization

The DUT is a 650 V 30 A rated cascode GaN device. The active hard switching turn-on and turn-off transient waveforms of DUT at 400 V and 25 A are shown in Fig. 9a and 9b respectively. The blue trace is the drain source voltage of the

TABLE I
Major Components in the Prototype

Component	Value	Component	Value
L_S	$1.2\,\mathrm{mH}$	D_1,D_2	C4D20120A
L_r	$1.1\,\mu\mathrm{H}$, $3.2\,\mu\mathrm{H}$	S_A	CMF20120D
C_{in}	$40\,\mu\mathrm{F}$	D_3, D_4	MUR1100E
R_{SS}	SDN-414-10	D_5,D_6,D_7,D_8	1SS355
R_{limit}	$100\,\Omega$	Q_1,Q_2	BCV62

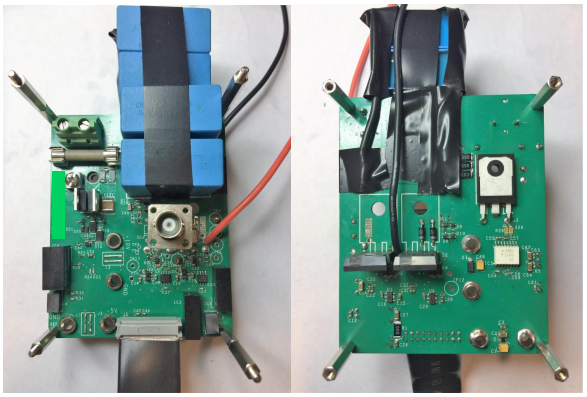
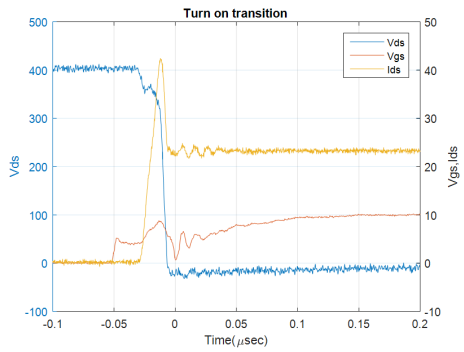


Fig. 8. Hardware setup of the proposed multifunctional DPT

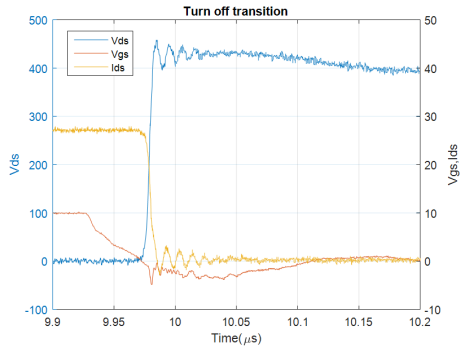
DUT, the red trace is the gate source voltage of the DUT and the yellow trace is the drain source current of the DUT. As seen in Fig. 9a, when the DUT turns on there is a large current through the device. It is caused by the top device output capacitor charging, with small reverse recovery. The larger the output capacitor of S_T, the higher is the current peak. Also, the higher the voltage slew rate at the switching node, the larger is the charging current peak. For a fair comparison, the top switch S_T is suggested to be the same as the DUT [16].

Adding a temperature controlled hotplate to this setup, allows the device characterization conducted at different controlled temperatures. Fig. 10 shows the switching loss at different currents and different temperatures where, the blue solid, yellow dotted and green dashed traces correspond to the turn on losses at $25\,^{\circ}\mathrm{C}$ $75\,^{\circ}\mathrm{C}$ and $125\,^{\circ}\mathrm{C}$ respectively, and the red solid, purple dotted and cyan dashed curves correspond to the respective turn off loss of the device. At $25\,^{\circ}\mathrm{C}$, the device turn on loss increases with the load current from $53\,\mu\mathrm{J}$ to $153\,\mu\mathrm{J}$ as the load current is increased from $5\,\mathrm{A}$ to $25\,\mathrm{A}$. At $125\,^{\circ}\mathrm{C}$ the corresponding switching loss varies from $55\,\mu\mathrm{J}$ to $165.8\,\mu\mathrm{J}$. However, the turn off loss remains almost constant and low at about $25\,\mu\mathrm{J}$. From the results, the maximum turn-on loss variation with temperature is $12.8\,\mu\mathrm{J}$ at $25\,\mathrm{A}$.

In Fig. 9a, at the beginning of the transition, there is an obvious dip on the DUT drain source voltage. In [15], voltage dip and the derivative of drain source current is used for deskewing the voltage probes. In [7], the drain source voltage dip at the beginning of the turn on transition has been



(a)



(b)

Fig. 9. Experimental hard switching waveforms at 400 V and 25 A

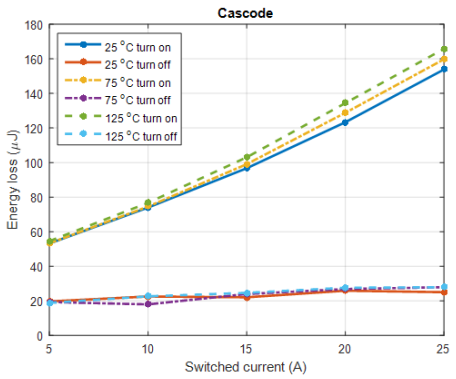


Fig. 10. 400 V switching loss with different current at different temperature

shown caused by the loop leakage inductance. Therefore, the high frequency loop inductance can be estimated by fitting the voltage dip with the derivative of the measured drain source current. The result from 400 V and 25 A turn on transition is shown in Fig. 11. The red trace is the derivative of the measured drain source current times the loop leakage inductance and offset by the dc link voltage, and the blue trace is the measured DUT drain source voltage. A good matching is seen between the two which validates that the probes have been aligned. It also estimates the leakage inductance to be about 18 nH, which is different from the FEA result, due to the unaccounted parasitic inductance in the device package, shunt resistor and decoupling capacitor. Later in section V-C, the device package inductance is further discussed.

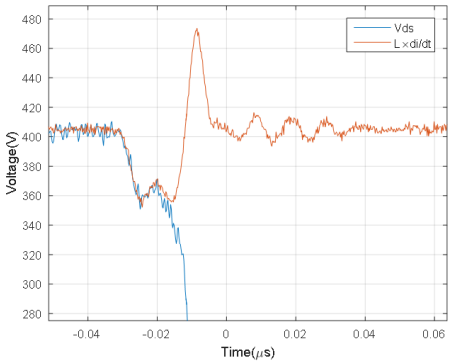


Fig. 11. Deriving the high frequency loop inductance from measured DUT voltage dip at turn-on

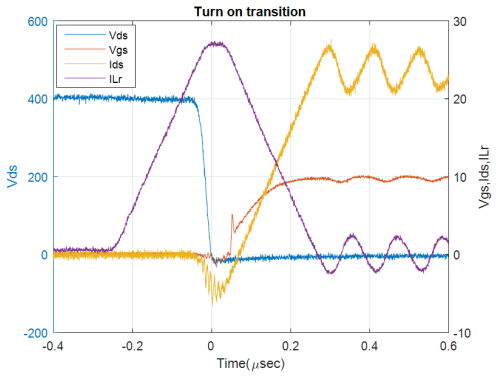


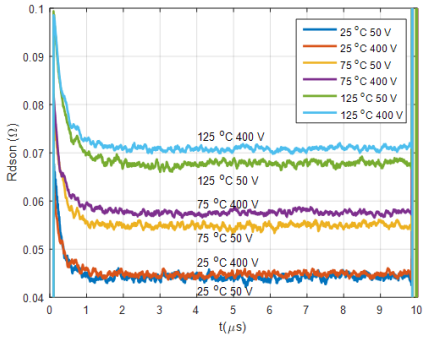
Fig. 12. Turn on transition under ZVS conditions at 400 V and 25 A

B. Turn on transition under zero voltage switching

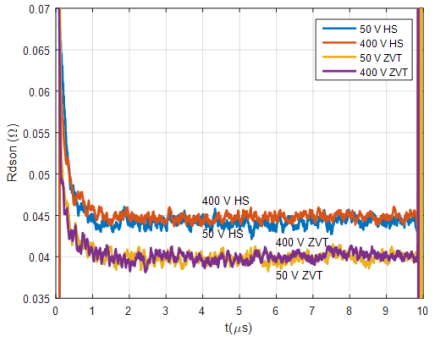
The ZVT case of 400 V and 25 A soft turn on is shown in Fig. 12, where the blue trace is the drain source voltage, the red trace is the gate source voltage, the yellow trace is the drain source current and the purple trace is the curren through the resonant inductor. Compared to Fig. 9a, the gate does not experience the Miller effect. Therefore, the ZVT also reduces the gate drive loss. In Fig. 12, as expected from previous analysis, after the resonant inductor current reaches zero a resonance starts.

C. Dynamic Rdson

The dRdson is also measured at both hard switching and soft switching conditions. The results are shown in Fig. 13a and 13b respectively. Fig. 13a shows the measured Rdson versus time after 50 V and 400 V stress under different temperature. Fig. 13b shows the measured Rdson versus time after 50 V and 400 V stress at hard switching and at ZVT. In Fig. 13a at 25 °C the fast electron release completes in less than 1 µs after device turn on. And its Rdson does not change with stress voltage. However, at higher temperature the dRdson slow release of trapped electrons effect is seen [3] [20]. In Fig. 13b, a lower dRdson is observed at ZVT condition. For a 25 A current conduction, a ZVT device can save about 3 W in conduction loss. This is a unique phenomenon in cascode devices. Before the device turn on, the channel current in cascode device goes from source to drain as shown in Fig. 14. Even though the Si device is not on, its body diode conducts current with the GaN



(a) dRdson under hard switching at different temperatures



(b) dRdson under hard and soft switching at 25 °C

Fig. 13. Measured dynamic Rdson

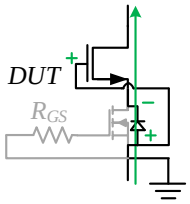


Fig. 14. Cascode device before zero voltage turn on

HEMT channel. The forward voltage drop of the Si device body diode actually applies a small positive voltage on the GaN device gate and source. For a normally on GaN HEMT the positive gate voltage increases its detrapping speed further. Therefore, a lower RDSon is expected.

In Fig. 12, ringing in the drain source voltage corresponding to the ringing in current is not seen due to its low resolution. But when measured with the clamping circuit, the ringing exists as shown in Fig. 15. The top plot shows the drain source voltage measured by the clamping circuit. The bottom plot shows the manipulated drain source voltage without the ripple. The bottom plot is V_{ds}^{*} formed by using the formula in (6) where, V_{ds} is the drain source voltage measured by the clamping circuit, i_{ds} is the drain source current through the DUT, and L_{pkp} is the device package parasitic inductance. With the ripple canceled out, the package inductance is estimated to be about $6\,\mathrm{nH}$. Therefore, as the top switch has the same package, the devices themselves contribute about $12\,\mathrm{nH}$ into the loop inductance. With the measured loop inductance being $18\,\mathrm{nH}$, device packages contribute $12\,\mathrm{nH}$, and PCB parasitic

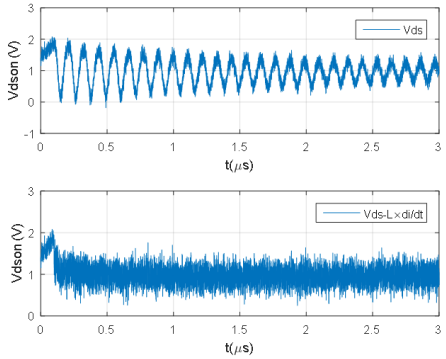


Fig. 15. Extracting device package inductance by eliminating DUT drain source voltage ringing in ZVT test

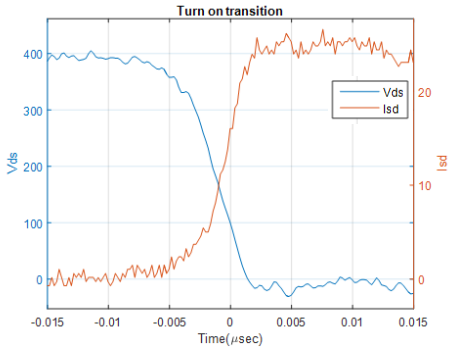
inductance being $2.88\,\mathrm{nH}$, the shunt resistor and decoupling capacitor contributes $3.12\,\mathrm{nH}$ in total.

$$V_{ds}^{*} = V_{ds} - L_{pkp}\frac{di_{ds}}{dt} \tag{6}$$

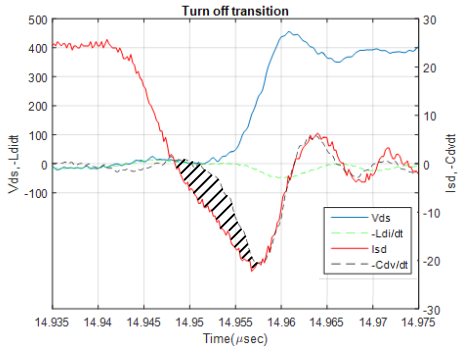
D. Passive switching characterization

As mentioned before, the body diode characterization can be conducted with the same circuit board. The reverse conduction turn-on and turn-off transitions of the DUT are shown in Fig. 16a and 16b for the $400\,\mathrm{V}$ $25\,\mathrm{A}$ case. In Fig. 16a the blue trace shows the drain source voltage and the red trace shows the source to drain current. The energy corresponding to the overlap between the current and voltage is calculated to be $6.4\,\mu\mathrm{J}$. In Fig. 16b, in addition to the drain source voltage and source to drain current, there are two other dashed lines. The black dashed line which matches with the source drain current after the current peak is the voltage derivative times the output capacitance. The green dashed line which matches with the drain source voltage before $14.95\,\mu\mathrm{s}$ is the source drain current derivative times the package parasitic inductance value. The shaded area shows the charge difference between the measured source drain charge and the calculated charge stored in output capacitor. With the current slew rate being $2.6\,\mathrm{A/ns}$, the actual reverse recovery charge due to the Si MOSFET body diode is $49\,\mathrm{nC}$. The energy absorbed by the device during this turn off is $19.5\,\mu\mathrm{J}$. Therefore, comparing the turn on released energy and turn off absorbed energy, the total loss is $13.1\,\mu\mathrm{J}$. This is the energy loss due to capacitance mismatch [9].

Also, the reverse voltage drop can be measured accurately when the device is conducting the reverse direction current. This feature is unique for this tester due to the clamping circuit. The results for $400\,\mathrm{V}$ test with different reverse currents are plotted in Fig. 17 with blue star markers. It should be noted that the reverse voltage drop increases almost linearly with the reverse current. Different from a discrete MOSFET device, the reverse current here goes through the low voltage Si MOSFET diode in series with the GaN channel as shown in Fig. 14. The reverse voltage drop can be modeled as a resistor in series with a current dependent voltage source. As the dRdson under ZVT has been measured in previous section V-C, the pure Si



(a) DUT reverse conduction turn on



(b) DUT reverse conduction turn off

Fig. 16. 400 V 25 A passive switching waveform

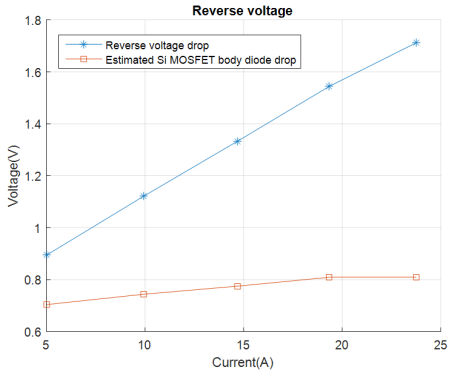


Fig. 17. Measured reverse voltage drop with reverse current

body diode voltage drop can be extracted. By subtracting the resistive voltage drop in GaN channel, the reverse voltage on the Si MOSFET can be estimated as shown by the red trace with square markers in Fig. 17. It varies from 0.7 V to 0.8 V. At high current, the major part of the forward conduction loss is still due to the GaN channel resistor. Therefore, the ZVT dRdson result from the previous section can be used for reverse voltage drop estimation. With dRdson, a dynamic reverse voltage drop also exists.

VI. Conclusion

The parasitic parameters of a conventional DPT make it less accurate in dynamic characterization of GaN devices that have very high switching speeds. For reducing the parasitic effects, soldering the DUT on to tester board with closely placed components is typically the way for improving accuracy. However, when both double pulse test and diode reverse recovery characterization need to be done, moving DUT from one setup to another makes the characterization less reliable. Also, GaN device electron trapping effect cannot be evaluated by conventional DPT. All of those challenges are overcome by the proposed tester setup. It completes the double pulse test and reverse recovery test on the same board. Furthermore, it can measure device dRdson at both hard switching and soft switching conditions.

The tester prototype has been built with careful design of board layout and component selection. Actual high frequency loop and device package parasitic inductors are extracted from the test results. With the help of FEA tool, major contributors to the parasitic inductances can be identified and quantified.

With a cascode GaN device as the DUT, some special properties can be identified with the new tester. These include: lower dRdson after ZVS compared to hard switching, ZVS turn on loss (device capacitance mismatch), and dynamic reverse voltage drop. The proposed tester can also be used for enhance mode (E-mode) GaN device characterization. Different to cascode device, E-mode GaN device does not have the issue of ZVS turn on loss and typically possesses higher reverse voltage drop.

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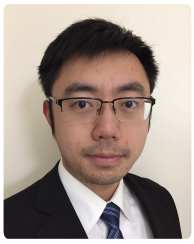

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