Low-Loss Integrated Inductor and Transformer Structure and Application in Regulated LLC Converter for 48-V Bus Converter

Mohamed H. Ahmed, Ahmed Nabih, Fred C. Lee, and Qiang Li

***Abstract*— In this article, an LLC converter using gallium nitride (GaN) transistors is proposed for a 48-V regulated and isolated bus converter. Compared with pulsewidth modulation (PWM)-based topologies, the soft switching capability of an LLC allows operation at very high frequencies. In addition, the size of the magnetic components is reduced without sacrificing the efficiency. In this article, a novel magnetic structure that integrates a matrix transformer and inductor with minimum winding and a single magnetic core is proposed, to allow a high-density and high-efficiency LLC converter design for a bus converter. A 40—60-V input and regulated 12-V output converter is developed to deliver a 1-kW output power in a quarter brick form factor. The designed converter can achieve a power density of 700 W/in^3 with a maximum efficiency of 97.82% at half-load, dropping to 97.7% at full-load operation.**

***Index Terms*— 48-V bus converter, integrated magnetics, LLC converter, matrix transformer.**

I. Introduction

AN INTERMEDIATE bus architecture using 48-V intermediate bus converter (IBC) has been widely used in telecom power supplies, and recently in data centers, using a 48-V rack architecture [1]. With the massive increase in digital content, the need for higher power converters with high power density and high efficiency is inevitable. The 48-V IBCs can be categorized as non-regulated converters [2] and [3], semi-regulated converters [4] and [5], and the fully regulated bus converters which will be the focus of this article [6] and [7].

Constant-frequency pulsewidth modulation (PWM) phase-shift full-bridge converters are commonly used in regulated bus converters. Despite the simple closed-loop implementation and simple electromagnetic interference (EMI) filter designs for constant-frequency operation, these converters have limited soft switching capabilities under different loading conditions.

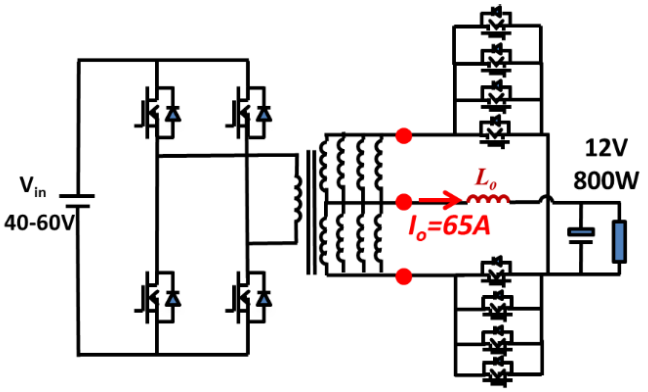

Fig. 1. SOA 48/12-V IBC with phase-shift full-bridge.

This forces the operation to a lower switching frequency (100–200 KHz) to avoid switching related loss [8] and [9]. A state-of-the-art (SOA) IBC converter with PWM operation circuit diagram is shown in Fig. 1. The low-frequency operation of these converters results in bulky magnetic components, and therefore, only one transformer can be used to deliver the desired high output power. With only one transformer, secondary windings and synchronous rectifiers (SRs) are paralleled to reduce the conduction loss; however, current sharing problems between these devices and windings will exist and can be detrimental. An additional issue for this structure is the large termination loss between the ac points of the transformer and the filter inductor and SRs, which represents a huge portion of the conduction loss, especially with high-frequency operation [2].

Variable frequency-controlled resonant converters are gaining more attention in industry practice nowadays for their ability to realize soft switching operation under different operating conditions, and this enables higher frequency of operation to realize both high efficiency and power density [10] and [11]. In this article, an LLC converter with variable frequency control is proposed for regulated bus converter applications [12] and [13]. Compared with PWM topologies, an LLC converter can achieve zero voltage switching (ZVS) for primary and secondary devices under all loading conditions. In addition, zero current switching (ZCS) for secondary side SRs and minimum turn-off current for the primary devices is realized. This enables higher frequency operation (>1 MHz)

without sacrificing the efficiency while reducing the size of the magnetic components. Using GaN devices for this LLC converter with their superior figure of merits (FOMs) over their counterparts silicon devices (Si) in terms of lower output capacitance, gate charge, and low turn-off losses enables such higher frequency operation while achieving high power density and efficiency.

Many challenges arise with the proposed converter for this application. First, high operating frequency will result in high transformer-related winding and termination loss, due to the eddy current and proximity effects. One benefit of the LLC converter with high-frequency over the low-frequency operated PWM-based IBCs is the smaller magnetic components; as a result, the matrix transformer concept with printed circuit board (PCB) winding implementation can be used. In that case, parallel secondary windings and SRs are used to reduce the conduction loss with equal current sharing. In addition, the ac termination loss can be minimized by splitting the high output currents among different transformer outputs [14].

Second, the LLC converter resonant inductor should be large enough to achieve regulation capability, and the transformer leakage inductance is not enough for such purpose. In [15], a magnetic structure using multiple E-cores stacked on top of each other for both transformer and inductor has been reported for regulated LLC converter, and the reported converter can achieve high efficiency; however, the structure is very complicated for better manufacturability. In this article, an integrated resonant inductor and transformer winding structure is proposed for this converter; the structure also uses a single core for both transformer and inductor resulting in a smaller footprint and lower loss, while achieving the required regulation capability.

This article, which is the modified version of the previously published conference article [12], with added contribution of the integrated single-core solution for the magnetic structure and its impact on the converter performance with the design and optimization details of the LLC converter, is organized as follows: Section II discusses the matrix transformer structure with a PCB winding for the proposed LLC converter. Section III describes the integrated inductor and transformer structure. Section IV examines the magnetic structure design and optimization. Section V presents the converter prototype and experimental results. The summary and conclusions are given in Section VI.

II. Matrix Transformer Structure Selection and Optimization for LLC Converter-Based IBC

The matrix transformer has proven to be the best candidate for the LLC transformer to avoid penalties of high-frequency-related loss [14], [16], [17]. Breaking down a single transformer into multiple elemental transformer arrays, interwired to form a single transformer, helps reduce the conduction loss and termination loss. The designed LLC converter is required to have a turns ratio of (4:1), whereby the converter operates close to the resonant frequency during nominal condition of 48/12 V, to ensure the highest operating efficiency at nominal condition. With targeted power of 1 kW ($I_{\text{output}} = 83$ A),

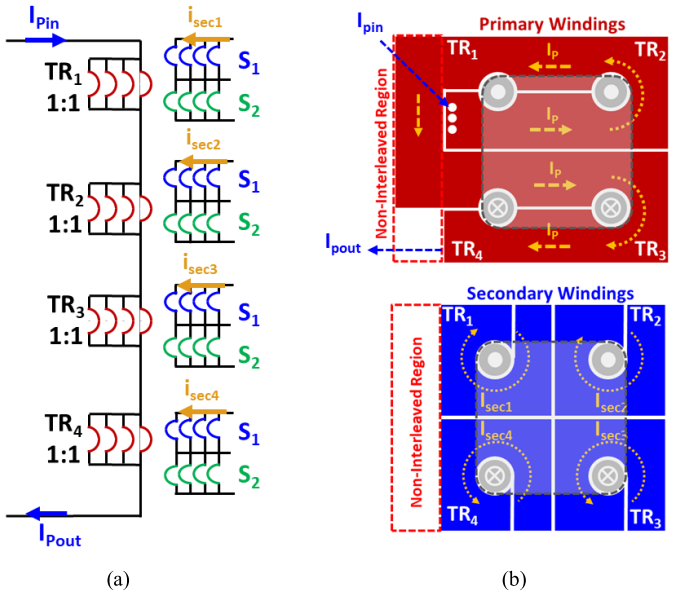

Fig. 2. LLC converter with 4 × 1:1 matrix transformer structure based on [19]. (a) Transformer architecture and (b) PCB winding implementation.

the single (4:1) transformer is broken into four elemental matrix transformer structures to reduce the conduction loss [18]. Multiple methods have been reported in the literature to integrate these four elemental transformer structures using a single core by the flux cancellation and integration concept [2].

In [19], the four transformers were connected in series from the input side and in parallel from the output side, following the same structure of the proposed LLC converter with (4:1) transformer; the resulting matrix transformer architecture and primary winding PCB implementation are shown in Fig. 2. The difference in this transformer from previous work is the smaller total number of turns required on the primary side. With a total (4:1) turns ratio required, each elemental transformer has a turns ratio of (1:1) which can be implemented using one PCB layer, as shown in Fig. 2(b). The interconnection between the four transformers' primary windings is shown in the dotted red box, occurring outside the overlapped region with the secondary windings. This will result in a non-interleaved current creating higher leakage flux, and as a consequence, more primary side winding conduction loss.

The interleaving of the primary and secondary currents is very essential to reduce the ac loss created by the eddy and proximity effects. In the center-tapped rectifier structure used with this transformer, each two secondary layers will have a primary winding layer between them to have a perfectly interleaved structure as shown in Fig. 3(a). With high output currents, a single secondary layer will result in high conduction loss; for that reason, multiple secondary layers are required to be parallel connected to reduce the secondary side conduction loss as shown in Fig. 3(b) and (c) stack arrangement of one elemental transformer. With only one primary turn required to realize the (1:1) turns ratio in each elemental transformer and to maintain the interleaving structure, with the addition of each secondary parallel layer another primary layer will

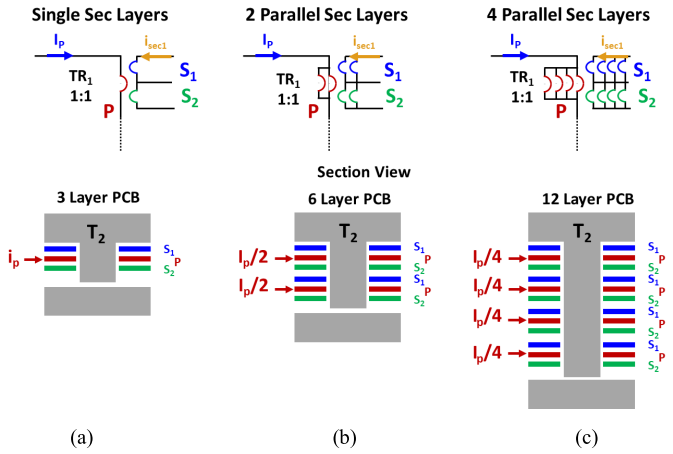

Fig. 3. PCB winding structure of a (1:1) transformer with different secondary winding parallel structures. (a) Single layer. (b) Two parallel layers. (c) Four parallel layers.

be added. In the proposed structure, a 12-layer PCB will be used with four layers for each secondary winding (S1 and S2) connected in parallel; as a result, all the primary layers will also be connected in parallel. Achieving equal current sharing between all primary and secondary four parallel layers is very challenging as reported in [20].

In [18], another method of integrating the four transformers using a single core while reducing the core loss in the magnetic plates has been reported. This method requires at least two primary PCB layers to be connected in series in each elemental transformer. Using the same concept, the resulting matrix transformer architecture and primary winding PCB implementation are shown in Fig. 4(a) and (b), respectively. In this structure, all the primary winding PCB layers are connected in series as shown in the stack arrangement in Fig. 4(c). With all the primary PCB layers carrying the same current, an equal current sharing is achieved for all the secondary winding parallel layers. However, each elemental transformer has a turns ratio of (4:1), and for that the four transformers can only be connected in parallel from the primary side and secondary side to have the total required turns ratio of (4:1) as shown in Fig. 4(a). The current balancing between all these transformers will suffer if the primary winding has an unsymmetrical structure. In Fig. 4(b), one can see that following this PCB implementation method will always result in an unsymmetrical primary winding structure which is not an issue if these transformers are all connected in series; however, in that case all of them are connected in parallel. Meaning that TR1 and TR4 will always have a shorter current path compared with TR2 and TR4, and this will create a current balancing problem between the individual parallel transformers.

The limitation of using previous reported methods of integrating four transformers in a single core is solely due to the need of lower total primary side turns. In this article, we propose the matrix transformer structure as shown in Fig. 5(a). As opposed to series connection of all elemental transformers while paralleling all the primary winding PCB layers as in Fig. 2, or the unsymmetrical parallel connection of all elemental transformers with all primary PCB layers

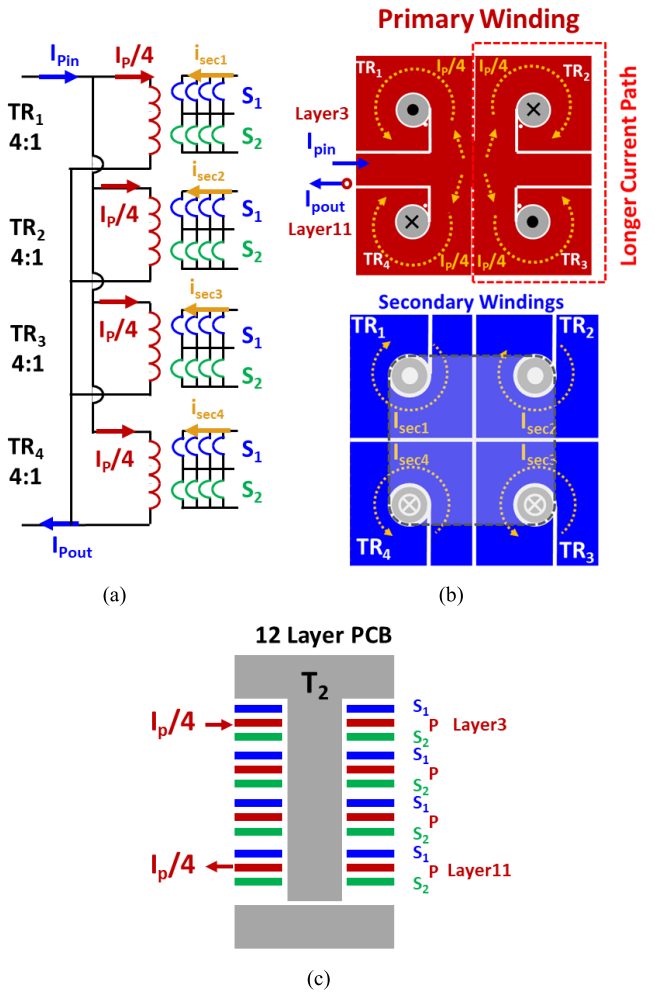

Fig. 4. LLC converter with 4 × 4:1 parallel matrix transformers structure based on [18]. (a) Transformer architecture, (b) PCB winding implementation, and (c) elemental transformer stack arrangement.

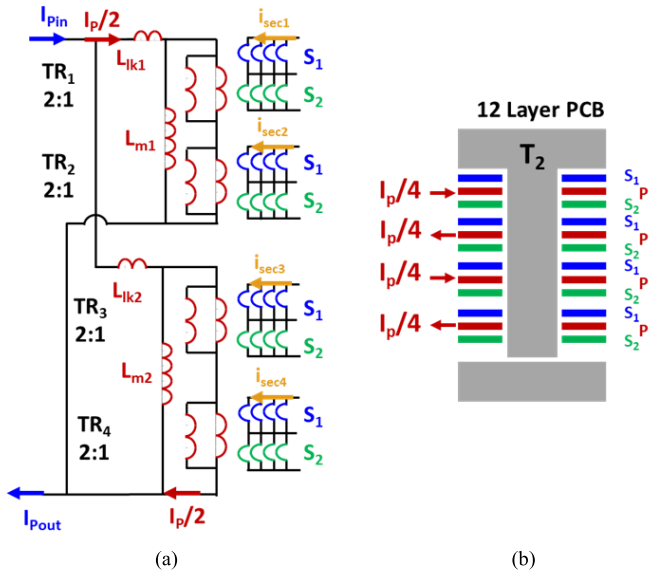

Fig. 5. Proposed LLC converter with 2 × 2:1 parallel matrix transformer structure. (a) Transformer architecture. (b) PCB winding arrangement.

connected in series as in Fig. 4. The proposed structure uses two parallel matrix transformer structures with two parallel

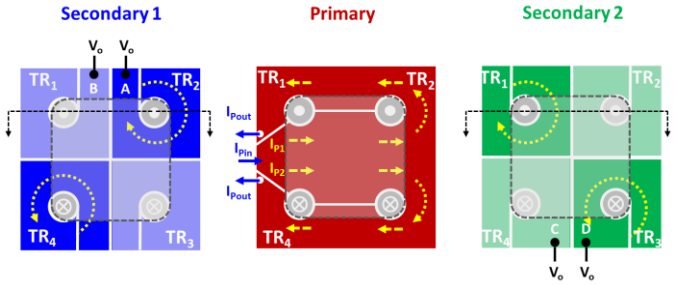

Fig. 6. Symmetrical PCB winding implementation for the proposed 2 × 2:1 parallel matrix transformer structure.

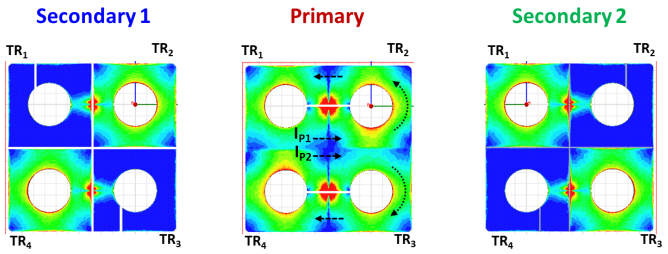

Fig. 7. FEA simulation current density result for primary and secondary current windings in symmetrical winding implementation.

primary PCB layers as shown in Fig. 5(b). The parallel matrix transformer structure can still be integrated using a single-core structure by the flux cancellation and integration concept as reported in [12]. Each parallel matrix transformer comprises two elemental transformers connected in series to ensure a perfect current sharing between them; however, the current sharing between these two parallel matrix transformers is challenging and needs to be guaranteed to get the benefits of the proposed architecture.

These two matrix transformers will have two separate leakage inductances L_{LK1} and L_{LK2} and two separate magnetizing inductances L_{m1} and L_{m2}. By ensuring that both leakage and magnetizing inductances are equal, that is, $L_{LK1} = L_{LK2}$ and $L_{m1} = L_{m2}$, perfect current sharing between these two parallel matrix transformers can be ensured. The leakage inductance for each of these parallel matrix transformers is highly affected by the winding length and interleaving structure. The proposed symmetrical PCB winding implementation is shown in Fig. 6. One can see that the primary windings between the upper and lower parallel matrix transformers are identical to ensure the first condition for equal current sharing, that is, $L_{lk1} = L_{lk2}$. With integrating all the transformers using a single core, the second condition, that is, $L_{m1} = L_{m2}$, can also be ensured. In addition, all the primary and secondary windings are overlapped to have perfect interleaving without any need for additional non-interleaved interconnections compared with the case described earlier in Fig. 2(b).

From the finite element analysis (FEA) simulation results shown in Fig. 7, it is clear that current is equally shared between the upper and lower parallel transformers with single-core integration and a symmetrical PCB winding implementation. However, there exists a severe current crowding in the primary and secondary windings.

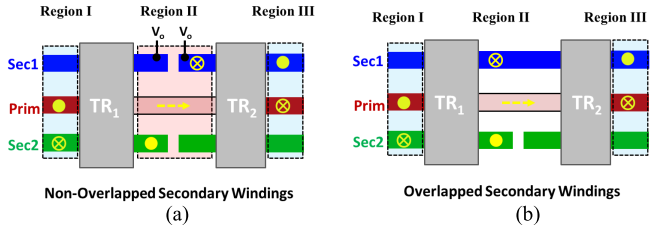

Fig. 8. Sectional view of the PCB windings. (a) Non-overlapped winding. (b) Overlapped secondary winding.

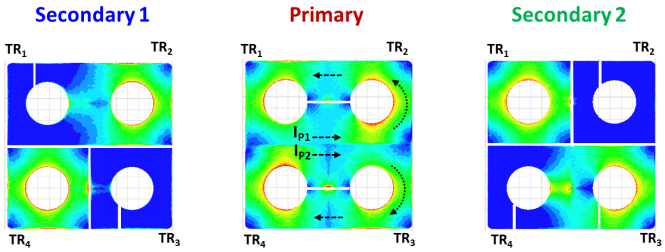

Fig. 9. FEA simulation current density result for primary and secondary current windings in symmetrical winding implementation with overlapped secondary windings.

The reason for this current crowding can be shown from the sectional drawing of PCB winding arrangement shown in Fig. 8(a); in the outer winding section (Region I and Region III), there is a perfect interleaving between the primary and secondary winding currents; however, in the middle section (Region II) where the current crowding exists, the primary winding current is no longer overlapped with the secondary winding current and it flows in a perpendicular direction, and thus there is no means to cancel the leakage flux created between these two layers and as a result current crowding will occur. An overlapped secondary winding structure reported in [20] can help solve this issue. In the secondary 1winding drawing shown in Fig. 6, the marked points (A and B) in (TR1 and TR2) have the same voltage potential as both are connected to the output voltage terminal. The current always flow in one part of the secondary 1 winding in each half-cycle, which means these two points can be connected to each other and the gap between them can be removed as shown in the section drawing shown in Fig. 8(b), and this will allow the secondary 1 current to flow into a longer current path and overlap with the current in secondary 2layer. With that, the perfect interleaving can be maintained to cancel the generated leakage flux, and the same overlapping concept can be applied to points (C and D) in the secondary 2 windings of (TR3 and TR4). The FEA current density simulation result of the transformer windings with the overlapped secondary windings is shown in Fig. 9; it is clear that all the current crowding has been eliminated and perfect current sharing between the two parallel transformers is realized.

III. Integrated Resonant Inductor With Matrix Transformer Winding

A. LLC Converter Design for IBC Application

The LLC converter proposed for the 48-V IBC uses variable frequency control to change the gain of the LLC resonant tank

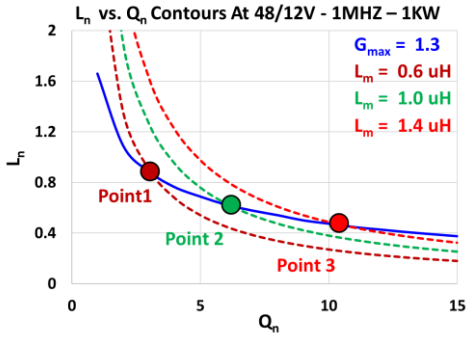

Fig. 10. LLC converter L_n and Q_n maximum gain contour plots.

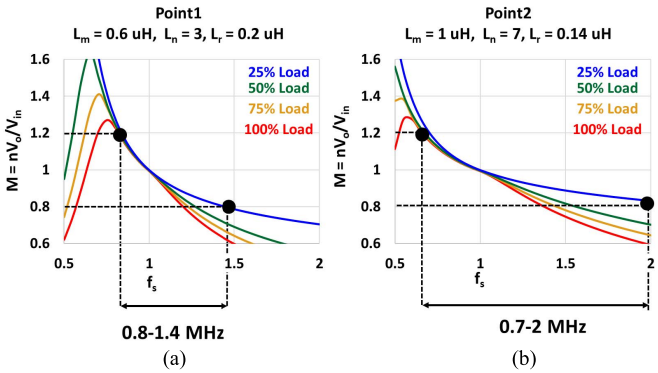

Fig. 11. LLC converter simulated gain characteristics with different design points. (a) $L_m = 0.6\ \mu$H, $L_r = 0.2\ \mu$H. (b) $L_m = 1\ \mu$H, $L_r = 0.14\ \mu$H.

and realize output voltage regulation. The designed converter is required to deliver a constant output power of 1 kW at a regulated output voltage of 12 V. The nominal input voltage of this converter is 48 V; however, this voltage is normally connected to a battery, the voltage of which might vary between 40 and 60 V when fully discharged during power outages or when fully charged. This means the designed converter is required to have a voltage gain of $M = \mathrm{n}V_o/V_{\mathrm{in}}$ that varies from 1.2 to 0.8 to regulate the output voltage at 12 V when the input voltage changes from 40 to 60 V, respectively.

The selection of the magnetizing (L_m) and resonant (L_r) inductances have a great impact on the designed gain characteristics of the converter and the operating frequency range when regulating the output voltage. The converter will be designed to have a maximum gain of $G_{\max} = 1.3$ to have some margin from the desired maximum gain of $G_{\max} = 1.2$. According to [21], the first step of the design is the selection of L_m to achieve the desired $G_{\max}$. The governing equations for the LLC converter are listed in (1) and (3), where C_r is the resonant capacitor, $f_o = 1$ MHz is the resonant frequency, R_L is the load resistance, $n = 4$ is the transformer turns ratio, L_n represents the ratio between L_m and L_r, and Q_n represents the resonant tank quality factor with different loading conditions. To achieve the desired $G_{\max} = 1.3$, SIMPLIS simulation was used to get the maximum gain contour with different L_n and Q_n values and the results are shown in the blue line of Fig. 10. Any combination of (L_n, Q_n) on this line can achieve a maximum gain of 1.3.

Another contour plot which represents the product of ($L_n Q_n$) as given in (4) can be plot on the same graph; the intersection between these two contour plots will determine the minimum L_n value required to achieve the desired $G_{\max}$. The second contour plot is dependent on different circuit parameters; in this design, the resonant frequency, turns ratio, and load have been already determined, which means the second contour is only changing with different magnetizing inductances. Shown in Fig. 10 is the simulated maximum gain contour with the $L_n Q_n$ contour with different L_m values. Marked on the curve are the three design points each of which can achieve the desired $G_{\max}$. To select the proper design point, the gain characteristics at each point with load variation have been simulated and the results are shown in Fig. 11. It is clear that with different design points the desired maximum gain can be achieved; however, the larger L_n values (Point 2) will result in a very wide frequency range that reaches 2 MHz operating frequency to achieve the $G_{min} = 0.8$ value at light load conditions, and this will result in a significant light load efficiency reduction with the benefit of smaller resonant inductance. In this design, Point 1 was selected for the designed converter by which a resonant inductance of $L_r = 200$ nH and a magnetizing inductance of $L_m = 600$ nH are desired to regulate the output voltage with a reasonable frequency range of 800–1.4 MHz at full-load condition and the maximum operating frequency is 1.6 MHz during light load condition.

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$L_n = \frac{L_m}{L_r} \tag{2}$$

$$Q_n = \frac{\sqrt{L_r C_r}}{n^2 R_L} \tag{3}$$

$$L_n Q_n = \frac{2\pi f_o}{n^2 R_L} L_m \tag{4}$$

B. Integrated Inductor and Transformer Structure of LLC Converters

The magnetizing inductance can be easily achieved by increasing the air gap of the matrix transformer core. However, in the designed PCB winding transformer, the windings are interleaved to reduce the ac conduction loss, resulting in very small transformer leakage inductance ($L_{lk} \approx 15$ nH). This is not enough to achieve the required gain characteristics and achieve output voltage regulation. For this reason, an extra resonant inductor is required. The LLC resonant inductor is needed to handle the high primary side ac currents of the converter. Usually, litz wire inductors are used to minimize the ac-related loss of these inductors; however, the resulting inductors are bulky and labor-intensive to implement. In this work, a PCB winding inductor is proposed for high power density and manufacturability of the proposed converter. Originally, a separate inductor and transformer would be used, as shown in Fig. 12. Clearly, with the proposed transformer and inductor PCB winding structure, the part of the inductor in the dashed black box can be removed as it is duplicated in the transformer

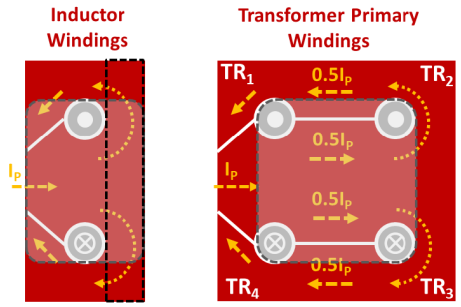

Fig. 12. Separate resonant inductor and transformer structure.

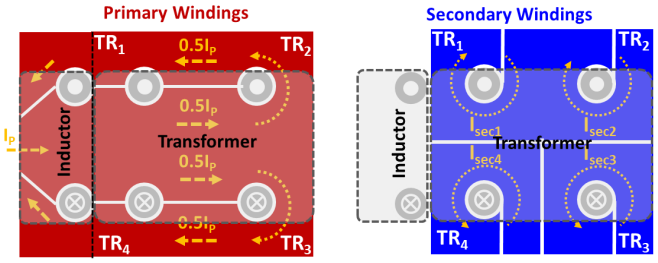

Fig. 13. Integrated inductor and transformer winding structures. (a) Primary winding. (b) Secondary winding.

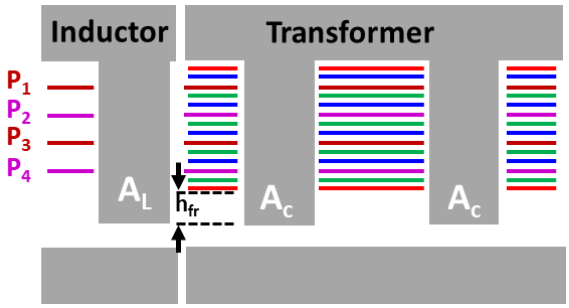

Fig. 14. Integrated inductor and transformer PCB winding arrangement.

primary winding, and both inductor and transformer primary windings can be integrated together, as shown in Fig. 13.

In this integrated structure, the extension of the primary winding without overlapping with any secondary winding as shown in the vertical PCB winding arrangement in Fig. 14 will create leakage flux; by adding two more core pillars, this flux will be confined within the core and a controllable leakage inductor can be realized with minimum PCB winding and footprint. The same concept can be used for an integrated inductor and transformer with any converter to realize inductance with minimum winding and loss; in this article, the concept was applied on the designed LLC converter to achieve the desirable regulation capability.

Multiple benefits can be achieved with this integrated magnetic structure; first, the integrated structure has 10% lower footprint compared with using separate inductor and transformer structures. Second, by saving the winding length required to create the leakage flux, a significant reduction in the total winding loss can be achieved. The FEA current density simulation results shown in Fig. 15 compare the total winding loss of both integrated and separate winding structures for P1 layer where a 38% reduction in the total winding

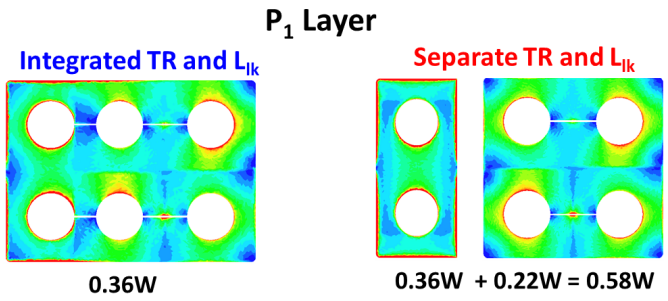

Fig. 15. Comparison of FEA current density simulation results of the separate and integrated magnetic structures.

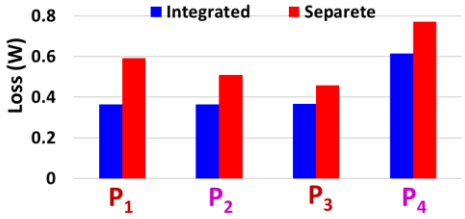

Fig. 16. Primary layers' winding loss comparison of integrated and separate structures.

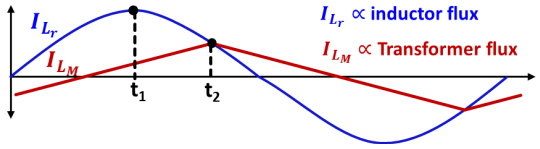

Fig. 17. Series and parallel resonant inductors' current waveforms.

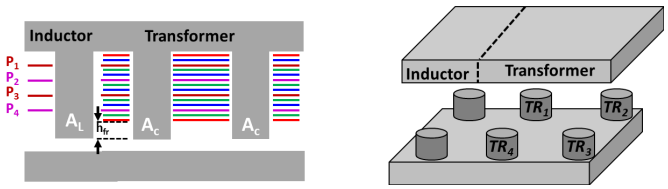

Fig. 18. Single-core structure of the integrated transformer and inductor.

loss is achieved. The same results were achieved for all four primary winding layers as shown in Fig. 16 resulting in a total winding loss reduction of 30%.

Third, with the proposed integrated structure, the two magnetic cores can be either separated or integrated in a single-core structure. Each of these cores has its own flux component depending on the excitation current of each one of them; the leakage inductor in this structure will be used as the series resonant inductor of the LLC converter (L_r), while the magnetizing inductance (L_m) of the transformer will be used as the parallel resonant inductor. The waveforms of both inductors' current components are shown in Fig. 17. The series resonant inductor L_r will see the primary side sinusoidal resonant current, while the parallel resonant inductor L_m will see the triangular magnetizing current resulting from the applied output voltage on the transformer winding. The maximum flux $\emptyset_{\text{max-Lr}}$ and $\emptyset_{\text{max-Lm}}$ which is proportional to the excitation current of both inductors will occur at the time instant t_1 and t_2, respectively.

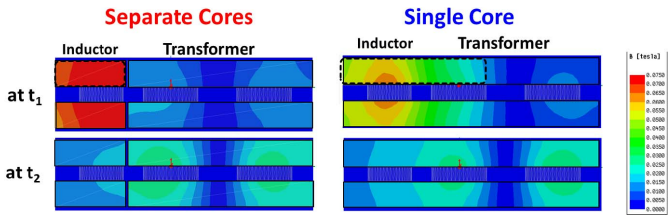

Fig. 19. Comparison of FEA flux density simulation result of separate- and single-core structures.

The core loss density in each core is functional in the maximum flux density $B_{\max} = \emptyset_{\max}/\mathrm{A}$ with its highest value at the peak of each flux component. Although these two current components are in phase, the maximum flux of the sinusoidal flux occurs at time instant t_1, while the maximum flux of the triangular flux component occurs at time instant t_2. By integrating the two magnetic cores in a single-core structure as shown in Fig. 18, both the inductor and the transformer will share the top and bottom magnetic plates. By this way, we can take advantage of the phase shift in the maximum flux instants where each component will see larger core area that will help reduce $B_{\max}$ at each time instant only in the magnetic plates. This will result in a smaller core loss density only in the magnetic plates while keeping the same core loss density in the core legs. From the FEA simulation flux density results shown in Fig. 18, we can clearly see the reduction in the flux density at the time instant t_1 for the integrated structure over the separate-core structure with a better utilization of the magnetic plates, and this reduction in the flux density will result in over 30% core loss reduction as will be shown later in the experimental section.

C. Integrated Magnetic Structure Design Optimization

The proposed matrix transformer structure, as shown in Fig. 5, consists of primary and secondary windings' parallel connections. The current sharing between these layers is essential to fully use the PCB layers to reduce the conduction loss. Considering the transformer winding separately, the symmetrical PCB winding arrangement with alternating magnetomotive force (MMF) structure reported in [12] and [20] can be used to ensure a perfect current sharing between all parallel layers of each elemental transformer as shown in Fig. 20.

However, with an integrated inductor structure, the lack of interleaving in the inductor winding structure results in strong leakage flux that might negatively impact the whole magnetic structure current distribution. For simplicity of FEA simulations, one elemental transformer integrated with an inductor is considered for further analysis. The simplified integrated structure equivalent circuit and PCB arrangement are shown in Fig. 21. Each elemental transformer primary winding and inductor consists of two-turns implemented using four PCB layers. Two turns are connected in series using layers 3 and 6, while the other two turns are connected in series using layers 9 and 12. These two separate series connections are then connected in parallel, represented by i_1 and i_2 current paths. From the FEA current density simulation results shown in Fig. 22, the current density for these two parallel currents,

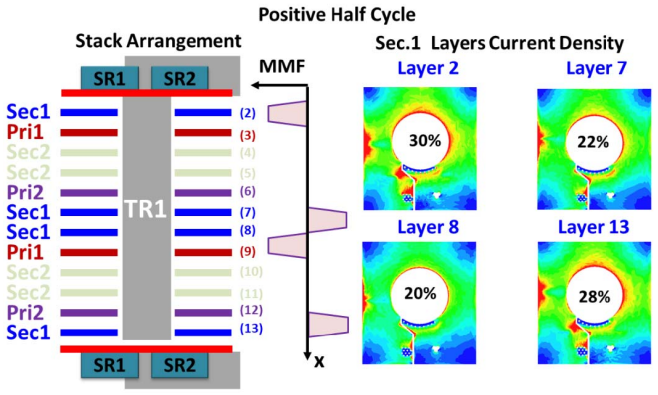

Fig. 20. PCB winding symmetrical arrangement and the corresponding MMF diagram and secondary winding layers' current density during positive half-cycle.

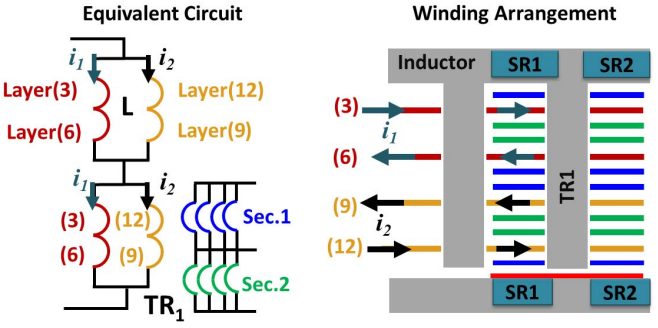

Fig. 21. Equivalent circuit and PCB winding arrangement of integrated one transformer and inductor.

i_1 and i_2, is almost equal with the symmetrical PCB winding arrangement previously mentioned. The introduction of the inductor winding to the structure will change the current density distribution dramatically. All the primary current is forced to pass through layer 12, resulting in current distribution of $i_1 = 2\% i_{\mathrm{Total}}$ and $i_2 = 98\% i_{\mathrm{Total}}$ which means half the PCB layers added to reduce the conduction loss are not used. The reason behind that is the strong inductor fringing flux concentrated near layer 12 as shown in Fig. 23. This flux will attract all current to this layer, and a severe current sharing problem will exist.

A fractional turn inductor structure with an interconnection between PCB layers is proposed to overcome this issue where both primary currents, that is, i_1 and i_2, are affected equally by this air gap fringing flux. The proposed structure equivalent circuit and PCB arrangement are shown in Fig. 24.

The PCB implementation method of this interconnection is shown in Fig. 25. The first current component i_1 goes to a fraction of turn on layer 3, then the current interconnects with another fraction of turn on layer 12 through vias, and then continues to a full turn on layer 6. Similarly, i_2 will start with a fraction of turn on layer 12, then the current interconnects with another fraction of turn on layer 3through vias, and then continues to a full turn on layer 9. Both current components will have to pass through layer 12, by which the leakage and fringing flux impacts both of them equally. It should be noted that with any additional parallel path, the same interconnection

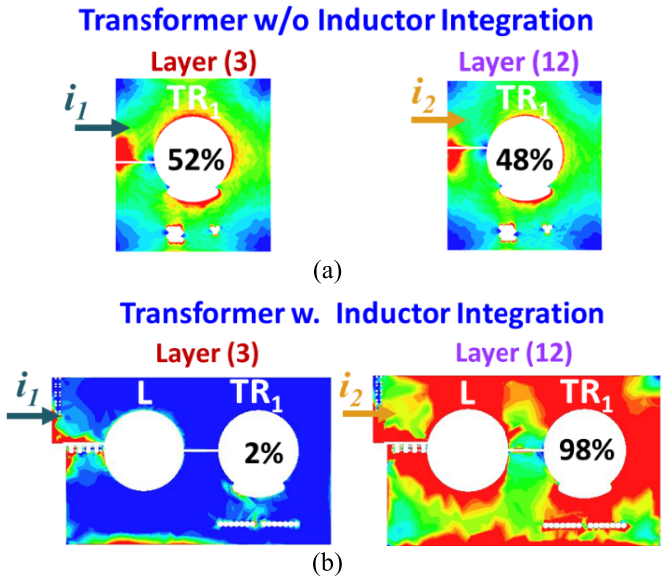

Fig. 22. Current density distribution in primary winding parallel layers. (a) Transformer only. (b) Transformer integrated with inductor.

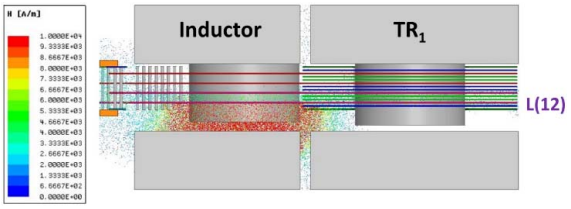

Fig. 23. Field intensity FEA simulation results of the integrated structure.

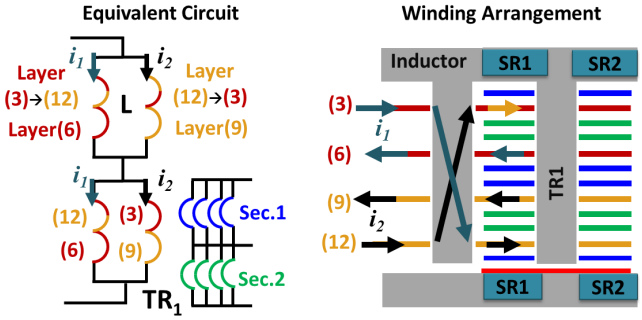

Fig. 24. Equivalent circuit and PCB winding arrangement of integrated transformer and inductor with fractional turn interconnection.

method is required to ensure balanced currents among all these parallel layers which will make the implementation more complicated.

The interconnection location between these two layers impacts the current distribution between the two parallel paths; shown in Fig. 26(a) is the primary winding with the interconnection location at distant x from the core center; using FEA simulations, we sweep different x values and record the current sharing between these two parallel paths; the current distribution ratio shown in Fig. 26(b) clearly shows that at $x/r = 0.35$, equal current sharing can be realized.

The current density FEA simulation results, as shown in Fig. 27, show the comparison of the current distribution with and without the fractional turn connection; it is clear that with

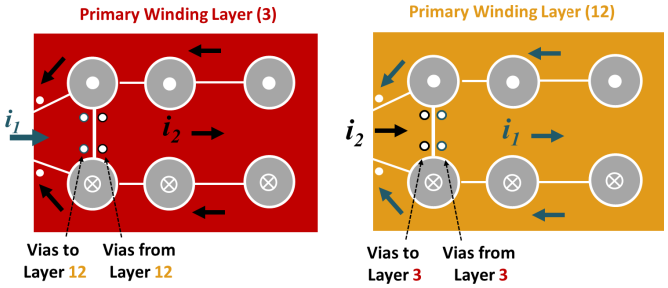

Fig. 25. PCB implementation of the fractional turn interconnection between PCB layers 3 and 12 in the integrated magnetic structure.

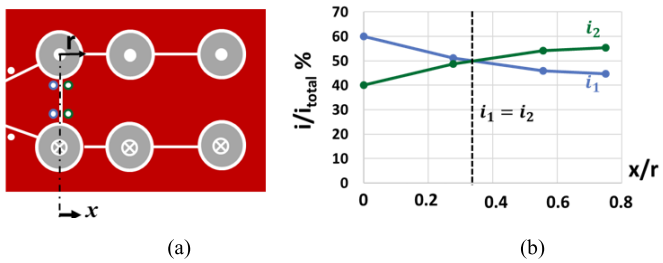

Fig. 26. Interconnection location impact on current sharing. (a) Primary winding with interconnection. (b) Current distribution ratio.

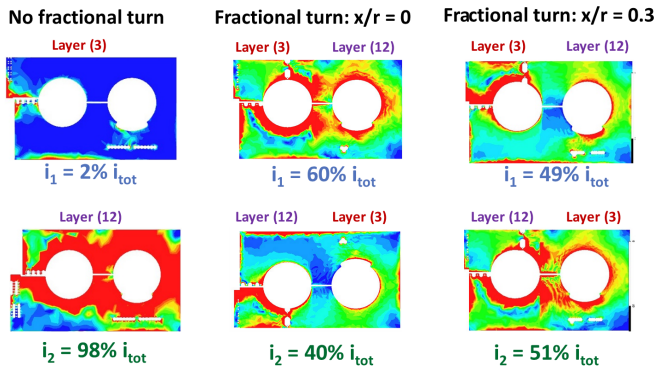

Fig. 27. Comparison of the current density distribution in primary winding parallel layers with and without the fractional turn interconnection.

$x/r = 0.35$, the two parallel current components are almost equal; therefore, all the primary and secondary parallel layers of the integrated structure can be used to the full potential with a total winding loss reduction of 30% being achieved by fully using the parallel connection of both the primary and secondary windings.

The designed inductor in the proposed structure uses an air gapped core, by which the air gap reluctance highly affects the inductance and the fringing flux impact. The designed core leg is extended away from the PCB winding by a distance ($= h_{FR}$) to reduce the eddy current loss associated with the fringing flux as shown in Fig. 18. Using FEA simulation, different h_{FR} values have been evaluated, and from the results shown in Fig. 28, if the core leg is extended more than 1 mm the fringing flux loss reaches a diminishing return point where further extension will not serve any purpose. If this extension becomes less due to manufacturing tolerance or a mismatch exists between the created air gaps on the two inductor legs, the designed interconnection point might not ensure equal

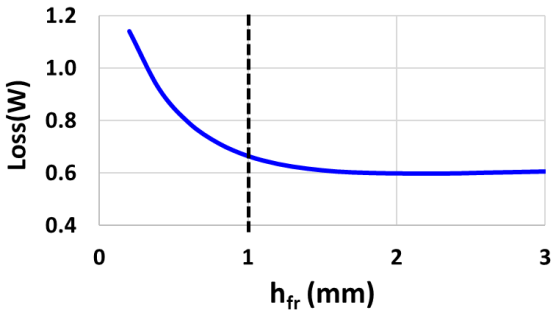

Fig. 28. Inductor winding loss with core leg extension to avoid fringing flux loss.

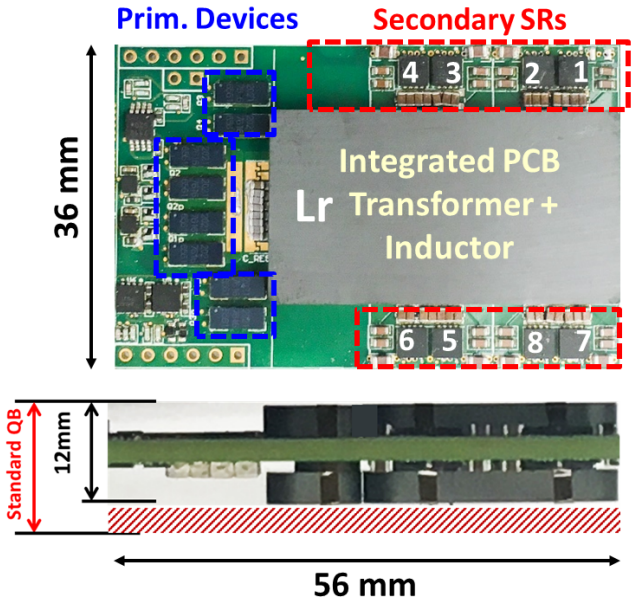

Fig. 29. 48-/12-V 1-kW LLC converter experimental prototype.

current sharing, and as shown in the results evaluating the interconnection point impact shown in Fig. 26, a 60%/40% current sharing can be considered as the worst case which will not have a significant impact on the winding loss.

D. Converter Prototype Design and Experimental Results

The experimental prototype, as shown in Fig. 29, was built for the proposed 48-V LLC bus converter with an integrated magnetic structure. The designed converter parameters are listed in Table I; EPC2021-100-V GaN devices were used on the primary side due to their low FOM and small turn-off losses, 40-V Si were used on the secondary side, and the magnetic core uses ML-91 material from Hitachi metals and is a custom-made structure. The designed converter can deliver a continuous power of 1 kW in a quarter brick form factor. With a profile of 12 mm which is 3 mm lower than the standard quarter brick size, the designed converter can achieve a power density of 700 W/in3. To achieve the regulation requirements, the designed converter operates in a frequency range of 0.7–1.6 MHz during all operating conditions. The total devices' loss breakdown under different operating conditions is shown in Fig. 30, and the total devices' loss is only 1% of the total delivered power at full-load condition.

TABLE I
LLC CONVERTER PROTOTYPE DESIGN PARAMETERS

Parameter	Value
Input voltage (V_{in})	40-60V
Regulated output voltage (V_o)	12V
Maximum output power (P_{omax})	1000 W
Primary Devices	EPC2021
Secondary Devices	BSZ0500NSI
Transformer/Inductor Core Material	ML91
Operating Frequency Range (F_s)	0.7 – 1.6 MHz
Resonant Inductor (L_r)	200 nH
Magnetizing Inductance (L_m)	600 nH
Resonant Capacitor (C_r)	110 nF

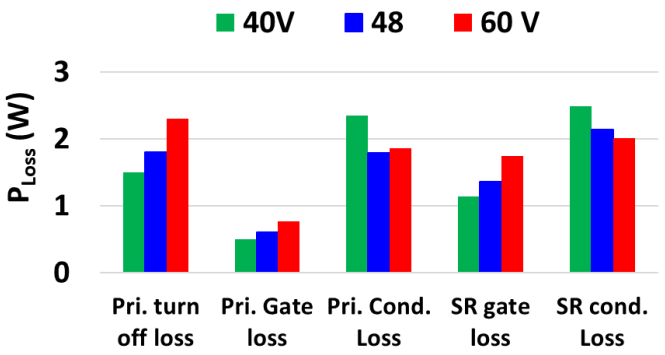

Fig. 30. Total converter devices' loss breakdown at different input voltages and full-load condition.

The steady-state operating waveforms under nominal input voltage 48 V and full-load condition are shown in Fig. 31(a). ZVS can be achieved for both primary and secondary devices with a very small turn-off primary side current. Fig. 31(b) and (c) shows the full-load operating waveforms' input voltage of $V_{\text{in}} = 40$ V and $V_{\text{in}} = 60$ V where the frequency is changed to 780 KHz and 1.3 MHz, respectively, to regulate the output voltage at 12 V. In both cases, ZVS operation is still achieved for both primary and secondary devices.

To verify the concept of integrated core structures, the same converter efficiency was tested at nominal condition with both single-core and separate-core structures, and the testing results shown in Fig. 32 show that the converter can achieve a maximum efficiency of 97.8% while maintaining an efficiency above 97% from 25% to 100% loading conditions. The single-core structure helps increase the efficiency at full-load condition by 0.6%, both with similar efficiency during light load; the reason for that is the dependence of the inductor core loss on the excitation primary side current meaning that the core loss has a very marginal impact during light load operation.

The thermal image comparison of both core structure of this converter at nominal condition (48/12 V) and full-load operation is shown in Fig. 33. The core temperature (SP1) has dropped by more than 16° with the single-core solution

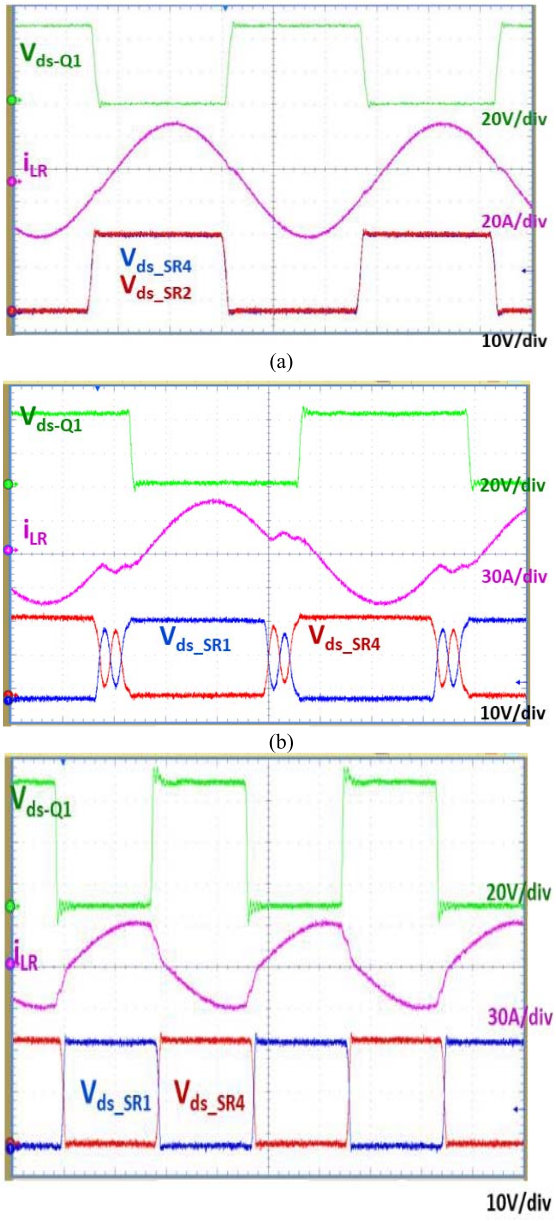

Fig. 31. LLC converter operating waveforms at full-load conditions and 12-V output voltage (green), primary side device drain to source voltage (purple), and resonant inductor current (red and blue) secondary side SR drain to source voltages. (a) $V_{\text{in}} = 48$ V and $F_s = 1$ MHz. (b) $V_{\text{in}} = 40$ V and $F_s = 0.78$ MHz. (c) $V_{\text{in}} = 60$ V and $F_s = 1.3$ MHz.

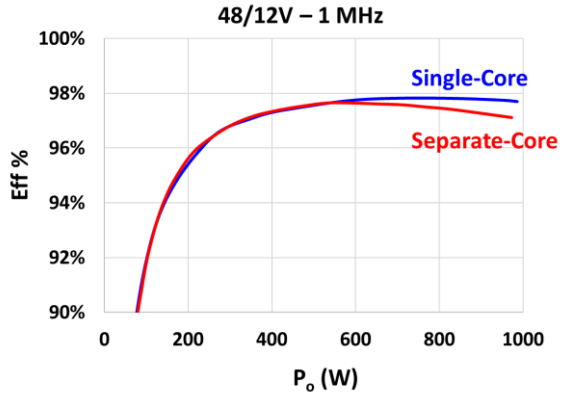

Fig. 32. LLC-converter-measured efficiency at nominal conditions.

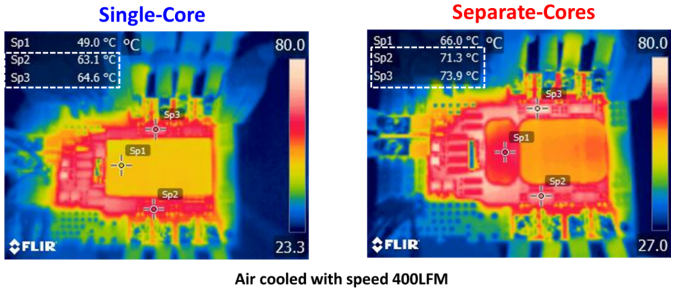

Fig. 33. Converter full-load thermal image comparison with different core structures at nominal voltage.

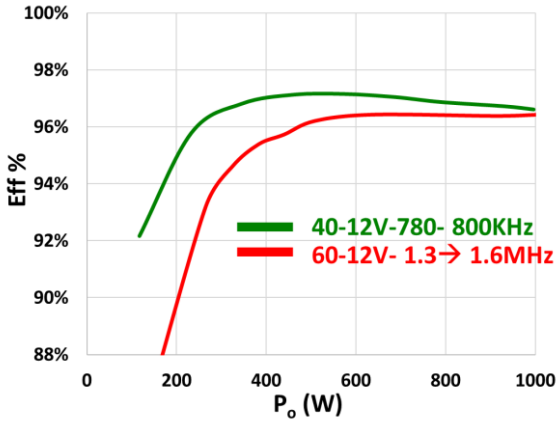

Fig. 34. Converter-measured efficiency at different input voltages.

over the separate-core solution due to the reduction in the core loss. One can see the highest temperature across the board is only 74° with such high-power-density solution. The temperature at SP2 and SP3 represents the SR temperature on two parallel elemental transformers; the temperature on both SRs is almost equal. This proves the validity of the proposed parallel matrix transformer structure where equal current sharing can be achieved on both transformers using a symmetrical winding implementation and integrating all four transformers using one core structure.

The converter-measured efficiency with the input voltage variation is shown in Fig. 34. With variable input voltage away from the resonant frequency, the efficiency will drop; however, the overall converter efficiency is maintained above 96.5% under all conditions. A digital control method was used to regulate the output voltage of this converter; the proposed method is beyond the scope of this article and has been described in detail in [13].

Table II summarizes the performance comparison between the proposed converter and other SOA solutions; the proposed converter can achieve the highest maximum and full-load efficiency compared with all other SOA solutions while operating at higher frequency. The proposed converter can achieve the highest power density comparing to all SOA solutions operating with the same input and output voltage range; the SOA solution reported in [22] achieved higher power density;

TABLE II

PERFORMANCE COMPARISON OF THIS WORK WITH SOA SOLUTIONS

Parameter	This work	[11]	[23]	[22]	[7]
Input voltage	40-60V	40-60V	40-60V	40-60V	40-60V
Output voltage	12V	12V	12V	12V	12V
Maximum power	1000W	600W	1000W	1300W	800W
Frequency	0.7 - 1.4 MHz	0.3-1 MHz	230 KHz	230 KHz	150 KHz
Maximum efficiency	97.8%	97.8%	97.3%	97.4%	96.3%
Full load efficiency	97.6%	97.5%	96.8%	96.6%	96.1%
Power Density	700 W/in^3	300 W/in^3	624 W/in^3	812 W/in^3	480 W/in^3

however, it can only operate at narrower voltage range with lower efficiency than the proposed converter.

IV. SUMMARY AND CONCLUSION

This article proposes a novel integrated matrix transformer and inductor for regulated LLC converter proposed for 48-/12-V bus converter applications. Integrating four elemental transformers using a single core, with a symmetrical PCB winding arrangement, is recommended to realize equal current sharing between parallel transformers. With a simple extension in the primary winding, a controlled leakage inductance required by the LLC converter to achieve the output voltage regulation is realized, with minimum losses and footprint. A symmetrical PCB winding arrangement for the matrix transformer with fractional turn interconnections between the inductor windings is proposed to achieve equal current sharing between all parallel PCB layers. The transformer and inductor core was integrated using a single-core structure that helps reduce the core loss and improve the full-load converter efficiency. A GaN-based converter prototype for 48-/12-V 1 kW is built that can achieve a power density of 700 W/in3 with maximum efficiency of 97.82% with outstanding performance over other SOA solutions in terms of efficiency and power density.

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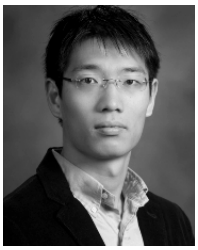
During the tenure at Virginia Tech, he has supervised the completion of 71 Ph.D. and 80 master's degree students. He is currently a University Distinguished Professor with Virginia Tech, Blacksburg, VA, USA, and the Director of the Center for Power Electronics Systems (CPES), a National Science Foundation Engineering Research Center (NSF ERC) established in 1998, with four university partners—the University of Wisconsin–Madison, Madison, WI, USA, the Rensselaer Polytechnic Institute, Troy, NY, USA, North Carolina A&T State University, Greensboro, NC, USA, and the University of Puerto Rico-Mayaguez, Mayagüez, Puerto Rico, and more than 80 industry members. The center's vision is to provide leadership through global collaboration to create electric power processing systems of the highest value to society. More than the ten-year NSF ERC Program, CPES has been cited as a model ERC for its industrial collaboration and technology transfer, and education and outreach programs. He holds 69 U.S. patents. He has published 238 journal articles and more than 596 refereed technical articles. His current research interests include high-frequency power conversion, renewable energy, high-density electronics packaging and integration, and modeling and control.

Dr. Lee has served as the President of the IEEE Power Electronics Society from 1993 to 1994. He was named to the National Academy of Engineering in 2011. He received the William E. Newell Power Electronics Award in 1989, the Arthur E. Fury Award for Leadership and Innovation in Advancing Power Electronic Systems Technology in 1998, and the Ernst-Blickle Award for achievement in the field of power electronics in 2005.



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Dr. Li received the First Place Prize Article Award for the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2016. He was also a recipient of the 2017 U.S. National Science Foundation (NSF) Career Award.