Vertical GaN Superjunction Diode on Sapphire with Kilovolt Dynamic Breakdown Voltage

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***Abstract*— The development of superjunction structures for use in vertical wide bandgap power devices promise to break the 1-D material limits. Additionally, the possibility of utilizing heteroepitaxial GaN-on-Sapphire wafer for vertical devices can significantly trim the material and device cost. This work introduces a quasi-vertical GaN-on-Sapphire superjunction PN diode design utilizing sputtered p-NiO on the etched GaN fins for superjunction formation. DC breakdown voltage is shown to vary with superjunction charge imbalance and significantly exceed the expected 1-D planar limit of 350V given the epilayer design used. A maximum breakdown voltage of 840 V is extracted for near charge balance conditions limited by leakage current. Dynamic breakdown of the device is characterized as a function of reverse voltage slew rate. A maximum dynamic breakdown voltage of 1160 V under a reverse voltage slew rate of 2000 V/µs is found.**

Keywords—GaN, Superjunction, Quasi-vertical, NiO, dynamic breakdown

I. INTRODUCTION

Superjunction (SJ) formation in vertical drift regions allows for power device performance to surpass traditional limits set by material constraints [1], [2]. Through the formation of charge-balanced lateral PN junctions within the drift layer, the specific on-state resistance ($R_{on,sp}$) of high-voltage device designs can be scaled linearly with breakdown voltage (V_{br}), in contrast to the quadratic scaling of $R_{on,sp}$ with V_{br} in 1D planar device designs. Si superjunction MOSFETs have been successfully commercialized for breakdown voltages between 600-1200 V. Superjunction devices have also been recently demonstrated for wide bandgap (WBG) and ultrawide bandgap (UWBG) materials, including SiC [3], [4], [5], epitaxial GaN-on-GaN [6], [7] and β-Ga_2O_3 [8]. For GaN, the possibility of using foreign substrates such as GaN-on-Si or GaN-on-Sapphire for superjunction device formation can enable significantly lower material cost as compared to GaN-on-GaN or SiC [9]. Kilovolt quasi-vertical GaN-on-Si and GaN-on-Sapphire diodes have been recently reported [10], [11], strengthening such promise.

A major issue with SJ formation in GaN lies in the difficulty of selective-area p-type doping of GaN, either through implantation and annealing or via selective p-GaN regrowth in etched areas, due to the compensation in implant damaged GaN or the interface state formation after p-GaN regrowth [12]. An alternative method to implantation or regrowth is to utilize an alternative, wide bandgap p-type material that can be deposited conformally to form a heterojunction with GaN. NiO is a WBG (3.7 eV) p-type material with a critical breakdown field greater than 4 MV/cm which can be deposited via low temperature magnetron sputtering to form conformal p-n heterojunctions with GaN [13], [14]. Recent work presented in [7] has shown the viability of superjunction formation using sputtered p-NiO/n-GaN to form heterojunctions with RIE etched n-GaN pillars. Such a technique can be directly extended to a heteroepitaxial GaN-on-Sapphire SJ device design. However, the effect of the high dislocation density in GaN-on-Sapphire substrates on the static and dynamic SJ reverse blocking performance is unclear and must be further investigated.

This work presents a quasi-vertical GaN-on-Sapphire SJ PN diode design fabricated using magnetron sputtered p-NiO on RIE etched n-GaN fins for SJ formation. The DC reverse blocking performance of the GaN-on-Sapphire SJ diodes successfully show the effects of charge imbalance on device V_{br}, leading to a V_{br} of 840 V at near charge balanced conditions. An on-wafer unclamped inductive switching (UIS) system is

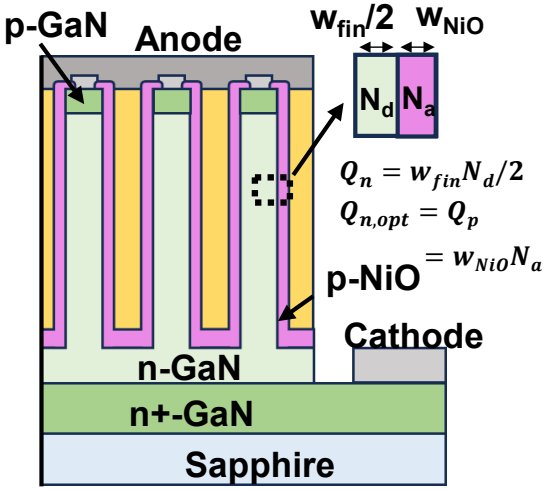

Fig. 1. GaN-on-Sapphire PN SJ device design. The superjunction unit cell and charge balance condition are also illustrated.

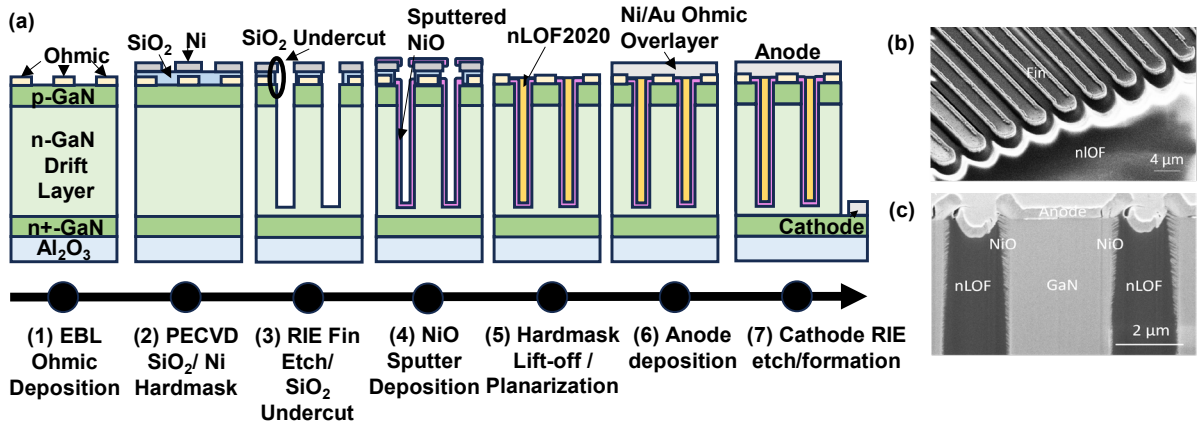

Fig. 2. (a) Processing flow for GaN-on-Sapphire PN SJ fabrication. (b) SEM image of fins after NLOF planarization. (c) FIB-SEM image of device cross section in the fabricated superjunction region.

designed to characterize the dynamic breakdown performance of the SJ devices. A dynamic breakdown voltage of over 1150 V is demonstrated for reverse bias slew rates of 2000 V/µs. These results demonstrate the high dynamic performance of GaN SJ devices on low-cost GaN-on-Sapphire substrates.

II. Device Design and Fabrication Process

Fig. 1 shows the SJ device design. The devices presented in this work are fabricated on a GaN-on-Sapphire epilayer grown via MOCVD by Enkris Semiconductor. The epi consists of a 40 nm p++ GaN cap layer, 300 nm of p+-GaN ($N_a > 1x10^{19}$ cm^{-3}), 8 µm of n-GaN ($N_d=8x10^{16}$ cm^{-3}), 4 µm of n+-GaN ($N_d=5x10^{18}$ cm^{-3}), followed by a UID AlN buffer layer on a sapphire substrate. Lateral PN heterojunctions are formed between magnetron sputtered p-NiO and ICP-RIE etched n-GaN pillars to enable superjunction formation. NiO films are deposited by room-temperature magnetron sputtering in with an Ar:O_2 partial pressure ratio of 20:1 at an RF power of 100 W. The N_a of the deposited NiO film was characterized via C-V characterization of p-NiO/n+-Ga2O3 diodes formed using the same sputtering recipe as that used for superjunction formation, and is found to be $1.2x10^{18}$ cm^{-3}. Further details on the optimization and characterization of the NiO sputtering conditions used in this work can be found in [13]. Charge balance in the superjunction is controlled via the balance between the total charge dose in the p-NiO film and half of the n-GaN pillar, as shown in equation in the inset of Fig 1(a). A constant film thickness of 45 nm was targeted for the deposited NiO, while the n-GaN pillar width was varied between 1 µm to 3 µm in 0.5 µm steps. This variation in pillar width corresponds to a predicted charge imbalance range between -27.3% to 113%.

Fig. 2(a) shows the device fabrication process. A self-aligned process is used to sputter NiO onto the GaN fin sidewalls and remove the NiO cap in a single lithography step [7], [8]. Ni/Au (5 nm/20 nm) p-GaN contacts are defined via EBL and annealed at 560 °C in air. PECVD SiO_2 is then deposited, followed by the deposition of a Ti/Ni hard mask. Cl_2 based RIE is then used to etch 7.5 um into the GaN n-layer for fin formation, with the fins aligned to the GaN m-plane. After the formation of an undercut in the PECVD SiO_2 with 20:1 BOE, the NiO film is deposited. 10:1 BOE is then used to lift-off the Ni hard mask as well as the NiO capping the p-ohmic contact. The space between the GaN pillars is planarized using the spin coated NLOF2020. The anode contact is formed using Au via e-beam deposition which bridges the fins. Finally, a photoresist hard mask is deposited and an additional RIE etch performed to

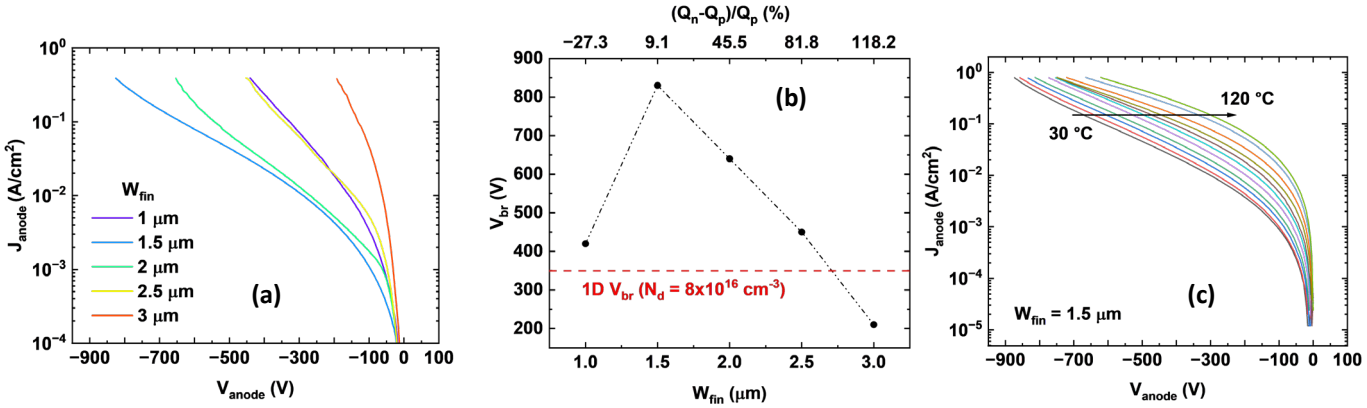

Fig. 3. (a) DC reverse leakage characteristics of the GaN-on-Sapphire SJ as a function of GaN fin width. (b) Breakdown voltage versus GaN fin width and estimated charge imbalance. (c) DC reverse leakage characteristics of the 1.5 µm W_{fin} device at various temperatures from 30 °C to 120 °C.

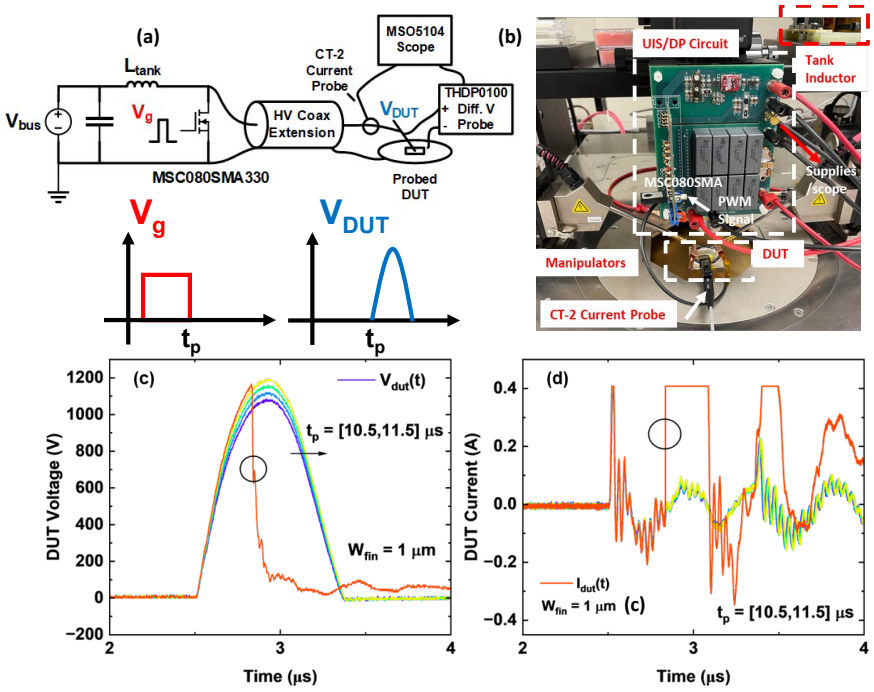

Fig. 4. (a) On-wafer UIS equivalent circuit. (b) Photo of the on-wafer UIS test system. (c) Device voltage waveforms as the inductor charging time (t_p) increases, up to dynamic breakdown. (d) Device current waveforms as the inductor charging time (t_p), up to dynamic breakdown.

expose the n+ GaN layer for cathode formation (Ti/Al/Ni/Au). FIB/SEM measurements (Fig. 2(b-c)) of the NiO film thickness after deposition show that the resulting NiO film thickness is non-uniform across the fin sidewall (80-100 nm at the top of the fin to 40 nm at ~2.5 um below the top of the fin, and 80 nm at the bottom of the trench separating the fins).

III. Static and Dynamic Breakdown

A. DC Characteristics

Fig. 3 presents the DC reverse and breakdown characteristics of the fabricated GaN-on-Sapphire SJ devices. Fig 3(a) shows the reverse leakage as a function of GaN fin width (W_{fin}) up to destructive breakdown. A maximum V_{br} is reached for a W_{fin} of 1.5 µm. The breakdown voltage as a function of W_{fin} and calculated charge imbalance based on the measured NiO doping and film thickness (using an averaged film thickness) are shown in Fig. 3(b). The V_{br} is found to vary significantly with charge imbalance, with a maximum DC breakdown voltage of 840 V achieved at an estimated charge imbalance of 9.1%. The measured V_{br} exceeds the expected 1-D breakdown voltage limit of 350 V given the magnitude of the drift region doping. Fig. 3(c) shows the temperature dependence of the reverse leakage of this device from 25 °C to 125 °C.

B. Dynamic Breakdown Performance

As the DC breakdown of GaN-on-Sapphire device could be limited by leakage current, we further characterize the dynamic breakdown performance, which unveils the true V_{br} under dynamic switching [15], [16]. A novel on-wafer UIS circuit was designed to perform this test [17]. Fig. 3(a) and 3(b) show the equivalent circuit and photograph of the on-wafer UIS testing system. The principle of this UIS test is illustrated in [15], [18]. A SiC MOSFET is used to charge a tank inductor, which then forms a resonant circuit with the capacitance of the MOSFET and DUT to give a sinusoidal voltage pulse across the on-wafer diode once the MOSFET is switched off. Variable tank inductance of 47 mH and 258 µH were used to examine the effect of variable reverse bias slew rate on the dynamic breakdown performance of the SJ diodes. Dynamic breakdown in the tested devices was monitored via a high voltage differential voltage probe connected in parallel with the device along with a CT-2 current transformer in series. The peak voltage can be controlled by the charging time of the inductor (t_p). Fig. 4(c) and (d) give an example of diode voltage and current waveforms under the increased t_p up to the dynamic breakdown in a device with a 1 µm fin width.

Figs. 5(a) and (b) demonstrate the dynamic breakdown performance of GaN-on-Sapphire SJ diodes as a function of W_{fin} with variable tank inductance (258 µH and 47 mH). The chosen values of tank inductance correspond to effective voltage slew rates of 200 V/µs (47 mH) and 2000 V/µs (258 µH). The dynamic breakdown as a function of W_{fin} is plotted versus the DC breakdown for measurements with both tank inductors in Fig. 5(c). In general, the dynamic breakdown performance exceeds the DC breakdown performance for tests with both tank inductances, with a maximum dynamic breakdown of 1160 V for a fin width of 1 um for tests with 2000 V/µs voltage slew rate. Dynamic breakdown voltage for tests with slew rates of 200 V/µs (47 mH) show a weaker dependence on fin width in comparison with DC breakdown. In contrast, dynamic breakdown in measurements of devices under

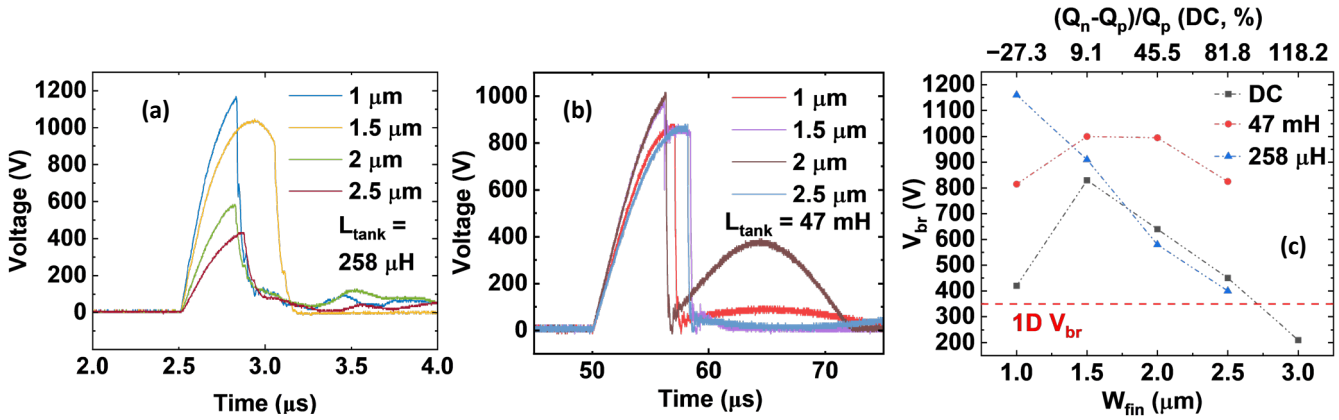

Fig. 5. (a) Device voltage waveforms at dynamic breakdown versus fin width, L_{tank} = 258 µH. (b) Device voltage waveforms at dynamic breakdown versus fin width, L_{tank} = 47 mH.(c) Comparison of dynamic, DC breakdown voltage variation versus fin width.

conditions with slew rates of 2000 V/µs show a sharp deviation from the fin width dependence of the DC V_{br}. This behavior may be explained by the deep first ionization energy of the V_{Ni} acceptor in NiO [19], which would result in a time-dependent deviation of charge balance in the SJ structure as some acceptor states remain filled during the pulse, changing the effective doping of the NiO [20] under very short pulses.

IV. Conclusions

In this work, a quasi-vertical GaN-on-Sapphire SJ PN diode is demonstrated via sputter deposition of NiO on RIE etched GaN fins to form the SJ structure. The DC breakdown performance of these diodes exceeds the 1-D limit by 600 V and demonstrates an expected variation of breakdown voltage with charge imbalance due to fin width variation. The dynamic performance of the fabricated SJ structures is examined using a novel on-wafer UIS test circuit and found to exceed the DC performance, with a maximum dynamic breakdown of 1160V under voltage slew rate conditions of 2000 V/µs.

Acknowledgments

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