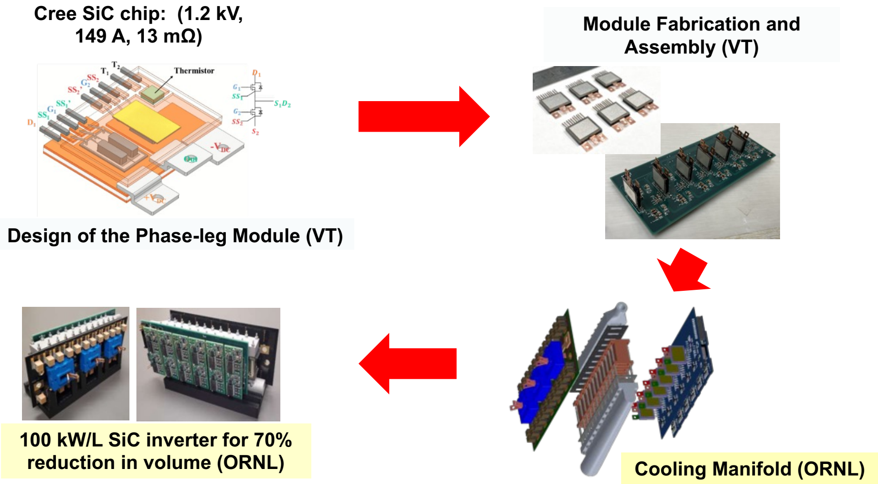
Virginia Tech Silicon Carbide Module Packaging Project
Final Technical Report



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PROJECT TITLE: Heterogeneous Integration Technologies for High-temperature, High-density, Low-profile Power Modules of Wide Bandgap Devices in Electric Drive Applications

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Disclaimer:

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Executive Summary

The goal of this project is to develop packaging technologies for making high-temperature, high-density, and low-profile wide-bandgap (WBG) power electronics modules for electric drives. These modules are aimed at enabling the DOE's University Consortium to reach its 2025 inverter targets of $\geq$ 100 kW/L and $\leq$ 2.7 \$/kW. The specific objectives are to: design and fabricate SiC half-bridge power modules with double-sided cooling and parasitic inductances < 5 nH, heat flux density > 400 W/cm^2, and working junction temperature of 200^{o}C; design, fabricate, and deliver a gate driver with double-sided cooled modules for the construction of a 100 kW/L inverter at Oak Ridge National Lab; and design and prototype intelligent gate drivers with integrated current sensor and a low-profile DC-DC power supply with air-core transformer for testing power modules at 200^{o}C junction temperature.

We followed an iterative technical approach of design, simulation, fabrication, and testing of various versions of modules, current sensors, and power supply. The state-of-the-art silicon carbide devices rated at 1.2 kV and 149 A were packaged by sintered-silver bonding on an aluminum nitride direct-bond-copper substrate for high thermal conductivity, high working temperature, and high joint reliability. Porous silver posts were used to interconnect the device's source pads to the other direct-bond-copper substrate for low mechanical stresses, ease of manufacturing, and double-sided cooling. A current sensor based on package parasitic inductance was developed to measure switching current. A dynamic feedback scheme was developed to compensate the effect of parasitic resistance and temperature variation. A constant-current class-E dc-dc converter with air-core transformer was developed. Air-core transformer was used due to the unavailability of magnetic core at high temperatures. Gate driver and power supply were integrated with the double-side cooled, high temperature SiC power modules for testing the modules at 200^{o}C junction temperature. Double-pulse and continuous testing of the integrated technologies validated the design and fabrication of the three component technologies. Throughout the project, we overcame the challenge for design verification caused by low prototyping yield, which then helped train the graduate students, the future workforce, to learn the engineering know-how for low-cost manufacturing of reliable products. Below is a summary of the major accomplishments of this project:

- development of a prototyping process for fabricating double-side cooled (1200 V, 149 A) SiC phase-leg modules capable of working to 200^{o}C $T_{j;}$
- simulation and experimental verification of the improvement of thermo-mechanical reliability of the double-side cooled SiC phase-leg module by using rigid encapsulant;
- design and experimental validation of a current sensor based on package parasitic inductance and a compensation solution for eliminating the effect of parasitic resistance;
- design and experimental validation of a low-profile power supply with six-output air-core transformer for gate driver;
- functional demonstration of a SiC phase-leg module integrated with its gate driver, current sensor, and an air-core power supply at 200^{o}C T_j in a double-pulse switching test setup and Buck converter continuous test setup;
- successful completion of six PhD and two MS students who are or will work at Apple Inc., Tesla Inc., Wolfspeed Inc., Microchip Inc., Monolithic Power Systems Inc., and LG Magna Inc.

I. ACTIVITIES AND ACCOMPLISHMENTS

1. Goal, Objectives, and Challenges

The goal of this project is to research, develop, and evaluate the integration and packaging technologies for making high-temperature, high-density, and low-profile wide-bandgap (WBG) power electronics modules. These modules are aimed at enabling the DOE VTO Electrification Technologies' University Consortium to reach its 2025 targets (listed below) for the cost, power density, and system peak power rating of automotive electric drive systems.

Table I. Power Electronics Requirements

Parameters	Measure
Cost ($/kW)	≤ 2.7
Power Density (kW/L)	≥ 100
System Peak Power Rating (kW)	100

The overall objectives of this project are to:

- develop a low-cost sintered-silver interconnect technology for packaging power modules and gate drivers capable of working at 200 °C junction temperature;
- develop designs and fabrication processes of 3D, planar power modules with parasitic inductances < 5 nH, heat flux density > 400 W/cm^2, and working junction temperature of 200 °C; and
- design and prototype intelligent gate drivers with integrated current sensor and protection for the modules.

A schematic of the hardware to be developed in this project is shown in Fig. 1. Phase-leg modules capable of working at 200 °C (Tj) are designed and fabricated. Six of the phase-leg modules are assembled with a bus bar, gate-driver board, and a liquid-cooling manifold for double-sided cooling. The gate driver boards have integrated current sensors, a class-E power supply, and other components that can work at 70 °C ambient.

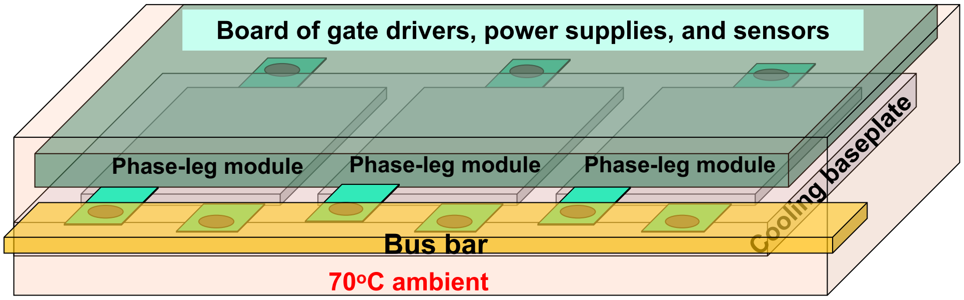


Fig. 1: Schematic of the hardware to be developed in this project.

We followed an iterative approach for the design, simulation, fabrication, and testing of various versions of modules, current sensors, and power supplies. This approach helped mitigate the challenges faced during design verification due to low prototyping yield. Additionally, continuous efforts to improve prototyping yield provided graduate students with valuable experience in debugging various engineering problems and learning essential skills for low-cost manufacturing of reliable products.

2. Project Activities and Accomplishments:

2.1.Prototyping of SiC Phase-Leg Modules for 100 kW/L Traction Inverter

2.1.1 Fabrication Approach and Delivery

The objective of this task is to package the 1.2kV, 149A 3rd Gen Cree SiC MOSFET devices in double-side cooled phase-leg modules for ORNL's 100 kW/L traction inverter. The fabrication approach involved silver sintering for die attachment and porous silver inter-posts for source-pad connection. Improvements on the fabrication process were developed to realize high yield and high precision. DBC substrates were first singulated from a large mastercard by dicing and then etching. An aluminum fixture was designed and machined to fix the power tabs and gate-driver pins during soldering on the module's DBC substrates. These process improvements increased the fabrication yield to more than 90%, and as a result, six additional power modules, shown in Fig. 2, were successfully fabricated for the project. Each of the modules was tested on a curve tracer, verifying that each could block 1.2 kV and had an on-resistance less than 17 mΩ, which is within the range specified in the device datasheet.

Fig. 2. Six additional double-side cooled SiC phase-leg modules for ORNL's 100 kW/L traction inverter.

After module fabrication, all six were soldered on the motherboard of the gate-driver circuit. See Fig. 3. Then, the assembly was screwed to a 3D-printed mockup busbar for delivery to ORNL team.

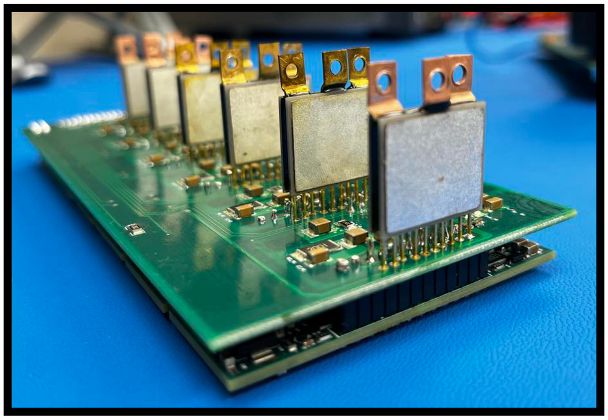
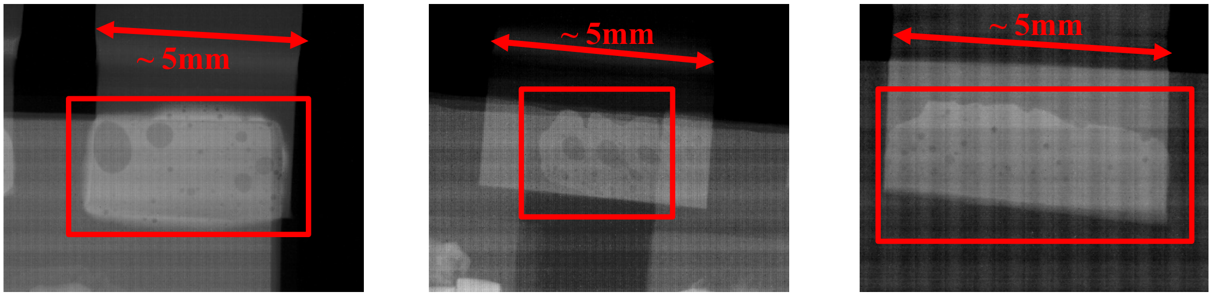


Fig. 3. Gate-driver motherboard with the six SiC phase-leg modules soldered on

Five additional phase-leg modules were fabricated to serve as redundant units to the original six modules delivered for the traction inverter. These backup modules were identical to the prior six, using the same sintered silver die attachment, porous silver interposers, and soldering fixtures during fabrication. These were also tested on a curve tracer to ensure the ability to block up to 1.2 kV and an on-resistance of under 17 mΩ.

These initial modules were fabricated using Sn 10/Pb 88/Ag 2 solder paste to bond the gate-driver pins and power tabs to the DBC substrates. This solder was chosen for its high melting point, ~300°C, to prevent undesired reflow during subsequent high-temperature processing steps. However, testing and observation showed that bonds within the modules formed with this solder contain significant voids, which could lead to higher electrical resistance and reduced mechanical strength in the bonds. Therefore, two alternative solder pastes, Sn 96.3/ Ag 3.7 and Sn 63/ Pb 37, were tested as candidates to replace the Sn 10/Pb 88/Ag 2. The reflow temperatures of these alternatives is lower than subsequent processing temperatures in module fabrication; therefore, a method of "pre-encapsulation" of the soldered bonds was tested. LORD ME-531 (the same epoxy used to encapsulate the module interior) was used to seal in the solder and hold the components in place during final sintering.

To compare the relative quality of the bonds formed by each solder, two additional phase- leg modules were fabricated, one for testing Sn 96.3/ Ag 3.7 solder and one for Sn 62/ Pb 27 solder. These, along with several test samples and an existing backup module using the Sn 10/ Pb88/ Ag 2 solder, were inspected with transmission X-ray imaging. The images of the power tab bonds, showing in Fig. 4, demonstrate moderate voiding in the Sn 10/ Pb88/ Ag2 bonds, substantial voiding and beading in the Sn 96.3/ Ag 3.7 bonds, and good coverage with low voiding in the Sn 63/ Pb 27 bonds.

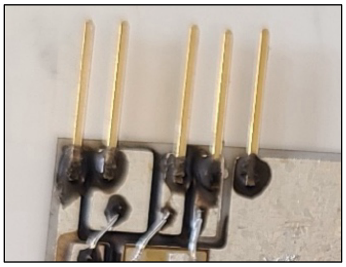


(a) (b) (c)

Fig. 4. Transmission X-ray images of test bonds using (a) Sn 10/Pb 88/ Ag2 (b) Sn 96.3/ Ag 3.7 and (c) Sn 63/ Pb 37. Lighter regions represent bonded areas, while darker regions represent voids or unbonded areas.

For the gold-plated gate driver pins, X-ray transmission revealed poor-quality bonds on test samples using any of the three solder pastes being evaluated (Sn 10/Pb 88/ Ag2, Sn 63/ Pb 37, and Sn 96.3/ Ag 3.7). Therefore, tests were conducted to determine the practicality of bonding the pins with nano-silver sinter paste. It was found that if the pins were sintered at 250° C under ~33 MPa of pressure, the resulting bond was electrically sound and provided decent mechanical strength; however, they were relatively brittle compared to the expected strength of solder bonds. To prevent breakage during the fabrication steps following the pin attach, the bonds were reinforced with beads of ME-531 underfill epoxy immediately after sintering, shown in Fig. 5.

Fig. 5. Pins bonded to a module substrate with nano-silver sinter paste and reinforced with underfill epoxy.



To ensure reliable and even sintering pressure on the pins for module fabrication, a two-part aluminum alignment fixture was designed. Trenches in the fixture hold the pins perpendicular to the front edges of the two substrates, while a recessed block rests on the inner ends of the pins, slotting into the fixture to provide even mechanical contact on all ten pins at once. During sintering, force is applied to the center of the block from above, which is transferred equally across each pin bond; see Fig. 6.

(a) (b)

Fig. 6. (a) CAD illustration of pin attach fixture showing pressure block placement; and (b) Aluminum pin attach fixture.

The initial set of phase-leg modules for this project were fabricated on direct-bonded copper (DBC) substrates with either Al_2O_3 or AlN ceramic cores. Later, new active metal brazed (AMB) substrates with Si_3N_4 cores were obtained for evaluation, including a set pre-patterned for a module layout identical to those previously delivered to ORNL. A full set of six new modules built with these substrates were fabricated for testing in ORNL's segmented traction inverter, shown in Fig. 7(a). Because the Si_3N_4 layer of the AMB substrates is half the thickness of the ceramic in the DBC substrates, spacers cut from sheet silver were sintered between the porous silver inter-posts and the pads on the corresponding substrate, such that the new modules would retain the same overall thickness as the previous iterations. An example is shown in Fig. 7(b).

(a) (b)

Fig. 7. (a) The completed set of Si_3N_4 phase-leg modules; and (b) An AMB substrate with the 1.2 kV SiC MOSFET and sheet silver spacer sintered in place.

2.1.2 *Improving Module Reliability by Using Rigid Encapsulant (Simulation and Experiment)*

Parametric simulations were conducted to evaluate the accumulated irreversible deformation of sintered silver bonds, in the form of plastic strain per cycle of the three bonds in modules with a generic DSC module layout, described in Fig. 8. The simulation was done under JESD22-A104-B temperature cycling conditions.

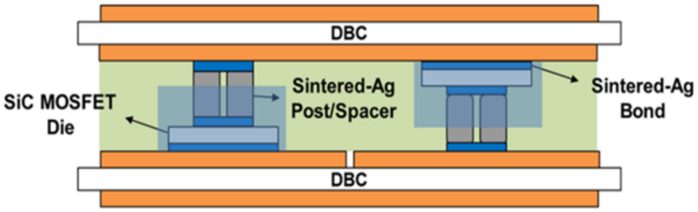
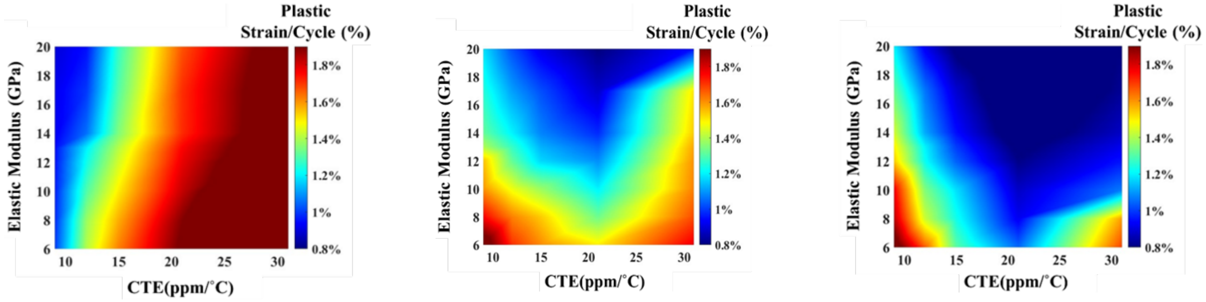


Fig. 8. Cross-sectional schematic of module Layout 2.5.

Fig. 9 is a summary of the finite element analysis (FEA) simulations showcasing the plastic strain per cycle for each bonded interface pair inside the module with different ranges of encapsulant properties. The results suggest that for the chip bond, shown in Fig. 9(a), increasing the encapsulant's modulus reduces the plastic strain per cycle, but increasing its CTE increases the strain. Fig. 9 (b) and Fig. 9(c) are the plots for the spacer-chip and spacer-substrate bond, respectively. For both interfaces, the strain can be minimized by using an encapsulant with a CTE of around 20 ppm/°C, and at this value, the higher its modulus, the lower the bond's plastic strain. It was found that an encapsulant with its CTE closely matched to the CTE of the metallic spacer or silver bond reduced the accumulated plastic strain at the interface.



(a) (b) (c)

Fig. 9. Plot of the simulated plastic strain at the sintered-silver (a) chip bond, (b) spacer-chip bond, (c) spacer-substrate bond per temperature cycle versus the encapsulants' elastic modulus and coefficient of thermal expansion.

Fig. 10 is a summary of the finite element analysis (FEA) simulations showcasing the SED per cycle for each bonded interface pair with three different commercial encapsulants. These results suggest that encapsulating the module with either of the two rigid encapsulants, ME-531 and EP-2000, can reduce the accumulated deformation inside the bonds, with EP-2000 producing the lowest deformation inside the bonded interfaces in the EDT module.

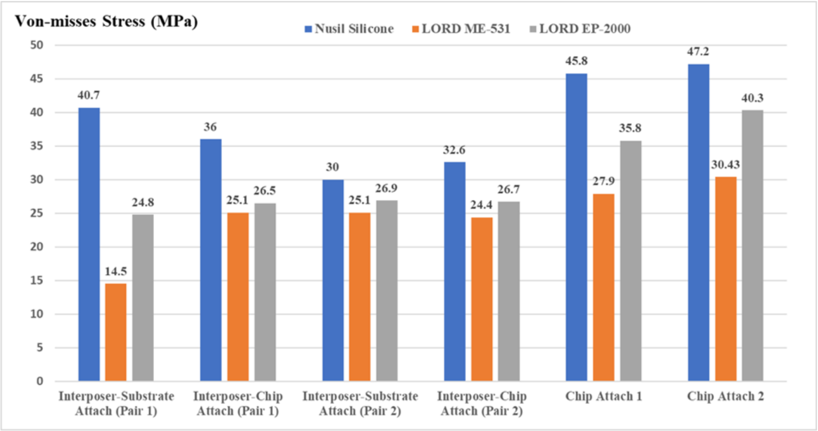


Fig. 10. Plots of the simulated maximum von-misses stresses at the three bonded interfaces in Module Layout 2.5 encapsulated in each of the three polymeric materials.

Following the simulations, a set of simplified DSC modules were fabricated for thermo-mechanical reliability testing. The procedure consisted of three main fabrication steps: chip and spacer-to-substrate silver-sintering, spacer-to-chip silver-sintering (half-piece stacking), and a final power module encapsulation step, as shown in Fig. 11. To ensure the consistency of samples, fixtures and alignment tools were designed and fabricated. The reliability modules were encapsulated with either two different commercially available rigid encapsulants or one soft silicone gel encapsulant, and the packaging lifetime of all three groups were tested and compared via experimental JESD22-A104-B temperature cycling conditions.

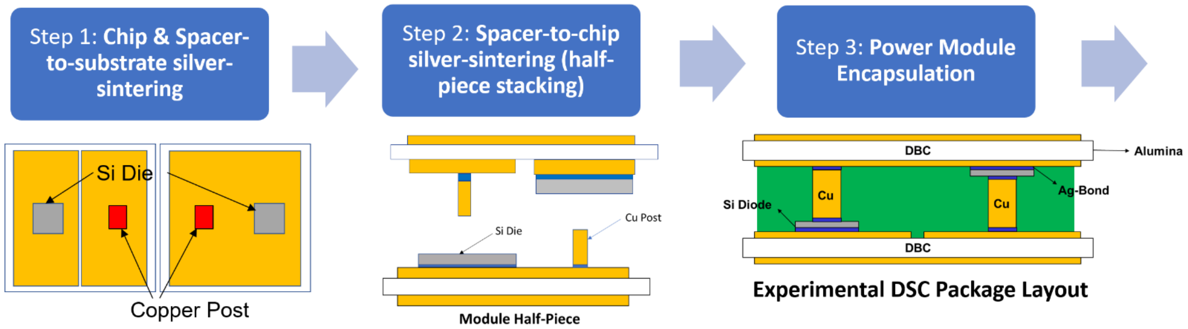


Fig. 11. Schematic of module fabrication procedure for temperature cycling reliability testing

Ten modules were made for each encapsulant. All modules were temperature-cycled between -40°C and 125°C and tested periodically for elevated on-resistances of the connected diodes on a curve tracer. In agreement with the simulations, experimental results indicated that the set of modules encapsulated in EP-2000, the most rigid encapsulant, survived an average of 240 cycles, compared to 150 cycles for ME-531 and 50 cycles for the silicone gel.

2.1.3 *Fabrication and Testing of 200^{o}C-T_j Phase-Leg Modules*

As required for Milestone M2.5, a 1.2 kV double-side cooled phase-leg module was fabricated using a high-temperature encapsulant, EP-2000 from Lord, capable of supporting 200˚C junction temperature. Except the encapsulant, the module, as seen in Fig. 12, has the same layout and was processed in the same way as the modules fabricated for the 100 kW/L inverter.

Fig. 12. EP-2000 encapsulated double-side cooled SiC phase-leg module capable of operating at 200^{o}C junction temperature

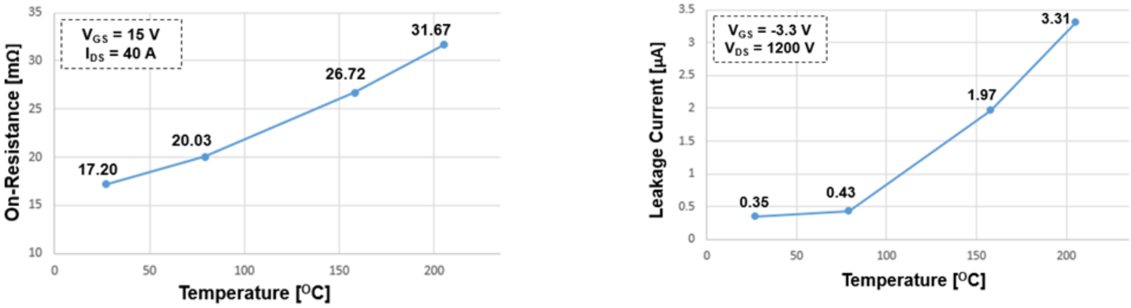
Based on the thermo-mechanical simulations reported previously, the 200°C-module is expected to be more thermomechanically reliable than those which were encapsulated in ME-531, especially at junction temperatures above 175°C. The bond deformation in the EP-2000 encapsulated module is estimated to be about 20% less than for ME-531.

The high-temperature module was tested for electrical performance at elevated temperatures with a test setup as shown in Fig. 13(a) and Fig. 13(b). The module under test was clamped between two copper plates. A resistive heater was inserted in the stack to heat one side of the module, the side that has a thermistor to monitor the module temperature. Only the lower device in the phase-leg, i.e., the one bonded to the same substrate as the thermistor, was tested.

(a) (b)

Fig. 13. (a) Schematic and (b) photo of the experimental setup for electrical testing of high-temperature power module at elevated junction temperatures.

Because the test was performed on a curve tracer, minimal self-heating was assumed, and the device junction temperature was assumed to be the same as the thermistor temperature. The on-resistance and leakage current of the MOSFET were measured at 25°C, 75°C, 150°C, and 200°C. The test data are shown in Fig. 14 (a) and Fig. 14. (b). Both the on-resistance and leakage current increased with junction temperature, which are expected from device physics.



(a) (b)

Fig. 14. (a) Measured on-resistance and (b) leakage current of the lower MOSFET in the phase-leg module versus the junction temperature.

2.2.Development of Current Sensor Based on Parasitic Inductance

High-bandwidth and high-accuracy sampling of device current is critical to the high-performance converter, especially considering the high switching speed of wide-band-gap (WBG) devices. The information of device current can be used for device characterization, short-circuit protection, and load current reconstruction. The conventional shunt resistor produces extra loss, takes extra space and increases the commutation loop inductance. Alternative current sensors like Rogowski coils and current transducers have been proposed but much extra space is required. Also, the parasitic capacitance of coil is the primary reason for the limited bandwidth of these two current sensors.

The parasitic in the power loop of converter is a potential tool to provide the current information of power device with a high bandwidth, high density and low cost. Parasitic resistance and inductance are inherent in all conductive components, including spacers, printed circuit board (PCB) traces, and bonding wires within power devices. No more external current sensor needs to be placed in the original power loops, which saves much cost and space, and the original power stage design is not interfered by the application of current sensor.

Parasitic resistance in the bonding wire of power modules has been used for current reconstruction, with the influence of parasitic inductance mitigated through RC low-pass filters. However, sensitivity to temperature and frequency make the gain of these sensors unfixed over a wide operational range.

Contrastingly, parasitic inductance remains insensitive to temperature and frequency variations, offering a stable gain for current sensors. An RC low-pass filter can capture high-frequency components of device current when applied to the induced voltage across the parasitic inductance, yet it fails to reconstruct low-frequency components, so this configuration is only used for short-circuit protection. Even if the active integrators are employed, distortion persists in the low-frequency component due to parasitic resistance, leaving a gap in the full picture of device current. To eliminate the influence of the parasitic resistance, some circuits with extra components have been proposed. However, the value of the parasitic resistance is difficult to obtain and is sensitive to temperature, so the method proposed is not robust enough and the performance is still not satisfactory. Therefore, two challenges must be solved in the utilization of the parasitic inductance for current sensing. The first challenge is to propose an integrator circuit with the controllable compensation for the parasitic resistance. The second challenge is to deal with the influence of the temperature on the parasitic resistance and its compensation, guaranteeing the correct compensation for any cases and operation conditions.

To address the first challenge, this project presents a novel integrator circuit featuring programmable compensation for parasitic resistance. This programmable compensation effectively eliminates the influence of parasitic resistance across the entire frequency spectrum. Regarding the second challenge of variable resistance, a closed-loop adaptive algorithm that regulates the compensation for parasitic resistance is proposed, accommodating variations in resistance over time. This adaptive compensation eliminates the need to measure the value of parasitic resistance and ensures accurate compensation under varying temperatures, enhancing the robustness of the current sensor.

With our proposed circuit and algorithm, the current sensor developed in this study stands as the first reported sensor capable of real-time, high-accuracy, and high-bandwidth device current reconstruction based on parasitic, while also equipped with robustness to the variable temperature.

2.2.1 Working Principle

The fundamental operation of the current sensor, relying on the parasitic inductance denoted as L, is illustrated in Fig. 15(a). In this configuration, the voltage induced across the parasitic inductance in series with device is integrated. The outcome of the integrator reflects the device current, as depicted in Fig. 15(b). This relationship is mathematically expressed in equation (1),

$$V_{out}=\frac{1}{sR_iC_i}V_i=\frac{1}{sR_iC_i}sLi=\frac{iL}{R_iC_i}, \tag{1}$$

where V_i is the voltage across the parasitic inductance, R_i and C_i are the resistance and capacitance of the integrator, V_{out} is the sensor output. According to (1), the gain of the proposed sensor G is shown in (2).

$$G=\frac{L}{R_iC_i} \tag{2}$$

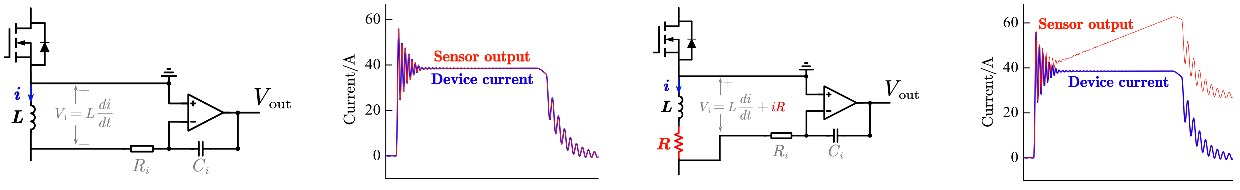
However, the presence of parasitic resistance R in the utilized trace introduces another proportional part in the induced voltage V_i across the trace, as shown in Fig. 15(c). The impact of this parasitic resistance is illustrated in (3), representing the transfer function of the proposed sensor while accounting for parasitic resistance.

$$V_{out}=\frac{V_i}{sR_iC_i}=\frac{i(R+sL)}{sR_iC_i}=\left(\frac{L}{R_iC_i}+\frac{R}{sR_iC_i}\right)i \tag{3}$$

(3) reveals that the parasitic resistance causes a zero in the voltage across the trace and thus adds one integral part to the sensor output compared to the ideal case in Fig. 15(a). As a result, a deviation is noticeable following the rising edge of the device current, as demonstrated in Fig. 15(d). (3) shows that the parasitic resistance causes a zero in the sensor output, therefore, a first-order circuit with one pole should be adopted to cancel the effect the influence of parasitic resistance. An integrator circuit with compensation for parasitic resistance is proposed as shown in Fig. 16(a), where a resistor R_1 is added to cancel the influence of parasitic resistance R. The transfer gain of the sensor with compensation is derived as (4). If the value of R_1 is selected as (5), (4) can be equivalized into (1), where the influence of the parasitic resistance is eliminated, and the sensor works as an ideal proportional amplifier. The bode plot of the current sensor with the proposed integrator circuit with compensation for parasitic resistance is shown in Fig. 17, where the gain is constant within the full frequency range.

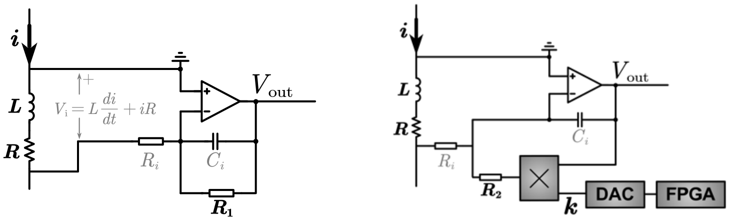
$$\frac{V_{out}}{i}=\frac{sL+R}{sR_iC_i+\frac{R_i}{R_1}} \tag{4}$$

$$R_1=\frac{L}{RC_i} \tag{5}$$



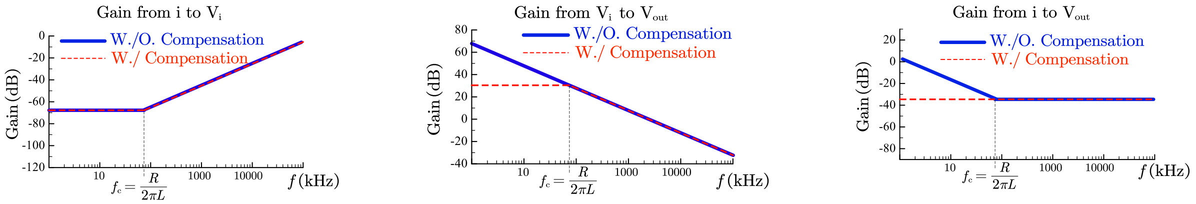
(a) (b) (c) (d)

Fig. 15 The working principle of proposed current sensor (a) Circuit only considering parasitic inductance (b) Waveforms only considering parasitic inductance (c) Circuit considering parasitic resistance (d) Waveforms considering parasitic resistance



(a) (b)

Fig. 16 The proposed integrator circuit with the compensation for parasitic resistance (a) With fixed compensation (b) With programmable compensation



(a) (b) (c)

Fig. 17 The bode plot of the proposed current sensor (a) Gain from device current to induced voltage. (b) Gain of the integrator circuit. (c) Gain from device current to sensor output

Although the influence of parasitic resistance can be canceled with the proposed circuit in Fig. 16(a), a variable and programmable R1 is preferred considering the variation of parasitic resistance due to temperature change, thus the circuit in Fig. 16(b) is proposed to provide a programmable compensation. In Fig. 16(b), a coefficient k is generated by a Field Programmable Gate Array (FPGA) and Digital-to-Analog converter (DAC), which can work together with the compensation resistor R2 to adjust the compensation. With R2 and k, (4) and (5) can be rewritten as (6) and (7), *respectively.*

$$\frac{V_{out}}{i} = \frac{sL + R}{sR_iC_i + \frac{kR_i}{R_2}} \tag{6}$$

$$\frac{R_2}{k} = \frac{L}{RC_i} \tag{7}$$

2.2.2 *Adaptive Compensation for Parasitic Rresistance*

In practical applications, obtaining the precise value of parasitic resistance can be challenging, and its sensitivity to temperature further complicates matters. Therefore, it is necessary to evaluate the influence of incorrect compensation for parasitic resistance and to develop a close-loop adaptive method for adjusting the compensation considering these uncertainties.

Assuming an error ΔR exists between the estimated parasitic resistance R_e used for the compensation and the real parasitic resistance R, as shown in (8).

$$\Delta R = R - R_e \tag{8}$$

With the existence of ΔR, the transfer function of the sensor can be derived as shown in (9).

$$\frac{V_{out}}{i} = \frac{L}{R_iC_i}\left(1 + \frac{\Delta R}{sL + R_e}\right) \tag{9}$$

Thus, the error between the sensor output and the real device current can be expressed as (10).

$$i_{\mathrm{error}} = \frac{\Delta R}{sL + R_e} i \tag{10}$$

In most pulse width modulation (PWM) converters, the device current is in the form of continuous pulses, where the device is turned on at the time of t_{on}, and turned off at the time of t_{off}. In the frequency domain, the pulse current can be expressed as (11).

$$i = \frac{I}{s}\left(e^{-st_{on}} - e^{-st_{off}}\right), \tag{11}$$

where I is the steady-state current. According to (8) and (10), the sensor output with the error ΔR can be derived, as shown in (12). The first part of (12) is the correct output of the sensor and the second part of (12) is the error caused by ΔR.

$$V_{out} = \frac{G \cdot I}{s}\left(e^{-st_{on}} - e^{-st_{off}}\right) + \frac{G \cdot I}{s}\left(e^{-st_{on}} - e^{-st_{off}}\right)\frac{\Delta R}{sL + R_e} \tag{12}$$

Converting (12) to the time domain, the sensor output can be depicted as (13).

$$\begin{aligned} V_{out} = {} & G \cdot I \cdot [u(t - t_{on}) - u(t - t_{off})] \\ & + V_{\mathrm{out\_error1}} + V_{\mathrm{out\_error2}} + V_{\mathrm{out\_error3}} \end{aligned} \tag{13}$$

where u(t) is the step function of unity magnitude. (13) can be broken into four parts. The first part is the correct response of the sensor, as shown in (14). The other three parts listed in (15)-(17) are the errors caused by the error of parasitic resistance ΔR. (15) is the error induced by the rising edge of device current, which is in the exponential form. (16) is the steady-state error, which is proportional to ΔR. (17) is the error corresponding to the falling edge of current.

$$V_{out1} = G \cdot I \cdot [u(t - t_{on}) - u(t - t_{off})] \tag{14}$$

$$V_{\mathrm{out\_error1}} = \frac{-G \cdot I \cdot \Delta R}{R_{\mathrm{e}}} e^{-\frac{R_e}{L}(t - t_{on})} u(t - t_{on}) \tag{15}$$

$$V_{\mathrm{out\_error2}} = \frac{G \cdot I \cdot \Delta R}{R_{\mathrm{e}}} [u(t - t_{on}) - u(t - t_{off})] \tag{16}$$

$$V_{\mathrm{out\_error3}} = \frac{G \cdot I \cdot \Delta R}{R_{\mathrm{e}}} e^{-\frac{R_e}{L}(t - t_{off})} u(t - t_{off}) \tag{17}$$

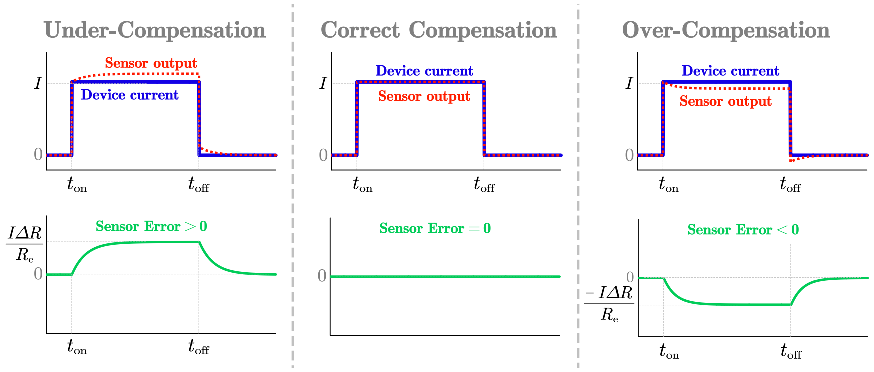
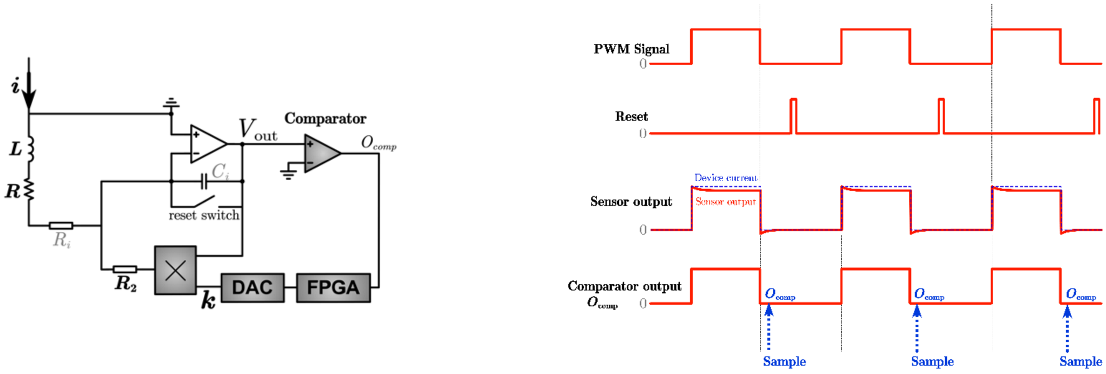


Fig. 18 The sensor output and output error with different polarities of ΔR.

According to (15)-(17), it can be observed that the sensor output error is positively related to the error ΔR and polarity of sensor output error identical to the polarity of ΔR. Therefore, three cases are defined according to the polarity of ΔR: under-compensation (ΔR>0), correct compensation (ΔR=0), and over-compensation (ΔR<0), as shown in Fig. 18. To control the sensor output error to be zero, the output error should be sampled and then the close-loop control can be implemented.

After the device is turned off, the device current is zero and the output error is identical to the sensor output, thus the output error can be detected by sampling the sensor output. A closed-loop algorithm is proposed in this project to achieve automatic and accurate compensation. Fig. 19 provides a detailed illustration of the proposed adaptive compensation algorithm. Fig. 19(a) shows the diagram of the sensor circuit and Fig. 19(b) shows the timing diagram of the proposed close-loop compensation algorithm. The compensation coefficient, denoted as k, is dynamically adjusted by monitoring the polarity of the sensor output after the device is turned off. A comparator is employed to identify the polarity of the sensor output, with a FPGA responsible for modifying the compensation by altering the coefficient k. Specifically, when the comparator output O_{comp} is positive, indicating a case of under-compensation (ΔR is positive), the coefficient k is increased. Conversely, when O_{comp} is negative, signifying over-compensation (ΔR is negative), the coefficient k is decreased. To eliminate the accumulated error of the op-amp caused by the bias current and offset voltage, the integrator should be reset some time after the device is turned off.



(a) (b)

Fig. 19 The circuit and algorithm of current sensor with adaptive compensation for parasitic resistance. (a) Circuit of the sensor with adaptive compensation (b) The timing diagram of the adaptive compensation algorithm.

A current sensor based on the proposed circuit and algorithm is designed. A simulation using a Buck converter is performed to validate both the proposed circuit and algorithm. For current reconstruction, a stray inductance of 0.9 nH is incorporated in series with the lower switch S2, as depicted in Fig. 20. The real parasitic resistance is 0.45 mΩ and the corresponding coefficient k should be 1. The dynamic process of automatic compensation adjustment is illustrated in Fig. 21. Initially, the coefficient k is set to 0.7, leading to a current sensor error due to under-compensation. At time t_1, the adaptive compensation mechanism is triggered. Subsequently, the compensation converges gradually to the correct value, ultimately eliminating the error in the sensor output.

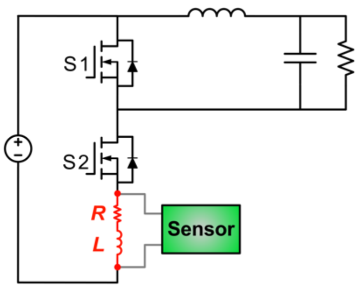


Fig. 20 Buck converter in simulation

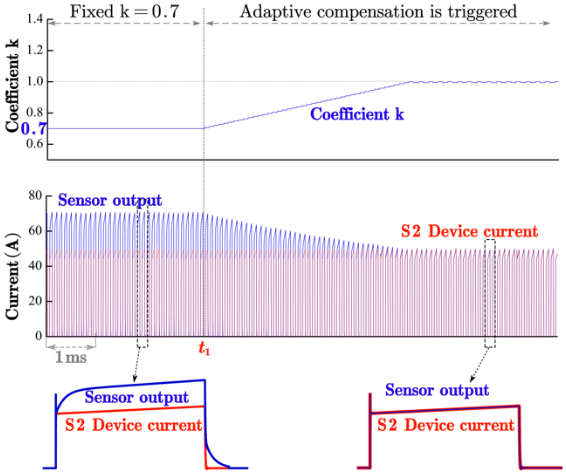
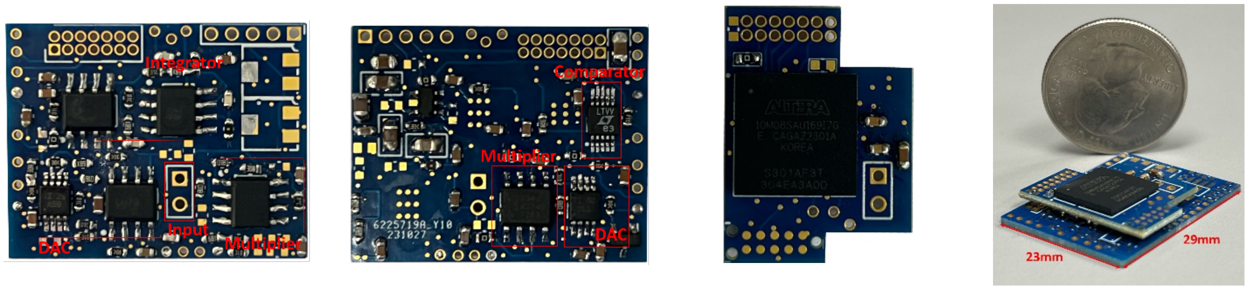


Fig. 21 Waveforms in the simulation: dynamic process of adaptive compensation adjustment.

2.2.3 *Experimental Results*

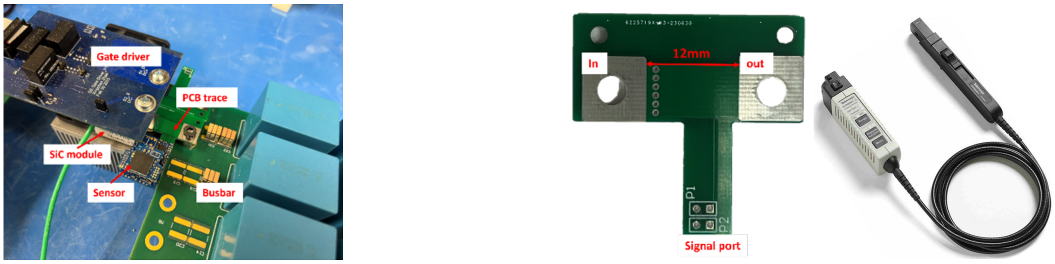
The hardware implementation of the proposed current sensor based on parasitic inductance is presented in Fig. 22. It comprises two stacked boards: an FPGA controller and an integrator with compensation. The compact and low-profile design of this sensor contributes to an increased density in the converter system. A SiC-based Buck converter is used to verify the performance of the proposed current sensor. The test set-up is shown in Fig. 23(a).

The parasitic inductance of the trace in the PCB busbar is used to reconstruct the current of the lower device S2. The commercial current probe TCP0030A with a bandwidth of 120 MHz is adopted to measure the device current and provide a reference for the results. To fit the PCB trace into the probe TCP0030A, a separated PCB trace of busbar is placed in series with the lower device S2, as shown in Fig. 23(b), and the parasitic inductance of the separated PCB trace is only 0.9 nH. It should be noted that the separated PCB trace is only for the convenience of measurement, and no extra trace is needed for the current sensing in the real applications. The parasitic inductances of the existing components or traces are enough for the proposed current sensor.



(a) (b) (c) (d)

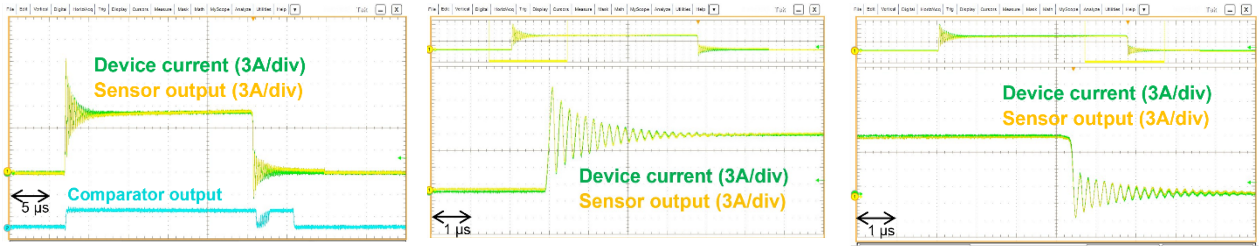
Fig. 22 Designed current sensor (a) Top view of integrator board (b) Bottom view of integrator board (c) FPGA board (d) Assembled current sensor



(a) (b)

Fig. 23. The test set-up with a SiC-based Buck converter. (a) SiC-based Buck converter. (b) Separated PCB trace of dc busbar (0.9 nH) and the commercial probe TCP0030A.

Fig. 24 (a) displays waveforms obtained with adaptive closed-loop compensation. The sensor output closely aligns with the current measurements captured by a commercial current probe TCP0030A, with a bandwidth of 120 MHz. Additionally, Fig. 24(b) and (c) demonstrate the capability of the proposed current sensor to accurately capture even the high-frequency oscillations during switching transients, which indicate that the proposed sensor features an ultra-high bandwidth.



(a) (b) (c)

Fig. 24 The waveforms of the current sensor (a) Sensor output in one switching cycle (b) Turn-on transient (c) Turn-off transient.

2.3.Development of Planar Gate Driver Power Supply

To better integrate the power supply with the power module and for potential high-temperature applications in the future, two planar power supplies with PCB based air-core transformers and inductors are designed and tested. The first power supply integrates one primary winding and six isolated secondary windings on a single PCB with 2 W maximum power delivered to each secondary output. During the design process, two winding structures are compared to maximize the coupling between the primary and secondary windings; physical dimensions are swept to minimize the coupling capacitance and winding loss. The designed power supply is verified in its performance on efficiency, thermal, output voltage accuracy and consistency, load transient, and under different ambient temperatures. The second power supply integrates one primary winding and two isolated secondary windings on a single PCB with 5 W maximum power delivered to each secondary output. Similar design process was taken to maximize the efficiency. The design was verified by integrating the power supply with gate driver and power module, and conducting a continuous buck test with 200°C junction temperature.

2.3.1 Design and Fabrication of the Air-Core Transformer

The three-phase inverter is composed of six devices in total. This requires the power supply to provide six isolated outputs with the same output voltage. One option is to have six power supplies with a single output. This requires a large footprint and six times the number of components. A better solution is to redesign the power supply to have six secondary windings and one primary winding.

Fig. 26 shows the schematics of the proposed power supply. Regarding the structure of the primary winding, two configurations are compared. Fig. 26 shows the lay-up of the proposed transformer structure. Fig. 27 shows the transformer structures with different primary winding configurations. Two transformers were designed with 300-nH mutual inductance. The split-winding structure achieved 45% less winding loss and a 70% reduction of the voltage stress on the primary windings.

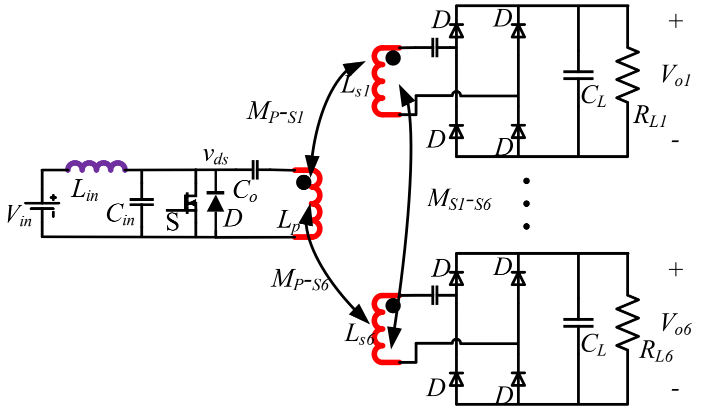
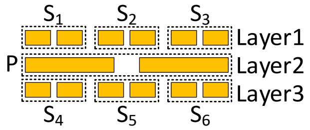


Fig. 25. Schematics of the class-e power supply with six secondary windings.



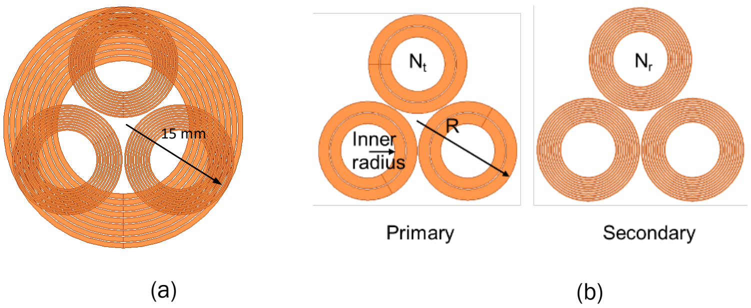
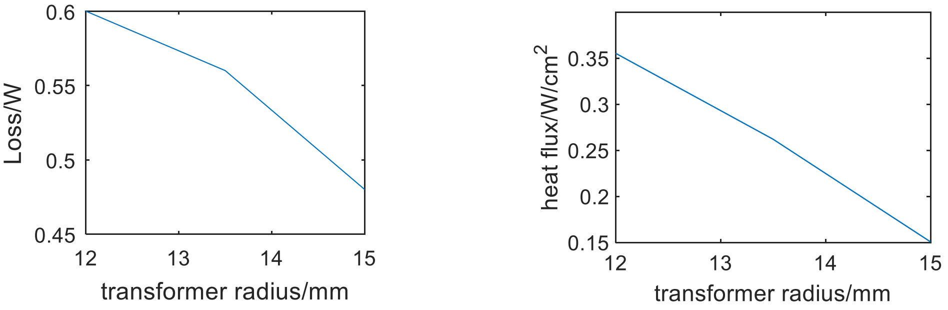


Fig. 26. Lay-up of the proposed transformer structure.

Fig. 27. Two primary winding configurations. (a) Single primary winding with large size. (b) Three small primary windings in series. Structure (b) achieved 45% less winding loss and a 70% reduction of the voltage stress on the primary windings.

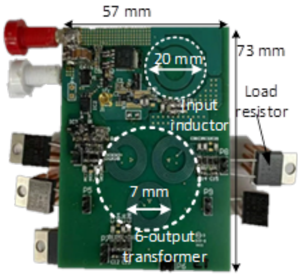
The transformer in Fig. 27(b) was further improved by applying two-layer windings for the primary and secondary. The double-layer winding structure enables wider windings for the secondary with a 10% loss reduction. A smaller transformer size can be used under the minimum trace-width requirement from the manufacture. Transformer size was then swept to study the loss variation. Fig. 28 shows the loss and heat flux variation with different transformer outer radius. For each transformer size, parameters in Fig. 27 (b) were swept to get the minimum loss. The isolation capacitance decreases by 32% from 15 mm to 12 mm with a 25% loss increase.



(a) (b)

Fig. 28. Loss and heat flux variation with transformer size. (a) Loss variation. (b) heat flux variation.

Fig. 29 shows the schematics and the hardware of the six-output power supply. Both the input inductor and 6-output transformer are designed with PCB winding and without any magnetic core. Power resistors are used as the load.



Part	Value	Manufacturer
S	EPC2214	EPC
Driver	UCC27611	Tex. Ins.
C_{in}	470 pF+220 pF, NP0	Yageo
C_t	470 pF+100 pF ×2, NP0	Yageo
C_s	220 pF+100 pF, NP0	Yageo
Oscillator	SIT8918AA-32-33E-6.780000	SiTime
Shunt regulator	TL431	Tex. Ins.
LDO	TPS7B8733QDDARQ1	Tex. Ins.
AND Logic	MC74VHC1GT08DBVT1G	Onsemi
Photocoupler	RV1S9160ACCSP-100V	Renesas

Fig. 29. Hardware and Bill of materials of the six-output power supply.

2.3.2 *Measurement and Performance*

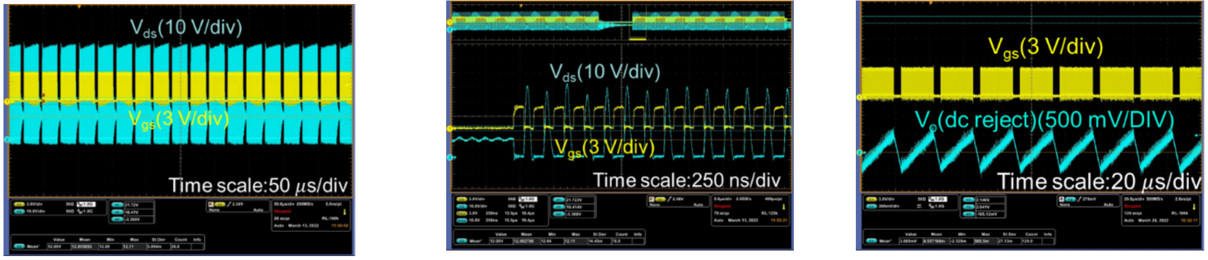
Fig. 25 shows the inductances to be measured, including the input inductance, the self-inductances, and mutual inductances of the transformer windings. An accurate inductance measurement will ensure proper capacitor compensation. Table II summarizes the measurement results compared with the Q3D simulation. It can be seen that the measured inductances match very well with the simulation.

Table II. Inductance measurement results

Parameters	Description	Simulated	Measured	Error
L_{in}	Input inductance	162 nH	163 nH	0.6%
L_P	Primary self-inductance	488 nH	532 nH	9%
L_{S1}	Secondary self-inductance	1.2 μH	1.286 μH	7.2%
$M_{P\text{-}S1}$	Primary-Secondary mutual inductance	273 nH	303 nH	11%
$M_{S1\text{-}S4}$	Secondary-Secondary mutual inductance	550 nH	601 nH	11%

2.3.2.1 Performance of the Power Supply with Load Resistor

The power supply was tested with the load resistor shown in Fig. 29. Fig. 30 shows the waveforms with output voltage regulation at 12 W. The output voltage is 20 V. The load resistance is 200 Ω for each output. On-off control is used with an upper limit of 19.6 V and a lower limit of 19 V. The average output voltages of the six outputs are shown in Table III. From the transient waveforms in Fig. 30 (b), the transient time for each on period is about 8 switching cycles. ZVS is observed from the steady-state waveforms. The ac component of V_o shows the ripple is as expected.



(a) (b) (c)

Fig. 30. Testing waveforms at 12 W output power. (a) Waveforms of V_{ds} and V_{gs}. (b) V_{ds} waveforms during on transient. (c) AC component of the output voltage.

Table III. Summary of the output voltages and efficiency

Vo1	Vo2	Vo3	Vo4	Vo5	Vo6	Pin	Efficiency
19.3 V	19.6 V	19.3 V	19.6 V	19.6 V	19.6 V	13.6 W	84%

2.3.2.2 Performance of the Power Supply at Different Ambient Temperatures

The high-temperature testing was conducted by placing the PCB in the environment chamber by Tenney. Fig. 31 shows the testing setup in the environment chamber. The temperature in the chamber varied from 25℃ to 72℃. Fig. 32 shows the efficiency at different temperatures. Fig. 33 shows the waveforms at 72℃. ZVS was maintained.

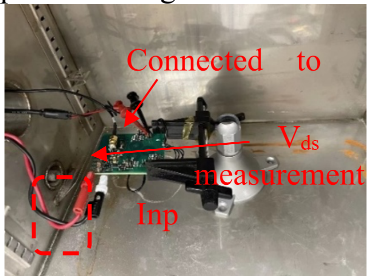


Fig. 31. Test setup in the environment chamber.

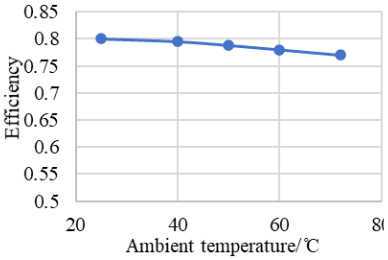


Fig. 32. Efficiency at different ambient temperatures.

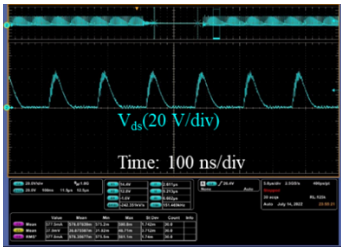


Fig. 33. Zoomed waveforms of V during steady state.

2.3.2.3 Performance of the Power Supply with Gate Driver and Power Module

The testing is to justify that the power supply provides the right voltage and enough power to drive the power module. Fig. 34 shows the test setup. The six outputs are paralleled as a single output and connected with the power input of the gate drivers on the daughter board. The power module is plugged under the motherboard. The PWM signals come from the function generator. The gate output is measured with the oscilloscope. Fig. 35 shows the measured two gate waveforms at 40 kHz switching frequency. The gate output voltage satisfies the requirement of the power module as +15V/-4V. The output power for the two gates is 1.6 W. Therefore, the rated 12 W output of the power supply is enough for six gate drivers.

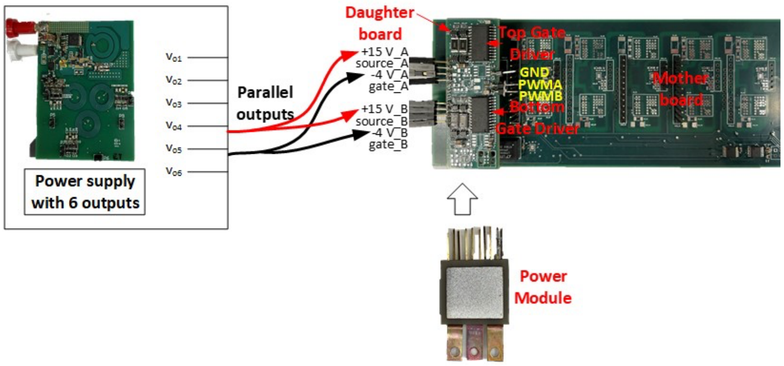


Fig. 34. Hardware setup for the testing with gate driver and power module.

Fig. 35. Gate waveforms of one power module at 40 kHz.

2.3.2.4 Load Transient Performance of the Power Supply

Load transient of the power supply happens when the inverter switch between standby and normal operation modes. Therefore, the purpose of the test is to evaluate the converter's performance under load step-up and step-down. The test setup is shown in Fig. 36.

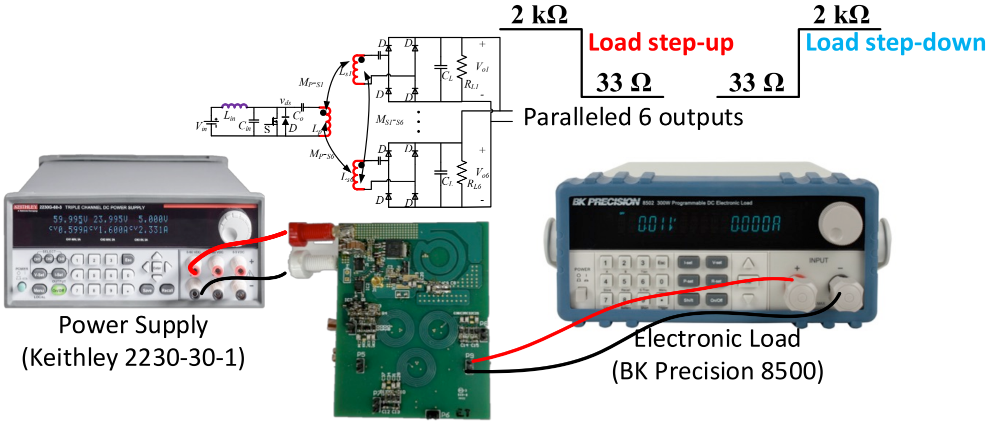
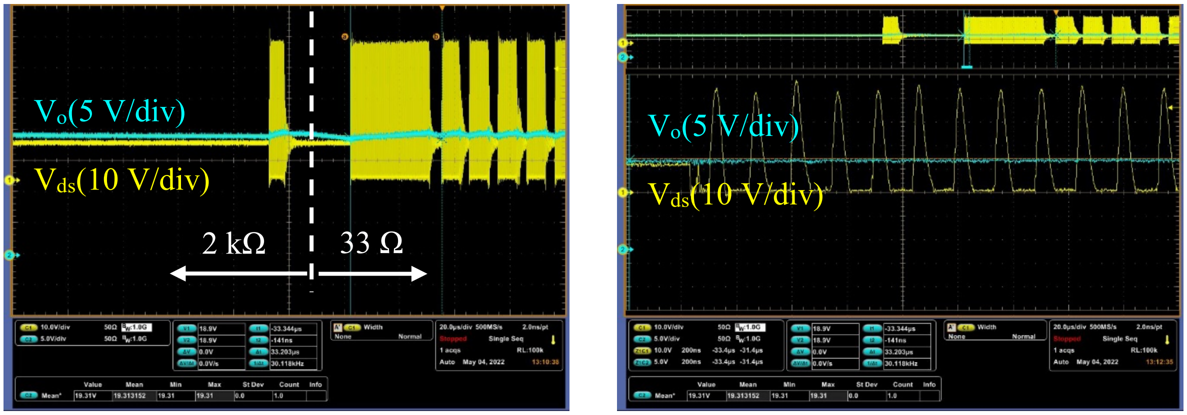


Fig. 36. Test setup for load transient evaluation.

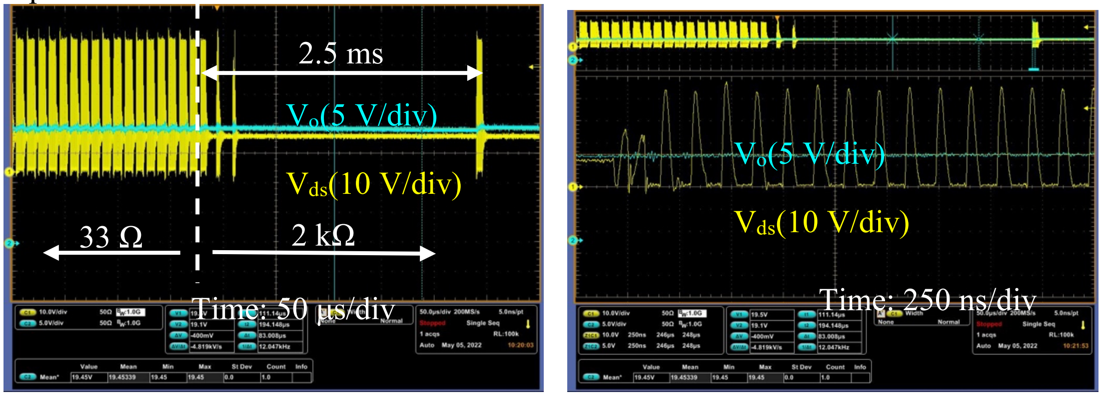
As Fig. 36 shows, the load step-up/down is performed with load resistance step-down/up with the electronic load. Fig. 37(a) shows the whole process of load step-up. Fig. 37(b) shows the zoomed-in waveforms of the first few pulses right after the load step-up. There's no significant output voltage undershoot. Steady-state v_{ds} waveforms start at the 8th pulse after the load step-up.



(a)waveforms of the whole process (b) zoomed in waveforms for the transient

Fig. 37. Testing waveforms of load step-up from 2 kΩ to 33 Ω.

Fig. 38(a) shows the whole process of load step-down. No significant voltage overshoot is observed. It takes about 2.5 ms until a normal on-period. Fig. 38(b) shows the zoomed-in waveforms of the first few pulses of this period. Steady-state v_{ds} waveforms start at the 9th pulse after the load step-up.

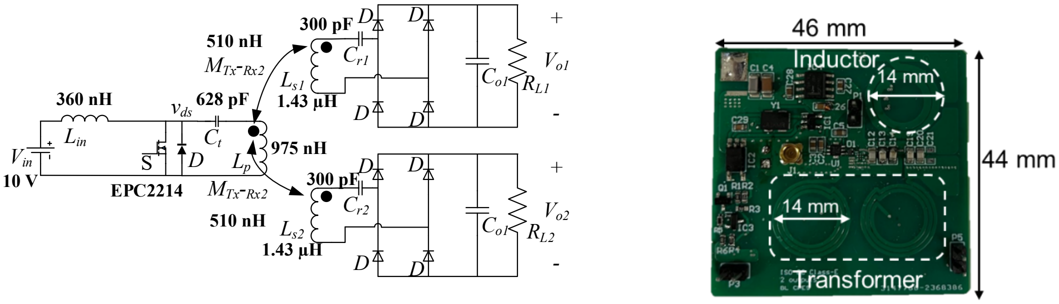


(a)waveforms of the whole process (b) zoomed in waveforms for the transient

Fig. 38. Testing waveforms of load step-down from 33 Ω to 2 kΩ.

2.3.3 *Design and Performance of the Dual-Output Power Supply*

A two-output Class-E dc-dc converter was fabricated. Fig. 39 shows the schematics and the hardware. Both the input inductor and two-output transformer are designed with PCB winding and without any magnetic core.



(a) (b)

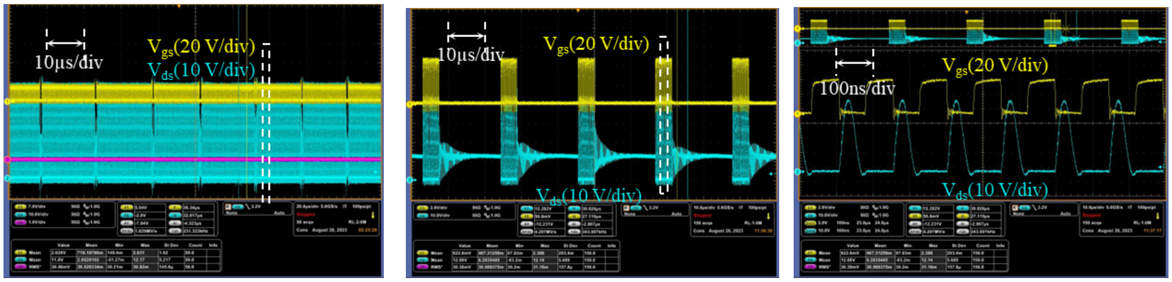
Fig. 39. The schematics and hardware of the two-output Class-E gate power supply.

Table IV summarizes the measurement results of the inductances compared with the Q3D simulation. It can be seen that the measured inductances match very well with the simulation.

Table IV. Inductance measurement results.

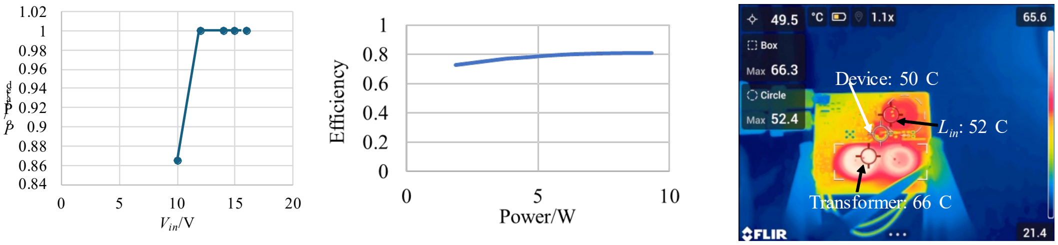
Parameters	**Description**	**Simulated**	**Measured**	**Error**
L_{in}	Input inductance	360 nH	335 nH	7%
L_P	Primary self-inductance	975 nH	1060 nH	9%
L_{S1}	Secondary self-inductance	1.43 μH	1.47 μH	3%
$M_{P\text{-}S1}$	Primary-Secondary mutual inductance	510 nH	500 nH	2%

The power supply was first tested with the load resistors to verify its function. Fig. 40 shows the gate and v_{ds} waveforms at full load and light load. ZVS is achieved as shown in the zoomed-in waveforms during the ON period. Fig. 5 shows the performance of the power supply. Full power output is provided with V_{in} >12 V. Constant output voltage at 19.5 V is observed for all measured V_{in} in Fig. 41(a). A 83% efficiency is measured at 10 W. Fig. 41(c) shows the thermal performance with natural convection. The transformer as the hottest point has a 44°C temperature rise.



(a) (b) (c)

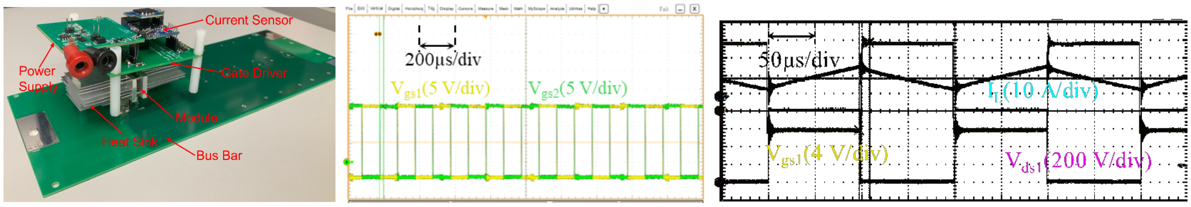
Fig. 40 (a)Waveforms of the V_{gs} and V_{ds} at 10 W output power. (b) Waveforms of the V_{gs} and V_{ds} at 2 W output power. (c) zoomed-in waveforms in the white dashed box in (b).



(a) (b) (c)

Fig. 41. (a) Power output capability vs. V_{in}. (b) Efficiency at different output power for 12-V V_{in}. (c) Thermal performance at 10 W.

The power supply was tested to provide power for a 1.2 kV SiC phase leg gate driver for a continuous buck test. Fig. 42(a) shows the test setup. Fig. 42(b) shows the top and bottom device gate waveforms. Both gates have +15.3 V and -4 V output, indicating identical output voltages among the power supply's two outputs. Fig. 42(c) shows the v_{gs}, v_{ds}, and inductor current during the continuous test. The gate output maintains steady during the power switch's switching transient.



(a) (b) (c)

Fig. 42. (a)Test setup with the power module. (b) Gate outputs of the phase leg. (c) v_{gs}, v_{ds}, and inductor current during continuous buck test.

In summary, planar power supply with PCB-based air-core transformers has been proven to be a viable and cost-effective solution for the integration of the power supply to the power module. The six-output power supply was first designed and verified on its efficiency, voltage accuracy, and ability to work under 72°C. The load transient test proved the proposed control is effective in maintaining the gate output when the gate driver switches between normal operation and standby mode. The dual-output planar power supply was then designed and tested with the power module to further validate the viability of the air-core solution to be integrated with the power module. With the air-core solution, the power supply can potentially operate nearer to power devices' junction when components with higher temperature rating can be selected.

2.4.Demonstration of Module/Current Sensor/Driver Power Supply Technologies

The three technologies developed in this project, i.e., the high-temperature double-side cooled SiC module packaging, module parasitic inductance based current sensor, and Class-E air core power supply were integrated and demonstrated. The latter two technologies were combined with a gate-driver board for switching the SiC phase-leg module. The module was encapsulated in Parker Lord E-2000 epoxy for supporting 200ºC junction temperature of the SiC devices. A circuit diagram of the phase-leg power stage with a busbar is shown in Fig. 43.

An assembly of the phase-leg power stage and a busbar is shown in Fig. 44. The gate driver consists of a motherboard where the gate-driver components are mounted and two daughter boards, one for the current sensor and the other for the power supply. Fig. 45 shows the measured gate waveforms of the integrated power module when the top and bottom drivers' input are complementary PWM signals. The power supply can provide the right turn-on and turn-off voltages for both gate drivers.

2.4.1 Double-Pulse Test

The setup of the high-temperature double pulse test (DPT) is shown in Fig. 46, where the power device is heated using a heating resistor. The temperature is monitored with the thermistor embedded in the power module. Fig. 47 shows the waveforms in the double-pulse test at room temperature and 200 °C. The *di/dt* and *dv/dt* are measured and listed in Table V. It can be observed that in general, di/dt and dv/dt are higher in the high-temperature test. The high-temperature test shows that the phase leg can work normally at the junction temperature of 200 °C.

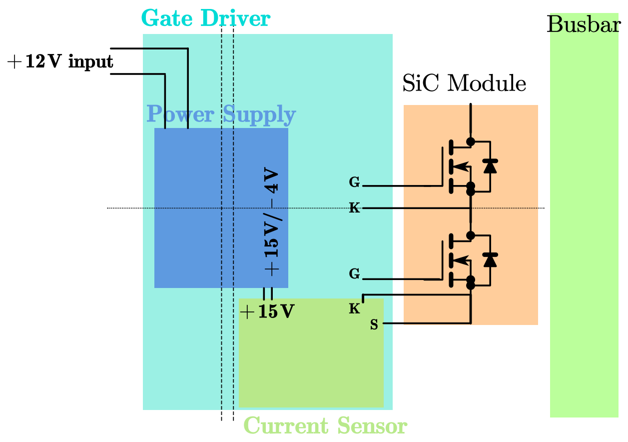


Fig. 43. An electrical diagram of the phase-leg module.

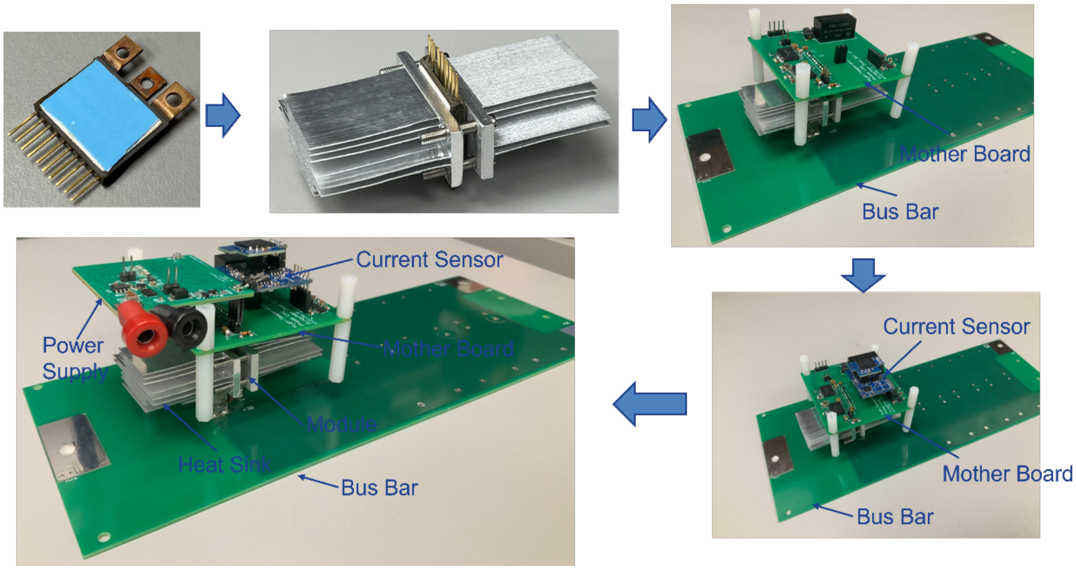
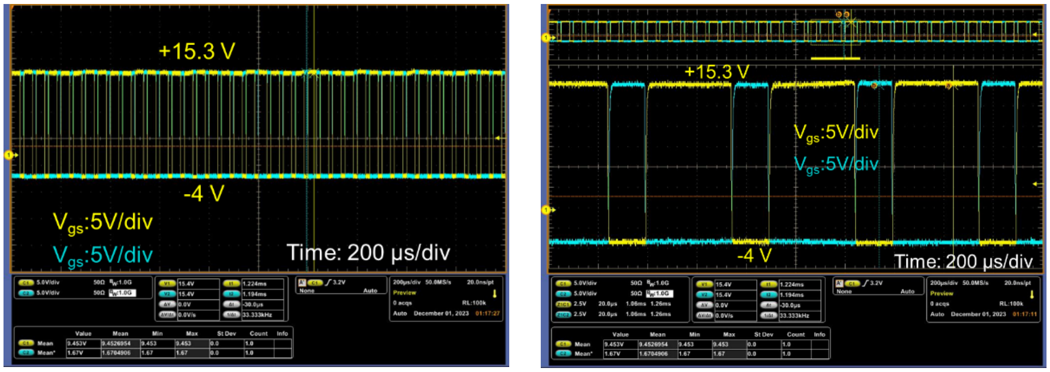


Fig. 44. An assembly of the phase-leg power stage demonstrating the integration of all three technologies developed in this project.



(a) Gate waveforms (b) Zoomed-in waveforms

Fig. 45. Measured gate waveforms of the integrated module.

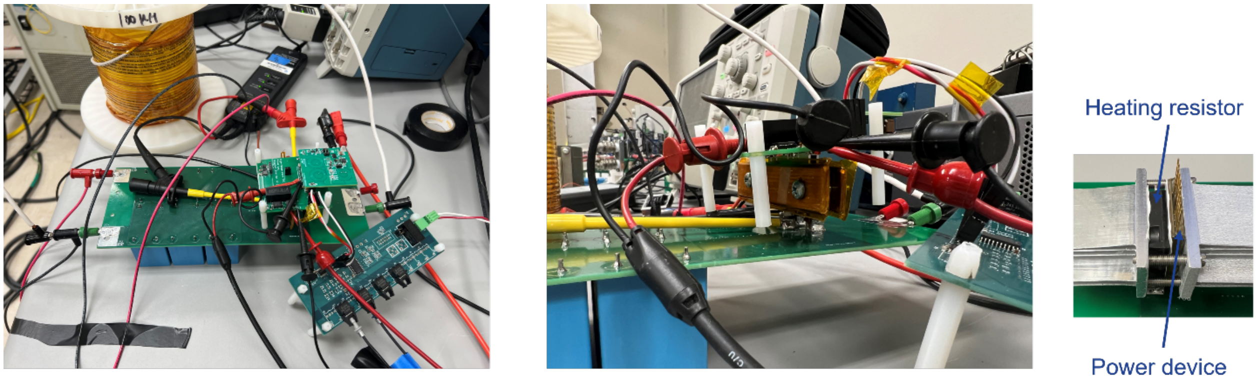


Fig. 46. High-temperature double pulse test set-up.

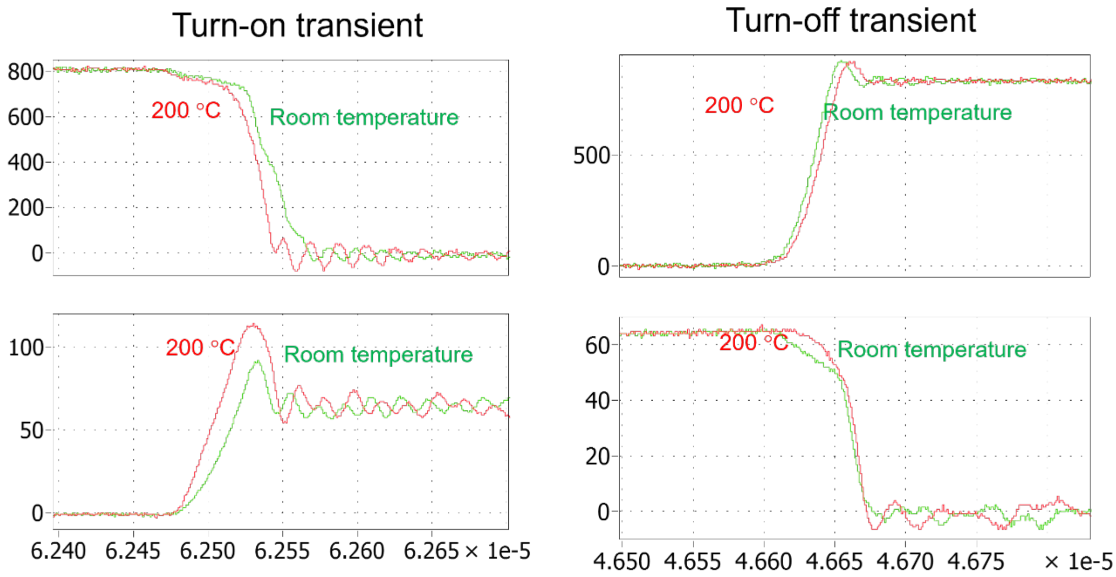


Fig. 47. Waveforms in the double pulse test

Table V. Double pulse test results.

		Room Temperature	200 °C
Turn-on	dv/dt (10% to 90% Vdc)	18.8 V/ns	22.9 V/ns
	di/dt (10% to 90% I_{dmax})	1.85 A/ns	2.38 A/ns
Turn-off	dv/dt(10% to 90% Vdc)	24 V/ns	22.2 V/ns
	di/dt (10% to 90% I_{dmax})	1.1 A/ns	1.8 A/ns

2.4.2 Continuous Test in a Buck Converter

We continued the technology demonstration with more tests on the integration of the three technologies developed in this project, i.e., the high-temperature double-side cooled SiC module packaging, module parasitic inductance-based current sensor, and Class-E air core power supply. In the last reporting period, the fabricated module was assembled with the bus bar, gate driver, and power supply, with a double pulse test conducted at T_j = 200°C. The effort of this reporting period is toward the continuous test of the whole assembly via a buck test.

An assembly of the phase-leg power stage and a busbar is shown in Fig. 48. The gate driver consists of a motherboard where the gate-driver components are mounted and two daughter boards, one for the current sensor and the other for the power supply.

Fig. 49 shows the circuit for the continuous buck test. The input voltage was 800 V. The load resistance at maximum load was 13 Ω. The top and bottom switches were driven with two complementary 50% duty PWM at 10 kHz. The gate resistance was 5 Ω. The junction temperature was measured with the thermistor inside the module. Forced air cooling was applied. During the test, the load resistance was gradually reduced until the junction temperature of the module reached 200°C. The V_{ds} of the bottom switch and the inductor current were measured to evaluate the module's performance.

Fig. 50 shows the V_{ds} and inductor current waveforms at 200°C T_j. With the load resistance shown in Fig. 49 the average output current reaches 31.8 A with a 36 A peak current through the module. The module works under the continuous current without failure.

In summary, the continuous buck test of the integrated power module verified the function of the power supply and power module in the real converter operation. At 200°C-T_j, the integrated power module delivered more than 12 kW to the load and 36 A peak current through the power module.

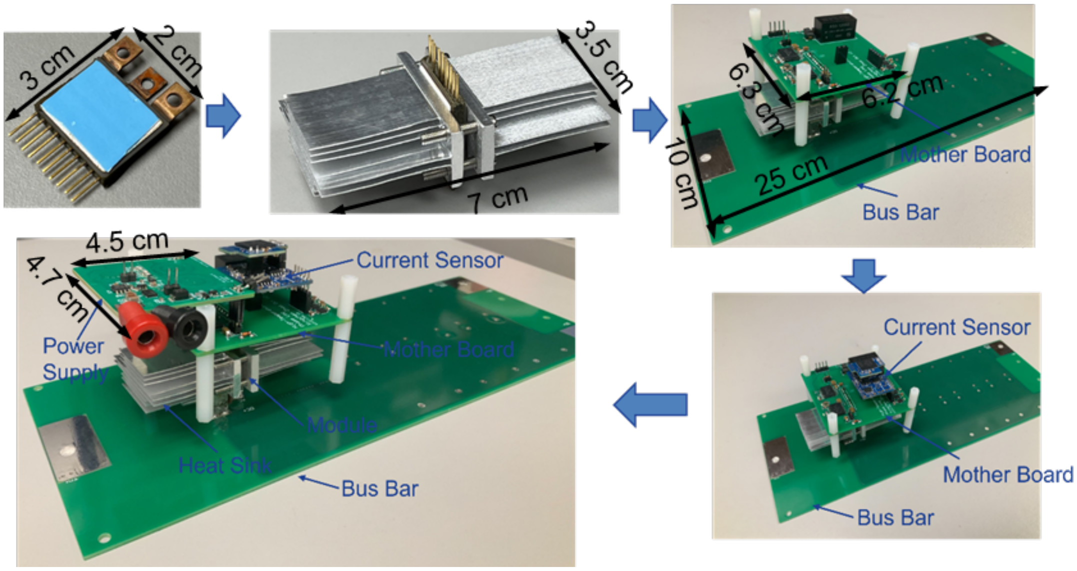


Fig. 48. An assembly of the phase-leg power stage demonstrating the integration of all three technologies developed in this project.

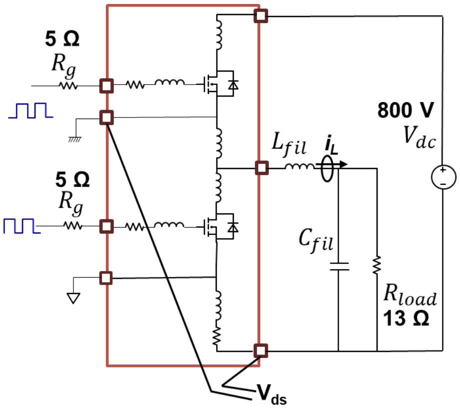
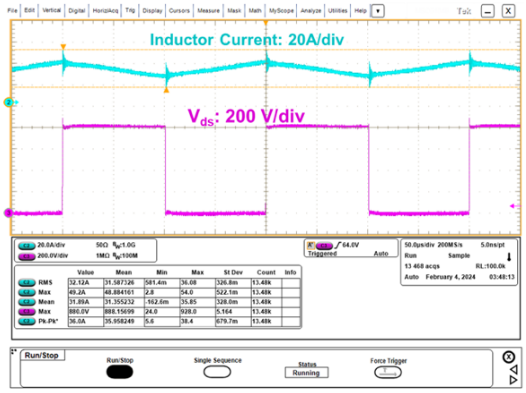


Fig. 49. Circuit setup of the module continuous testing.



C2 20.0A/div 50Ω B_W:1.0G
C3 200.0V/div 1MΩ B_W:100M

A' C3 ∫ 64.0V
Triggered Auto

50.0µs/div 200MS/s 5.0ns/pt
Run Sample
13 468 acqs RL:100.0k
Auto February 4, 2024 03:48:13

	Value	Mean	Min	Max	St Dev	Count	Info
C2 RMS	32.12A	31.587326	581.4m	36.08	326.8m	13.48k	
C2 Max	49.2A	48.884161	2.8	54.0	522.1m	13.48k	
C2 Mean	31.89A	31.355232	-162.6m	35.85	328.0m	13.48k	
C3 Max	880.0V	888.15699	24.0	928.0	5.164	13.48k	
C2 Pk-Pk*	36.0A	35.958249	5.6	38.4	679.7m	13.48k	

Status
Running

Fig. 50. Measured continuous waveforms at 200°C-T_j.

II. WORKFORCE TRAINING, PUBLICATIONS, AND PRESENTATIONS

1. Workforce Training

This project has provided professional development for 8 PhD and 2 MS students on research methodology and technical experience at Virginia Tech.

2. List of Publications and Patents

1. E. Arriola, Zichen Zhang, Y. Gao, G-Q. Lu, A. Ubando, X. Zhao, and D. Dong, “Double-Side Cooled 1.2 kV, 300 A SiC MOSFET Phase-Leg Modules at 200 kW, > 100 kW/L Traction Inverters,” proceedings of CIPS 2024, March 12-14, 2024, Dusseldorf, Germany.
2. B. Li, and K. Ngo, “An Improved Class-E Current Inverter With Two Coupled Inductors for Isolation and Power Scaling Without Affecting Switch Voltage Stress,” *IEEE Transactions on Industrial Electronics*, vol. 71 (8), 9947-9950, 2024.
3. C. Ding, S. Lu, Z. Zhang, K. Zhang, T. Nguyen, K. D. T. Ngo, R. Burgos, and G.-Q. Lu, "Double-Side Cooled SiC MOSFET Power Modules with Sintered-Silver Interposers for a 100 kW/L Traction Inverter," *IEEE Transactions on Power Electronics,* 38 (8), pp 9685 – 9694, 2023.
4. S. Lu, T. Zhao, Z. Zhang, K. D. Ngo, R. Burgos, and G.-Q. Lu, "Low Parasitic-Inductance Packaging of a 650 V/150 A Half-Bridge Module Using Enhancement-Mode Gallium-Nitride High Electron Mobility Transistors," *IEEE Transactions on Industrial Electronics,* vol. 70, no. 1, pp. 344-351, 2022.
5. S. Lu, Z. Zhang, C. Buttay, K. D. Ngo, and G.-Q. Lu, "Improved Measurement Accuracy for Junction-to-Case Thermal Resistance of GaN HEMT Packages by Gate-to-Gate Electrical Resistance and Stacking Thermal Interface Materials," *IEEE Transactions on Power Electronics,* vol. 37, no. 6, pp. 6285-6289, 2022.
6. C. Ding, H. Liu, K. D. Ngo, R. Burgos, and G.-Q. Lu, “A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization,” *IEEE Transactions on Power Electronics,* vol. 36, no. 10, pp. 11672-11680, 2021.
7. E. Arriola, G-Q. Lu, and A. Ubando, “Effect of Pores on Crack Propagation in Sintered-Silver Die Attach: A Baseline Model,” *Proceedings of the ASME 2023 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic*

Microsystems. *ASME 2023 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*. San Diego, California, USA. October 24–26, 2023.

8. C. Nicholas, F. Boshkovski, E. Arriola, Z. Zhang and G. -Q. Lu, "Thermo-Mechanical Analysis of a 650 V/150 A e-GaN HEMT Sandwiched Between a PCB and DBC Substrate," *2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, Charlotte, NC, USA, 2023, pp. 1-5, doi: 10.1109/WiPDA58524.2023.10382215.
9. F. Boshkovski, C. Nicholas, Z. Zhang, P. Paret, K. D. T. Ngo and G. -Q. Lu, "Effects of Encapsulant Properties on the Thermo-Mechanical Reliability of Double-Side Cooled Power Modules for Traction Inverters," *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, Nashville, TN, USA, 2023, pp. 5934-5938, doi: 10.1109/ECCE53617.2023.10362816.
10. D. Chao and G-Q. Lu, "Double-Side Cooled Power Modules with Sintered-Silver Interposers," Patent Application, PCT/US2022/071087.

3. List of Oral Presentations for Knowledge Dissemination

1. Q. Yuchi, J. Gardner, Z. Zhang, E. Arriola, G-J. Su, B. Ozpineci, and G-Q. Lu, "Packaging of a Compact, Dual-Side Cooled, Low-Chip Count 1.2 kV SiC Power Stage for 200 kW Traction Inverters," presented at 2024 SAE WCX, Detroit, MI.
2. G-Q. Lu, "Silver Sintering for Power Device and Module Packaging: The Science and Practice," a tutorial given at *2023 IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)*, Charlotte, NC, USA, 2023.
3. G-Q. Lu, "Packaging of Double-Side Cooled SiC Power Modules for Tracton Inverters," an Invited Presentation for PSMA Power Technology Roadmap Webinar Series, 09/21/2023.
4. Q. Yuchi, Z. Zhang, S. Lu, C. Ding, F. Boshkovski, B. Li, T. Nguyen, K. Ngo, R. Rolando, G-Q. Lu, G-J. Su, B. Ozpineci, P. Paret, and S. Narumanchi, "Packaging of Double-Side Cooled SiC Power Module for 100 kW/Liter Traction Inverter," presented in the industry session of "Highly Integrated Power Module for Traction Drives" at 2023 Applied Power Electronice Conference (APEC) in Orlando, FL.
5. G-Q. Lu and K. DT Ngo, "Power Electronics Materials and Modules," technical exchange/presentation, November 10, 2022, Wolfspeed, Inc.
6. G-Q. Lu, "Advanced Packaging Strategies for Silicon Carbide to Process More Power," keynote presentation at Asia-Pacific Conference on SiC and Other Related Materials (APCSCRM), November 14-15, Xi'an, China. (Online Presentation)
7. G-Q. Lu, "Advanced Strategies for Packaging High Power Density Silicon Carbide Modules," invited presentation at the WBG Power Symposium, December 14-15, 2022, Osaka, Japan. (Online Presentation)

III. PARTICIPANTS, COLLABORATION, REFLECTION, AND LISTS OF FIGURES AND TABLES

1. Participants

There were thirteen participants at Virginia Tech contributed to this project: three professors and ten graduate students. Eight of the ten students have graduated and joined the workforce.

2. Collaboration

Organization Name: National Renewable Energy Laboratory (NREL)
Location of Organization: Golden, Colorado, USA
Partner's contribution to the project: Collaborative research

More details on partner and contribution: Collaborated on processing sintered-silver samples for joint reliability evaluation.

Organization Name: Oak Ridge National Laboratory (ORNL)
Location of Organization: Oak Ridge, Tennessee, USA
Partner’s contribution to the project: Collaborative research

More details on partner and contribution: ORNL developed a segmented three-phase inverter and we provided our phase-leg modules, gate drives and protections for the demo-inverter, and we coordinated with ORNL on bus bar and heat sink design for the phase-leg module.

Below is an illustration of the internal and external biweekly meetings this team has participated with the other partners.

- **Internal Biweekly Meetings**

VIRGINIA TECH.
CPES
VT MSE
VT ECE
NREL

- **External Biweekly meetings**

OAK RIDGE National Laboratory
VIRGINIA TECH.
UNIVERSITY OF ARKANSAS
Stony Brook University

Sandia National Laboratories
SUNY POLYTECHNIC INSTITUTE
VIRGINIA TECH.
OHIO STATE
Stony Brook University

3. Reflection

The team wishes that there was a more engaging support mechanism for accelerating the technologies developed in our project to the market. We appreciate the opportunities for updating our findings to the EDT team members and receiving their valuable comments. But it would be great if in the later years, e.g., from BP 3 of the project, we were able to work closely with a technology-to-market (T2M) industry advisory board comprising a few of the industry members. The board and our team could have met, at a minimum, once per quarter, to explore marketing strategies for the technologies. With the board's help, our team could have built solid contacts with companies that may benefit from our technologies. In return, our team could have learned the limitations of the technologies and their qualification process. A portion of the budget could have been devoted to support the T2M activities. And the team would report on its T2M activities in the quarterly report along with the technical findings. Numerous promising technologies have been tucked away in laboratories because they do not seem to directly meet industry demands. A more proactive T2M support entity within a project would help steer the research endeavors towards addressing more industry-centric challenges.

4. List of Figures

5. List of Tables