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Flexible and Low-cost FPGA-Based SiPM Array Readout

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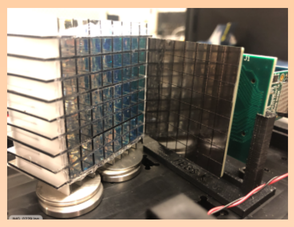
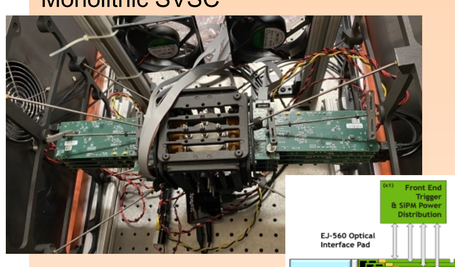
Motivation

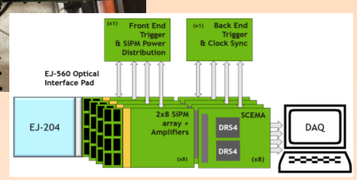
Common challenge for highly pixelated systems: Fast, scalable readout electronics

Pixelated scintillator array with one-to-one SiPM readout



Monolithic SVSC





Optically segmented SVSC

Scalable SiPM readouts

Digitizer-based

ASIC-based

[Other efforts]

FPGA-based

This work

FPGA-based readout solutions:

- Fast (and low-cost!) development cycle relative to ASICs
- Flexible: changes in system parameters require tweaks not costly redevelopment
- Lower footprint and power consumption relative to digitizers
- Tailor readout to system requirements

FPGAs are now a ubiquitous and continuously improving platform

Open questions:

- Fundamental performance (relative to ASIC or digitizer)
- Scalability to thousands of channels

Fundamental tension: using a digital platform to process analog signals

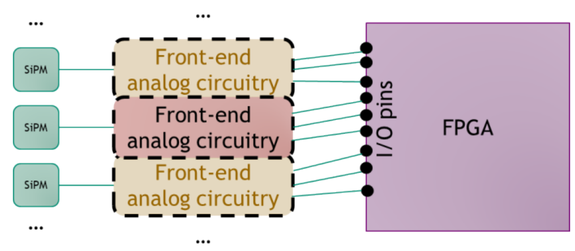
FPGA-based readout collaboration

BERKELEY LAB

E. Brubaker, J. Steele, M. Sweany, J. Cates, W.-S. Choong, M. Turqueti

Goals for scalability:

- Few, small, low-power analog components
- Minimal I/O pins needed per SiPM channel



Approach #1: Sigma-Delta Modulation

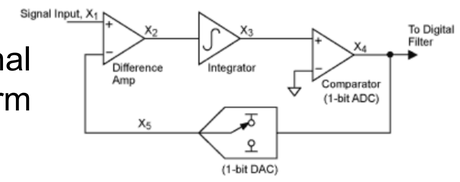
Convert analog signal into stream of uniform digital pulses

Implement most of circuit within FPGA

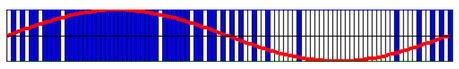
Used in ADCs for e.g. audio systems

Investigated for low-power radiation detection

Preserves integral of waveform; shape unless saturated; timing limited



Basic sigma-delta modulator circuit. (Credit: Maximintegrated.com)



Zhao et al., "A Novel Read-Out Electronics Design Based on 1-Bit Sigma-Delta Modulation", IEEE TNS 64, 2 (2017).

Sigma-delta modulation in FPGA:

1. **What are limits on sampling rate?**
2. **Multi-bit SDM for high photon temporal density?**
3. **Is PSD feasible?**

FPGA-based readout collaboration

BERKELEY LAB

Nov 2022 start

Flexible and low-cost FPGA-based SiPM readout

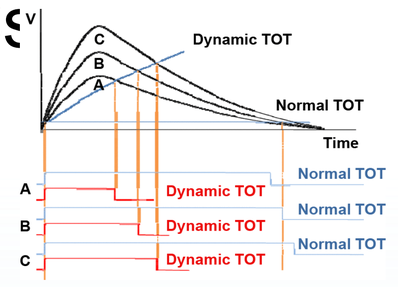
Toward high-performance, channel-dense SiPM readout without ASICs

Approach #2: TDCs and dynamic TOT

Sub-100 ps TDCs demonstrated many times in modern FPGAs

High-resolution pulse timing; amplitude via TOT

Dynamic TOT mitigates non-linear response of traditional TOT



Kenji Shimazoe et al., 10.1109/TNS.2012.2215338

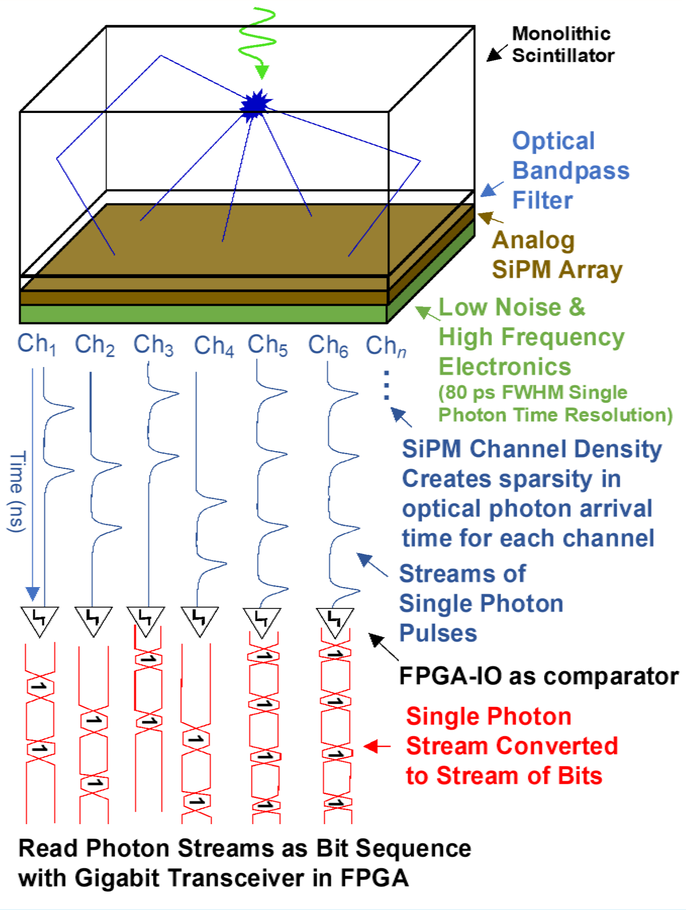
Yonggang et al., "A Linear Time-Over-Threshold Digitizing Scheme and Its 64-channel DAQ Prototype Design on FPGA for a Continuous Crystal PET Detector", IEEE TNS 61, 1 (2014)

TDC-based FPGA readout:

1. **Which FPGA-TDC architecture?**
2. **What should serve as global time ref/sync?**
3. **What is dTOT amplitude resolution?**
4. **How to enable PSD?**

Approach #3: Photon-counting detector

Uniquely count each photon arriving at detector array—extract maximal information from scintillator!



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