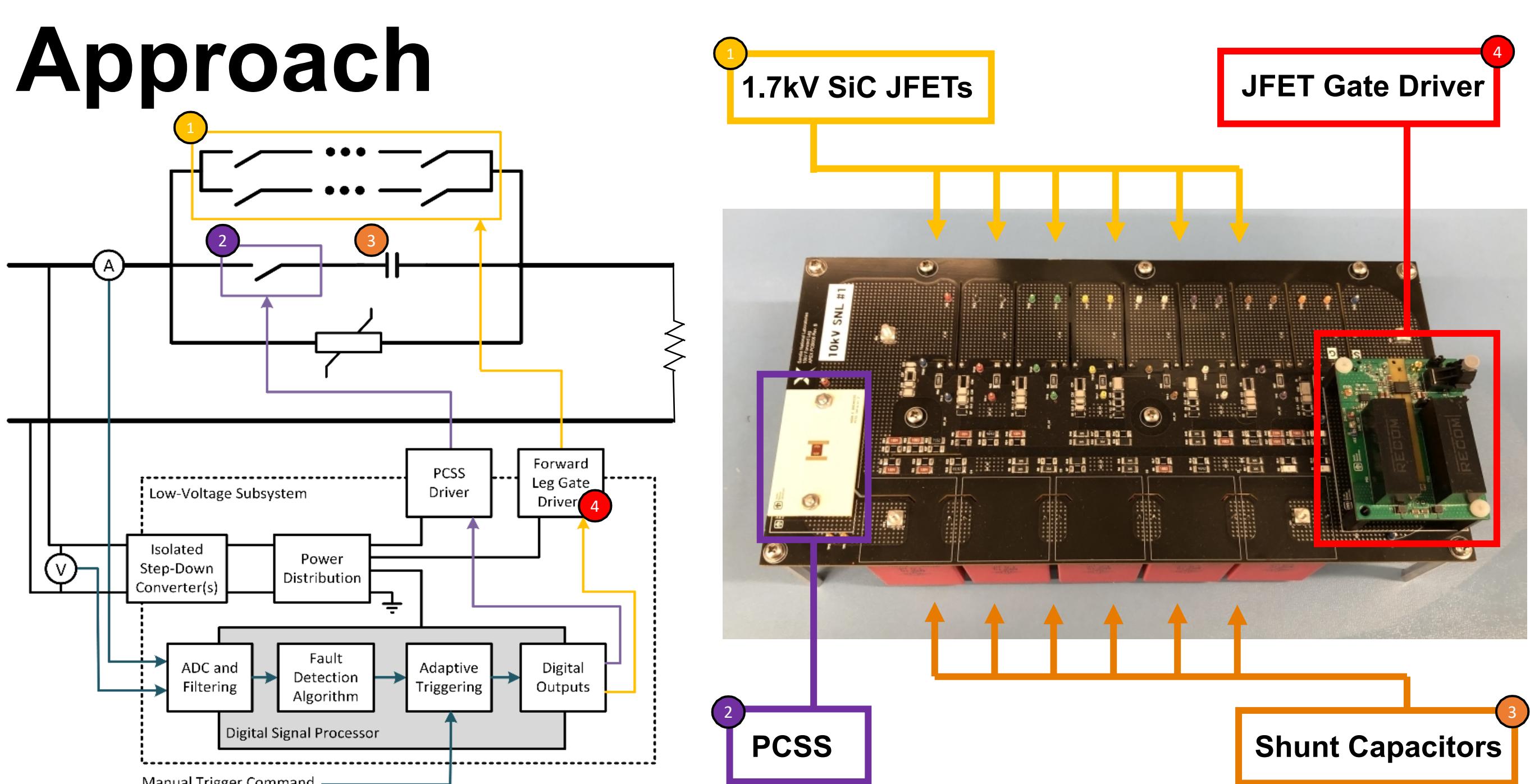


ARC-SAFE: Accelerated Response Semiconducting Contactors and Surge Attenuation for DC Electrical Systems

6 kV/5 A DC Circuit Breaker Demonstration

Approach

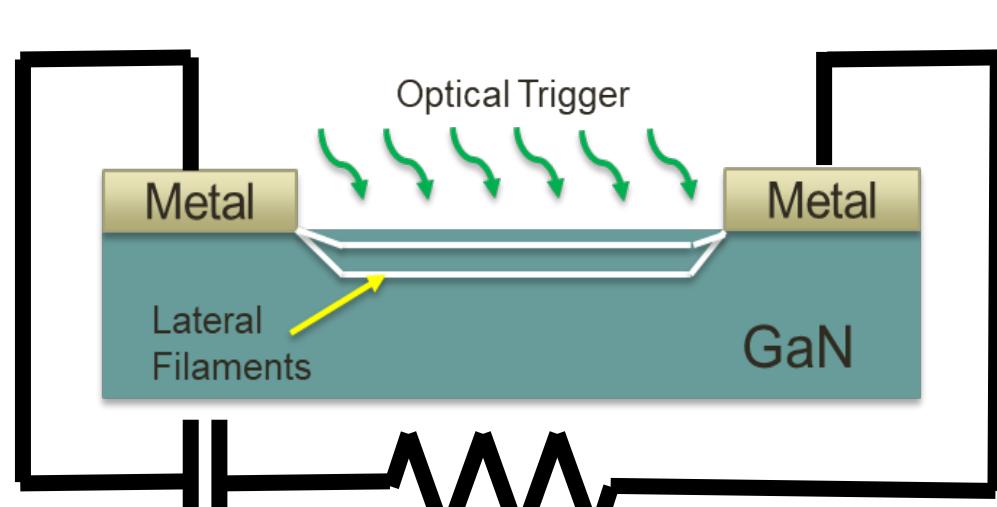


1. Normally-on Leg consists of cascaded SiC JFETs with passive balancing approach
2. Normally-off Leg uses GaN PCSS
3. Energy dissipating leg uses shunt capacitor to manage flyback current.
4. System control (sense and trigger) included in low-voltage subsystem
 - Instrumented to allow characterization of circuit breaker components
 - Shrinking design for 10 kV/100 A target

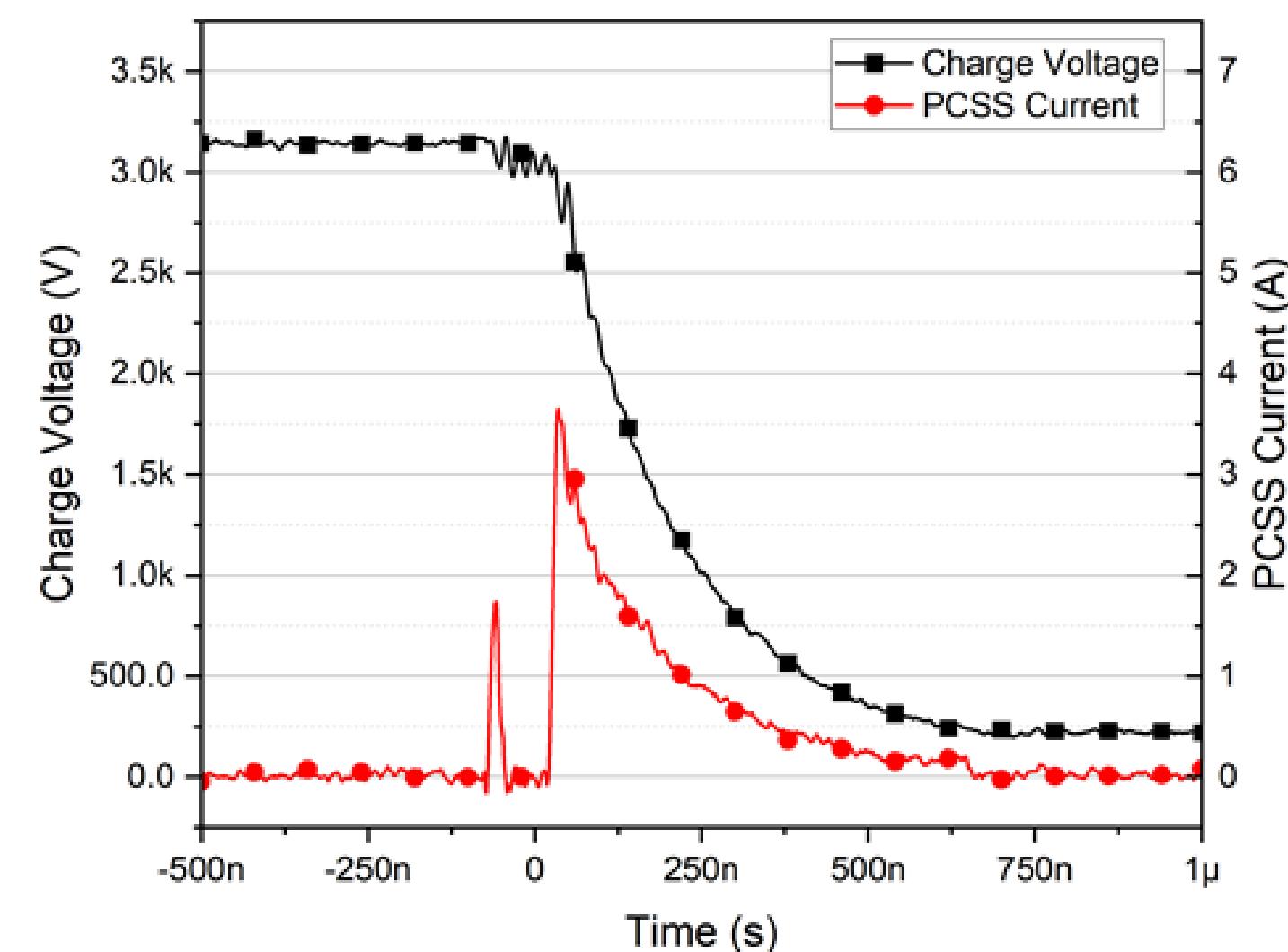
Benefits

- *Normally on, low loss JFETs improve CB efficiency*
- *Galvanic isolation from optically triggered GaN PCSS (fast acting)*
- *System control*

GaN PCSS (Lateral Design)



- >3 kV switches using 2.0 mm gap
- Optically triggered using 532 nm (Nd:YAG laser)
- Recent demonstration with optical trigger at ~800 nm

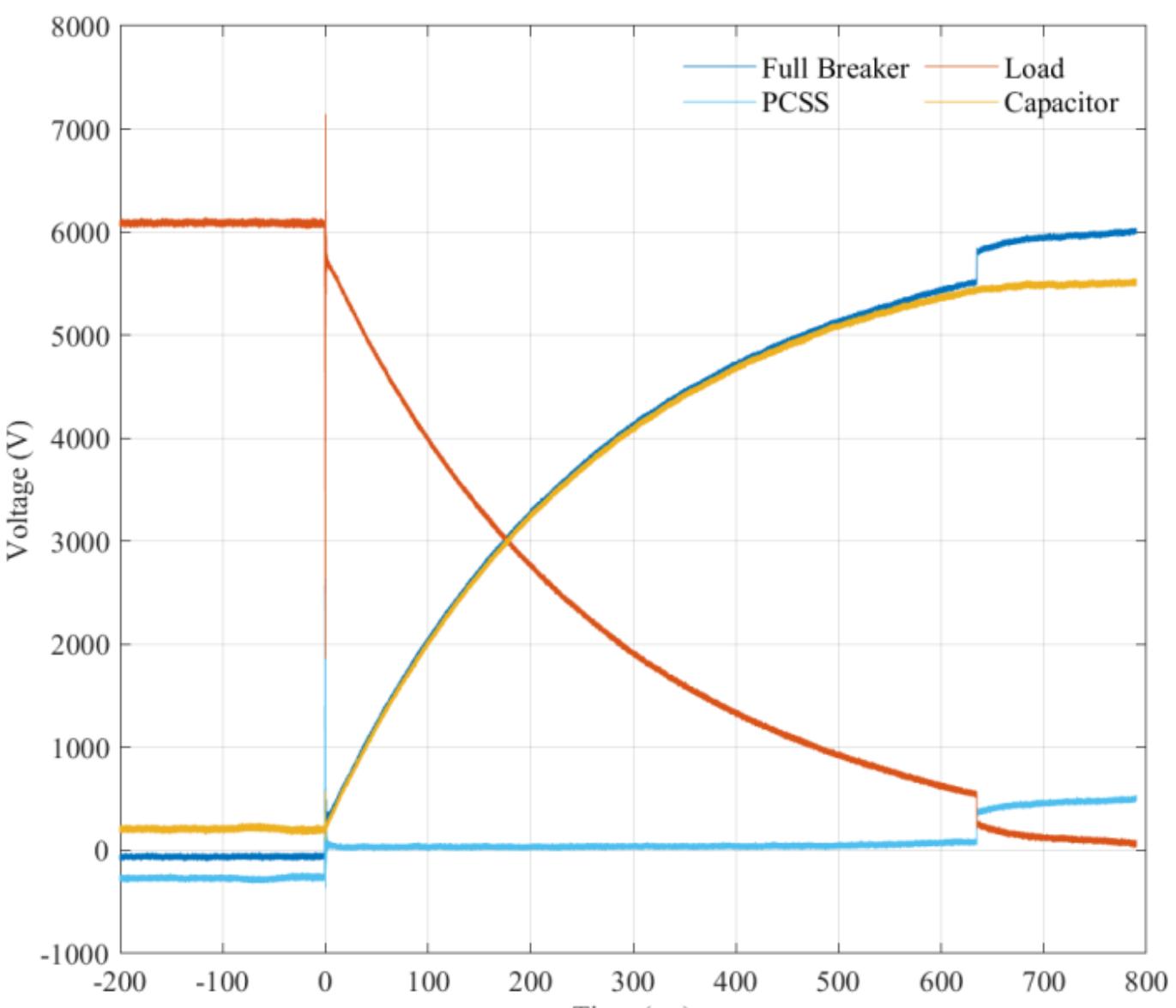


Circuit Breaker Packaging

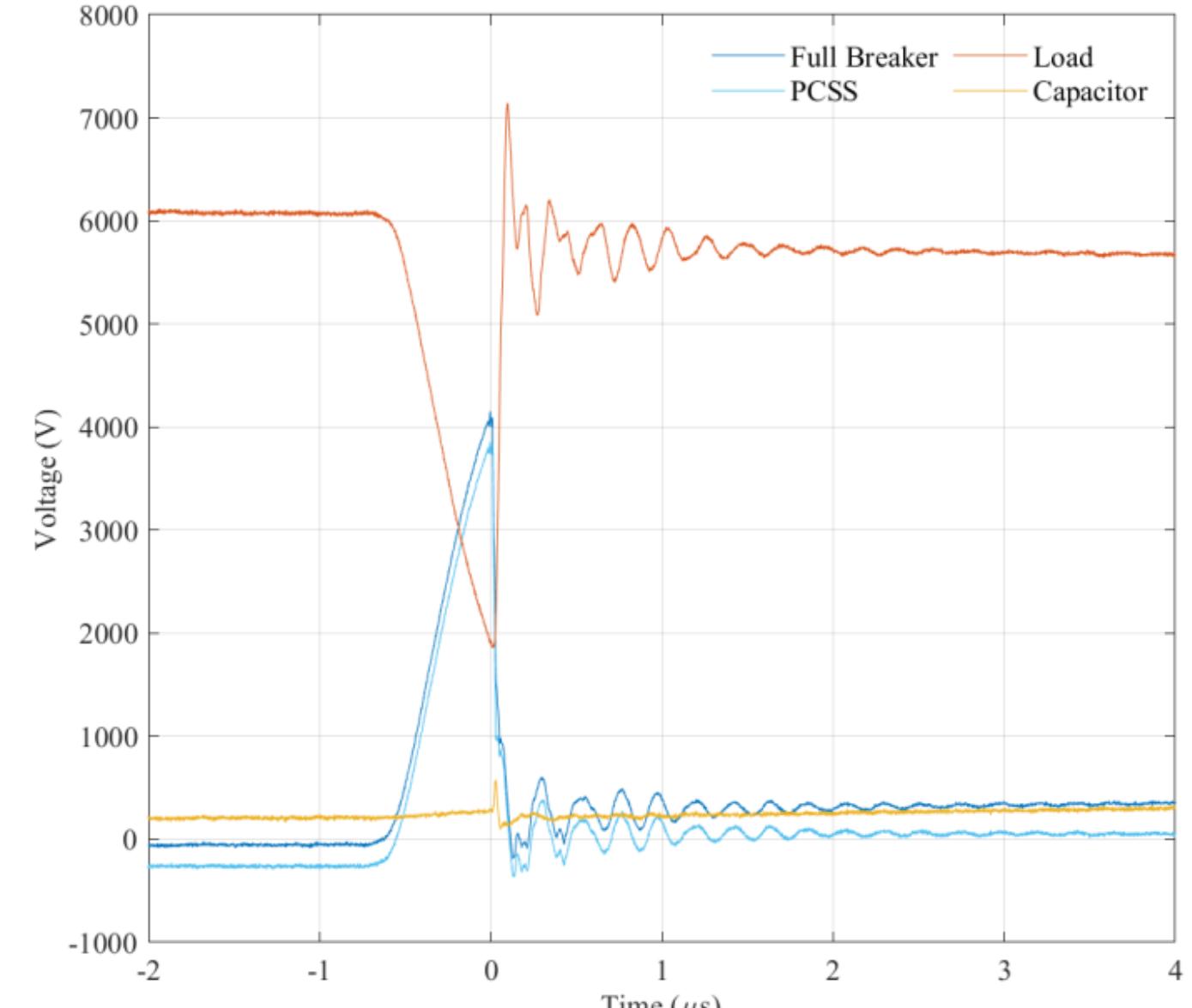


DC Circuit Breaker Operation

Nominal test shot capacitor charge



Nominal test shot transient



Interval I [$t_0 \rightarrow t_1$]

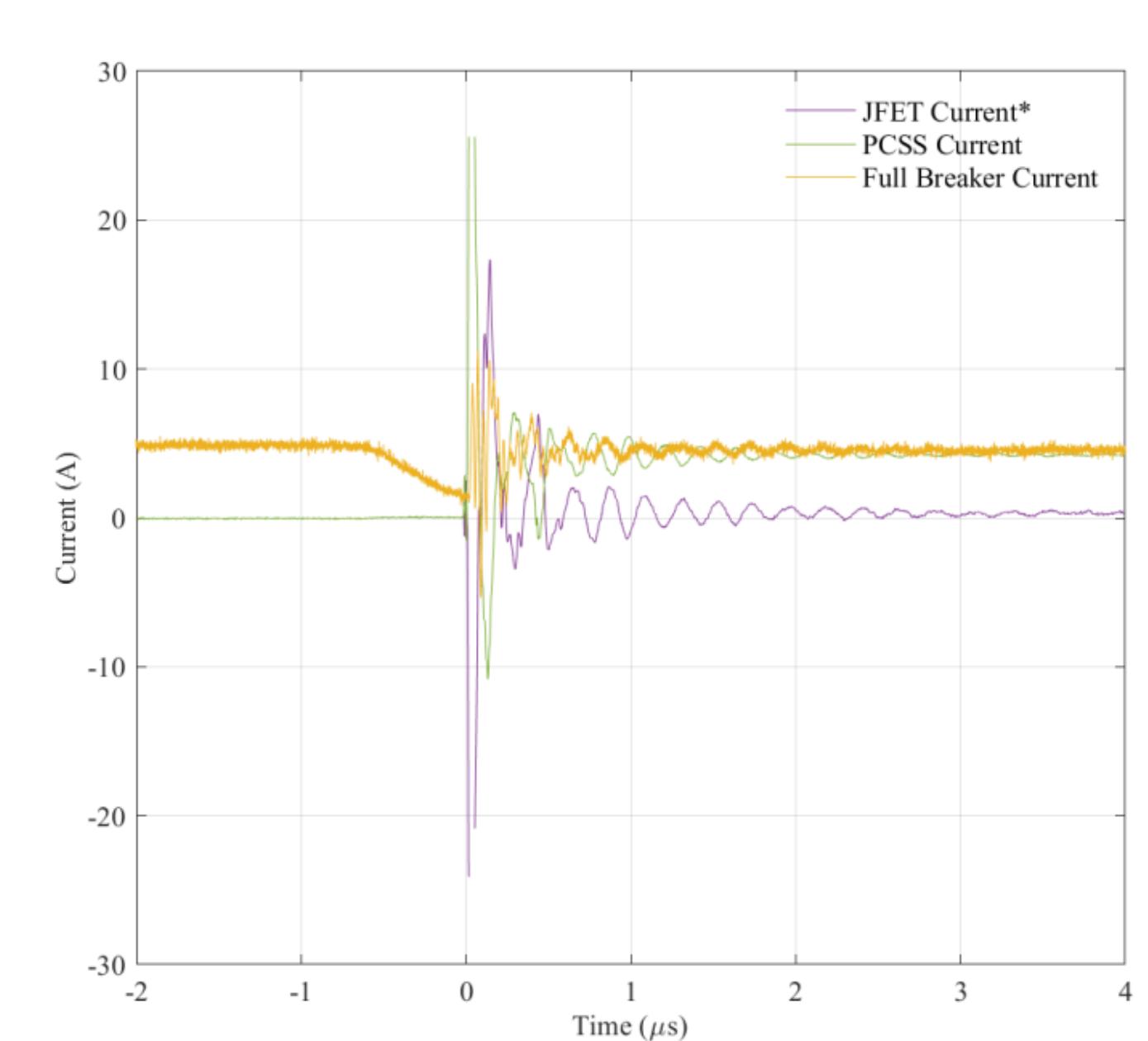
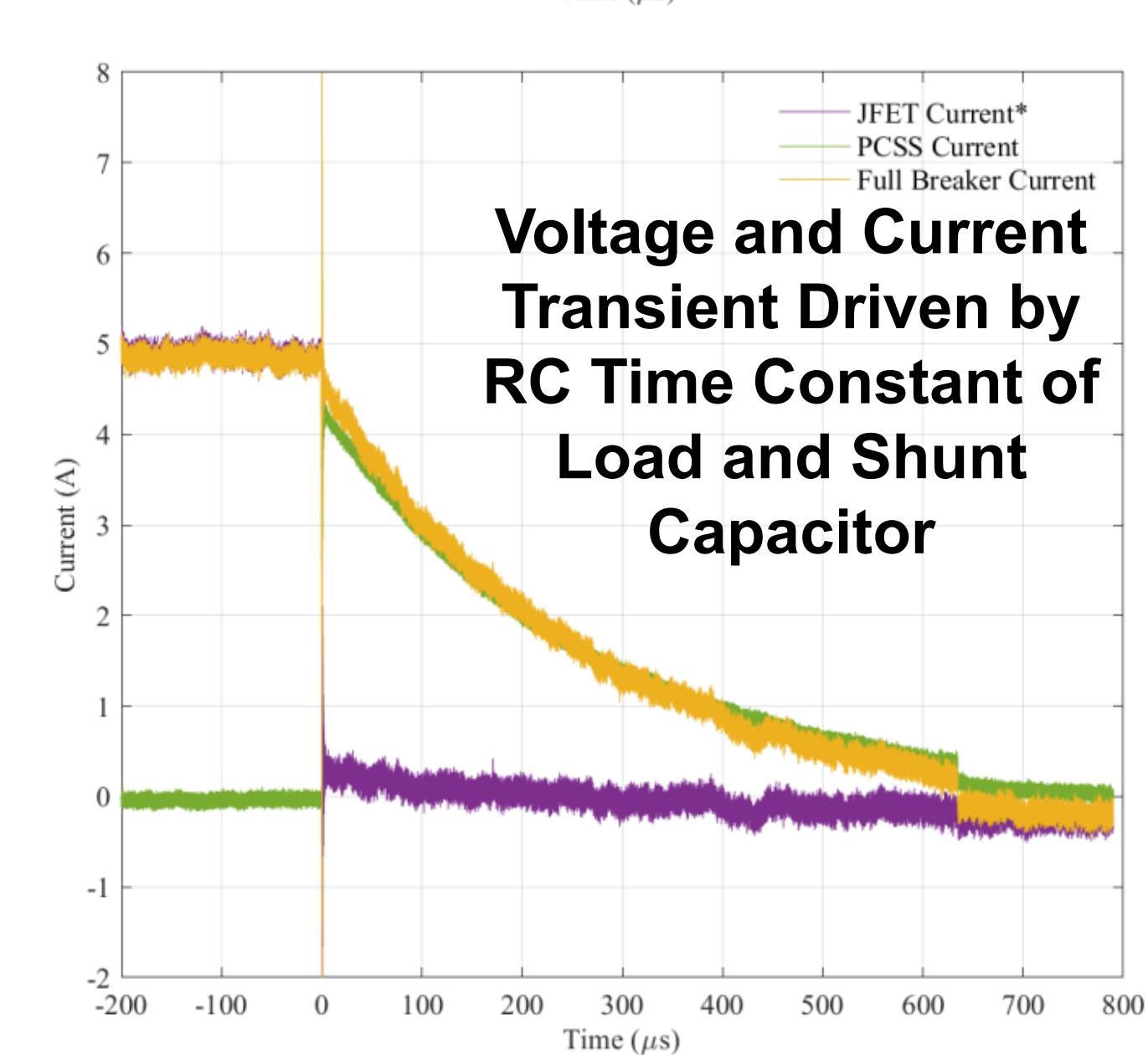
- Fault current rises at t_0 until t_1 when the fault current is detected, turning JFETs OFF

Interval II [$t_1 \rightarrow t_2$]

- JFET voltage starts to rise at t_1 and JFET/load current starts to decrease.

Interval III [$t_2 \rightarrow t_3$]

- PCSS is triggered at high-gain mode at t_2 , diverting fault current from JFET leg to shunt cap.
- Shunt capacitor voltage rises based on



Current limited by testing setup and GaN PCSS

