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Hardware Implementation of a Traveling Wave Protection Device for DC Microgrids

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***Abstract*—This paper elaborates the results of the hardware implementation of a traveling wave (TW) protection device (PD) for DC microgrids. The proposed TWPD is implemented on a commercial digital signal processor (DSP) board. In the developed TWPD, first, the DSP board's Analog to Digital Converter (ADC) is used to sample the input at a 1 MHz sampling rate. The Analog Input card of DSP board measures the pole current at the TWPD location in DC microgrid. Then, a TW detection algorithm is applied on the output of the ADC to detect the fault occurrence instance. Once this instance is detected, multi-resolution analysis (MRA) is performed on a 128-sample data buffer that is created around the fault instance. The MRA utilizes discrete wavelet transform (DWT) to extract the high-frequency signatures of measured pole current. To quantify the extracted TW features, the Parseval theorem is used to calculate the Parseval energy of reconstructed wavelet coefficients created by MRA. These Parseval energy values are later used as inputs to a polynomial linear regression tool to estimate the fault location. The performance of the created TWPD is verified using an experimental testbed.**

***Index Terms*—DC microgrid, Discrete wavelet transform, protection, traveling wave**

I. Introduction

DC microgrid's protection is of particular importance to accommodate a reliable source of power to the microgrid's customers. Fast tripping protection schemes in DC microgrids are required to isolate faults before the internal protection of power electronics converters operate. Doing so, one can ensure that these converters are not blocked and can supply power after the fault is isolated [1]. Most of the existing fast tripping protection schemes for DC microgrids utilize numerical techniques to extract traveling waves (TWs) and detect faults [2]. The TW-based protection of DC microgrids has been addressed in [3]–[7]. In [4], the fault detection and location of faults in DC microgrids are addressed by applying signal processing techniques on current and voltage TWs. These techniques extract the TW waveshape features such as the time constant. Based on these features, the article generates a look-up table that maps each extracted feature to a fault scenario. In [3], the TW features are extracted using multi-resolution analysis (MRA) which is based on discrete wavelet transform (DWT). These features are later used as inputs to machine learning techniques for fault detection, classification, and location. The fault detection and classification is conducted using support vector classifiers. The fault location is performed using Gaussian Process regression. The approach in [3] requires many simulation studies to gather the data required for training the machine learning algorithm. This issue has been addressed in [5] where the physical properties of TWs generated for different fault locations are used to generate data required for the training of machine learning algorithms.

In this paper, the previous work of authors in [5] is implemented on a commercial digital signal processor (DSP) board. In the developed TW Protection device (TWPD), first, the DSP board's ADC is used to sample the input at a 1 MHz sampling rate. The Analog Input card of DSP board measures the pole current at the TWPD location in DC microgrid. Then, a TW detection algorithm is applied to the output of the ADC to detect the fault occurrence instance. Once this instance is detected, multi-resolution analysis (MRA) is performed on a 128-sample data buffer that is created around the fault instance. The MRA utilizes discrete wavelet transform (DWT) to extract the high-frequency signatures of measured pole current. To quantify the extracted TW features, the Parseval theorem is used to calculate the Parseval energy of reconstructed wavelet coefficients created by MRA. These Parseval energy values are later used as inputs to a polynomial linear regression tool to estimate the fault location. The performance of created TWPD is verified using an experimental testbed.

II. Components of TWPD in the DSP Board

TWPD utilizes the pole current locally measured at its location to find the fault location along the cable. We have implemented the TWPD on a Texas Instrument's (TI) DSP

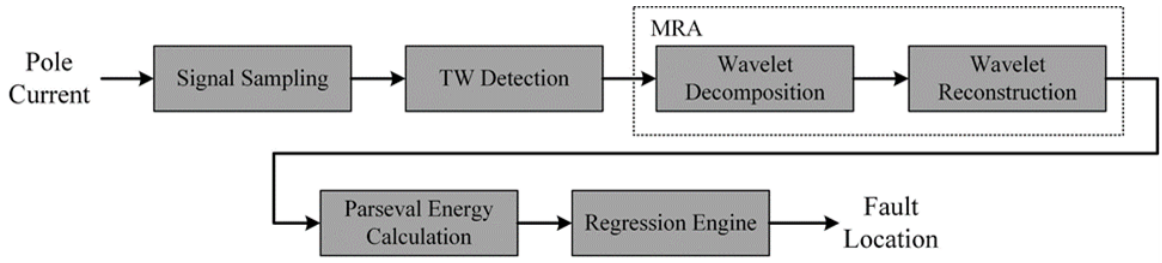

Fig. 1. The block diagram of TWPD in DSP board.

board called TMS320F28379D which is a member of the C2000™ microcontroller (MCU) product family. These boards are mostly used within embedded control applications. The F28379D dual-core MCU design is based on the TI 32-bit C28x CPU architecture. Each core is identical with access to its own local RAM and flash memory, as well as globally shared RAM memory. Sharing information between the two CPU cores is accomplished with an Inter-Processor Communications (IPC) module. Additionally, each core shares access to a common set of highly integrated analog and control peripherals, providing a complete solution for demanding real-time high-performance signal processing applications, such as digital power, industrial drives, inverters, and motor control. The block diagram of the different components required to implement the proposed fault location algorithm in the DSP board is illustrated in Fig. 1. In the following, each of these blocks is elaborated in detail.

A. Signal Sampling

The initial step is to perform high-fidelity sampling on the measured signal. We have implemented this step by considering a 1 MHz sampling rate on the pole current that is fed to the Analog Input (AI) card of DSP. The utilized DSP has two cores. Each core is associated with a co-processor namely the Control Law Accelerator (CLA). This enables DSP to perform parallel Floating-Point Unit (FPU) processing [8]. The CLA can enhance DSP's bandwidth for computing purposes by allowing CPU to focus on other tasks rather than reading results from the ADC. The ADC peripheral has two sampling resolutions of 12 or 16 bits. It can also have 16 or 8 different ADC channels, respectively. This depends on the sampling resolution. The CLA then reads 128 samples from ADC samples and then raises a flag to inform CPU when 128 samples are collected. These 128 samples are stored in a moving buffer as a new sample is read. The DSP has an FPU library that is capable of the execution of optimized complex mathematical operations. In this paper, we have used the signal convolution operator for implementing DWT and MRA. The detailed process on how ADC and CLA are configured is described in [9].

B. Traveling Wave Detection Algorithm

Once the measured pole current is properly sampled and a 128-sample data buffer is created, the TW detection algorithm is run to detect the fault incident. The algorithm requires knowing the fault instance in order to create an appropriate data buffer for the MRA stage. Once a fault occurs, the pole current experiences a rapid change. We utilize the discrete wavelet transform (DWT) decomposition and apply it to the 128-sample data buffer. The DWT uses Daubechies8 as the mother wavelet, which has a filter length of 16. For the sampling frequency of 1 MHz, DWT decomposition results in detail coefficients that correspond to the frequency range from 250 to 500 kHz. According to [9], since the convolution library in DSP applies zero padding, one needs to account for the effect of zero padding to avoid the edge effect on the processed data. To this end, in every data buffer, the algorithm adds the last 15 samples from the previous buffer to the beginning of the current buffer. This results in 158 coefficients after performing convolution. The algorithm then discards the first and last 15 samples. However, for the first data buffer that DSP reads, since no previous buffer is available, the algorithm removes the first and last 15 samples from the results of the convolution stage and then zero pads the beginning of the signal with 15 zeros. In the final stage, downsampling by the order of two is applied which results in 64 coefficients. The algorithm finds the maximum of these coefficients and compares it against a threshold to detect the TW incident. Since this TW incident is found on the downsampled data, the actual TW incident can be found by multiplying this value by two.

C. Preparing the Input to MRA

Once the TW incident is detected, a data buffer is created for the MRA stage to calculate MRA coefficients. A signal of length 128 values is given as an input signal to calculate its wavelet decomposition and reconstruction. In our implemented approach, the data buffer includes 64 data samples before the TW detection instance and 64 samples after the TW detection instance. If the TW instance ID is less than 64, samples from the previous data buffer are required in addition to the samples from the current buffer. If the TW ID is greater than 64, one requires to use data from next data buffer, which creates a delay. If the TW ID is exactly 64, the current 128-sample buffer is used. For pole-to-pole (PP) faults at 200 m of a cable, the created data buffers are shown in Fig. 2.

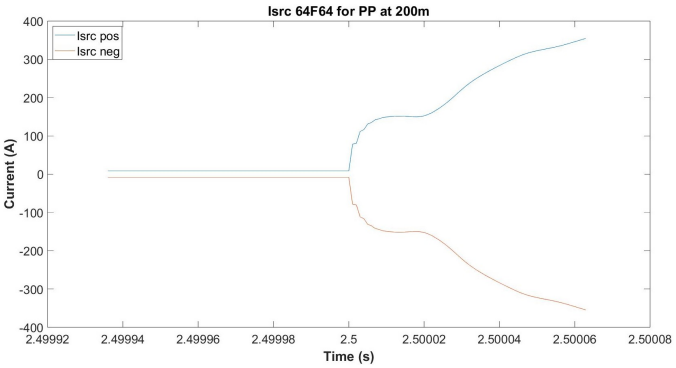

Fig. 2. 128-sample buffers created for MRA.

D. Extracting the High-Frequency Features of the Measured Current

In order to effectively extract the high-frequency features of measured pole current, this paper utilizes the MRA approach. The details of MRA is provided in [3], [5]. MRA can find wavelet coefficients of a signal for different frequency ranges using a set of low-pass and high-pass filters. The MRA will consist of two separate stages, namely wavelet decomposition and wavelet reconstruction. The mother wavelet Daubechies8 is used, which has a filter length of 16. After the MRA's reconstruction coefficients are calculated, they are passed through the Parseval energy calculator to effectively quantify these coefficients. Parseval energy can correlate the wavelet reconstruction coefficients to the measured signal energy spectrum. The details of Parseval energy calculation is provided in [3], [5]. Herein, six MRA frequency levels are used to incorporate an adequate portion of the frequency spectrum for extracting fault current features as the fault location changes. For the six frequency ranges (i.e., Level 1 to Level 6), Level 1 denotes the highest frequency range. For each frequency range the corresponding Parseval energy value is calculated. The Parseval energy of a specific MRA constructed coefficient d_i, at m^{th} time step after an initial time t_0 is calculated as

$$E_{PRS,i}(m) = \sum_{j=1}^{m} d_i^2(t_0 + j\Delta t), \tag{1}$$

E. Regression Engine

The regression engine uses the six Parseval energy values to estimate the fault location along the cable. In order to effectively implement the regression engine in DSP board, we utilized polynomial linear regression as the regression engine. Polynomial regression is technically a special case of multiple linear regression that can be used to model nonlinear functions. This regression tool models the relationship between the independent variable x and the dependent variable y and is formulated as an n^{th} degree polynomial of x. In the case of fault location on a DC cable, we use six levels of Parseval energy values as the input and the output is the fault location. This multi-input polynomial regression of 3rd degree can be formulated as

$$y = b_0 + \Sigma_{i=1}^{6}\Sigma_{j=1}^{3} b_{ij} {x_i}^j \tag{2}$$

where x_1, x_2, x_3, x_4, x_5, and x_6 are the six levels of Parseval energy values and y is the fault location. b_0 and b_{ij} are the polynomial model coefficients.

III. Verification Results

In order to verify the performance of TWPD on a DSP board, the simulated pole current signals in PSCAD/EMTDC are played back on another DSP board. The playback DSP board's analog output (AO) is connected to the analog input (AI) of the DSP with TWPD. The experimental testbed is shown in Fig. 3. The test circuit is adopted from [5] and is shown in Fig. 4. The parameters of this microgrid are provided in [5]. The created TWPD is located at R25 protecting the cable from Bus 2 to Bus 5. We have utilized the training approach proposed in [5] to train the polynomial linear regression engine. The training and testing datasets are created based on PP faults at every 25 m of the cable length. Out of this set, the faults at 150 m, 250 m, 350 m, ..., are used for testing the TWPD. In fact, the positive pole current measured at R25 in PSCAD/EMTDC is played back on playback DSP. The TWPD DSP reads the fault current from the AO card of the playback DSP. To verify the performance of MRA and Parseval Energy calculator, the results gathered from the DSP board are compared against the results from different Python libraries for three levels of MRA for a PP fault at 350 m. These comparisons are summarized in Figs. 5 to 7. For the reconstruction coefficients in Figs. 5 to 7, "sigconv" denotes the "convolve" library of "Scipy"; "npconv" denotes the convolve library of "Numpy"; "wavedec" denotes the Python's wavelet transform tool. Fig. 8 compares the Level 1 Parseval energy value calculated by DSP against the value calculated in Python. As seen, the created code in DSP can effectively calculate the MRA reconstructed coefficients and Parseval energy values. DSP uses the 111^{th} data buffer index number of Pareval Energy values as inputs to the polynomial linear regression tool. The Parseval Energy Testing of the created regression model resulted in 1.64% of mean absolute percentage error. The estimated fault locations by the DSP against the actual fault locations are illustrated in Fig. 9.

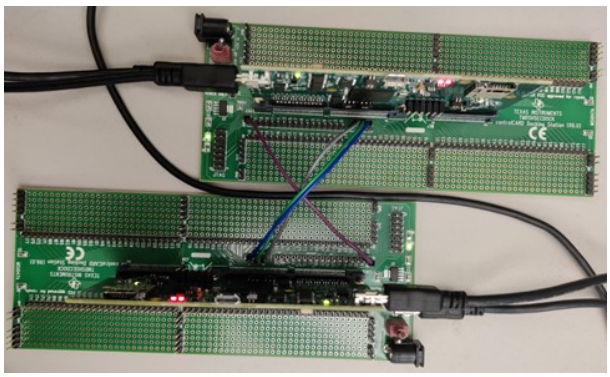

Fig. 3. Experimental testbed with two DSP boards.

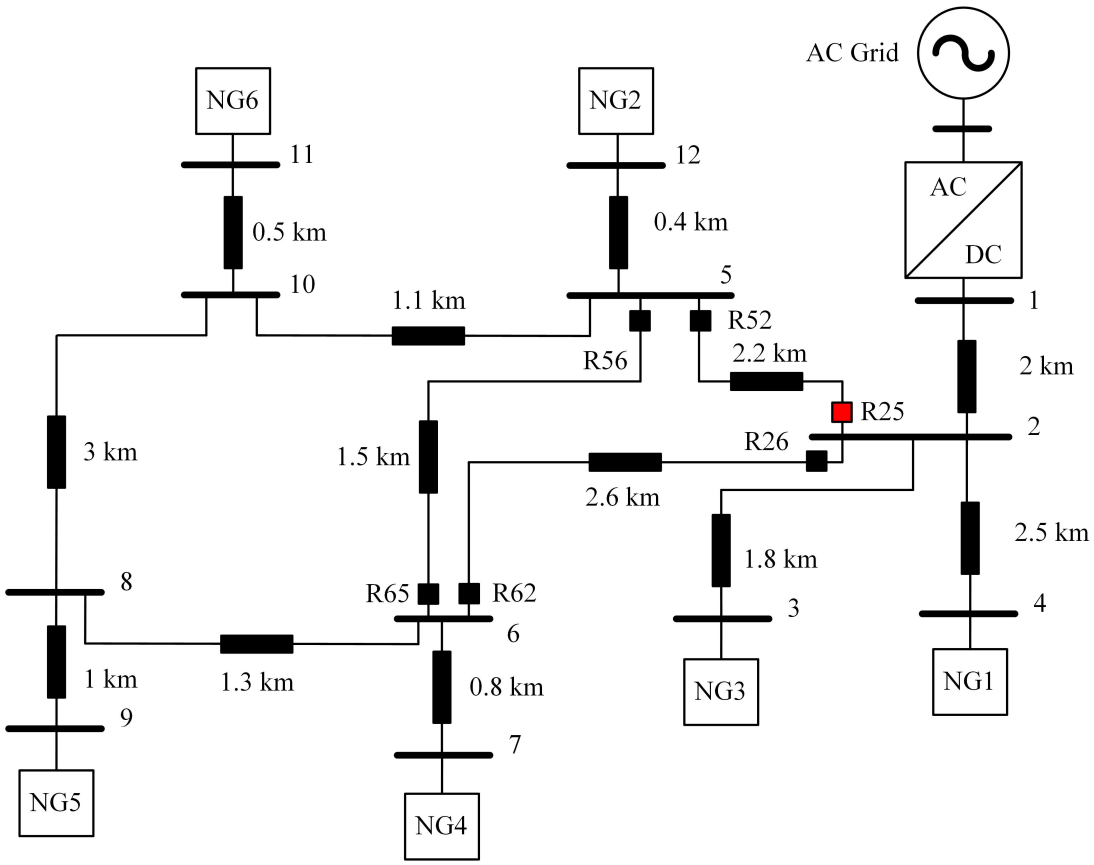

Fig. 4. Circuit diagram of the DC microgrid under study.

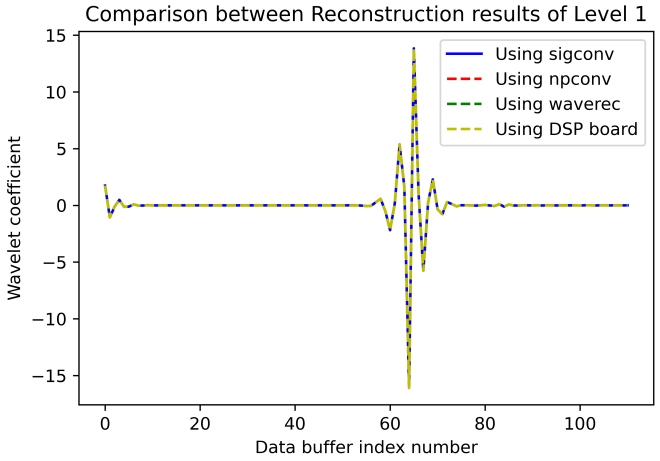

Fig. 5. Comparison between reconstruction coefficients of frequency level 1 collected from DSP board versus Python.

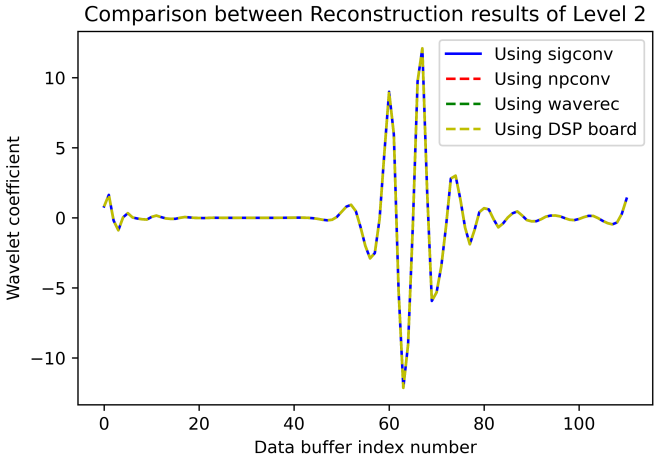

Fig. 6. Comparison between reconstruction coefficients of frequency level 2 collected from DSP board versus Python.

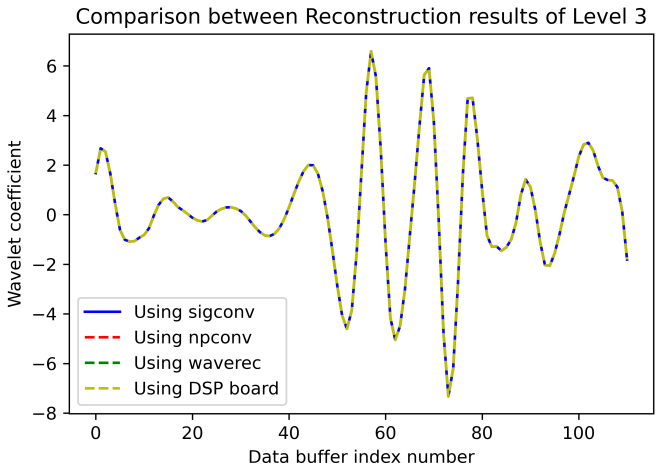

Fig. 7. Comparison between reconstruction coefficients of frequency level 3 collected from DSP board versus Python.

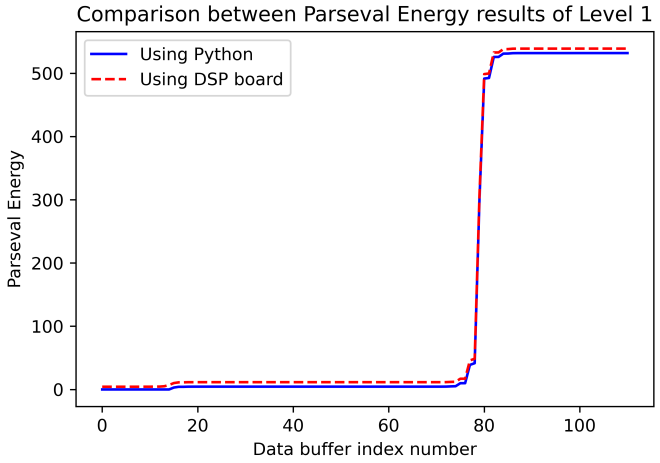

Fig. 8. Comparison between Parseval Energy of frequency level 1 collected from DSP board versus Python.

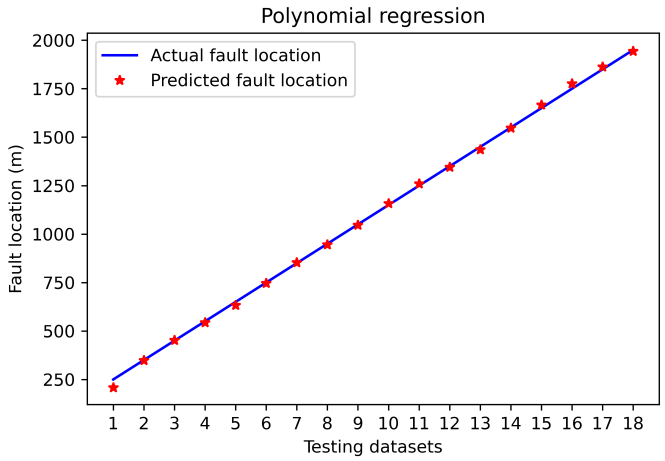

Fig. 9. Fault location prediction by polynomial regression.

IV. Conclusion

In this paper, a TWPD for DC microgrids is implemented in a commercial DSP board. The DSP board's ADC is configured to sample the input at a 1 MHz sampling frequency. A TW detection algorithm based on DWT is developed to detect the fault occurrence instance. Once this instance is detected, MRA is performed on a 128-sample data buffer that is created around the fault occurrence instance. The Parseval energy values of MRA coefficients are used as inputs to a polynomial linear regression tool to estimate the fault location. The performance of created TWPD is verified using an experimental testbed which shows that the created TWPD on a commercially available DSP board is able to locate faults with high accuracy.

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