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A Solid State Transformer for Electric Power Grid HEMP/GMD Mitigation

Timothy Donnelly
Electrical Sciences and Experiments
Sandia National Laboratories
Albuquerque, New Mexico
Email: tjdonne@sandia.gov

Lee Rashkin
Electrical Sciences and Experiments
Sandia National Laboratories
Albuquerque, New Mexico
Email: lrashki@sandia.gov

***Abstract*—A high altitude electromagnetic pulse (HEMP) or other similar geomagnetic disturbance (GMD) has the potential to severely impact the operation of large-scale electric power grids. By introducing low-frequency common-mode (CM) currents, these events can impact the performance of key system components such as large power transformers. In this work, a solid-state transformer (SST) that can replace susceptible equipment and improve grid resiliency by safely absorbing these CM insults is described. An overview of the proposed SST power electronics and controls architecture is provided, a system model is developed, and the performance of the SST in response to a simulated CM insult is evaluated. Compared to a conventional magnetic transformer, the SST is found to recover quickly from the insult while maintaining nominal ac input/output behavior.**

I. Introduction

Today a variety of both man-made and natural events threaten the reliable operation of the electric power grid, including the threats posed by high altitude electromagnetic pulses (HEMP) and solar-geomagnetic disturbances (GMD) [1]–[3]. During such events, changes in the earth's magnetic field – caused by a nuclear explosion or charged particles from a coronal mass ejection colliding with the magnetosphere – result in a time- and spatially-varying electromagnetic field at the earth's surface. This field, coupling with long transmission lines, can introduce low-frequency common-mode (CM) currents flowing through grounded power transformers. These geomagnetically induced currents (GICs) in turn can result in the magnetic cores of the transformers becoming saturated, leading to distorted ac waveforms, increased losses, the potential thermal damage, and in the worst-case, an extended period of power system disruption [2, 3].

To date, several approaches for minimizing the impact of GICs on power system operation have been investigated, including: passive blocking devices [4], corrective line switching [5], and more recently active devices to disrupt GICs in the transformer neutral [6, 7]. At the same time, solid-state transformers (SSTs) have emerged as a technology that aims to supplant conventional magnetic transformers with designs based on modern solid-state switching devices and power conversion circuits [8]. Because of the flexibility afforded by power electronics, SSTs are envisioned to enable a new avenue for increased reliability, resiliency, efficiency, and security in the electric power grid [9]. The goal of this research is to develop an SST which actively mitigates low-frequency CM insults caused by a HEMP/GMD event by using a unique power electronics and controls architecture.

A schematic of the proposed SST is shown in Fig. 1. It consists of a primary-side ac-dc converter, an intermediate dc-dc converter, and a secondary-side dc-ac inverter designed to feed downstream loads. Because of the ac-dc-ac topology, this SST is classified as Type 4 converter [8]. In additional to the standard Type 4 components, the proposed SST also includes an energy storage system (ESS). By controlling CM current on the grid side of the SST, and by utilizing the ESS to absorb the incident CM energy, it is expected that the SST can mitigate the HEMP/GMD insult while maintaining the nominal input/output behavior expected of a transformer.

The remainder of this paper is organized as follows: in Section II, a simulation study which demonstrates the weakness of conventional transformers in response to a low-frequency CM insult is provided. In Section III, the architecture and control scheme of the proposed CM-resilient SST is described. In Section IV, an analogous simulation study is performed to evaluate the resilience of the proposed SST to CM insult. Finally, in Section V, conclusions and directions for future research are outlined.

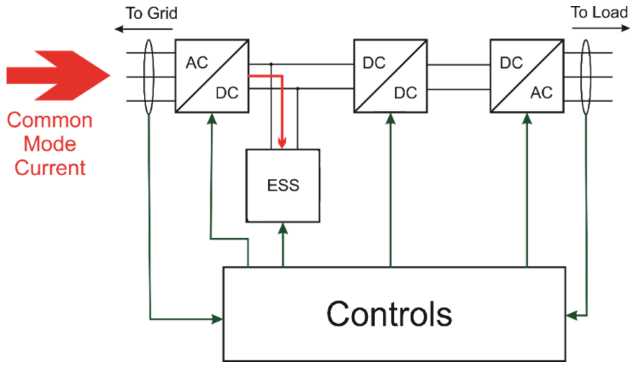

Fig. 1: A Solid State Transformer (SST) designed to neutralize common-mode insults.

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TABLE I: Grid and saturating transformer parameters

V_{ac} [V_{rms}]	V_{cm} [V]	R_g [Ω]	L_g [mH]	R_n [Ω]	I_m p.u.	Φ_m p.u.
230	200	0.5	1.4	5	{0,0.0024,1}	{0,1.2,1.52}

II. Half-cycle Saturation in a Conventional Magnetic Transformer

In conventional ac power systems, the main purpose of a transformer is to step voltages up for long distance transmission and step voltages down again for customer use. Assuming ideal behavior, the transformer functions as linear mutual inductance between two windings, and energy is transferred seamlessly between them. In practice, the magnetic core exhibits several non-ideal behaviors, including the phenomenon of magnetic saturation. Although some degree of saturation is acceptable in many power system applications, an abnormal and potentially severe saturation can occur if the transformer enters half-cycle saturation. This happens when a offset in the magnetic flux (e.g., due to GICs) results in the core becoming saturated during parts of the ac cycle when the ac component and dc component add constructively. An illustration of half-cycle saturation is shown in Fig. 2.

In order to demonstrate this phenomenon in practice, a simulation study of a CM insult impacting a conventional magnetic transformers is provided. A schematic of the circuit considered is shown in Fig. 3. The parameters for the three-phase voltage sources V_{ac}, line impedances L_g and R_g, ground resistance R_n, and finally a simulated CM voltage insult (V_{cm}), are given in Table I. To illustrate the half-cycle saturation effect, the CM insulted is modeled with a step-function that activates at $t = 0.5$ s.

The simulation results for the conventional transformer subjected to a CM voltage insult are shown in Fig. 4. Plotted are the primary-side grid voltages, currents, and corresponding

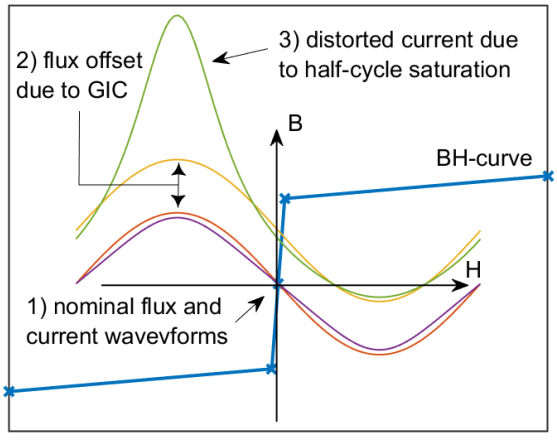

Fig. 2: Half-cycle saturation in a magnetic core due to a dc offset in flux resulting in distorted current waveform

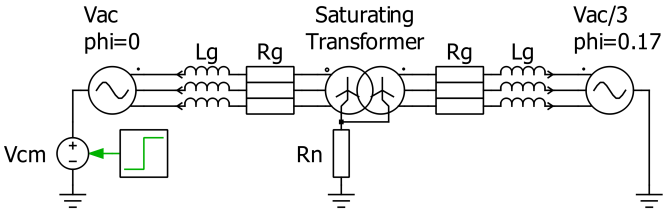

Fig. 3: Simulation study of a conventional magnetic transformer subjected to a CM voltage insult

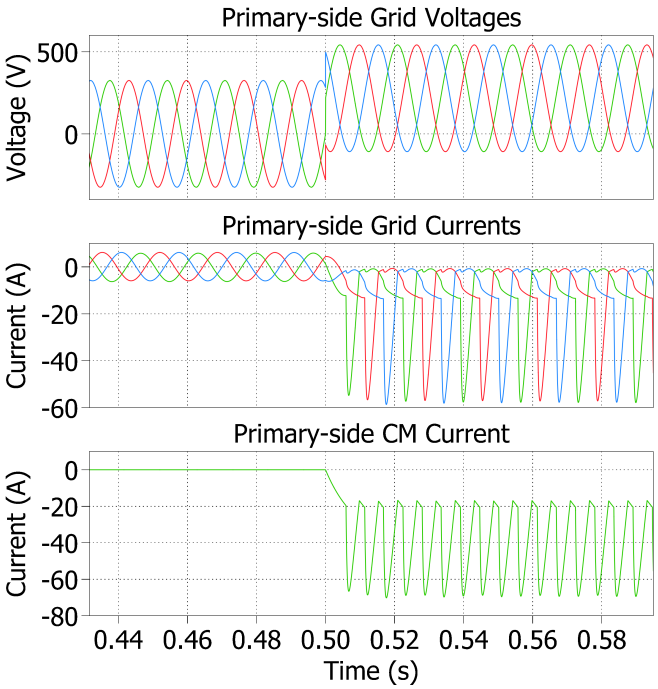

Fig. 4: Simulation results illustrating half-cycle saturation of a conventional magnetic transformer in response to a CM insult

CM current. CM current is defined as the average of the phase currents:

$$i_{cm} = \frac{i_a + i_b + i_c}{3} \tag{1}$$

which is equivalent to the zero-sequence component in the DQ0 rotating reference frame [10]. Before the CM insult, the primary-side voltages and currents are sinusoidal signals with no dc offset and the CM current is zero.

At $t = 0.5$ s, the simulated CM insult begins and the grid voltages immediately increase due to the CM offset. This applied CM voltage also causes a CM current to flow through the transformer primary-side winding and return through R_n. This dc current is large enough to push the transformer into a region of half-cycle saturation, which results in the distorted primary-side grid current shown in Fig. 4. Although a complete analysis of the impact that half-cycle saturation can have on transformer and power system performance is beyond the scope of this work [11], it is clear that the insult has a significant negative impact on the behavior of the transformer.

III. Solid State Transformer Architecture

The SST proposed in this work is designed to overcome the susceptibility of magnetic core transformers to low-frequency CM insults while still maintaining the step-up/down ac/ac conversion capability of conventional transformers. This section describes the power electronics circuits and controls design of the SST which enable this capability.

A. Four-Leg Inverter

One of the key contributions of the proposed SST design is the utilization of a four-legged converter for the ac/dc conversion instead of the standard three-leg inverter design. By adding an additional phase-leg, not only can the inverter control the standard dq components of the phase currents, but it can also control the zero-sequence (CM) component [12]. An illustration of the four-leg inverter is shown in Fig. 5, and it is noted that the mid-point of the fourth-phase leg is grounded. This enables either the upper or lower dc rail to connected to ground depending on the switch state, thus enable control of CM current. The parameters for the inverter system are shown in Table II.

Because of the addition on the fourth phase-leg, standard space vector modulation (SVM) is not applicable. Instead, a 3D-SVM scheme is required [13]. The 3D-SVM described in [14] was used to control the four-leg inverter shown in Fig. 5. An illustration of various switch states and their corresponding voltage in abc coordinates is shown in Fig. 6. It is recalled that in standard 2D-SVM there are 8 possible switch states, and the three-leg inverter can be made to output any voltage vector in a circularly bounded region of the dq-plane inscribed by a hexagon. The same approach applies for 3D-SVM, however now the a four-leg inverter can be made to output any voltage vector in a 3D region bounded by a dodecahedron [12].

B. Dual Active Bridge & Energy Storage System

Besides the four-leg inverter, the SST also consists of the isolated dc-dc converter and the energy storage system (ESS). The dc-dc converter is a dual-active bridge (DAB), which consists of a high-frequency transformer between the two full bridge converters. The two converters operate with a constant 50% duty cycle, and an adjustable time-delay (phase-shift) between the respective switching signals of each converter enables the power through the transformer to be controlled [15]. A schematic of the DAB is shown in Fig. 7 and it is noted the transformer has a turns ratio of 4:1. The remaining circuit parameters for the DAB are provided in Table III.

The ESS in the proposed SST plays a key role in ensuring that during a CM insult, the nominal dq behavior of the overall ac/ac converter remains unaffected. Although in practice any

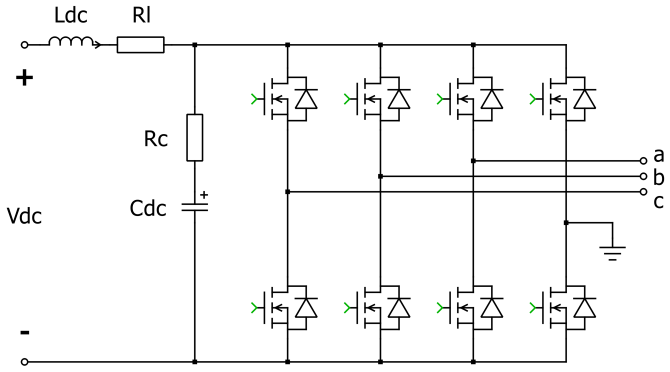

Fig. 5: A four-leg inverter

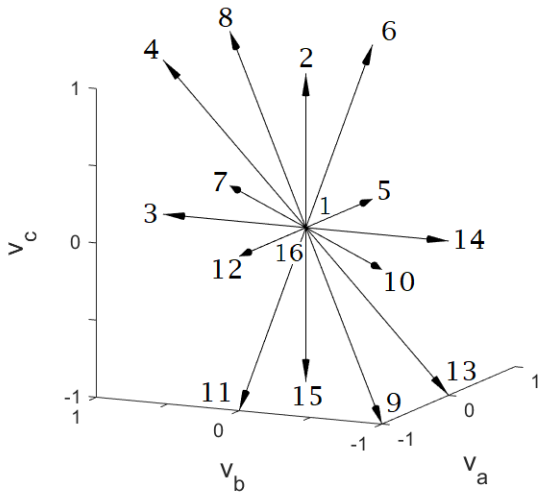

Fig. 6: Possible switch states of a four-leg inverter in abc coordinates [14]

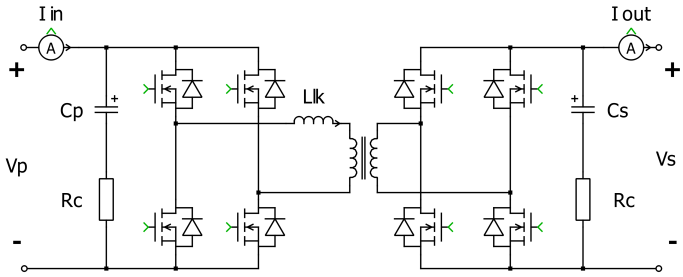

Fig. 7: DAB converter that provides galvanic isolation and step-up/down ratio for the SST.

TABLE II: Four-leg inverter parameters

L_{dc} [mH]	R_l [Ω]	C_{dc} [mF]	R_c [mΩ]	F_{sw} [kHz]
1	0.1	5	10	20

TABLE III: DAB & ESS parameters

DAB				ESS		
C_p, C_s [mF]	L_{lk} [μH]	R_c [mΩ]	F_{sw} [kHz]	V_{bat} [V]	L_s [μH]	R_s [Ω]
5	20	10	100	700	100	0.1

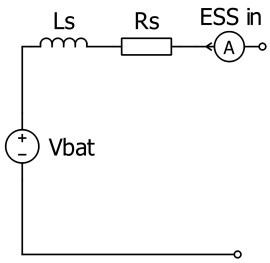

Fig. 8: ESS modeled with a voltage behind an RL filter

physical ESS will likely have its own (potentially complex) dynamic behavior, for simplicity in this work the ESS is modeled using an ideal voltage source behind an RL filter, as shown in Fig. 8. The parameters of the ESS are also listed in Table III.

C. Controls

The controls scheme for the SST can pedagogically be considered in two parts: 1) the ac/ac (i.e., dq) control behavior, and 2) the zero-sequence/CM control behavior. The ac/ac controls of the SST are configured such that the load-side inverter outputs a constant d- and q-axis current ($i_d^* = 10$, $i_q^* = 0$). A synchronous current regulator is used to ensure this commanded value is reached in steady-state [10]. On the grid-side, the ac-dc rectifier is configured to draw enough power into the SST via a d-axis current command to feed the downstream load. This is accomplished using a PI regulator to ensure that in steady-state, the power entering/leaving the ESS is zero. The time constant for this control loop was tuned to be larger than the RL time constant of the ES so that during a transient such as a CM insult, the ESS acts as the primary response mechanism. Power is tranfered from the grid-side to the load-side via DAB which using the same controller demonstrated in [16].

For the zero-sequence control of the SST, the primary objective is to ensure that during a CM insult, the CM current is returned to zero as quickly as possible. A high-level illustration of control scheme used to regulate the CM current entering the four-leg converter is shown in Fig. 9. Like the d- and q-axis current controls, the zero-sequence current is controlled via a synchronous regulator. These are illustrated in Fig. 9 by the block labeled current control loop.

IV. Simulation Results

A simulation model of the SST, modeled in PLECs [17], is shown in Fig. 10. In the simulation, a CM insult on the primary side of the transformer occurs at $t = 0.5$ s. The same grid parameters used for the conventional transformer study in Section II were used here. The results are shown in Fig. 11. The three-phase ac voltage, current, and corresponding CM current are shown in Fig. 11a. In Fig. 11b, the dc voltage on both sides of the DAB, the dc currents for the DAB and ESS, and load-side ac/dc converter output currents are shown.

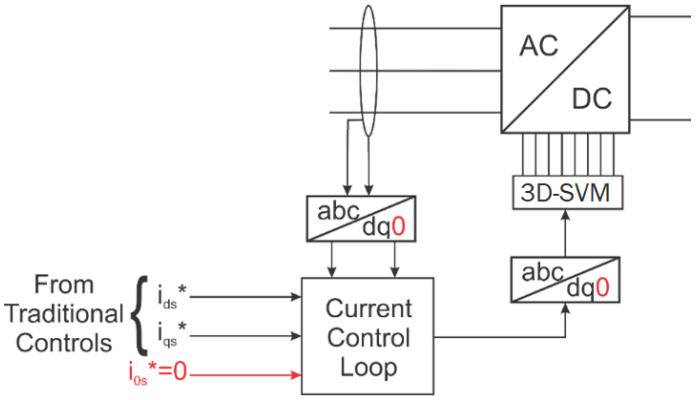

Fig. 9: Control architecture for the proposed SST

As can be seen in Fig. 11, when the CM voltage insult occurs the SST momentarily deviates from its steady-state operating condition. At $t = 0.5$ s, the CM current on the grid side immediately jumps to a negative value. This causes the feedback control loop to increase the CM voltage output by the inverter and drive the CM current back to its reference value (0 A). During this time, a CM current is flowing into the CM voltage generated by the inverter, hence CM power is being absorbed by the SST. This can be confirmed by the corresponding increase in current into the ESS during this transient, which ultimately returns to zero as the CM current on the ac side returns to zero. In total, the ESS experiences a peak power flow of approximately 3 kW, however since this lasts for much less than a 0.1 s, the total energy transfer is less than 100 J.

It is noted that during the CM insult transient, the voltage on both the primary and secondary sides of the DAB is maintained within $\sim 0.07\%$ of its desired set-point. Furthermore, there is no evidence of the primary-side CM insult having any effect on the load-side behavior. Compared to conventional magnetic transformer, the SST responds much more desirably to a CM insult, with only a minor and transient impact on primary side currents, and no impact on the the SST regarding input/output behavior.

V. Conclusion

This work presents an SST design that is able to control the CM component of ac grid currents. It is intended to replace existing grid infrastructure which today is susceptible to both naturally occurring and man-made CM insult threats. The power electronics and controls architecture of the proposed SST have been described, and simulation results of the SST responding to a CM insult are provided. Future work related to this research will focus on modeling and developing controls for the proposed SST in representative grid HEMP/GMD event scenarios, and will focus on developing/testing a hardware prototype.

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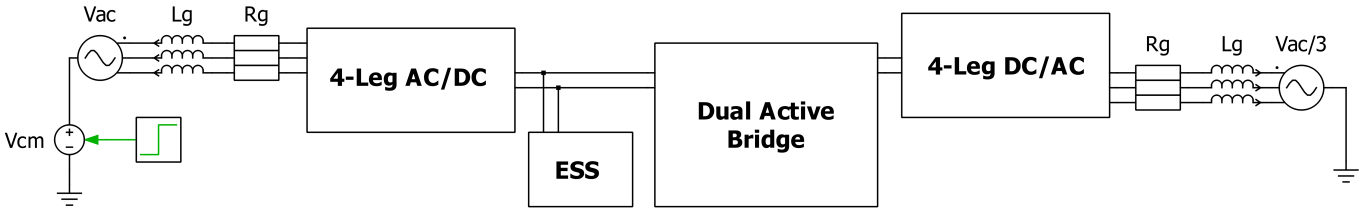
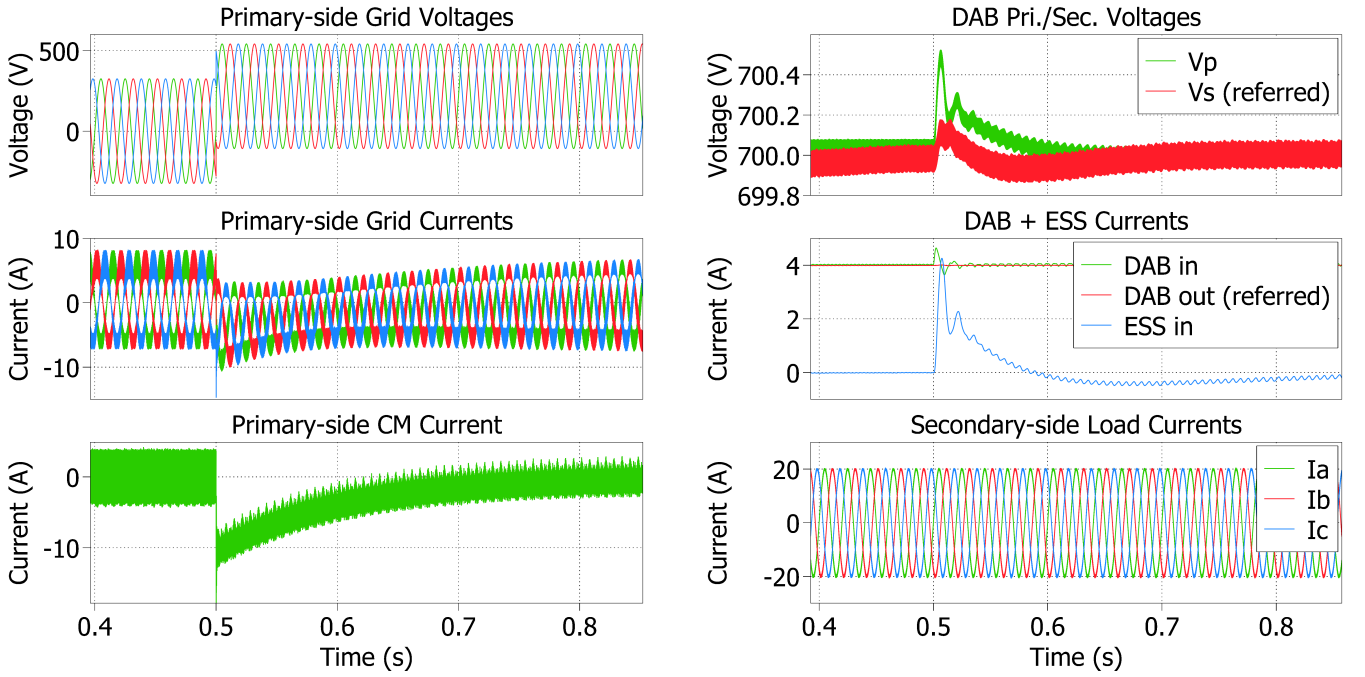


Fig. 10: Simulation model of proposed SST, subjected to a CM insult



(a) Grid-side dynamic behavior of SST in response to CM voltage insult. A feedback PID regulator returns the CM current to zero after a brief transient.

(b) DC and output dynamic behavior of SST in response to CM voltage insult. Current supplied to ESS temporarily increases as energy from CM insult is transferred to the dc-side.

Fig. 11: Dynamic behavior of SST in response to CM voltage insult.

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