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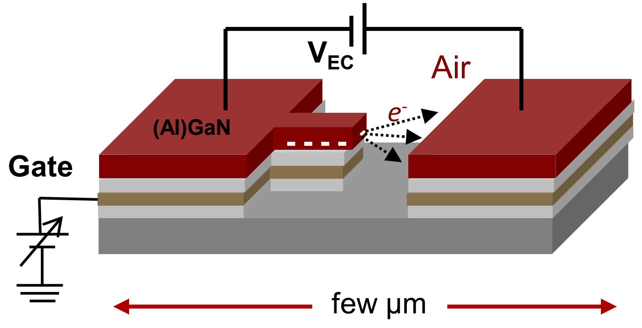

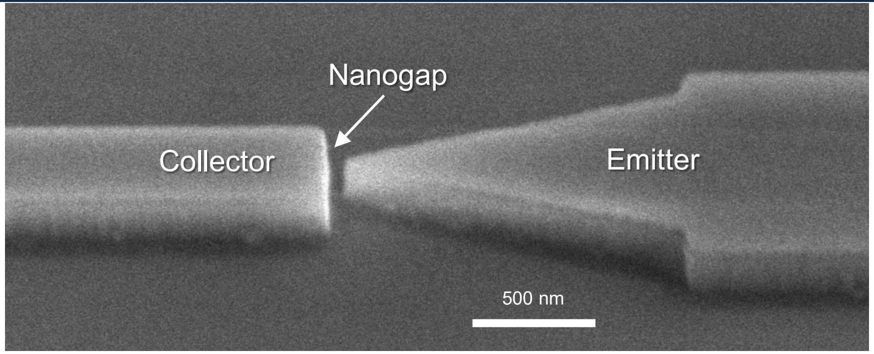

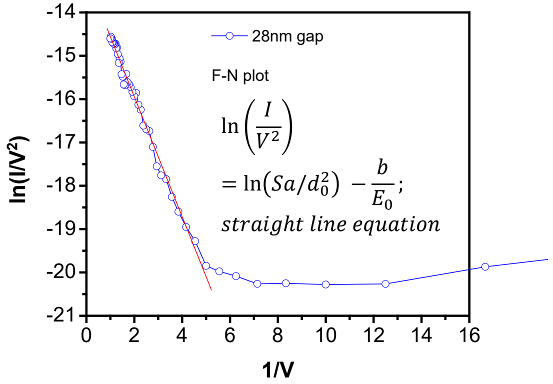

GaN Vacuum Nanoelectronics

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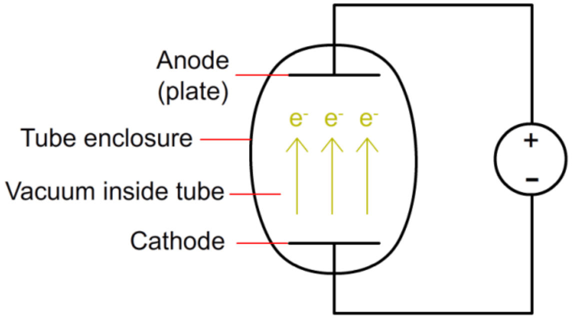
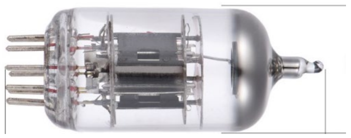
Vacuum Electron Devices (VEDs)

- Silicon solid state devices began to replace vacuum tubes > 60 years ago
- But vacuum electron devices (magnetrons, traveling wave tubes, klystrons, etc.) have distinct advantages and are still in use!
  - **Communication:** Radar, RF broadcasting
  - **NASA:** Satellite communications, electronics for space missions
  - **Commercial/Industrial:** Microwave ovens, CRTs, industrial RF heating, THz technologies, Microwave electronic applications

Vacuum electron device diagram

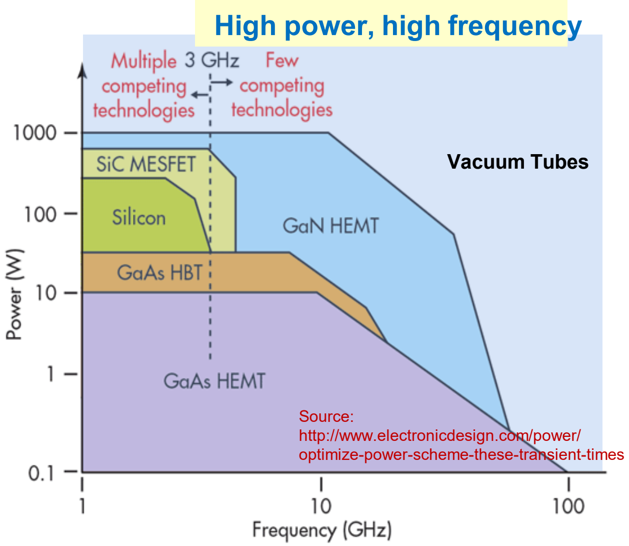




https://www.engineering.com/ElectronicsDesign/ElectronicsDesignArticles/ArticleID/16337/Vacuum-Tubes-The-World-Before-Transistors.aspx

Advantages: operation at higher frequencies, power, temperature, radiation than solid-state semiconductor devices

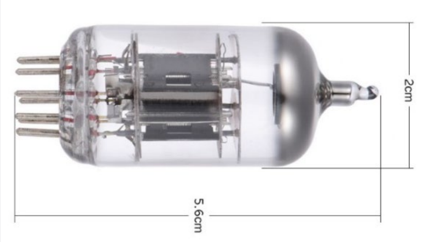
- **Ballistic transport in vacuum channel** (vs. scattering in solid channel)
- **No heat generation** during electron transport in vacuum
- **High dielectric breakdown** (Dielectric strength of perfect vacuum = 10^{12} MV/m)
- Operation in **harsh environments (radiation, temperature)**: no junction, vacuum channel unaffected



Drawbacks of vacuum tubes: Size, cost, energy efficiency (thermionic emission), lifespan, lack of integration, vacuum requirement

On-chip solid-state vacuum electronics

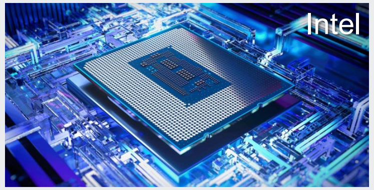
On-chip vacuum nanoelectronics: Combines advantages of vacuum electron & semiconductor devices!



Vacuum: high frequency/voltage,
EMP/radiation hardness, high T operation

BUT: Bulky, power hungry, fragile, lack of integration

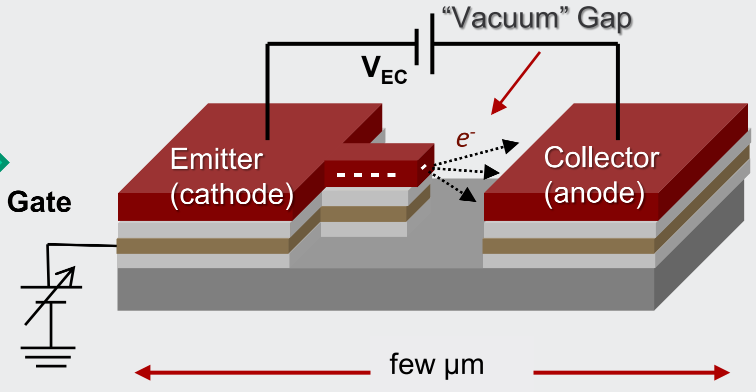
+



Semiconductor: miniaturization, integration, energy efficiency, cost, reliability

BUT: Heating, limited electron mobility, dielectric breakdown

Solid-state vacuum electronics!

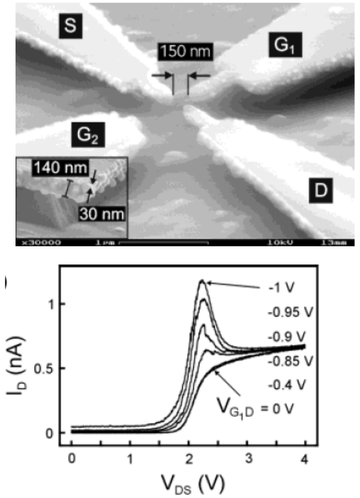


Hypothesized advantages of solid-state vacuum electronics

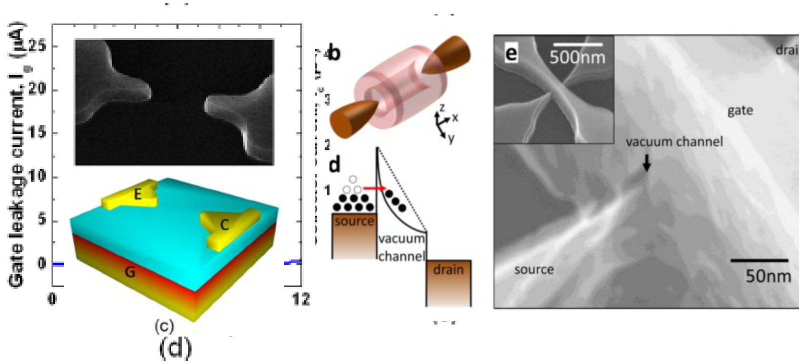
- **Cold field emission** for energy-efficient operation & **operability in air** (for gap sizes < mean free path of e^- in air)
- **High breakdown field:** Measurements of field emission from planar GaN show a vacuum breakdown field of ~36 MV/cm, ~ **10 times higher** than that the breakdown field of GaN (~3 MV/cm)
- **Ultra-fast response/switching time:** transit time of e- across vacuum gap can approach speed of light
- **EMP resilience**: no dielectric breakdown or p-n junction to induce second breakdown effects
- **High T operation**: no p-n junction to damage; transport across gap not affected by temperature
- **High radiation hardness:** - no p-n junction, small cross-section

“Nanogap” Vacuum Electronics (~2012-present)

- **Nano-scaling** of cathode-anode gap/channel (e.g. < 200 nm)
- Enhancement of local electric field: **reduction of operating voltage and emitter sharpness requirement**
- **Operable in air:** vacuum channel < mean free path of electron in air (~500 nm)

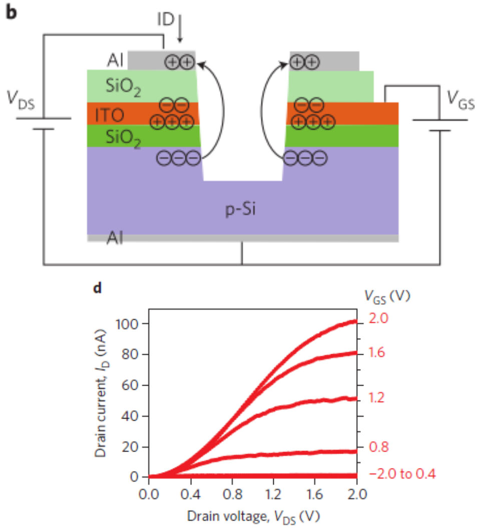


Lateral field-emission triode at atmospheric pressure on SOI
Pescini et al., Adv. Mat. (2001)

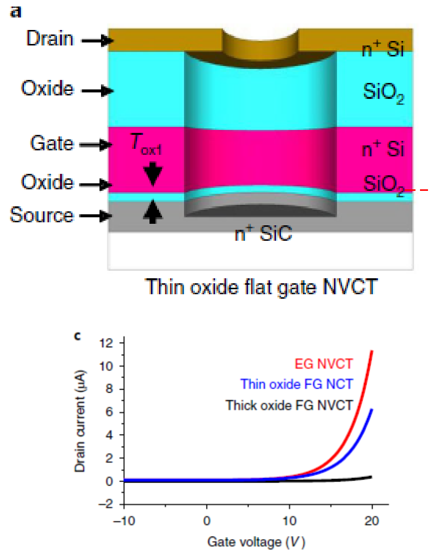


Lateral back-gate-insulated & surround gate nano vacuum channel transistor
Han et al., APL (2012), Han et al., NL (2017)

- NASA: vacuum-free “vacuum” Si transistor with estimated cutoff frequencies to **460 GHz** (2012)
- Operating **V < 5**, I > 3 uA (2017)



Vertical nano-void vacuum channel FET on Si
Srisonphan et al., Nat. Nanotech. (2012)



Vertical SiC vacuum channel transistors
Han et al., Nat. Elec. (2019)

New class of solid-state “nanogap” vacuum electronics have strong potential for high-speed, resilient electronics, but outstanding challenges remain & further R&D needed!

GaN: A Superior Platform for Solid-State Vacuum Nanoelectronics?

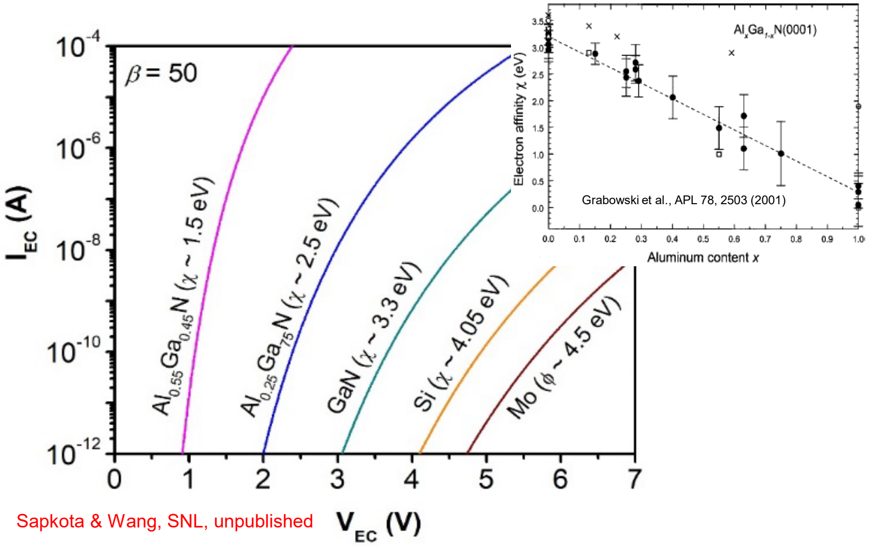
1. Low voltage field emission

Fowler-Nordheim (FN) equation

$$J = A\left(\frac{\beta^2 V^2}{\phi d^2}\right)\exp\left(-\frac{B\phi^{3/2}d}{\beta V}\right)$$

φ ➔ work function;
φ ~ χ (electron affinity) for n-type semiconductor

GaN: low χ ➔ Low voltage field emission

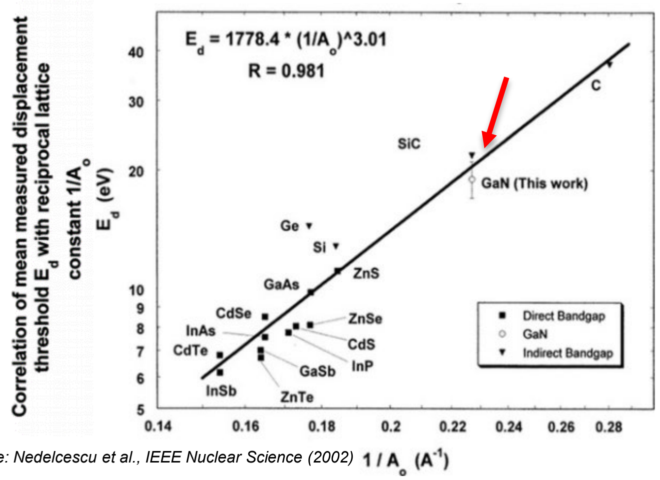


Sapkota & Wang, SNL, unpublished

2. Stability and reliability

GaN has significantly higher bond strength than Si

- ✓ Resistance to degradation
- ✓ Chemical stability
- ✓ Operable at high temperature
- ✓ Radiation hardness

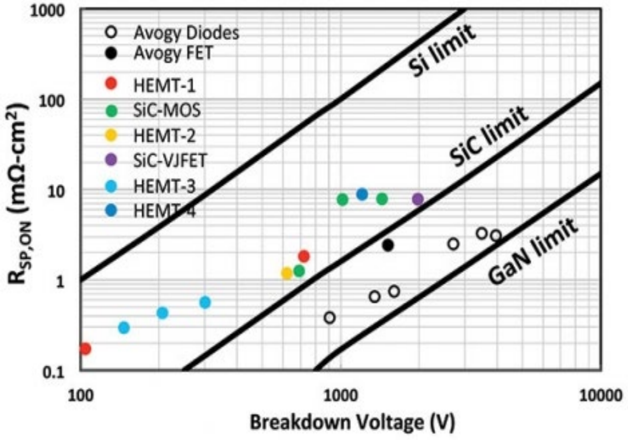


Source: Nedelcescu et al., IEEE Nuclear Science (2002)

3. High Power Operation

GaN has High Breakdown Field

- ✓ 3.3 MV/cm vs 0.3 MV/cm for Si
- ✓ High power operation
- ✓ High frequency operation



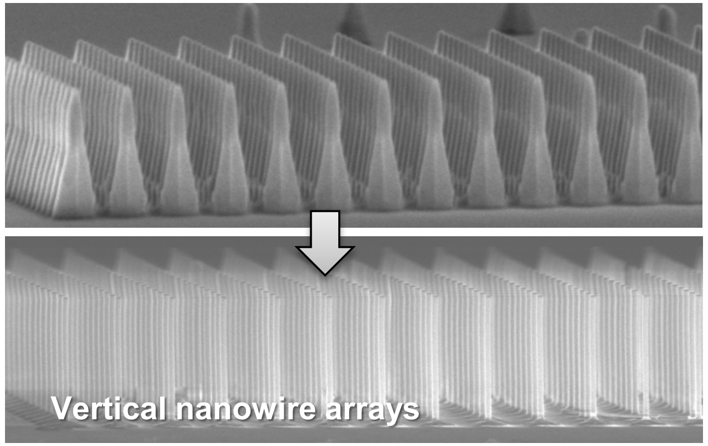
Source: https://compoundsemiconductor.net/article/98990

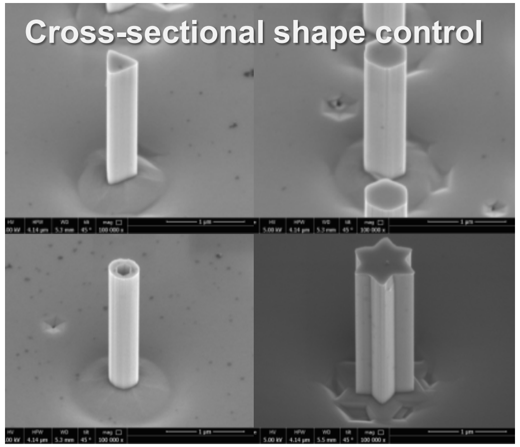
4. Mature & scalable materials & device platform (commercial UV-visible, LEDs, lasers)

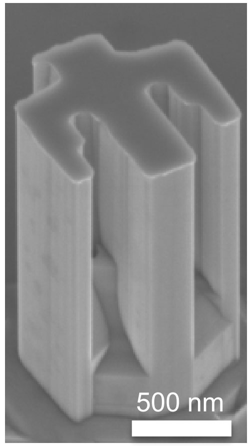
Enabling Capability: Top-Down 3D GaN Nanofabrication

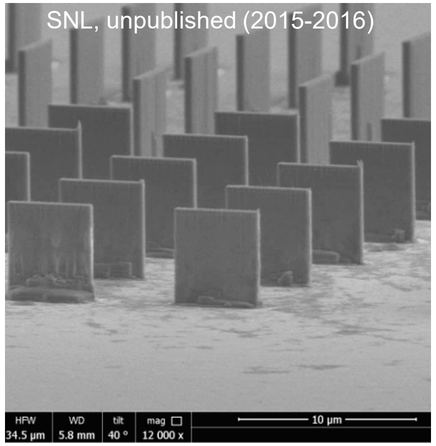
High quality, smooth & damage-free GaN-based nanostructures

Two-step dry + wet (KOH-based) GaN vertical etch

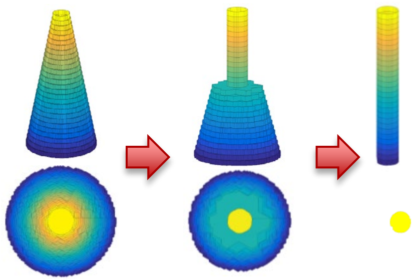








Simulation of facet etch evolution

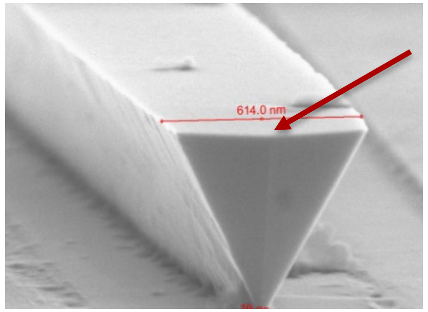


Q. Li et al., *Optics Express* **19**, 25528 (2011)

Q. Li et al., Opt. Exp., **20**, 17873 (2012)

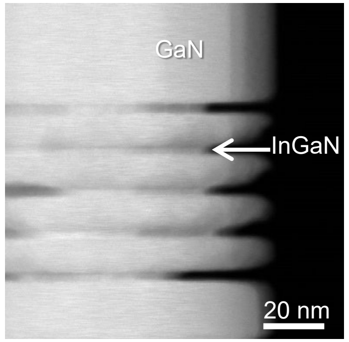
Li, Changyi, et al., *Nanoscale* ***8***, 5682 (2016). …etc.

GaN undercut etch



Sharp emitter geometry for enhanced field emission

(In)GaN lateral etch



Selective removal of quantum wells allows for **ultrathin** vertical nanogap vacuum channel

Xiao et al, Elec. Acta 162, 163 (2015)

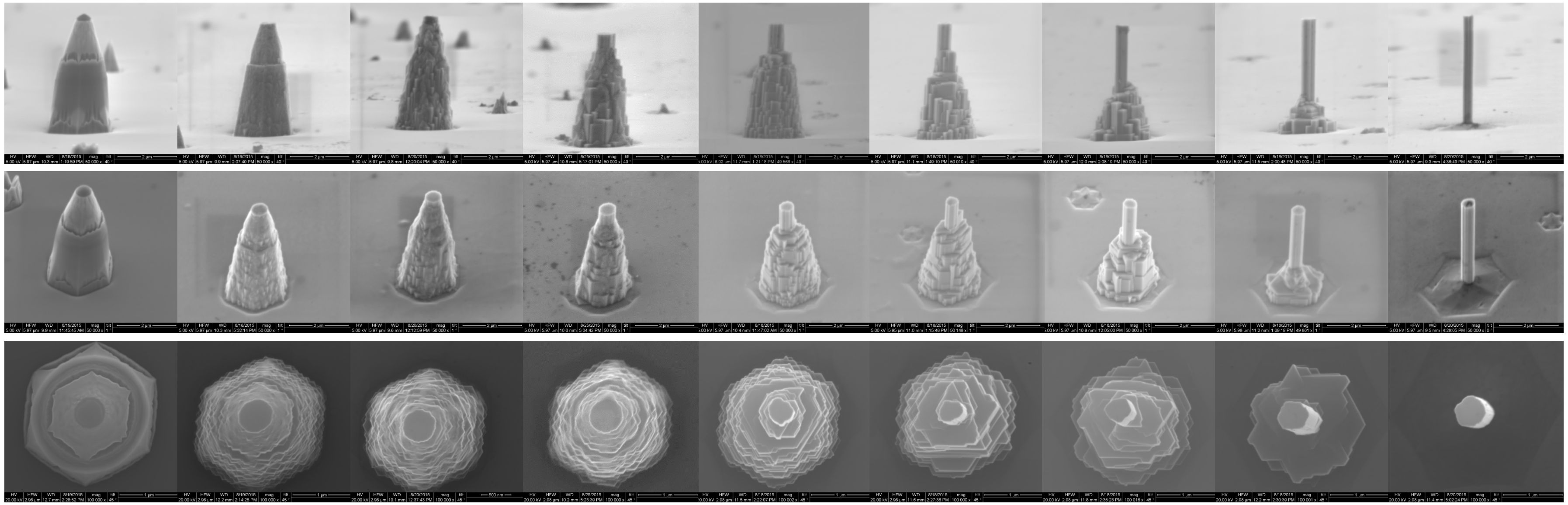
Wet etch evolution for nanowires

As ICP etched | 1 min | 2 min | 5 min | 10 min | 15 min | 20 min | 30 min | 52 min

Side view

45°

Top view

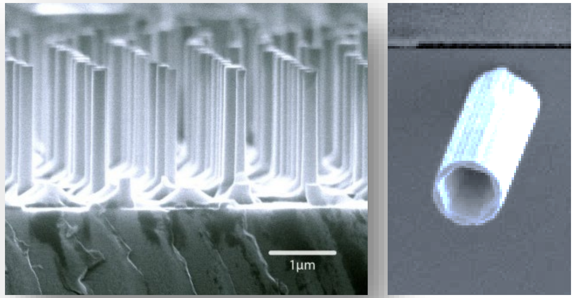


AZ400K, 65^{o}C

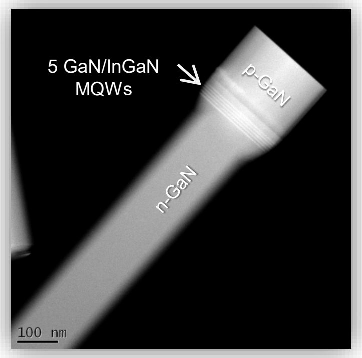
Wet etch proceeds “vertically” rather than horizontally

Top-down fabricated nanowire photonics

Precision top-down fabrication *controlled geometries*

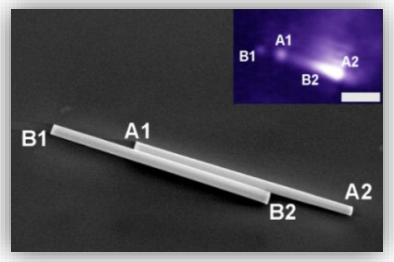


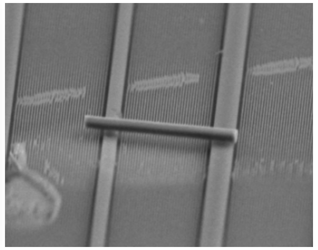
Axial nanowire LED "flashlight"



Q. Li et al., *Optics Express* **19**, 25528 (2011)

Mode, polarization and beam shape control in GaN nanowire lasers

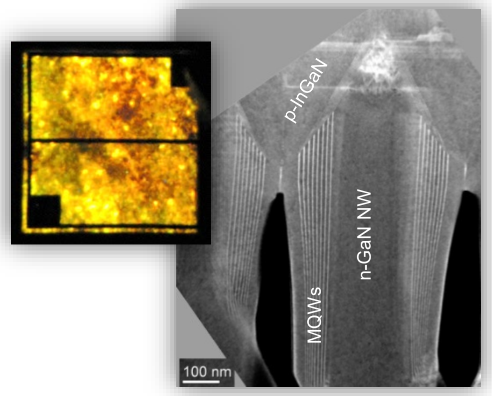




Q. Li et al., *Optics Express* **20** 17874 (2012)
H. Xu et al., *Appl. Phys. Lett.* **101** 113106 (2012)
H. Xu et al., *Appl. Phys. Lett.* **101** 221114 (2012)
Li, Changyi, et al. *Nanoscale* **8**, 5682 (2016).

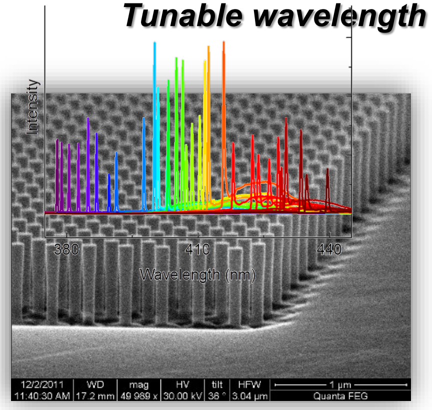
J.B. Wright et al., *Appl. Phys. Lett.*, 104, 041107 (2014).
C. Li et al., *ACS Photonics*, **2**, 1025 (2015).

Radial nanowire LEDs, solar cells

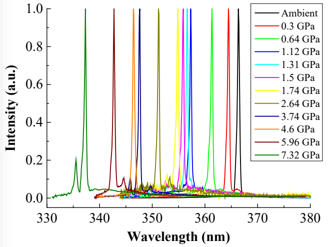


J. Wierer et al., *Nanotechnology* **23** 194007 (2012)
Riley, J. et. al., *Nano Lett.* **14**, 4317 (2013).
G. T. Wang et al., *Phys. Stat. Solidi A*, **211**, 748 (2014)

Tunable wavelength nanowire lasers

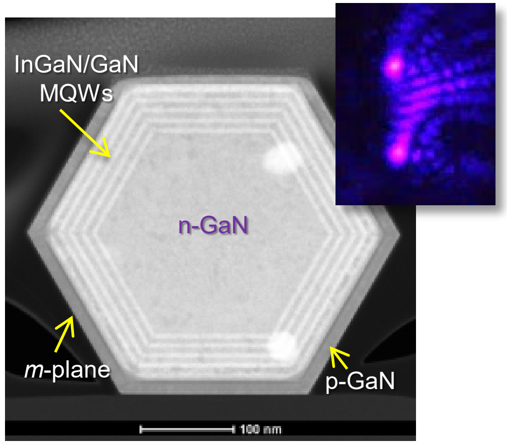


J.B. Wright et al., *Sci. Reports* 3, Art no. 2982 (2013) doi:10.1038/srep02982



S. Liu, C. Li, J. J. Figiel, S. R. Brueck, I. Brener, G. T. Wang, *Nanoscale*, *7*, 9581 **(2015)**.

Nonpolar core-shell nanowire lasers

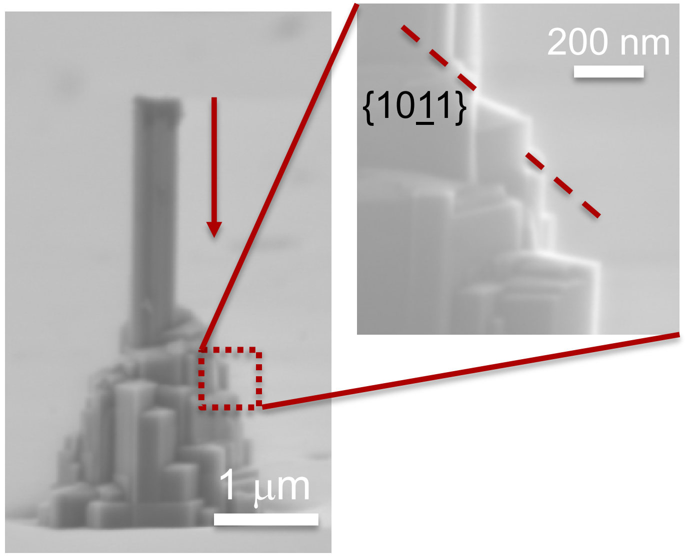


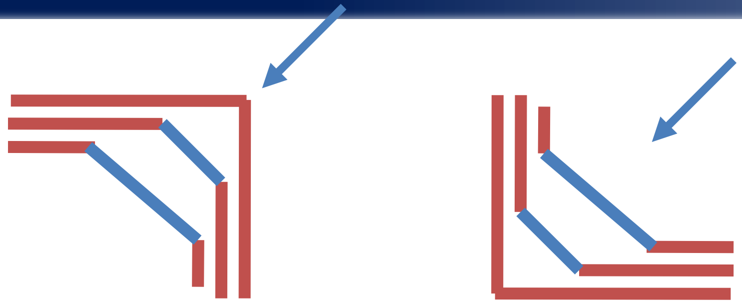
C. Li et al., *Nano Lett*, **17**, 1049 (2017)

Mechanism/Basis for evolution of facets during etching

What is the mechanism from *tapered to smooth vertical sidewalls* through faceting?

Slow etching: c-plane, m-plane
Fast etching: Semipolar $(10\bar{1}1)$

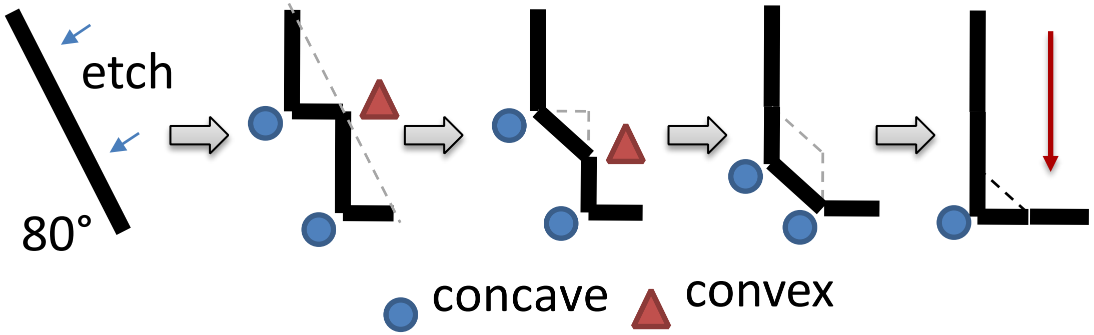




Convex
Fast etch facet persists

Concave
Slow etch facets persists

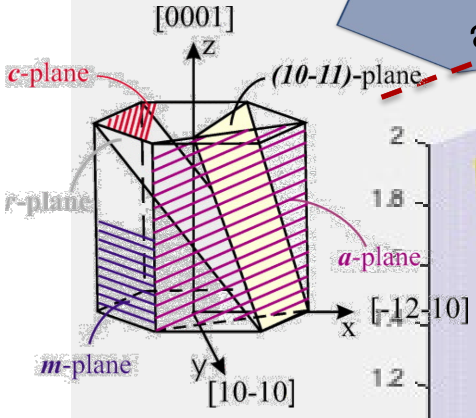
The facet etch sequence:



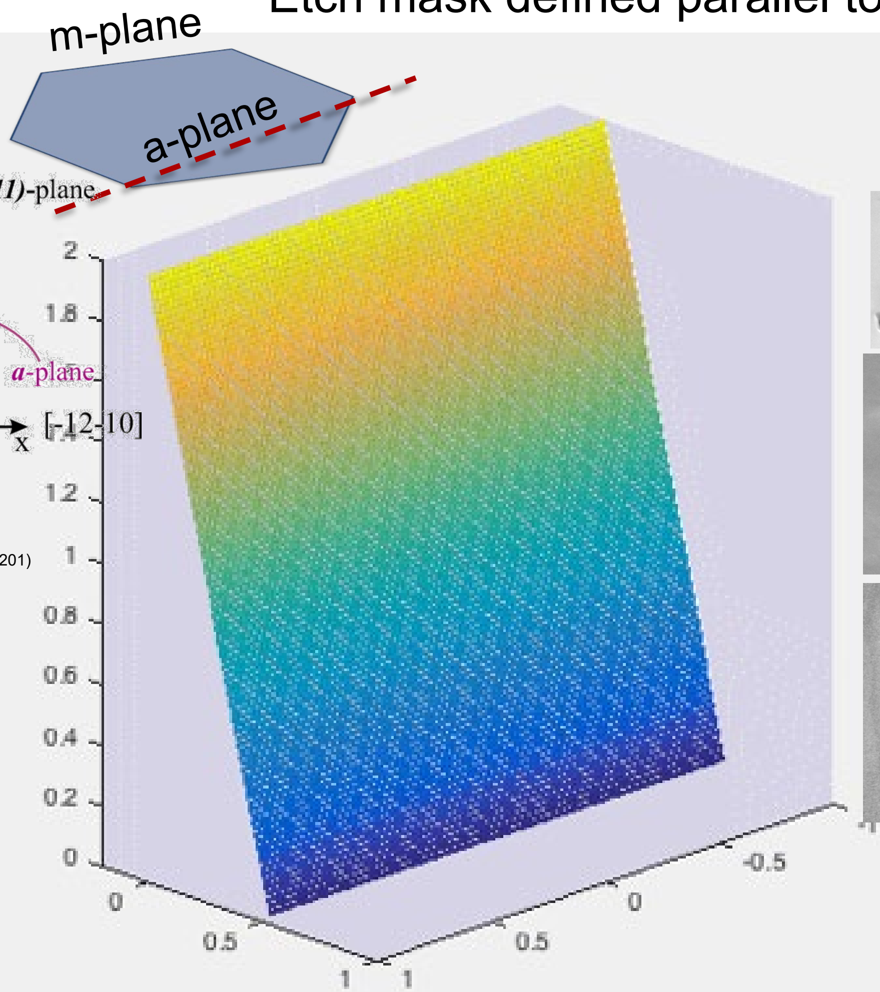
The appearance (disappearance) of fast (slow) etching facets in concave (convex) geometries is the basis of the etch mechanism

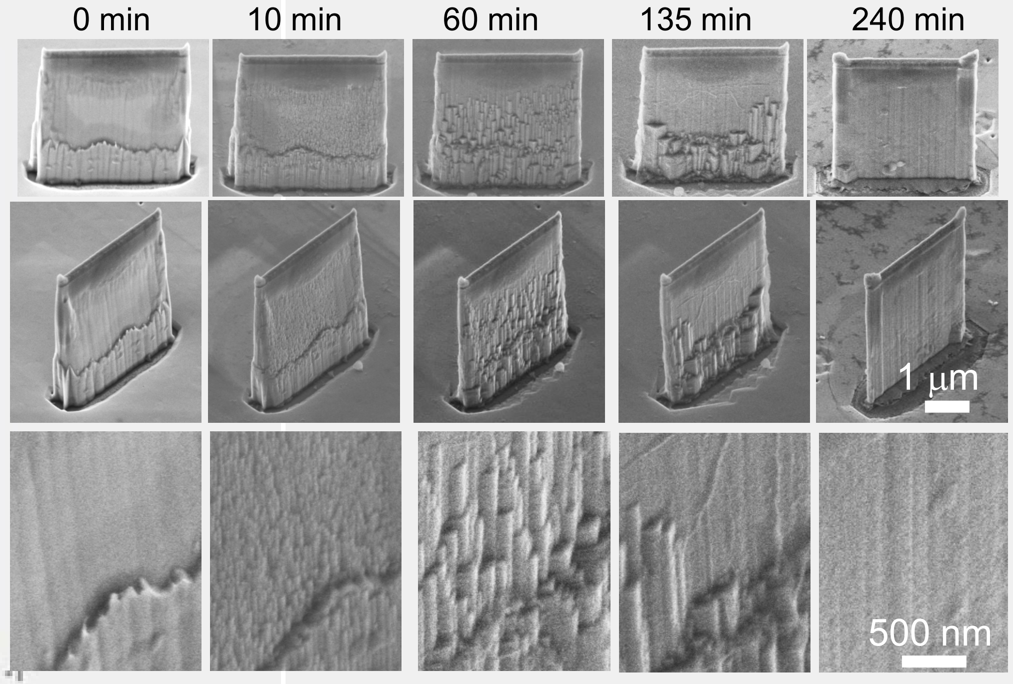
Etch evolution of a-plane wall

Etch mask defined parallel to *a*-plane



V. Darakchieva et al., JAP 108, 073529 (201)

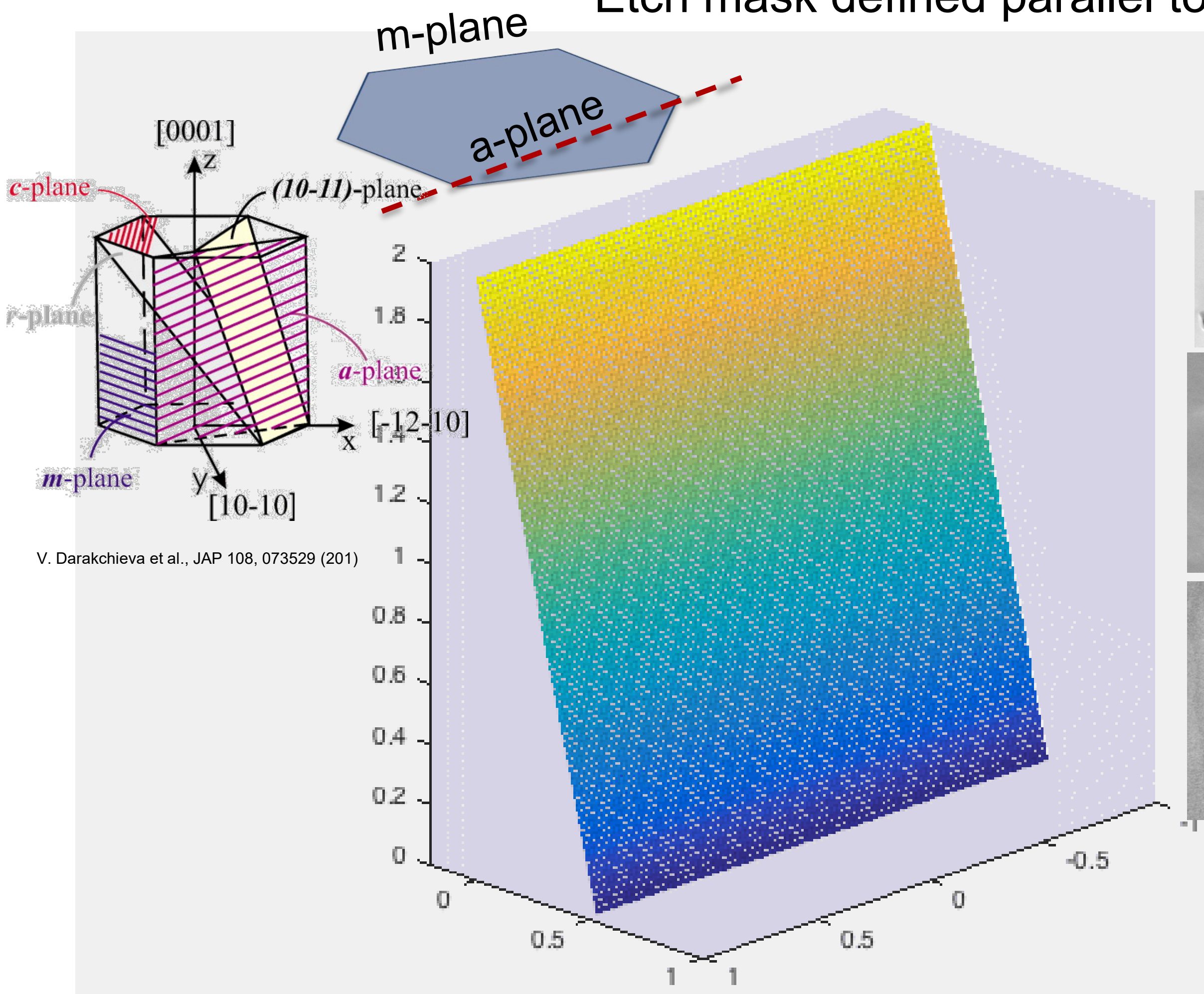




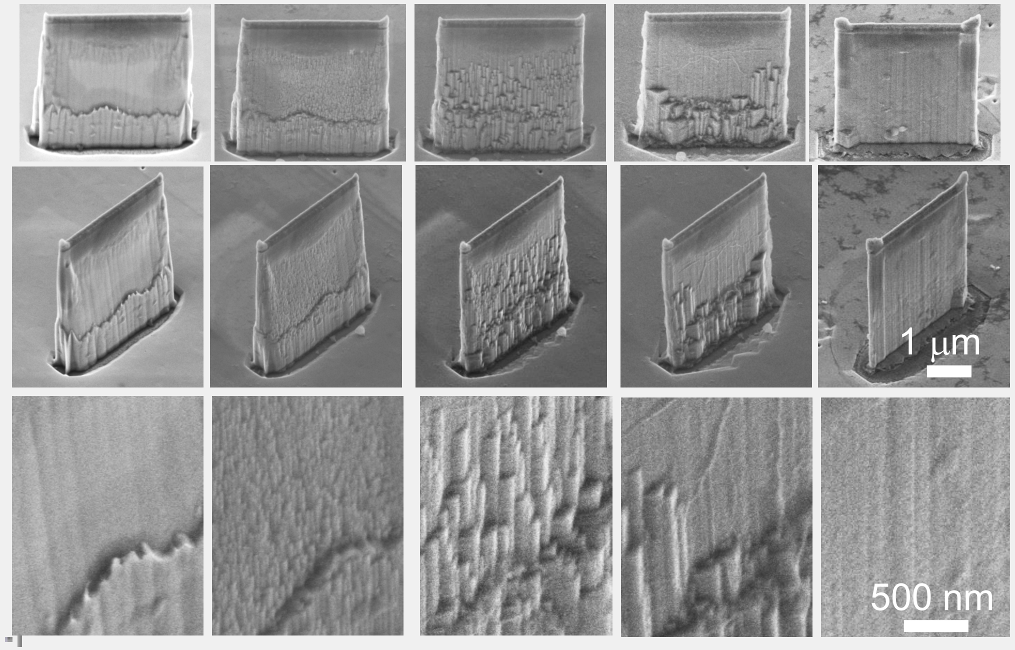
AZ400K, 65^{o}C

Etch evolution of a-plane wall

Etch mask defined parallel to *a*-plane



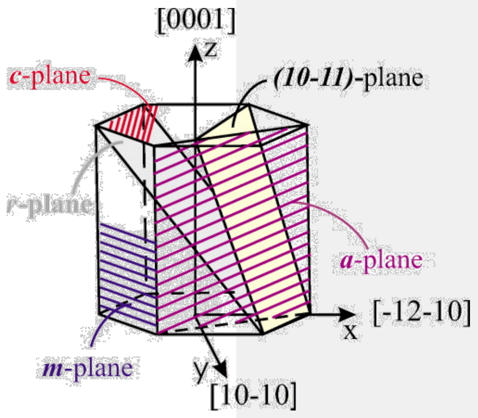
V. Darakchieva et al., JAP 108, 073529 (201)



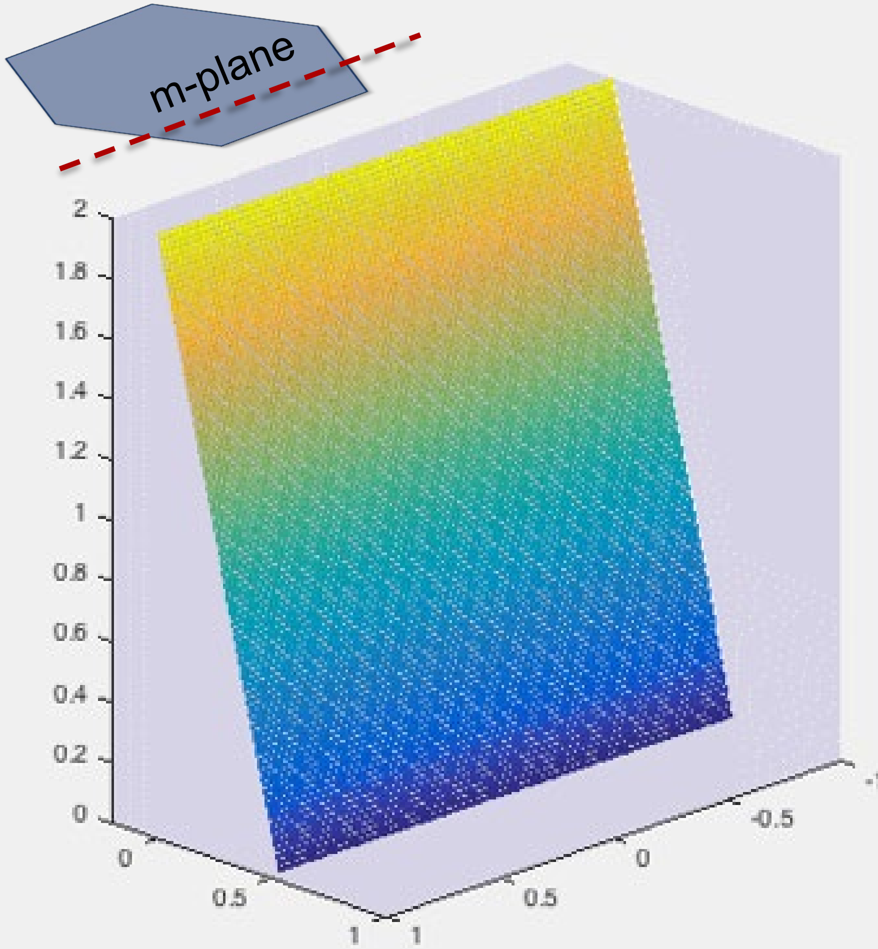
AZ400K, 65^{o}C

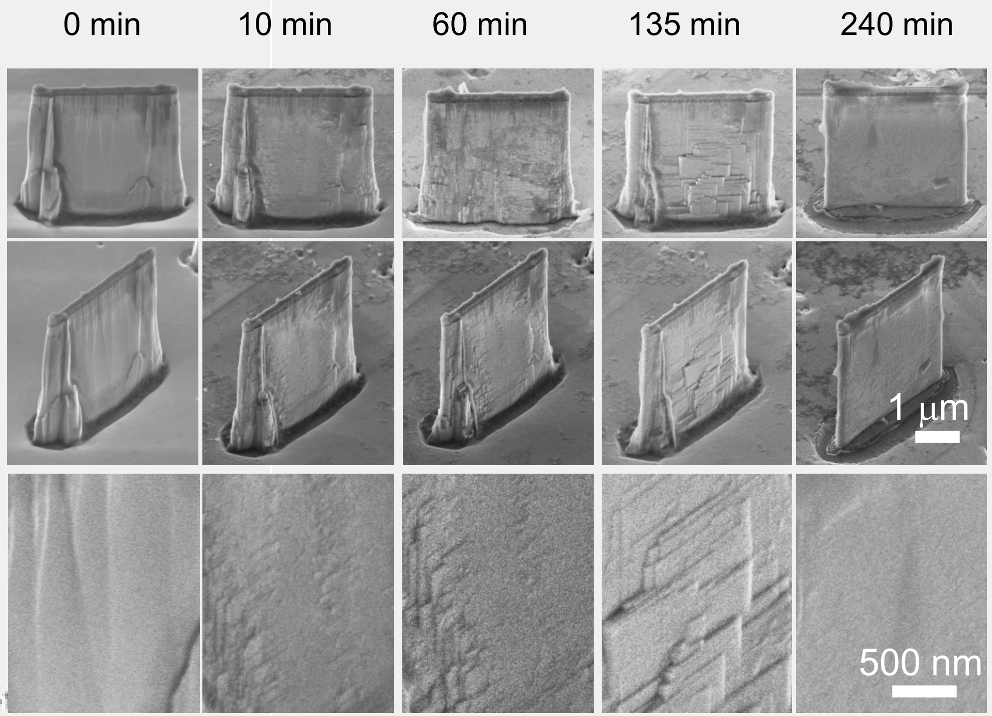
Etch evolution of m-plane wall

Etch mask defined parallel to *m*-plane



V. Darakchieva et al., JAP 108, 073529 (201)

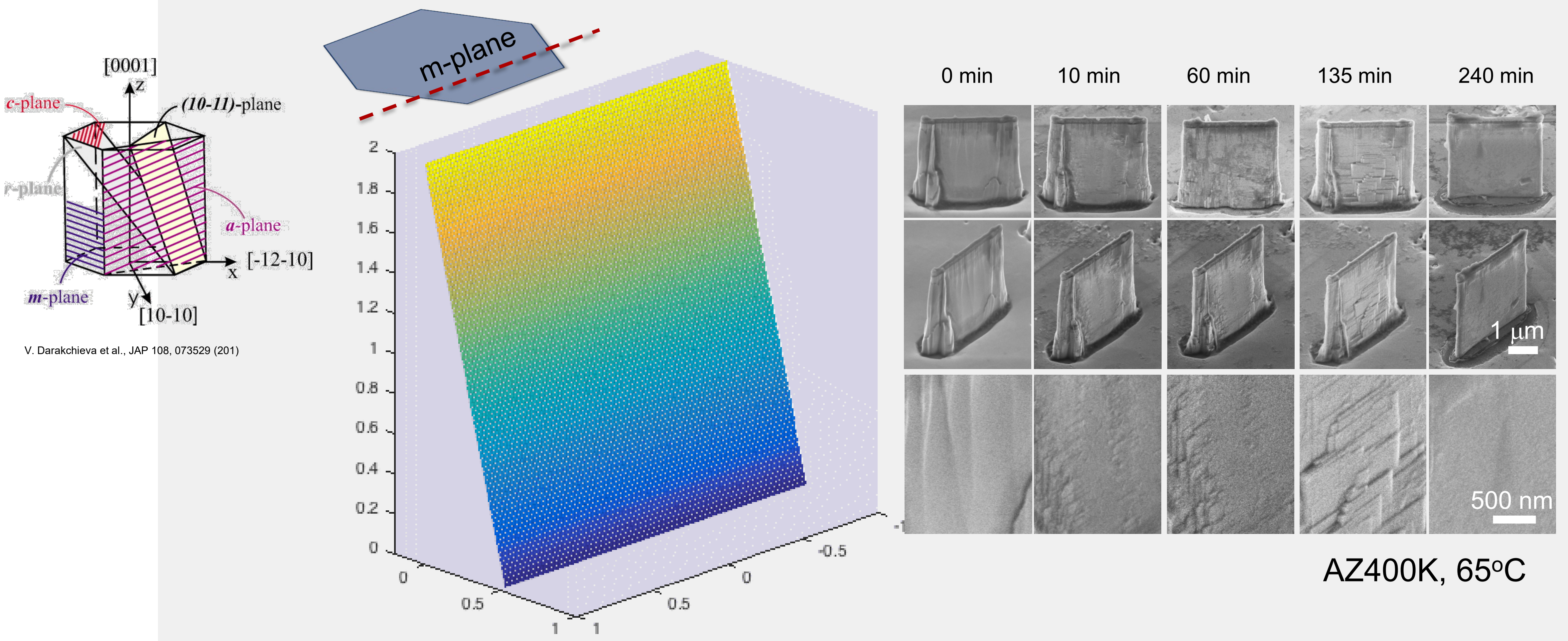




AZ400K, 65^{o}C

Etch evolution of m-plane wall

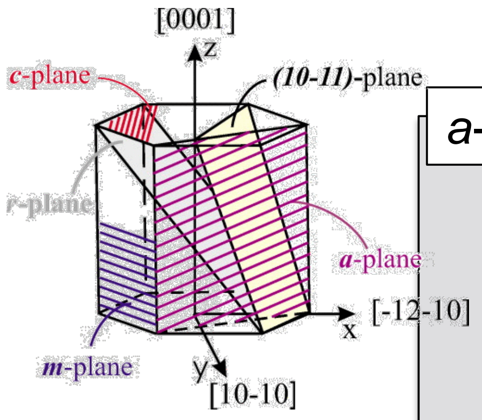
Etch mask defined parallel to *m*-plane



V. Darakchieva et al., JAP 108, 073529 (201)

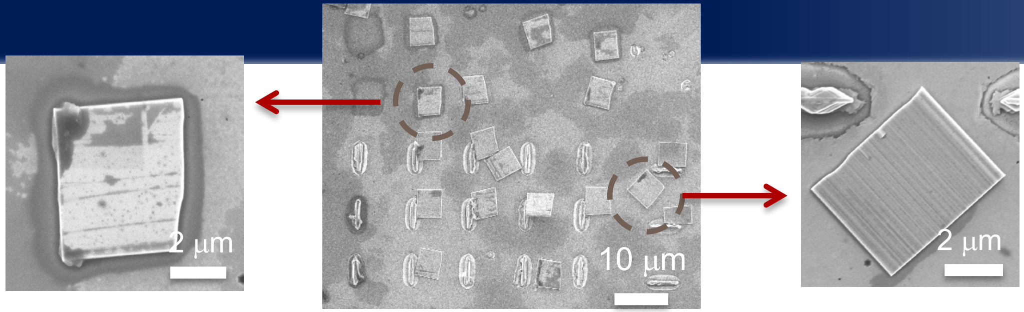
AZ400K, 65°C

Measured wet etched nanowall morphology by AFM

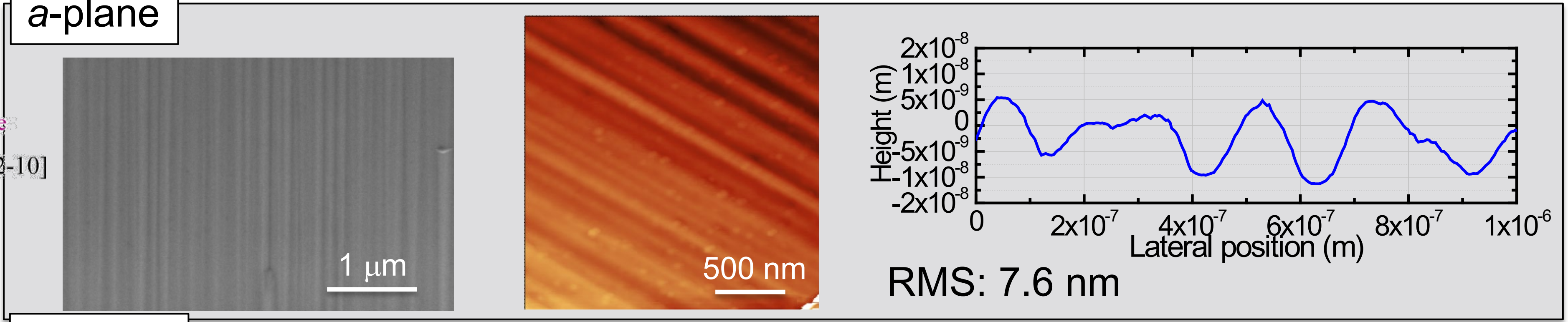


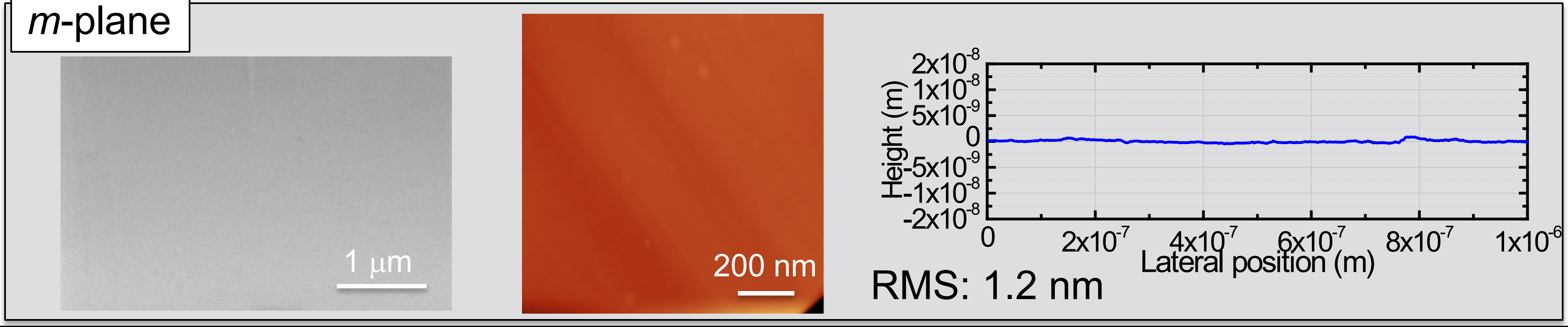
V. Darakchieva et al., JAP 108, 073529 (201)

m-plane wall



a-plane wall





Achieved atomically smooth m-plane surfaces through a two-step top-down process!

Fabrication: Integrated, lateral GaN nanoscale vacuum electron diodes

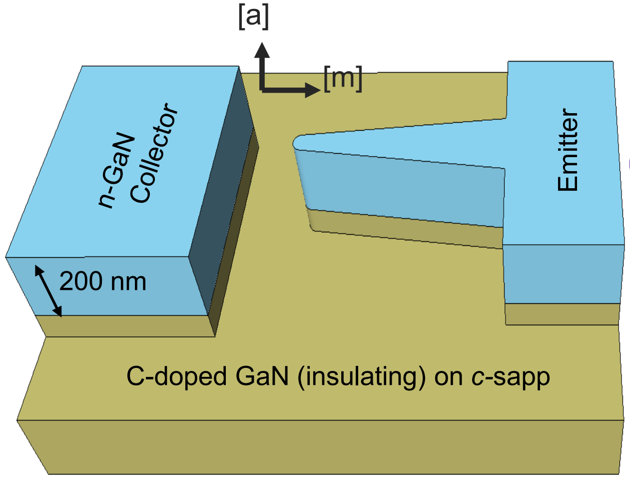
Sandia National Laboratories

III-N top-down fabrication process

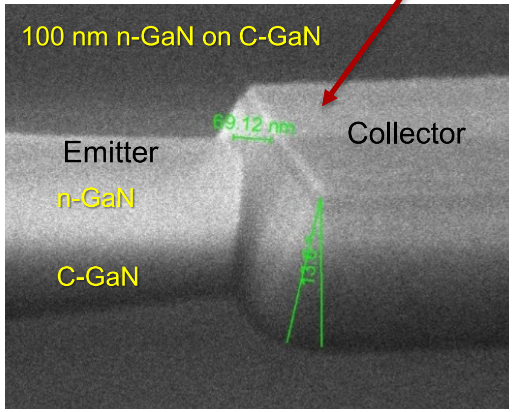
Electron Beam Lithography → Dry Etching (ICP/RIE) → Wet Etching (KOH based)

From our knowledge of KOH wet etching of GaN:

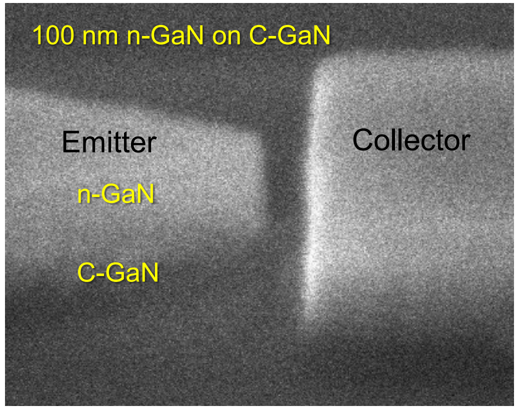
- Orient collector // to m-plane to avoid microfacet protrusions
- Limit wet etch time to reduce wedge retraction effect
- Consider dependence of wet etch on doping and composition



Ti/Au/Ni/Au ohmic contact layer on emitter & collector



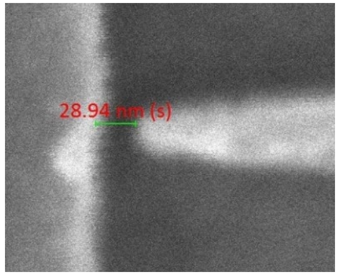
AZ400K wet etch



ICP dry etch:
Angled side walls – variable gap size, possible shorting at bottom, plasma sidewall damage

+ AZ400K wet etch:
Vertical side walls, cleared gap, removed sidewall damage, smoother m-face collector

~30 nm gaps and ~20 nm radius emitters routinely achievable!



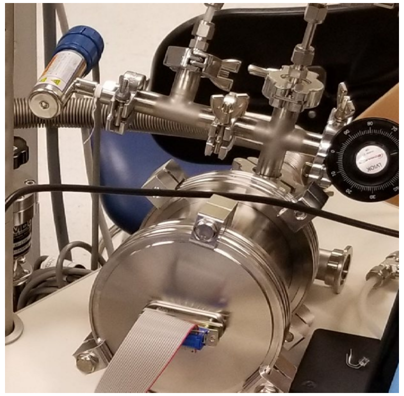
Device packaging and electrical testing

<u>Custom LabVIEW code</u>

- Automated measurements, greater control
- Improved accuracy, real-time data analysis
- Additional schemes: IV, stability, pulsed, time-dependent
- Multiple instruments for complex testing

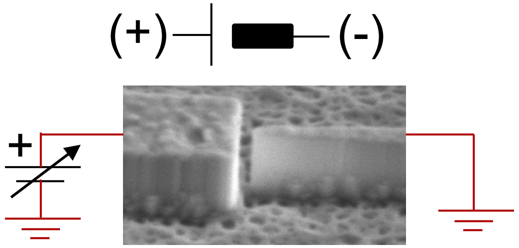
<u>Custom testing chamber</u>

- Pressure control: 1E-6 torr - Atmospheric

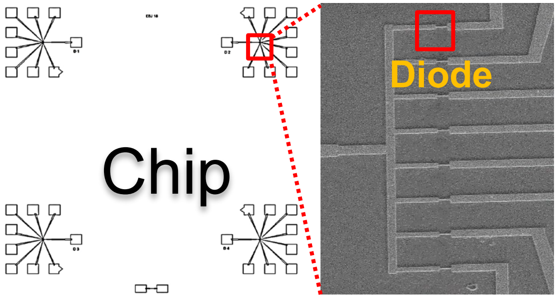


Home-made test chamber

Testing setup and symbol

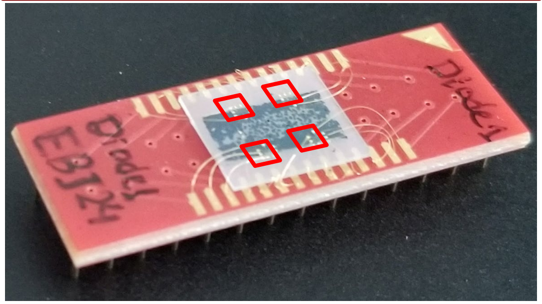


Electron Beam Lithography



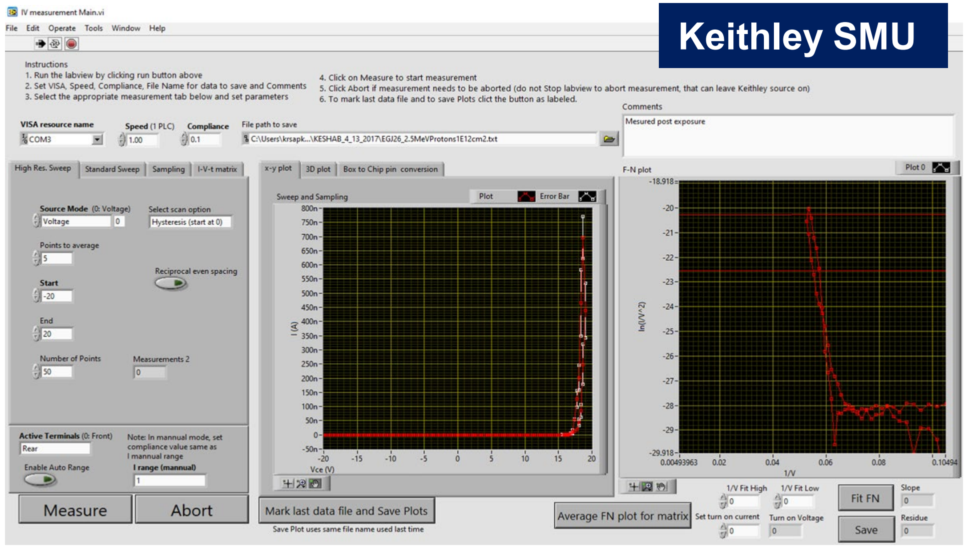
Pattern 28 vacuum channel diodes (4 regions) per chip

Wire bonding & Packaging



Wirebond and Package in a multi-pin chip carrier

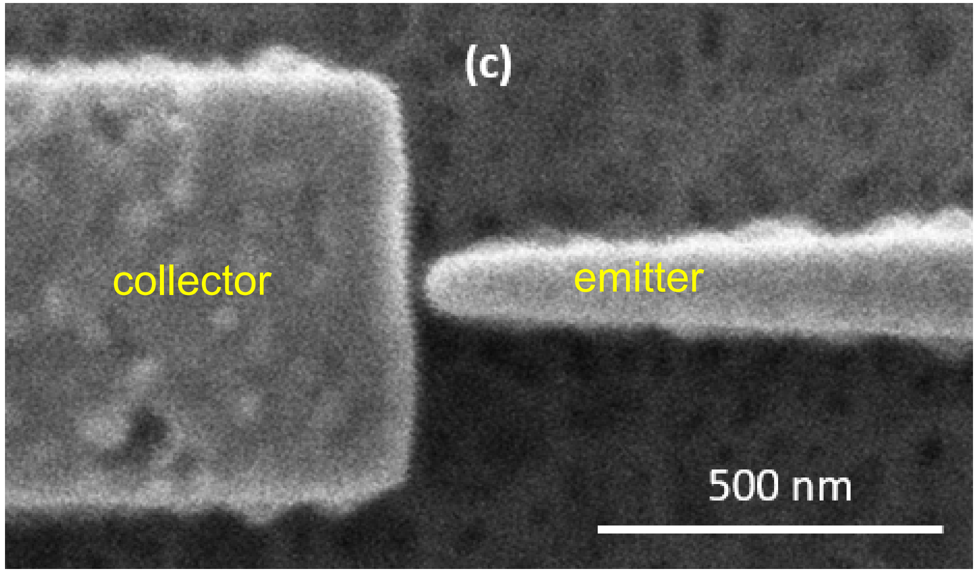
LabVIEW Program for the Electrical testing



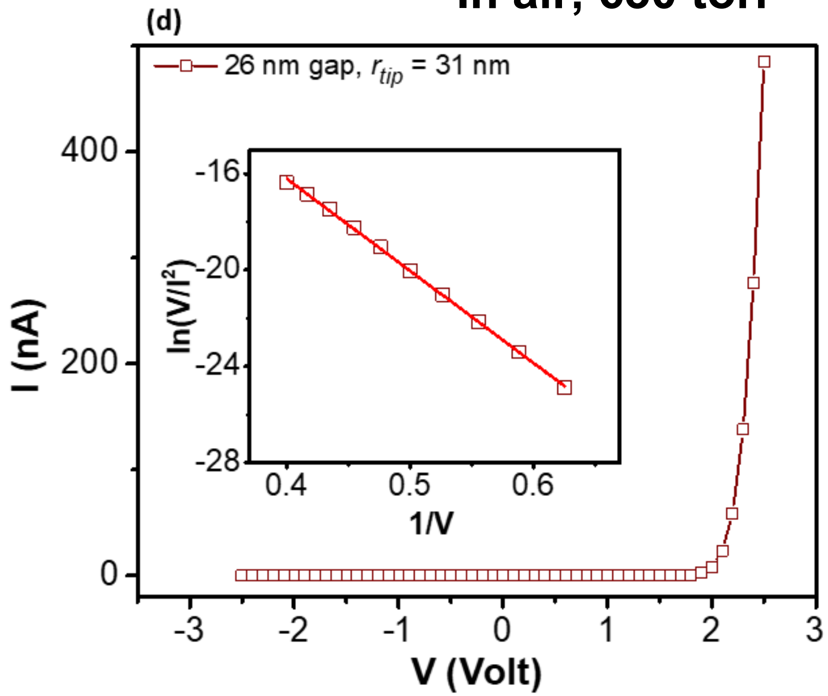
Working monolithic, on-chip GaN nanoscale vacuum electron diodes!

- Emitter tip radius ~ 31 nm; Nanogap size (emitter-collector separation) ~ 26 ± 5 nm
- **Low turn-on voltage (V_{on}) of ~1.8 V, high emission current (I_e) of ~485 nA at 2.5V!**
- **Field emission observed in air at atmospheric pressure (630 torr)**!
- I-V data good linear fit with the Fowler-Nordheim plot (confirms cold field emission)

In air, 630 torr



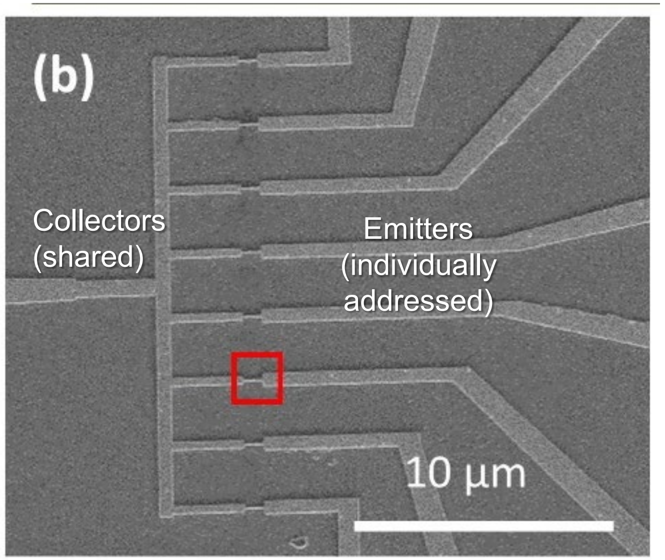
31 nm tip radius, **~26 nm** gap

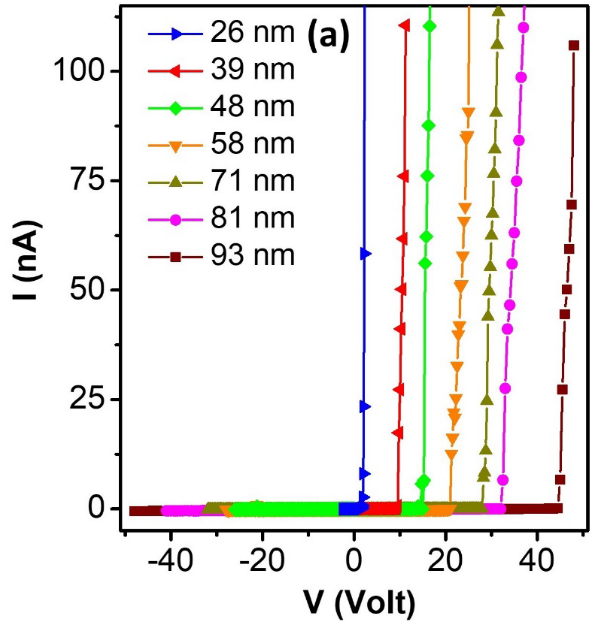


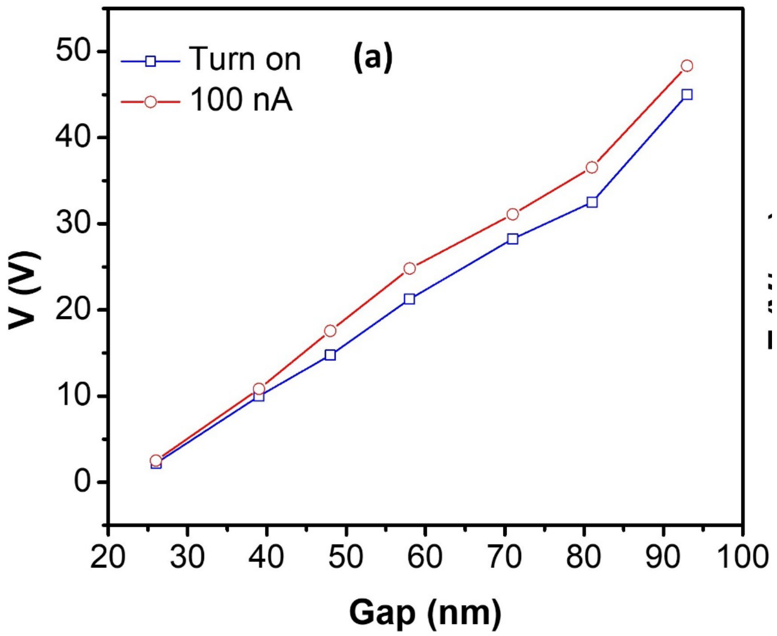
Nanogap Size Dependency of the Field Emission

Devices with seven nanogap sizes from ~26-93 nm were fabricated

- Emitter tip radius ~ 32 ±2 nm
- Field emission observed **from all seven devices (100% yield)** **<u>in air</u>** (atmospheric pressure), with very sharp current increase after turn on (turn-on V_{on}= V≥100 pA)
- I-V data: linear fit to the Fowler-Nordheim field emission equation (not shown)
- **Turn-on voltage increases *linearly* with increasing gap size**







Effect of Pressure on Nanogap Field Emission

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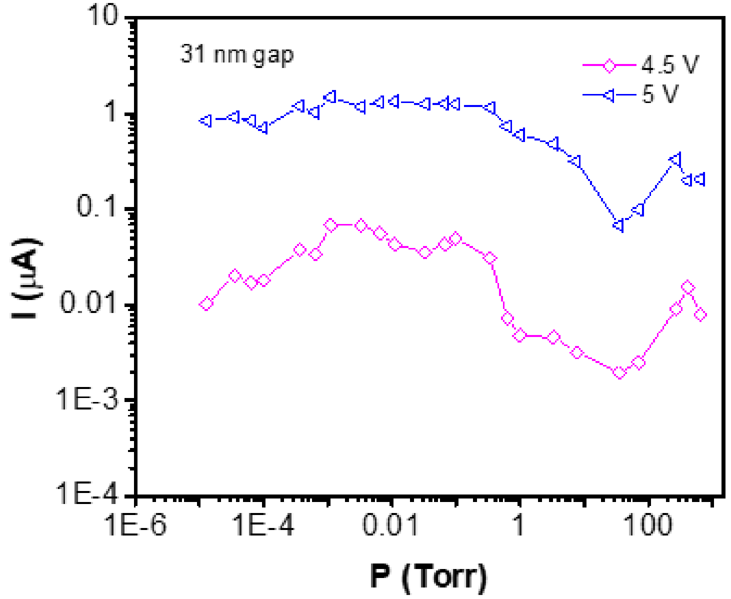
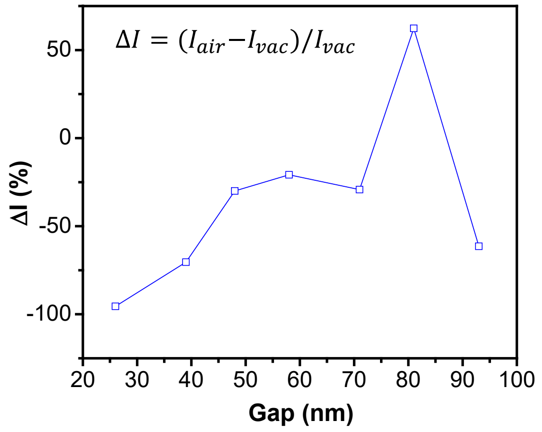
- **Assumption:** nanogap is vacuum-like if nanogap size << electron mean free path in air
- ***Does pressure actually affect field emission of nanogap device in this regime?***

Lateral GaN nanogap diodes measured from 5e-6 to 630 Torr (8 orders of magnitude)

- Performance at atmospheric pressure near to that at high vacuum (within factor of 10), can be compensated by slight boost in operating voltage
- *However, field emission is affected by pressure, but behavior complex (non-monotonic relationship)*

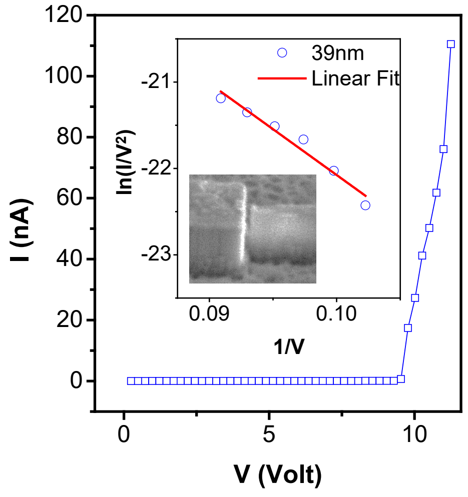




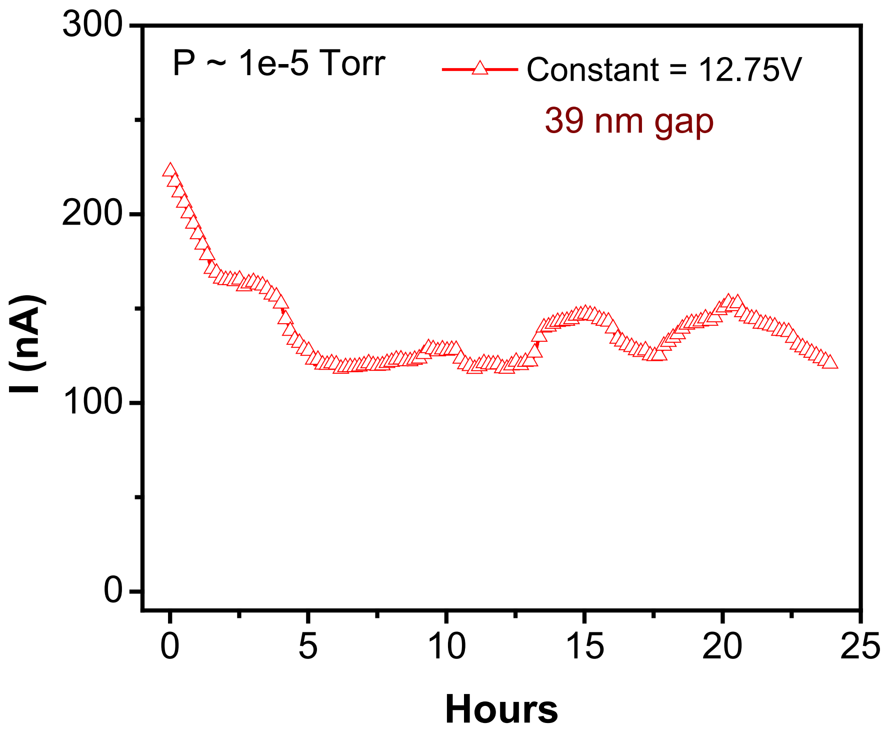
Reliability Measurements of GaN Nanogap Device (39 nm gap)

- **Continuously on** measurement: drop in current over first few hours, then stabilizes. Device performs for at least ~24 hours during continuous measurement (other device measured to 55 hours)
- **Pulsed** measurement: No degradation after 1.8×10^5 pulses at high currents (few μAs) (# pulses limited by measurement equipment)

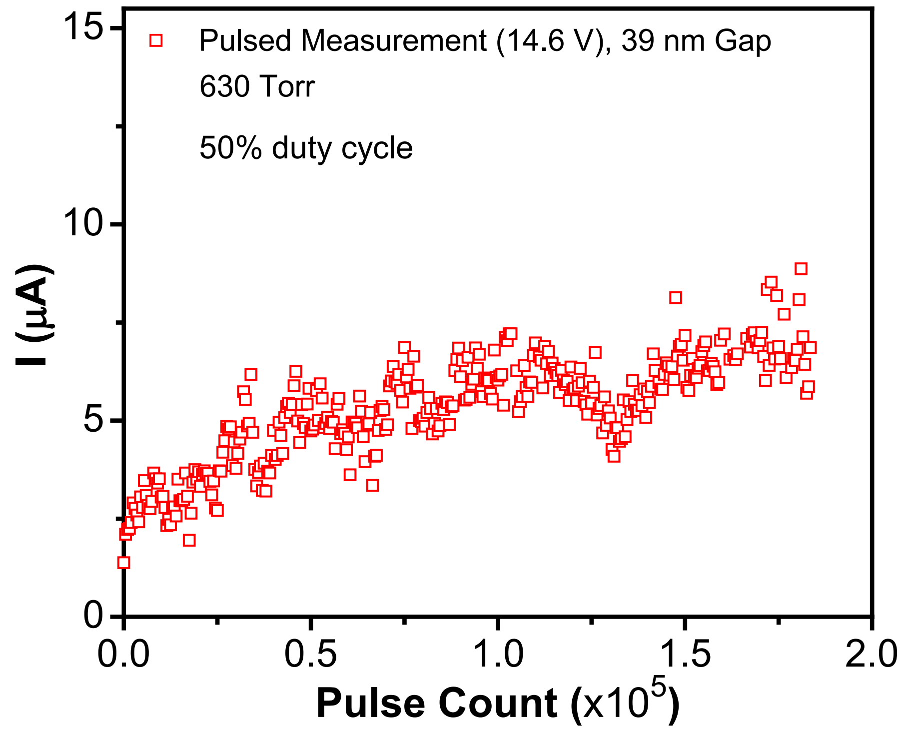
39 nm gap device I-V



Continuously On



Pulsed



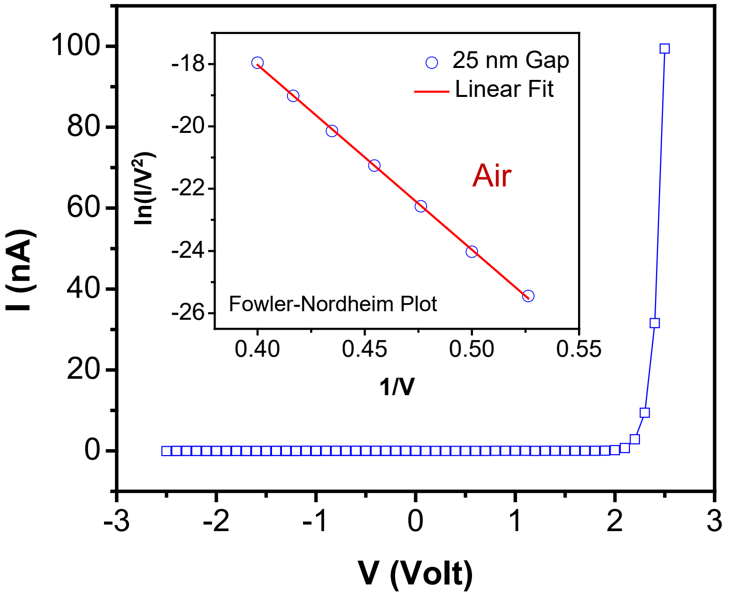
Effect of Emitter Tip Size on Field Emission

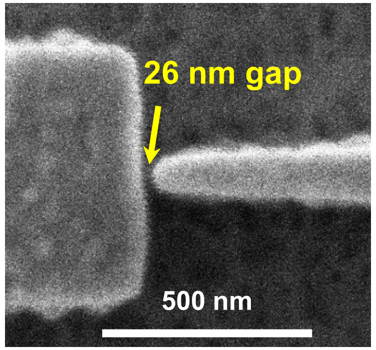
Sharper emitter is desired for lower voltage field emission

- Increases field enhancement β (depends on geometry)

$$J = A\left(\frac{\beta^2 V^2}{\phi d^2}\right)\exp\left(-\frac{B\phi^{3/2}d}{\beta V}\right)$$

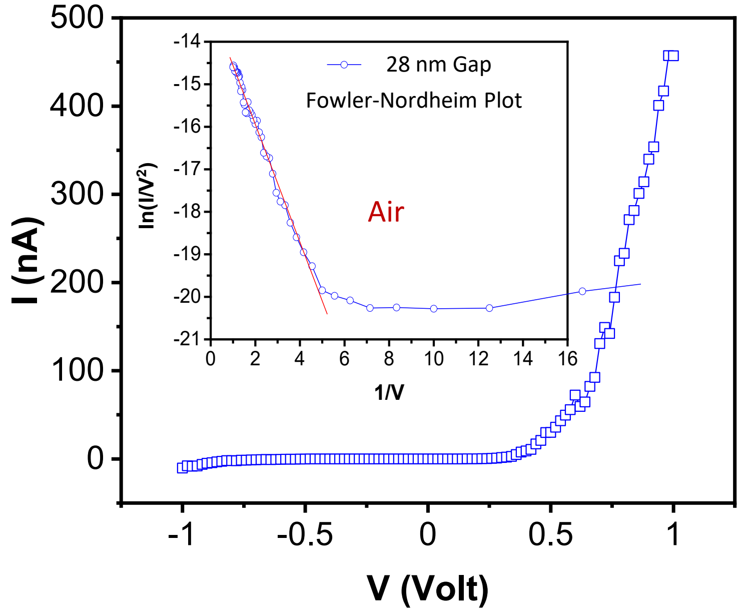
Emitter r_{tip} = 31 nm

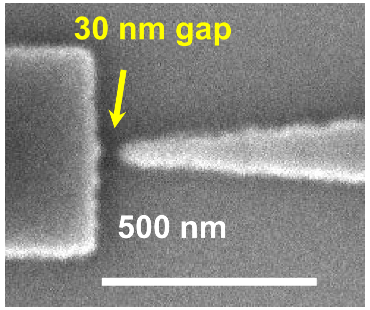




- Field enhancement factor (β) = 32
- Turn on voltage = **1.9 V** @ 50pA

Emitter r_{tip} = 17 nm





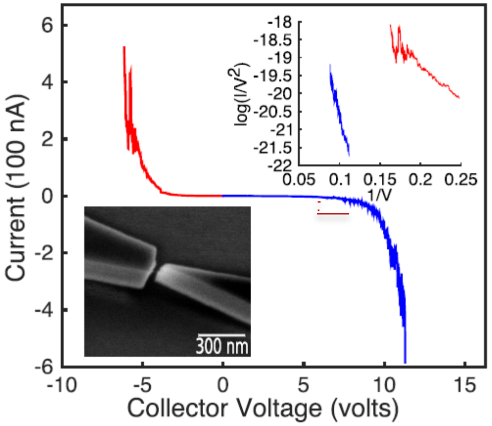
- Field enhancement factor (β) = 920
- Turn on voltage = **0.24 V** @ 50pA

Ultra-low turn-on voltage < 1 V achieved with 17 nm radius emitter!

Comparison of GaN to previous Si and SiC nanogap vacuum diodes

n-Silicon (200 nm) on 2000 nm SiO2

W.M. Jones et al., APPLIED PHYSICS LETTERS 110, 263101 (2017)



Gap/channel size: 22 nm

Tip radius: ~15 nm (est.)

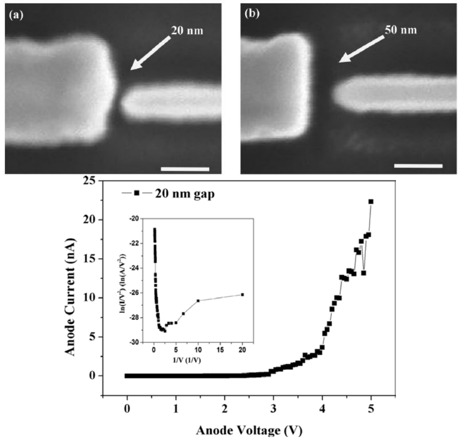
V_{on}: **~3.5 V**

I_e: 100 nA at ~4.8 V

In air? **No**

SiC nanowire (CVD grown & cut by FIB)

M. Liu et al., Journal of Vacuum Science & Technology B **35**, 031801 (2017); (R_{wire} = 0.015 Ohm-m.)



Gap/channel size: 20 nm

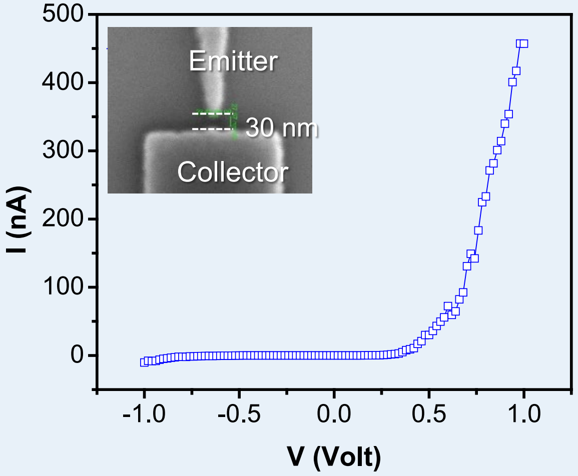
Tip radius: ~20 nm

V_{on}: **~2.6 V (est.)**

I_e: 22 nA at ~5.0 V

In air? **No**

This Work: n-GaN (200 nm) on C-GaN



Gap/channel size: 30 nm

Tip radius: ~17 nm

V_{on}: **~0.24 V**

I_e: **~457 nA at ~1.0 V**

In air? **Yes**

Note: V_{on}= V≥100 pA for all cases

*K. Sapkota et al., *Nano Lett*. 21, 1928 (2021)

GaN nanoscale vacuum electron diode shows far superior performance vs previous Si and SiC devices!

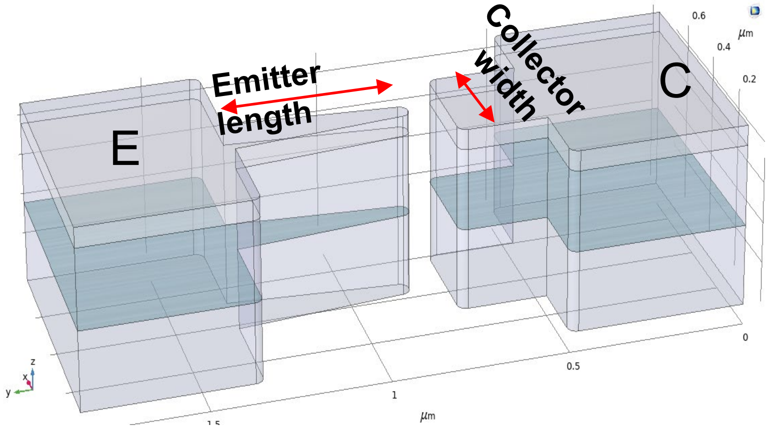
Optimization of GaN NVED: 3D Simulation

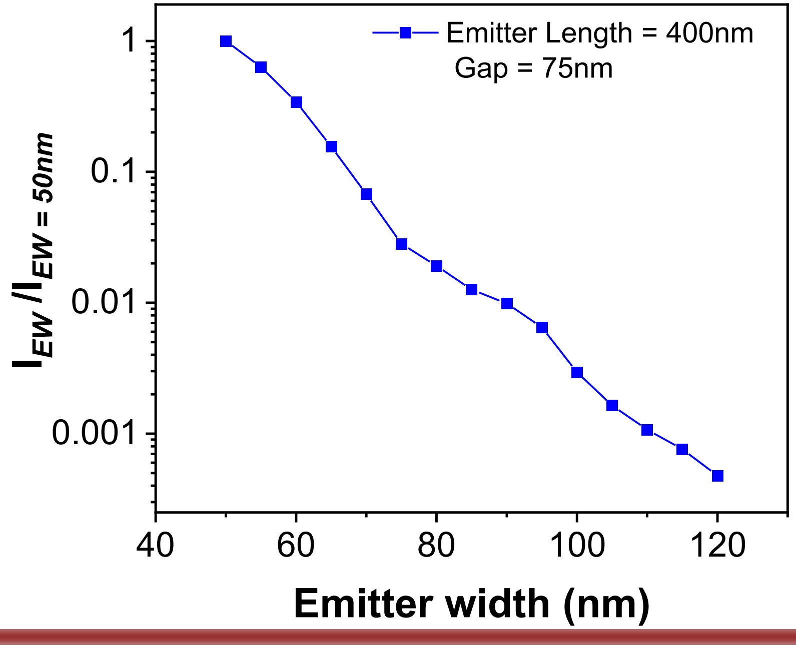
- Developed simple 3D COMSOL model to simulate field emission current as a function of various device parameters

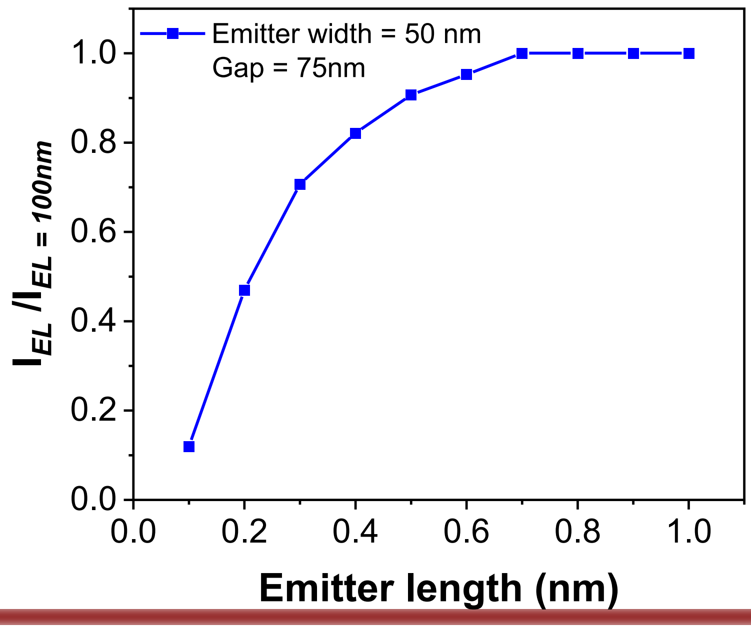
Electric field: $\boldsymbol{E} = -\nabla V$

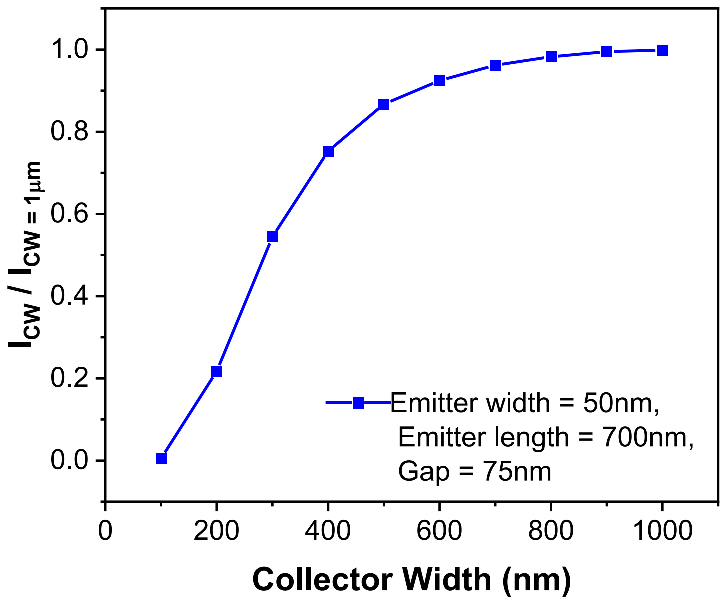
Poisson's Equation: $\nabla.(\epsilon_o \epsilon_r \boldsymbol{E}) = \rho_v$

Fowler Nordheim equation: $J = A\left(\frac{\beta^2 V^2}{\phi d^2}\right)\exp\left(-\frac{B\phi^{3/2}d}{\beta V}\right)$









23

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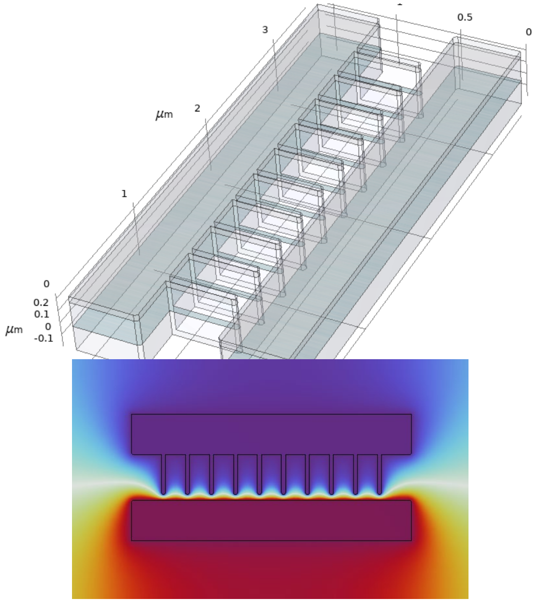
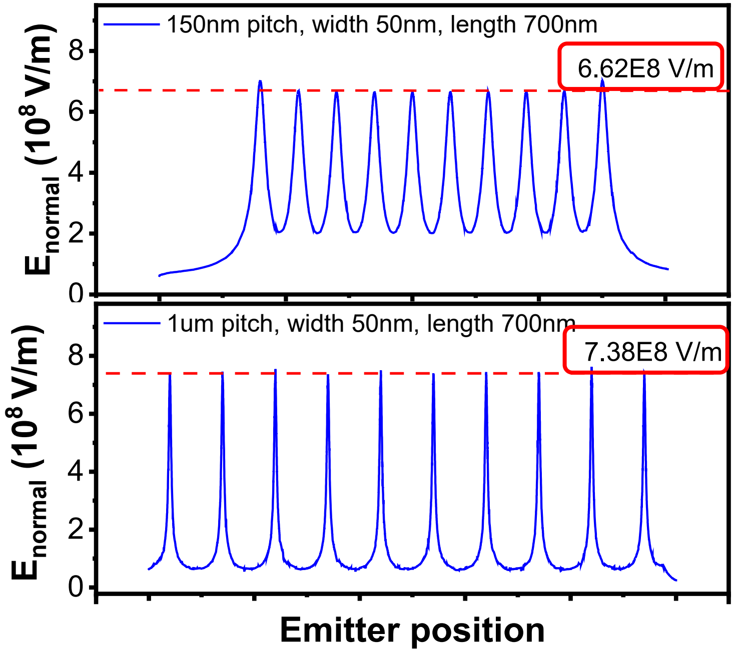
Designing array of diodes: Electric field screening effect

- Array of diodes suffer from the electric field screening due to presence of neighboring emitters
- Field emission current is negatively impacted for short emitter periodicity (emitter pitch).
- Optimal design: emitter pitch ≥ 500nm for given emitter geometry

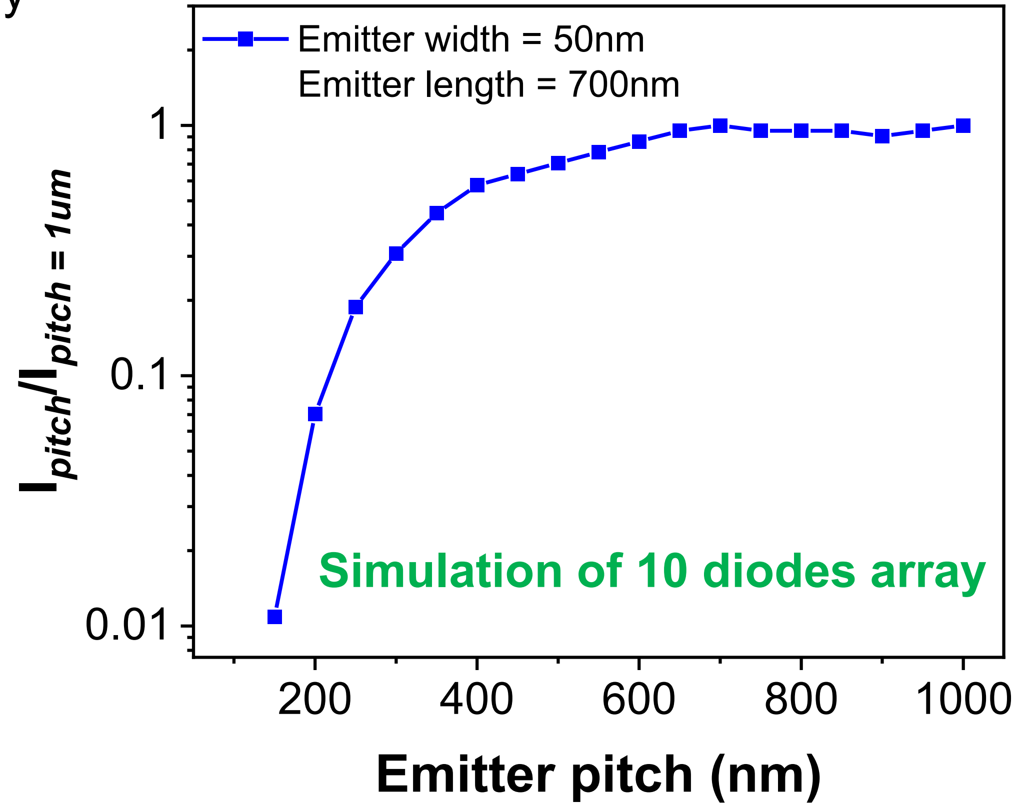


3D model of 10 diodes array

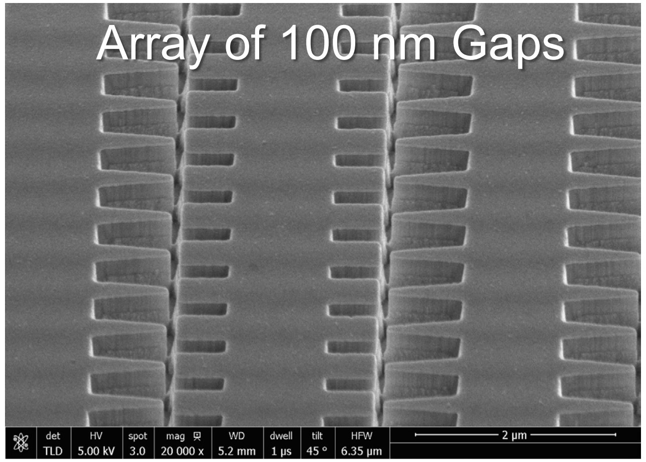


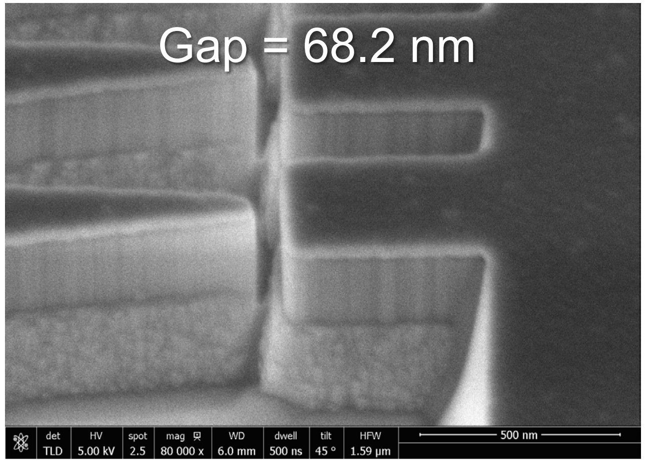
Electric field screening: field at the tips for 150nm and 1um pitch

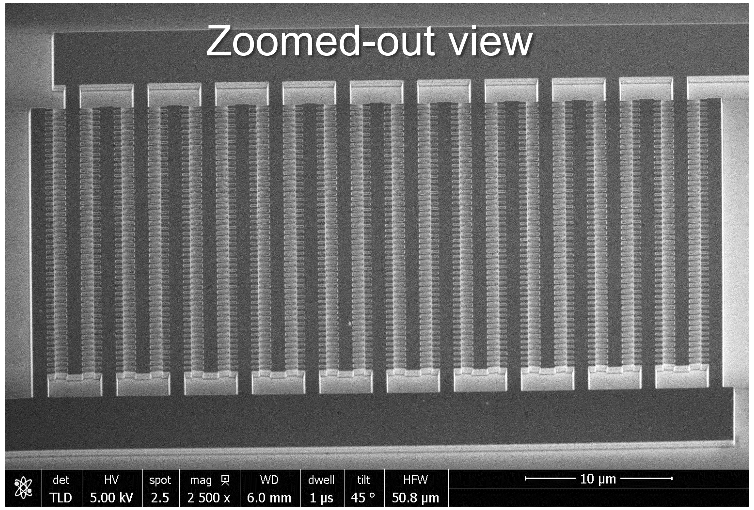
Field emission current vs. emitter pitch

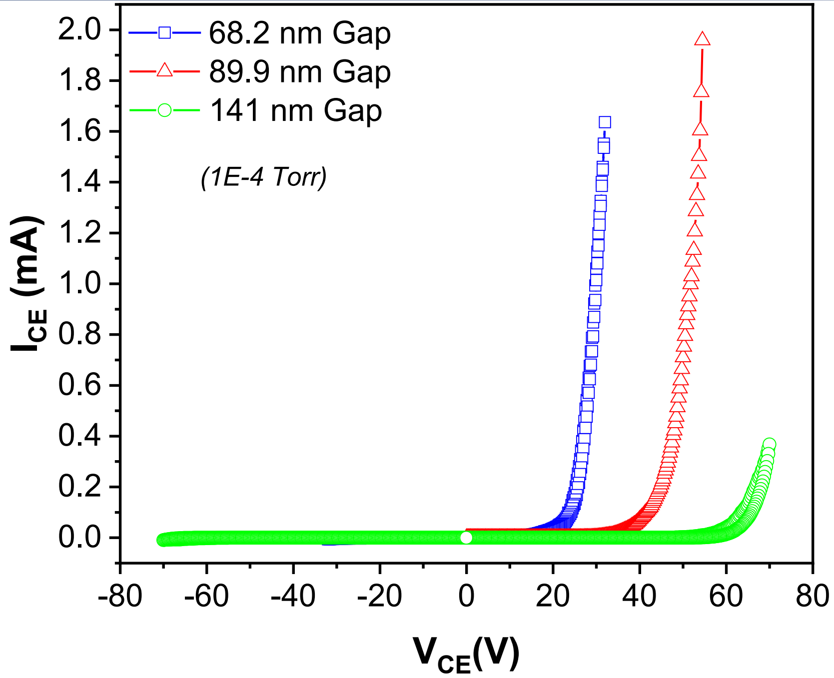


High-current, 1000 vacuum nanodiode arrayed device!









- Proof-of-concept array of 1000 connected GaN vacuum nanodiodes with ~ 2mA field emission current
- Array design can provide higher current, improve reliability, and device predictability compared to single devices
- Achieved current density 171 A/cm^2 (semiconductor record?)!
- Scale-up potential to amps of current?!

2.5 MeV Proton Irradiation Studies

Acknowledgement: George Burns, Michael King, Edward Bielejec

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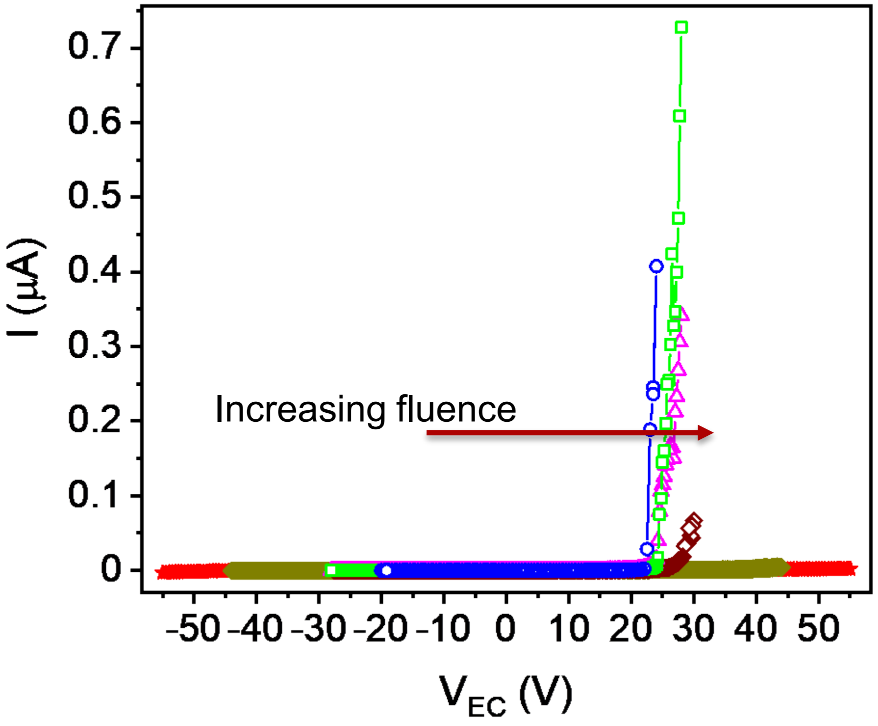
Done at Light Ion Microbeam (Pelletron) at IBL

- **Trend of slightly decreasing current up to certain fluence,** possibly due to carrier compensation in n-GaN due to defect formation (e.g. Ga vacancies), but **no substantial degradation**.
- At higher fluence, significant increase in V_{on} observed and eventually no field emission current observed at highest fluence

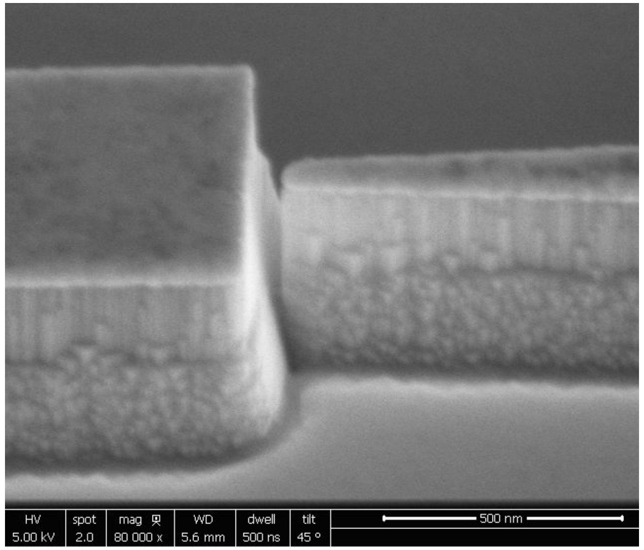
I-V vs total H^+ fluence



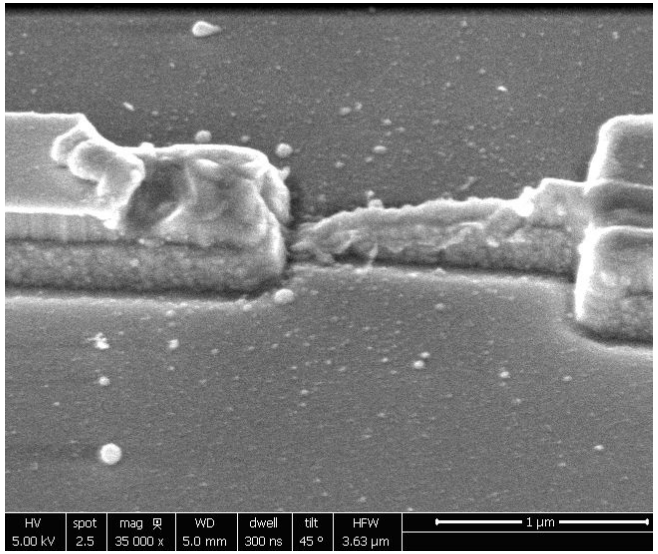
2.5 MeV Proton Irradiation Studies

- SEM shows **physical damage at highest fluence after** exposure & I-V measurement, likely due to Joule heating from increased resistivity based on damage occurring only at narrow emitter & collector regions.
- Very high damage threshold, likely vacuum channel architecture, GaN, and small interaction volume
- Other radiation testing currently underway (e.g. electron, neutron): also shows good radiation hardness

Before proton exposure

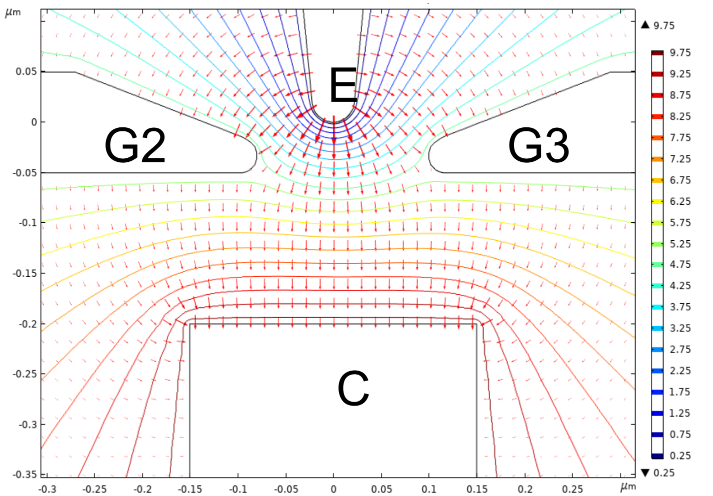


After exposure & I-V

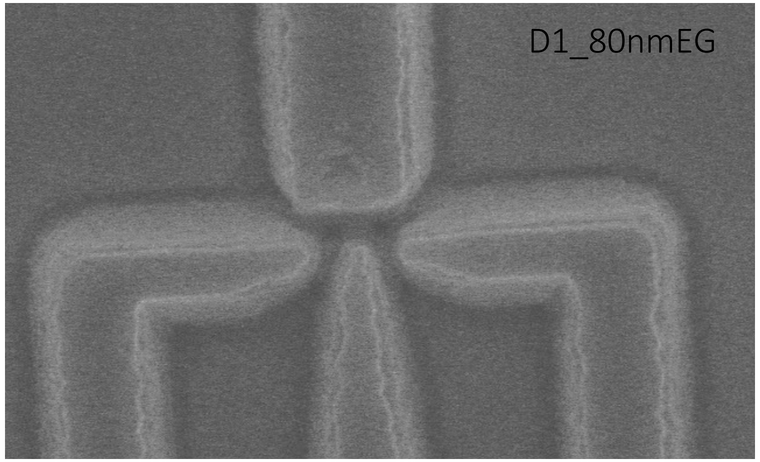


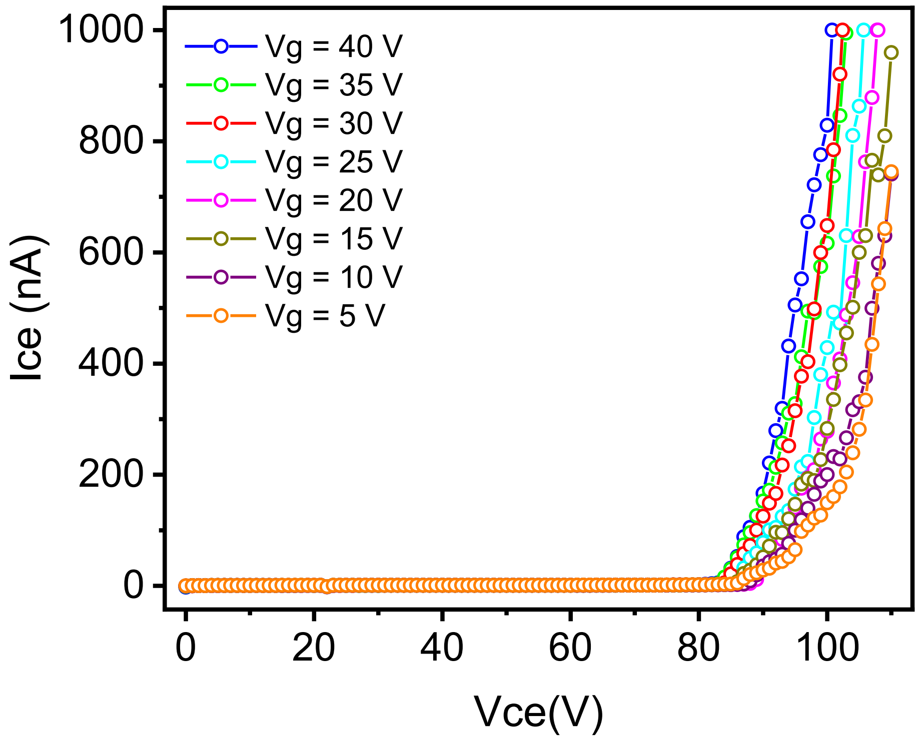
Lateral GaN nanogap field emission transistor

Electric field modulation simulation (COMSOL)



SEM – fabricated GaN lateral vacuum nanogap transistor

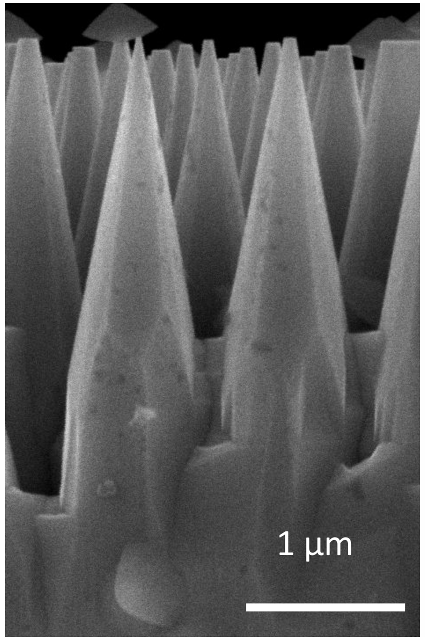




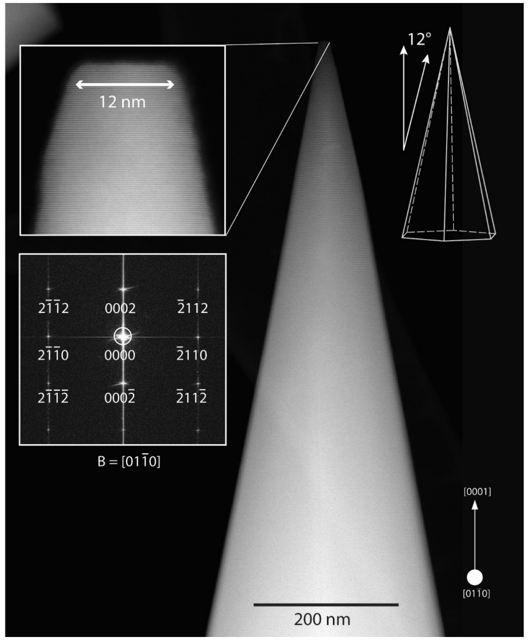
- Transistor – additional circuit element needed for various devices
- First lateral GaN vacuum nanotransistor demonstrated
- Gate voltage decreases the turn on, increases current (expected)
- Gate electrodes act as field emitter at V_g <= 5V
- Other designs (e.g. top gate, back gate) need exploring to increase response to V_g

Vertical GaN nanowire field emitter arrays

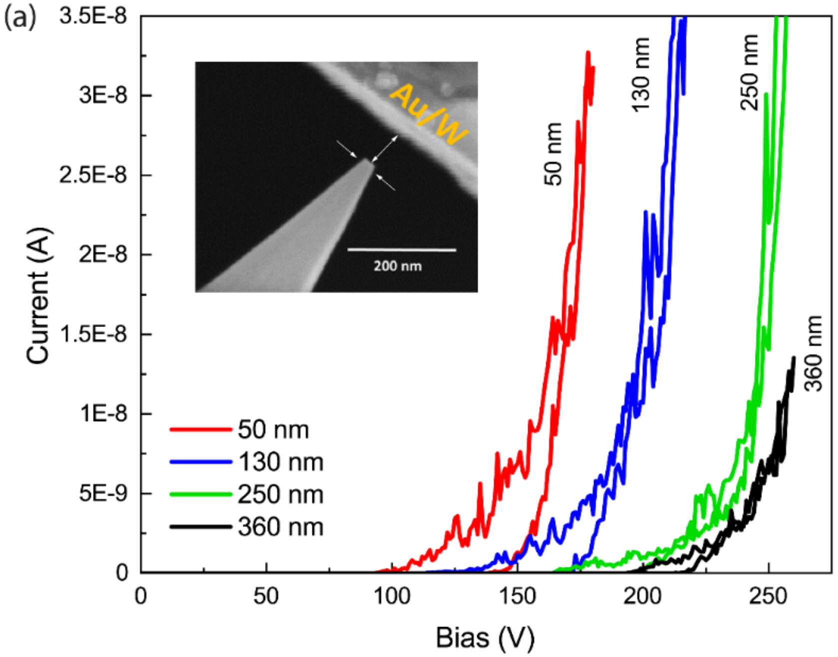
SEM

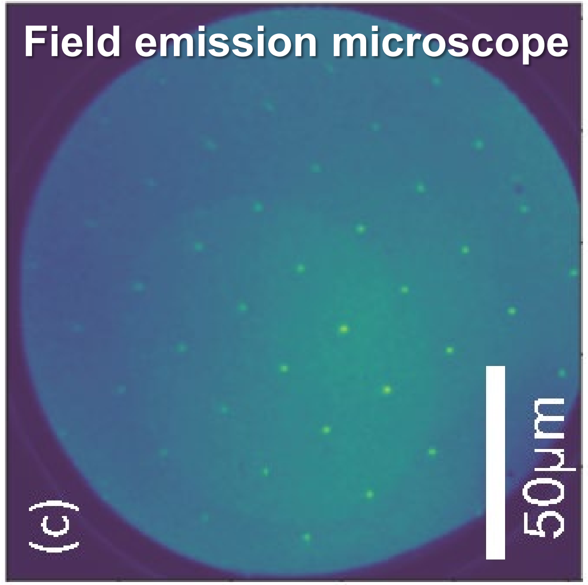


TEM



Field emission measurements (in-situ SEM)





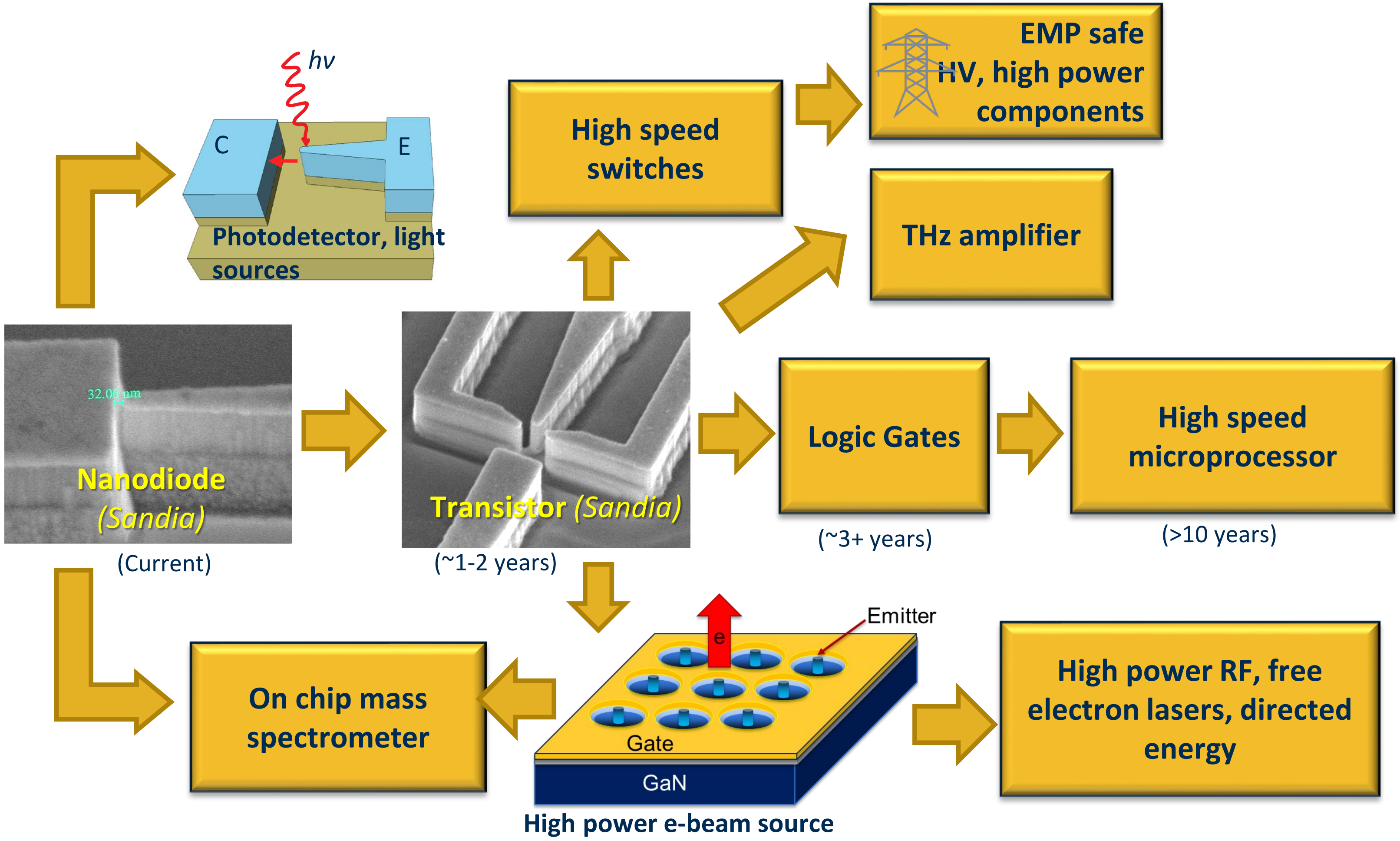
E. Bussmann, T. Ohta, *SNL*

w/B. Kazanowska, K. Jones, UF

- Developed **new H_3PO_4 etch** for tapered, vertical GaN nanowire fabrication*
- Field emission microscope: very uniform turn-on across nanowire array
- Can serve as field emitter arrays for **vertical** GaN vacuum nanoelectronic architectures.

*B. Kazanowska et al., *Nanotechnology* **33** 035301 (2022)

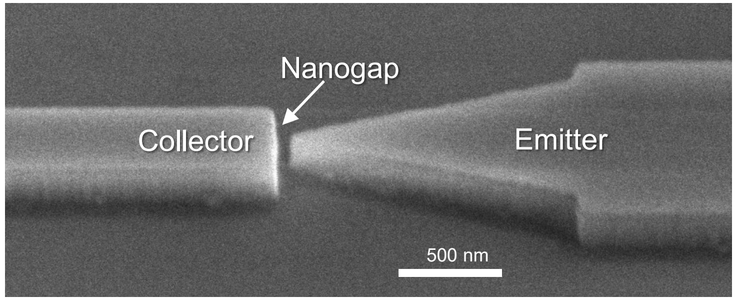
Future directions for nanogap vacuum nanoelectronics?



- What are the potential “killer” or niche apps for nanogap vacuum electronics?
- High speed microwave/RF devices
- High speed logic circuits
- On-chip electron sources
- Detectors
- Radiation hard & high temperature [opto]electronics

Conclusions

- Nanoscale on-chip vacuum electronics have the exciting potential to combine the advantages of vacuum electron and solid-state devices: ballistic electron transport, no junction to damage, high T operation, miniaturization, cost, efficiency
- High performance, on-chip lateral **GaN** nanogap field emission diodes were demonstrated using a **scalable** top-down fabrication approach: Ultra-low turn-on voltage **down to ~0.24 V is achieved in air** with high field emission current & good diode behavior. **1000 diode array** with **record(?) current density** demonstrated.
- Operating voltages are compatible with modern electronic circuits.
- **Challenges**: Relatively small field, need fundamental scientific understandings of field emission and electron transport in empty space at nanoscale regimes for a range of architectures and materials. Advantages, weaknesses, and potential application spaces still need to be identified.



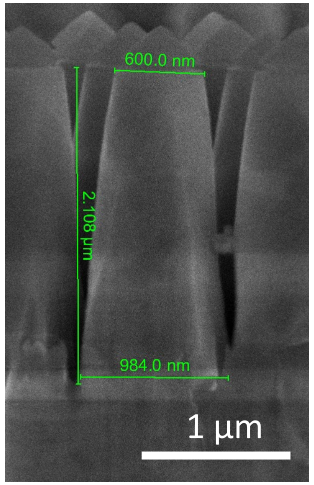
Contact: gtwang@sandia.gov

Backup Slides

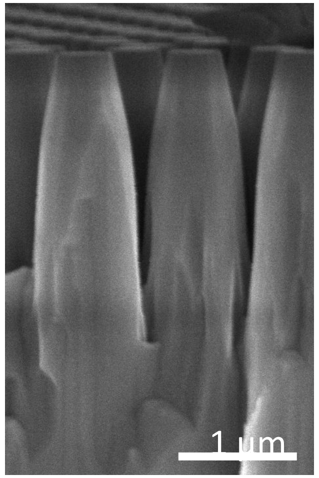
Sandia National Laboratories

H_3PO_4 wet etching of tapered GaN nanowires

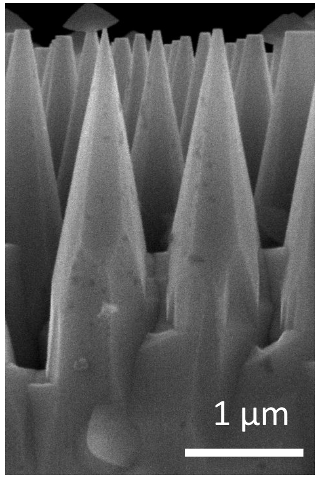
93-96 °C H_3PO_4



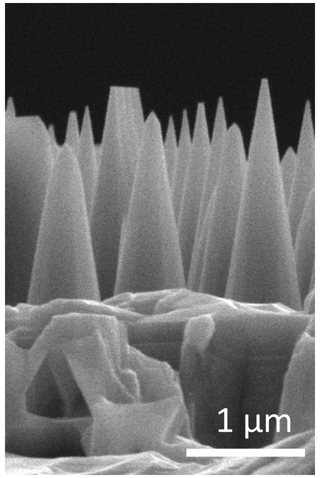
30 min ICP only



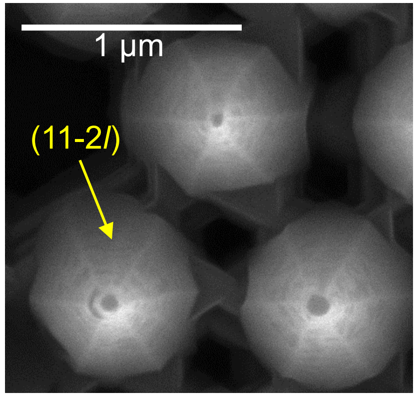
10 min H_3PO_4 (~95°C)



40 min



55 min



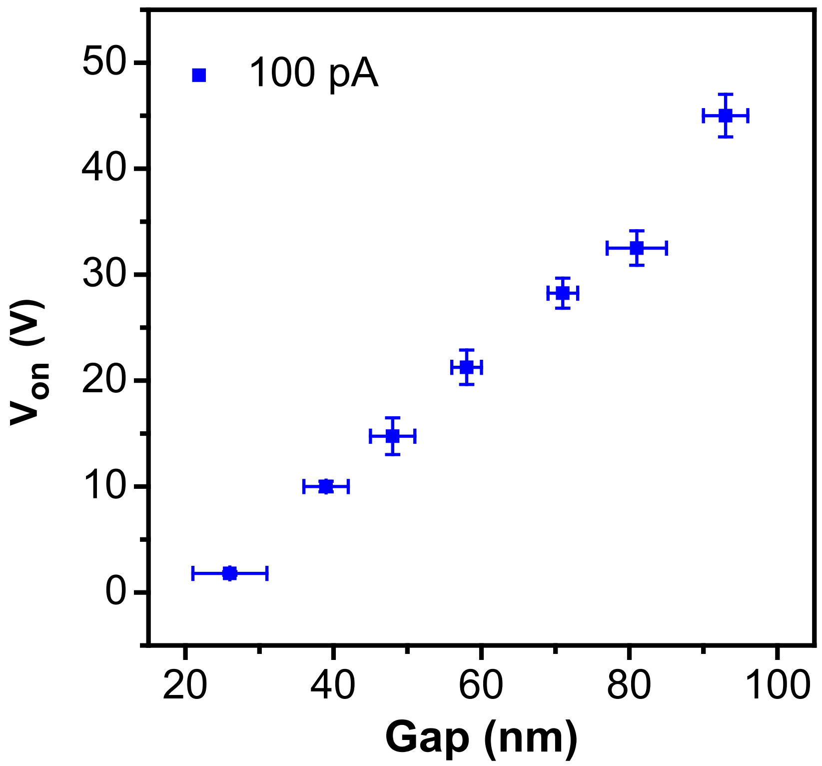
40 min, top view

- H_3PO_4 wet etching of ICP dry etched GaN nanowires leads to inclined {11-2*l*} facets not seen in KOH-based etch
- Micro-faceting not observed during etch in contrast to KOH-based etch. Also top corners not "protected" as in KOH-based etch.
- Leads to "pointy" tapered nanowires instead of straight vertical nanowires

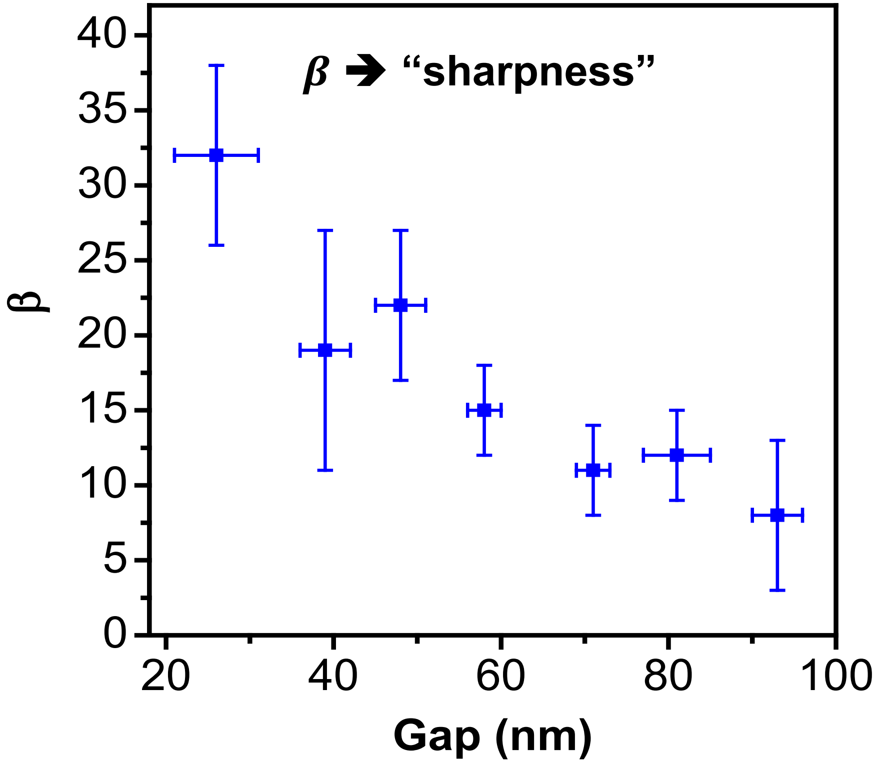
Gap size dependency of GaN nanoscale vacuum electron diode (NVED)

Devices with various nanogap sizes were fabricated

- Turn-on voltage depends linearly with nanogap size
- Field enhancement factor decreases with increase in gap size



Nanogap size dependent turn on voltage



Nanogap size dependent field enhancement factor

Sapkota et al., "Ultralow Voltage GaN Vacuum Nanodiodes in Air", *Nano Letters (2021)*