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COMPARISON OF GaAs JFETs TO MESFETs FOR HIGH-TEMPERATURE OPERATION

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Abstract

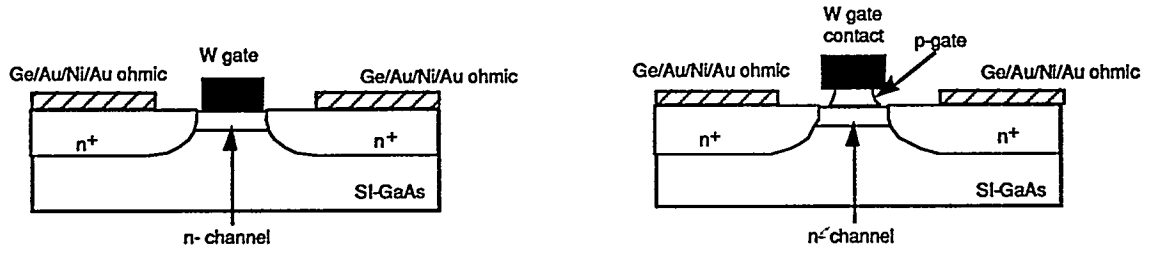
GaAs-based Metal Semiconductor Field Effect transistors (MESFETs) and High Electron Mobility Transistors (HEMTs) have been the focus of research for high-temperature operation due to the 1.42 eV band gap of GaAs that reduces thermal carrier generation as compared to 1.1 eV silicon-based electronics. Although schemes have been proposed to minimize substrate currents at elevated temperatures, high-temperature operation of these devices is ultimately limited by the gate leakage current of the Schottky gate contact. Since a Junction Field Effect Transistor (JFET) has a higher gate barrier to current flow than a Schottky barrier MESFET as a result of the p/n junction gate, JFETs should have superior performance at elevated temperatures. In this paper we compare the high temperature performance of a self-aligned GaAs MESFET and JFET. Both devices suffer from substrate leakage at high temperature; however, the JFET has superior gate characteristics and maintains a larger fraction of its room temperature transconductance at 300 °C.

INTRODUCTION:

GaAs-based MESFETs and HEMTs have been studied for high temperature operation due to the higher bandgap of GaAs as compared to silicon (1.42 versus 1.1 eV) (Gobert 1994; Sadwick 1994; Shoucair 1992; Wong 1992). The higher bandgap reduces thermal carrier generation and should result in superior high-temperature operation. However, high temperature operation also requires that the gate electrode maintain its rectification properties at temperature. Therefore, it is important to raise the gate barrier to current flow since thermal carrier generation over the gate barrier will become significant at elevated device temperatures. One approach to increasing the gate barrier for GaAs-based transistors is to employ a p/n junction gate as in a JFET where the barrier approaches the bandgap of GaAs as compared to the Schottky barrier in a MESFET of approximately one-half the bandgap.

In this paper, we compare the elevated temperature performance of self-aligned, ion implanted, GaAs MESFETs and JFETs. Figure 1 is a schematic representation of the two

devices. Both employ a refractory W-gate or gate contact and conventional Ge/Au/Ni/Au ohmic contacts. The pad metal for both devices is placed on semi-insulating GaAs, not isolated from the semiconductor with a dielectric layer. Therefore, this pad arrangement may allow an additional leakage path through the substrate at high temperatures. The JFET structure has been developed for low-power electronic applications and employs a self-aligned structure that minimizes the excess capacitance associated with the JFET. The room temperature performance of the JFET has been reported elsewhere (Sherwin 1994; Zolper 1994a,b, 1995). The JFET used for this study employs Cd-implantation to form the shallow p^+-gate region and has a room temperature unity current gain cut-off frequency of 26 GHz and a maximum oscillation frequency of 42 GHz (Zolper 1995).



(a) (b)

FIG 1: Schematic representation of ion implanted, self-aligned GaAs a) MESFET and b) JFET.

EXPERIMENTAL CONDITIONS

The variable temperature DC measurements were performed at the wafer level on a temperature controlled stage with the sample mounted with thermal grease. The temperature was measured with a thermocouple embedded in the stage. Measurements were made in ambient air using a HP4145 parameter analyzer. The same testing procedure was employed for both the MESFETs and JFETs with the exception that the gate bias on the JFET was taken to 1.5 V while the MESFET was only measured to a gate bias of 1.0 V due to its lower gate turn-on voltage. The devices are nominally 0.7 μm x 50 μm with a 4 μm source-to-drain spacing. No surface passivation or encapsulation has been incorporated on these transistors.

RESULTS AND DISCUSSION

Figure 2 shows the temperature dependence of threshold voltage (defined as the zero current intercept of ($I_{DS}^{1/2}$ vs V_{GS}) for the MESFET and JFET. Although the JFET shows a faster role-off of threshold voltage with increasing temperature, the general trend for the MESFET and JFET is similar. We attribute the temperature dependence of threshold voltage to an increase in conduction in the GaAs buffer material as has been reported by others (Wong 1992; Shoucair 1992). The larger threshold shift in the JFET may be due to differences in the substrate material as the devices were fabricated in LEC GaAs from different vendors. If the substrate conduction is reduced, such as with the use of AlAs buffer (Lee 1995; Ito 1996), the JFET should have improved threshold temperature stability as a result of less gate leakage as discuss later.

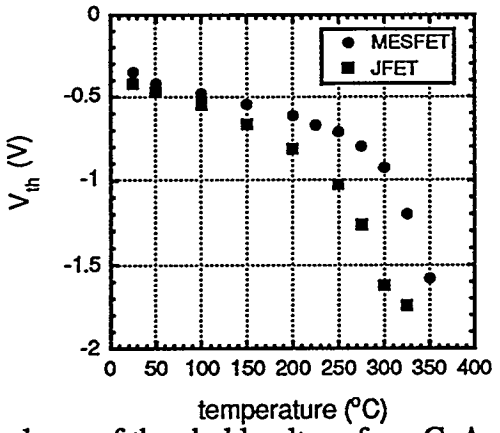


FIG 2. Temperature dependence of threshold voltage for a GaAs MESFET and JFET. V_{TH} is taken as the zero current intercept of $I_{DS}^{1/2}$ vs V_{GS}.

Figure 3a,b shows the temperature dependence of I_{DS} versus V_{GS} between 25 and 350 °C for the MESFET and JFET. At room temperature (RT) the on/off current ratio of the JFET is ~10^6 while for the MESFET it is ~10^5. At 300 °C this ratio degrades to ~10 for the JFET for the on current measured at V_{GS} = 1.0 V and to ~20 for the MESFET for the on current measured at V_{GS} = 0.5 V. Here again we suspect differences in the substrate properties may be contributing to the differences in elevated temperature sub-threshold performance since gate characteristics of the JFET are superior at high temperature as described below.

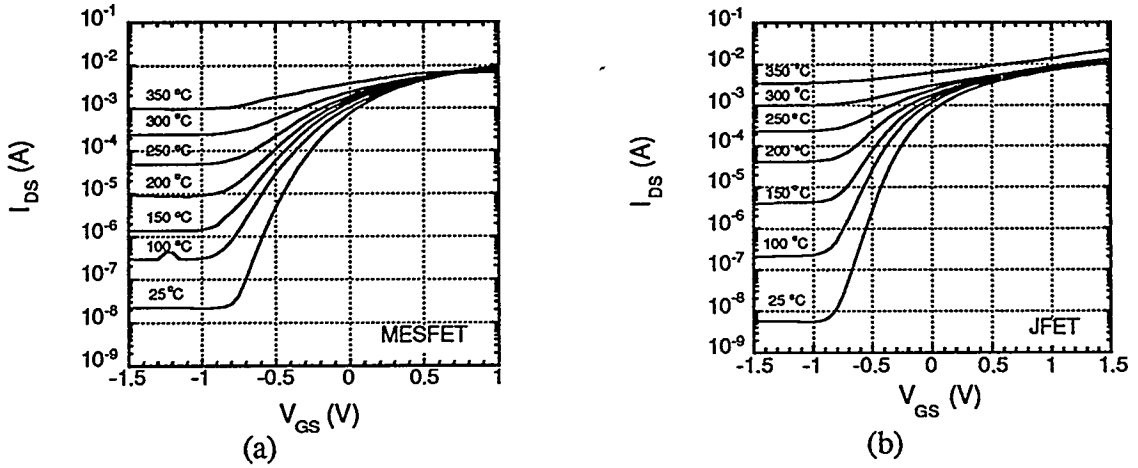


FIG 3. Temperature dependence of I_{DS} versus V_{GS} for V_{DS} = 2 V for a 0.7 μm x 50 μm GaAs a) MESFET and b) JFET.

Figure 4 a,b shows the temperature dependence of the gate diode characteristics for the MESFET and JFET between 25 and 350 °C. At RT the MESFET has a gate turn-on voltage (defined as 1 mA/mm of gate current or 50 μA for these 50 μm wide devices) of 0.52 V while the JFET's gate turn-on is 0.93 V. At 300 °C the gate turn-on voltage of the MESFET is ~0.14 V while the JFET has a turn-on of ~ 0.2 V but with a slower turn-on characteristics. That is, at 300 °C, for 0.5 mA of gate current the JFET requires a forward

voltage of ~0.55 V while the MESFET has only 0.3 V. The lower gate turn-on voltage of the MESFET at high temperature will significantly increase power consumption of the device and reduce the available logic voltage swing. More importantly, this increase in gate conduction for the MESFET appears to play a significant role in reducing the transconductance at elevated temperature as discussed next.

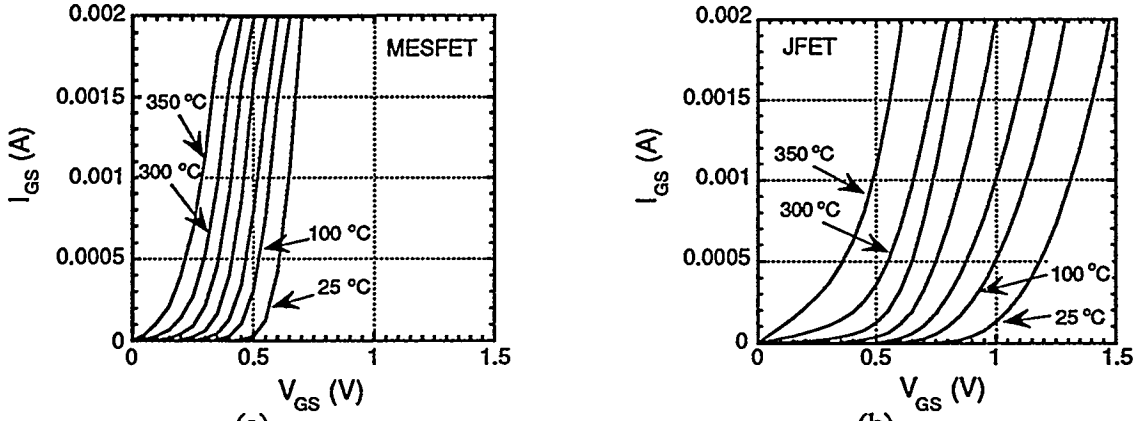


FIG 4: Temperature dependence of I_{GS} vs V_{GS} for a 0.7 μm x 50 μm GaAs a) MESFET and b) JFET. For each family of curves the temperature starts at 25 °C at the right, increases to 100 °C moving to the left, and then steps by 50 °C from right to left out to 350 °C.

Figure 5a,b shows the temperature dependence of the transconductance (g_m) versus gate bias for the MESFET and JFET between 25 and 350 °C. The effect of gate leakage becomes apparent as the MESFET has a ~46% reduction in its maximum transconductance between 25 and 350 °C while the JFET shows only a ~27% decrease over the same temperature range. We ascribe this difference to the lower gate leakage, and therefore better charge modulation, of the p/n junction gate JFET at elevated temperatures.

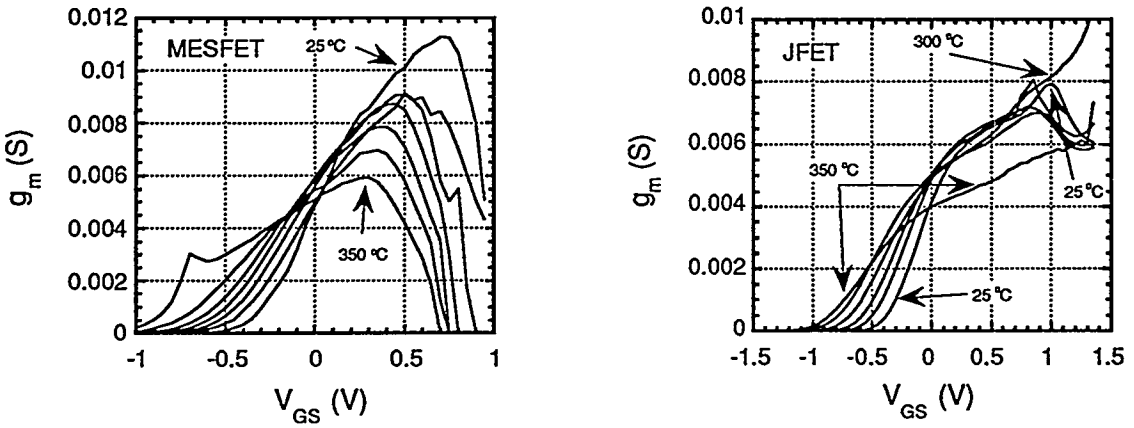


FIG 5: Temperature dependence of g_m versus V_{gs} for a GaAs a) MESFET and b) JFET. For each family of curves the temperature starts at 25 °C, increases to 100 °C, and then steps by 50 °C up to 350 °C. V_{ds} = 2 V for all curves.

CONCLUSION

The high temperature performance of an ion implanted, self-aligned GaAs MESFET and JFET were compared. Both devices demonstrated a negative threshold voltage shift with increasing temperature that is attributed primarily to an increase in substrate conduction since the shift is similar for both devices. Both devices also show a similar degradation in the on/off current ratio with increasing temperature that can also be attributed to substrate conduction. The JFET demonstrated lower gate leakage at all temperatures, due to the larger barrier to current flow in the p/n junction gate, and less degradation in maximum transconductance with increasing temperature. We attribute the improved thermal stability of transconductance in the JFET to the superior gate diode operation with temperature. More work is need to reduce substrate conduction in the JFET to fully realize the advantages of this device in high-temperature operation.

Acknowledgment

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