FERMILAB-SLIDES-24-010-ETD

Fermilab U.S. DEPARTMENT OF ENERGY Office of Science

22FDX Cryogenic Modeling

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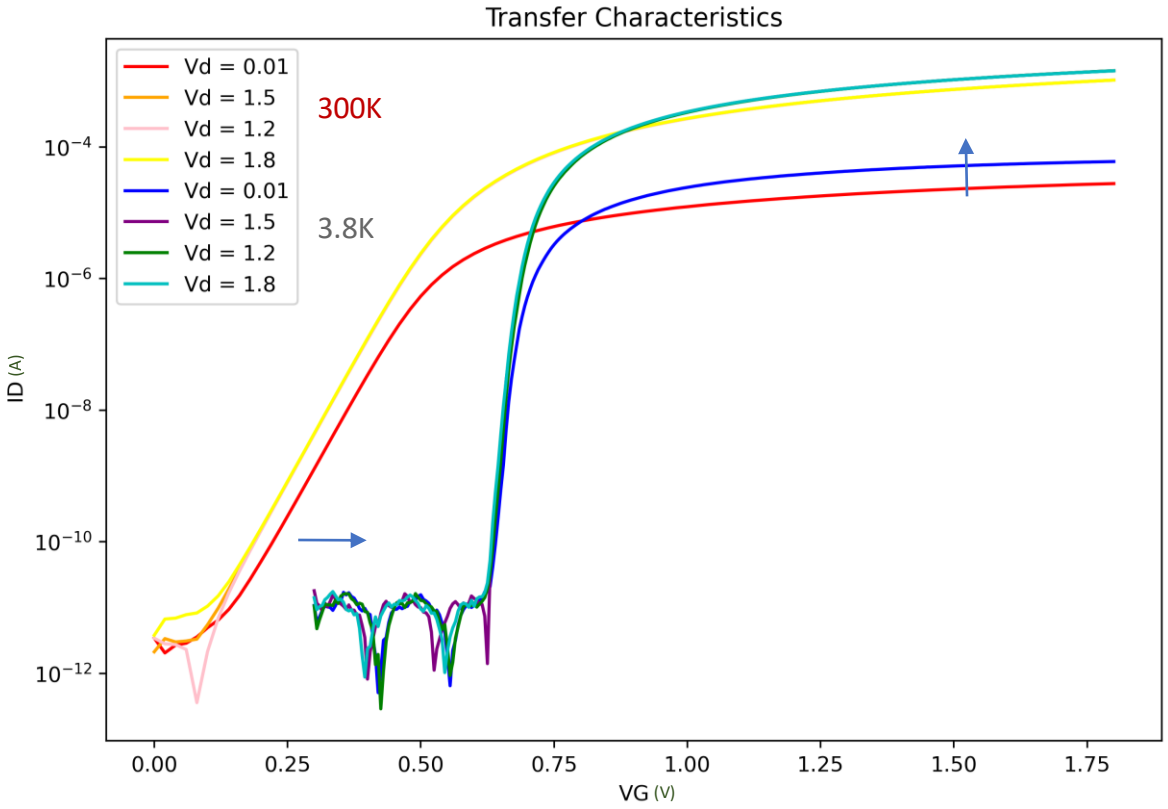
IceQubes 2024

Overview

- 22FDX for Analog/RF design
- 22nm FDSOI: 4K device models
  - EKV models
  - Brief overview of main changes in device performance
  - Cryo PDK models (BSIM-IMG)
- Future work

Olivia Seidel, Fermilab, UTA
Graduate Student

Fully Depleted-Silicon on Insulator (FDSOI) for RF/Analog Design

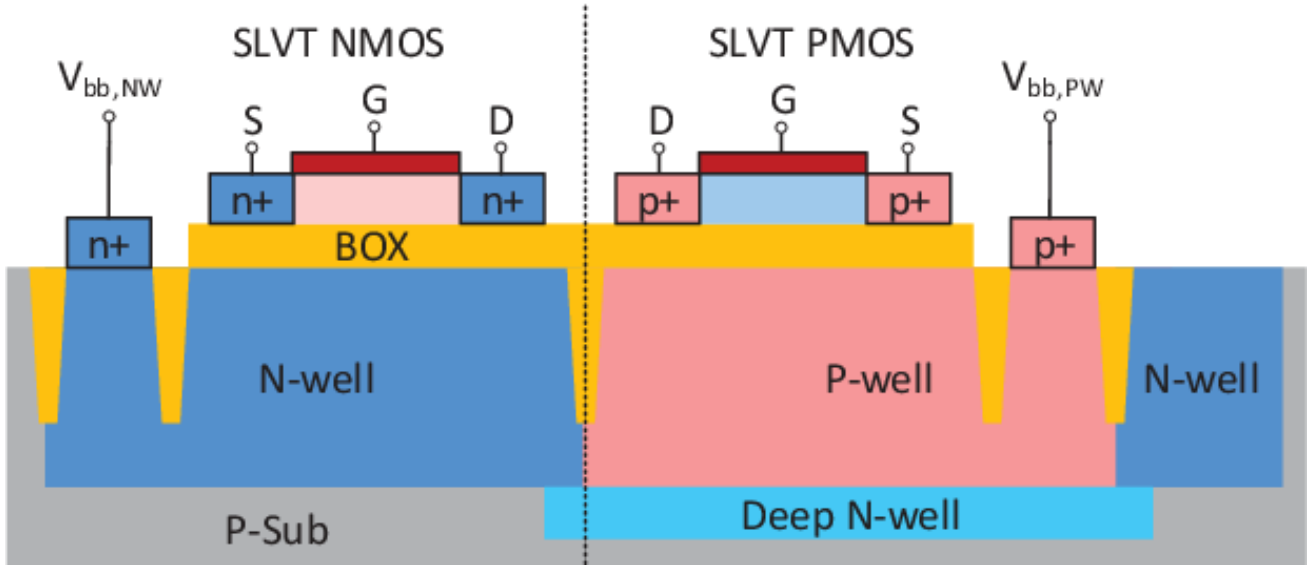


Drain current output as a function of gate voltage for an eglvt flavor nfet device with Gate length=0.2um and Width=2um [1]

- **Threshold Voltage increases** (due to substrate freezing)
- Availability of a **"back-gate"** in FDSOI technologies to lower the threshold and counter cryogenic increase

22FDX Advantages for RF/Analog Design

- Confined electrons in an undoped channel and total dielectric isolation → ultra low leakage
- Fully depleted → lower power
- Tighter V_T distribution
- Low parasitics → faster switching
- Ultra thin body → Reduced short channel effect, DIBL
- Back gate used to recover threshold shift at cryo → critical for low power at cryo



[1]

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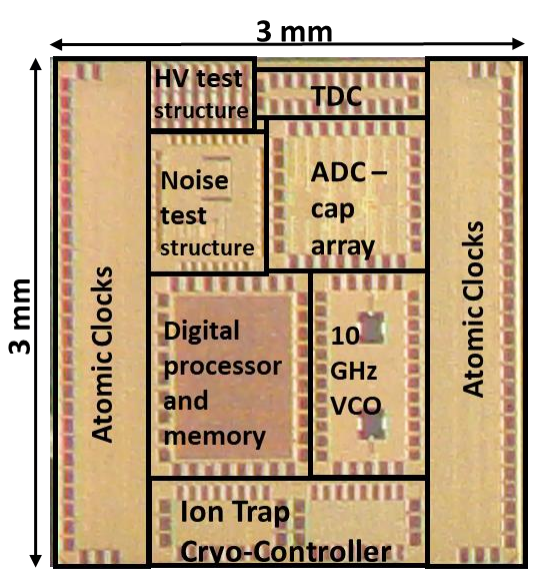
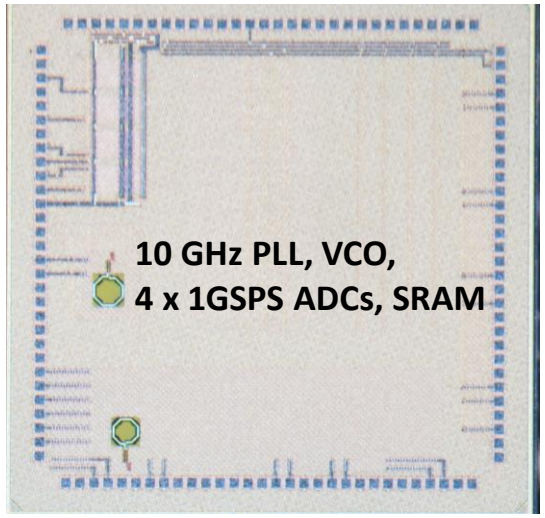
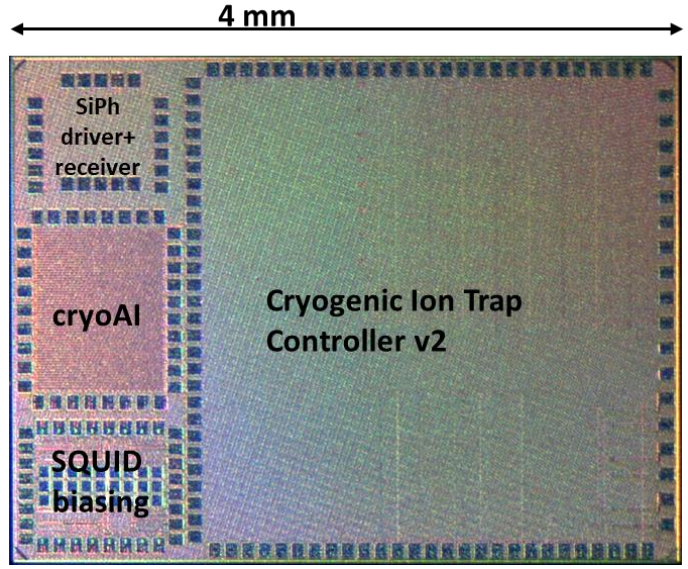
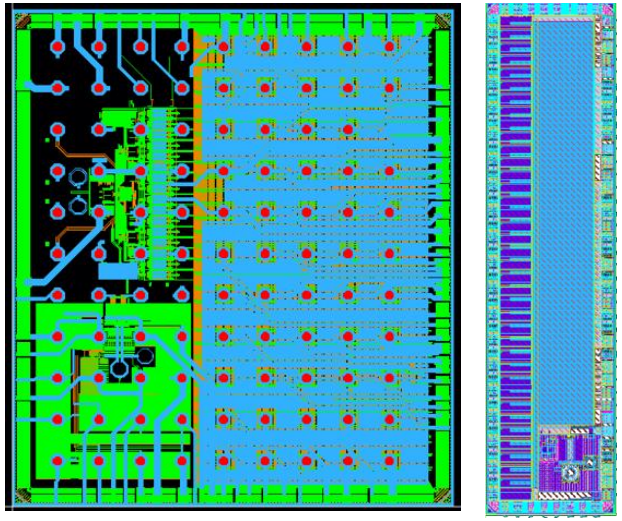
22FDX cryoChips at Fermilab









- **GF_test chip: (**11/21) Various designs
- **Michigan:** (07/22) 10 GHz PLL, VCO, 4 x 1GSPS ADCs, SRAM
- **Cryogenic Ion trap controller:** (01/23) 16 channel Ion trap control chip;
- **Si Photonic driver/receiver**;
- **cryoAI:** ultrafast NN for anomaly detection;
- **SQUIDDAC**: SLUG_biasing; various level shifter test structures
- **Glebe:** (with Microsoft) 10 GSPS ADC
- **Sunrock:** 32 channel SNSPD readout with ~ps time tagging

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Overview of Fermilab's 22FDX Cryo-CMOS modeling activities

Fermilab is leading several activities for the cryogenic characterization of 22FDX transistors:

With EPFL:

- Measurements of transistors at 4K
- Development of simplified EKV model for analog design
- Low noise test structure measurements

With Synopsys:

- Extraction of PDK-compatible BSIM-IMG (independent multi-gate) for 4K

In-house:

- Measurement and modeling of high voltage devices at 4K (BOXFET, LDMOS)
- ML/AI for Cryo-modeling

22FDX Cryogenic modeling - EKV

Collaboration with EPFL (Han, Enz, Charbon) for simplified EKV (S-EKV) modeling for inversion coefficient design methodology (for analog design)

Only four parameters:

1. n = slope factor
2. I_{spec} = specific current
3. V_{T0} = threshold voltage without short-channel effects
4. λ_c = parameter for velocity saturation

Developed an open-source Python-based parameter extractor (SEKV-E) for the simplified EKV (sEKV) model
https://gitlab.com/moscm/sekv-e

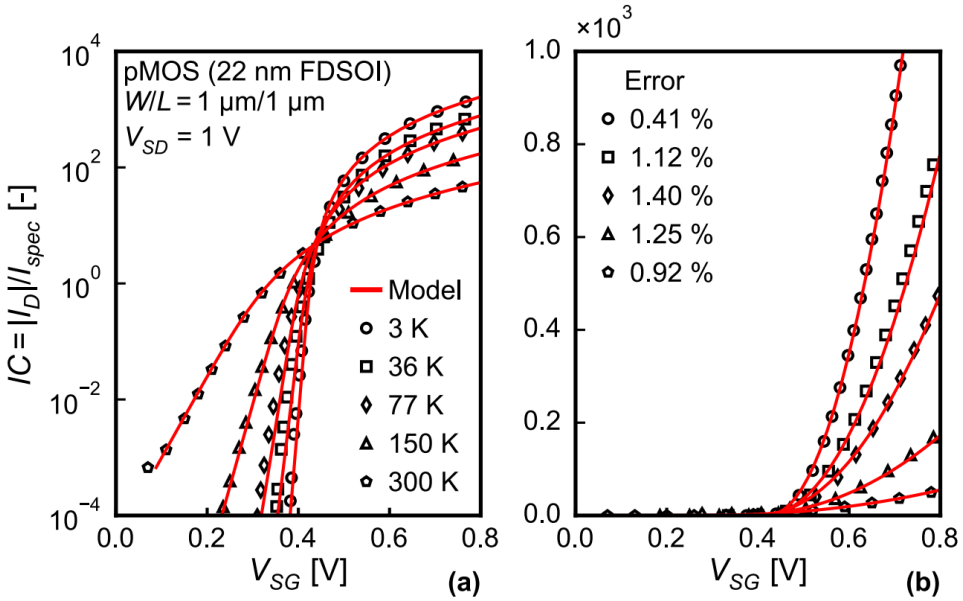


FIGURE 5. **Applying SEKV-E to a pMOS device of 22 nm FDSOI technology in saturation with V_{back} = 0 V [14] from room temperature down to deep cryogenic temperature. The legend in (b) shows the percent error.**

- Han, Hung-Chi, Antonio D'Amico, and Christian Enz. "Comprehensive Design-oriented FDSOI EKV Model." *2022 29th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. IEEE, 2022.
- H.-C. Han, F. Jazaeri, Z. Zhao, S. Lehmann, C. Enz, "*An improved subthreshold swing expression accounting for back-gate bias in FDSOI FETs*", in *Solid-state Electronics*, vol. 202, 108608, April 2023. Doi: 10.1016/j.sse.2023.108608
- Han, Hung-Chi, et al. "In-depth cryogenic characterization of 22 nm FDSOI technology for quantum computation." *2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS)*. IEEE, 2021.
- Han, Hung-Chi, et al. "Cryogenic RF Characterization and Simple Modeling of a 22 nm FDSOI Technology." *ESSDERC 2022-IEEE 52nd European Solid-State Device Research Conference (ESSDERC)*. IEEE, 2022.
- H. -C. Han, A. D'Amico and C. Enz, "SEKV-E: Parameter Extractor of Simplified EKV I-V Model for Low-Power Analog Circuits," in IEEE Open Journal of Circuits and Systems, vol. 3, pp. 162-167, 2022, doi: 10.1109/OJCAS.2022.3179046.

Measurement data:

EGLVT Flavor N/PFet 300K/3.8K (Vb=0):

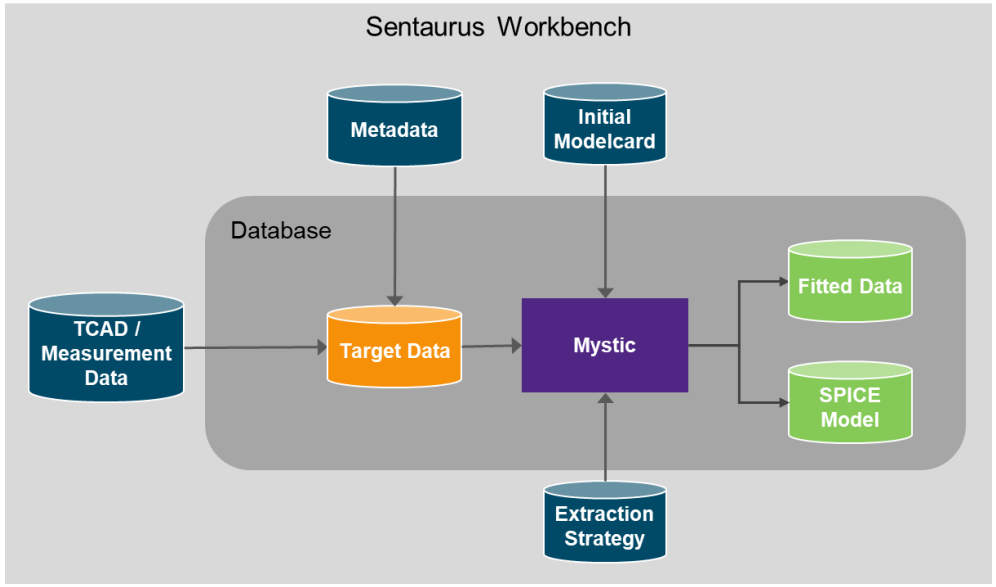
- Gate lengths: 0.07/0.2/2um
- Gate widths for each length: 0.16/0.5/2um
- Vd=0.01, 1.2, 1.5, 1.8V for various Transfer Characteristics
- Vg=1.0, 1.4, 1.8V for various Output Characteristics

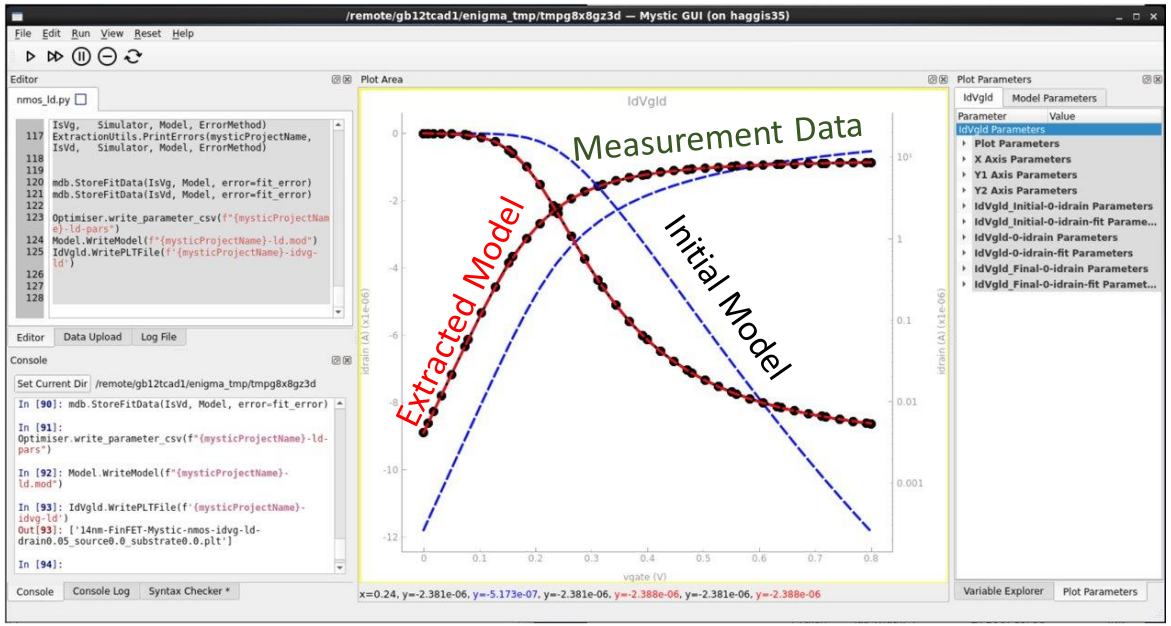
SLVT Flavor N/PFet 300K/3.8K:

- Gate lengths: 20nm-500nm for Gate Width=1um
- Gate Widths: 120-500nm for Gate Length=20nm
- Vd=0.01/1.0/1.5/1.8V at Vb=0 for various Transfer Characteristics
- Vg=1.0/1.4/1.8V at Vb=0 for various Output Characteristics
- High and low Drain for Vb=0.5/1/1.5/2 on nFet device of L=0.5/W=1um
- High and Low Drain for Bb=-4/-2/0/2/4 on pFet devices of L=0.5/W=1um

Mystic Software

- Synopsys SPICE model extraction tool for creating **automated parameter extraction** methodologies Integrated in the Synopsys Sentaurus Workbench TCAD platform
- Use **Synopsys Primesim HSPICE** as circuit simulator
- Features an interactive GUI, a custom **Python scripting environment,** and an extensive **optimization library** for finding the best parameter set for the selected SPICE model





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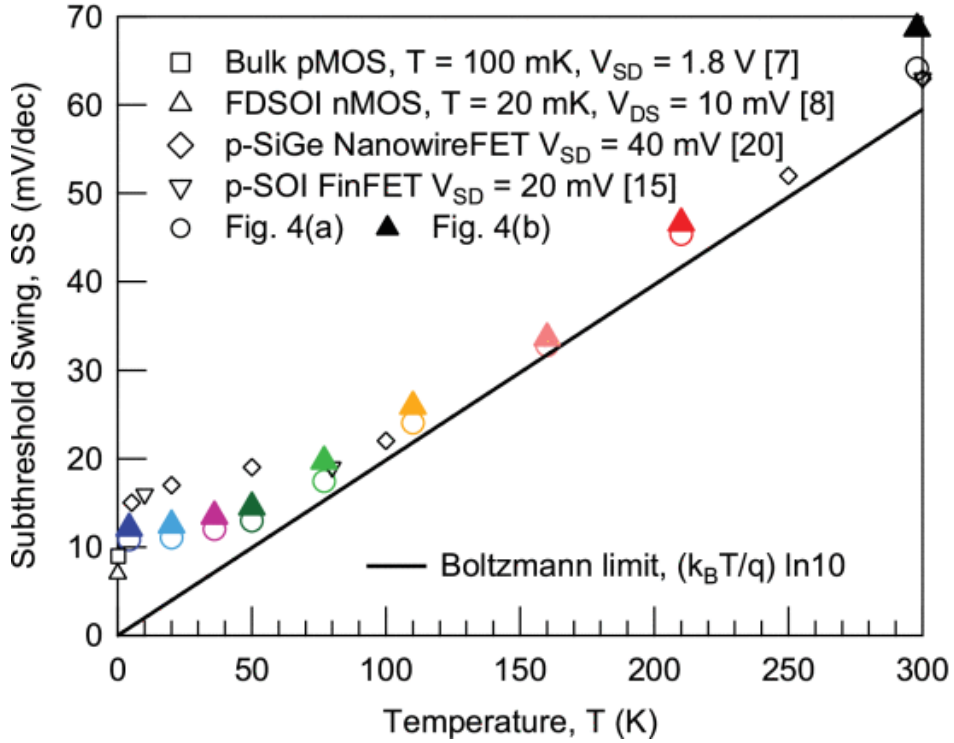
Our Model Approach

- Start with foundry PDK provided by GF --> **re-extract** the parameters we think will change at cryo
- Constrain the parameters to reasonable ranges based on physics expectations and literature when applicable
- **Isothermal** model at 3.8K
- Change the input pdk:
  - BSIM-IMG 102.8 doesn't include effects like subthreshold slope saturation [14][18] (but the latest **BSIM-IMG 102.9.6** does)
  - We model that by setting **temp** to the value where our **subthreshold slope saturates**
  - **Set temp = tnom** to remove temp dependent params
- Extracted values back into the PDK



Subthreshold Swing Saturation as a function of Temperature for various devices [18]

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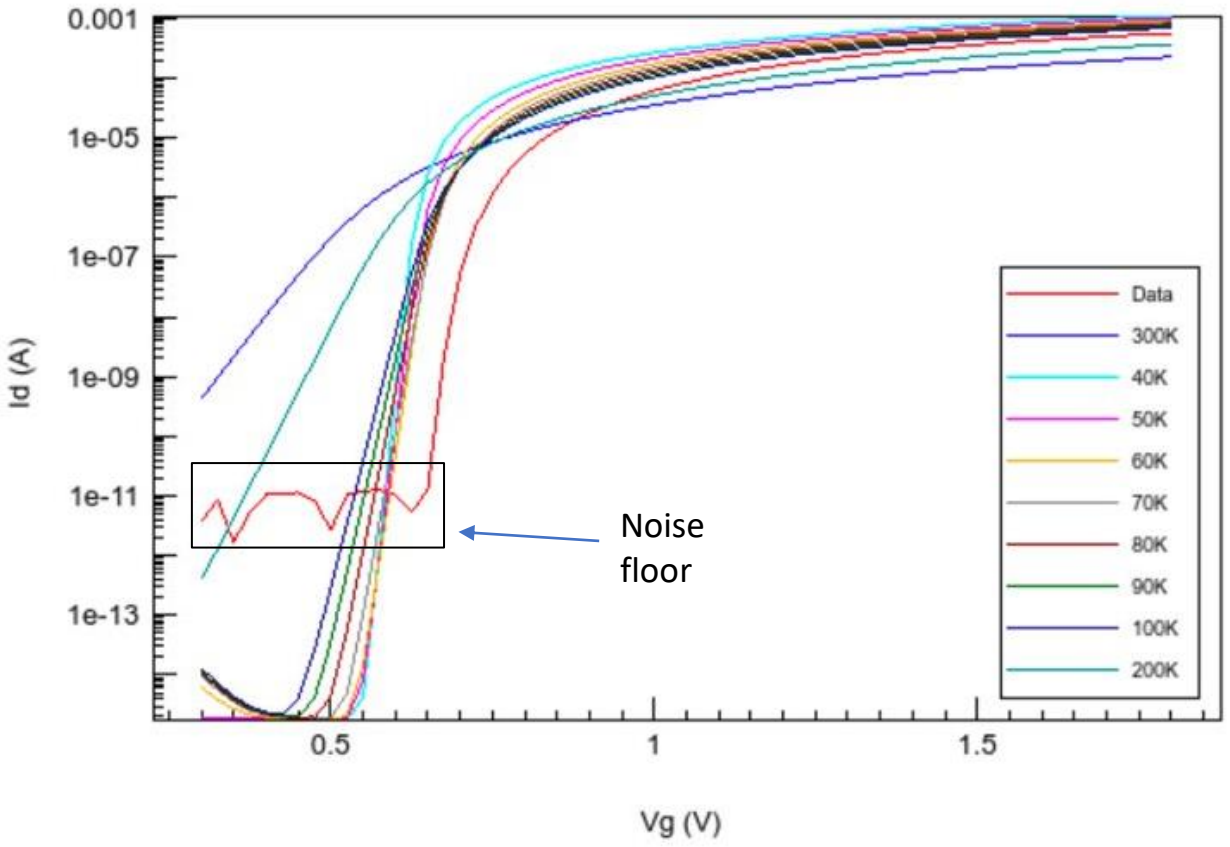
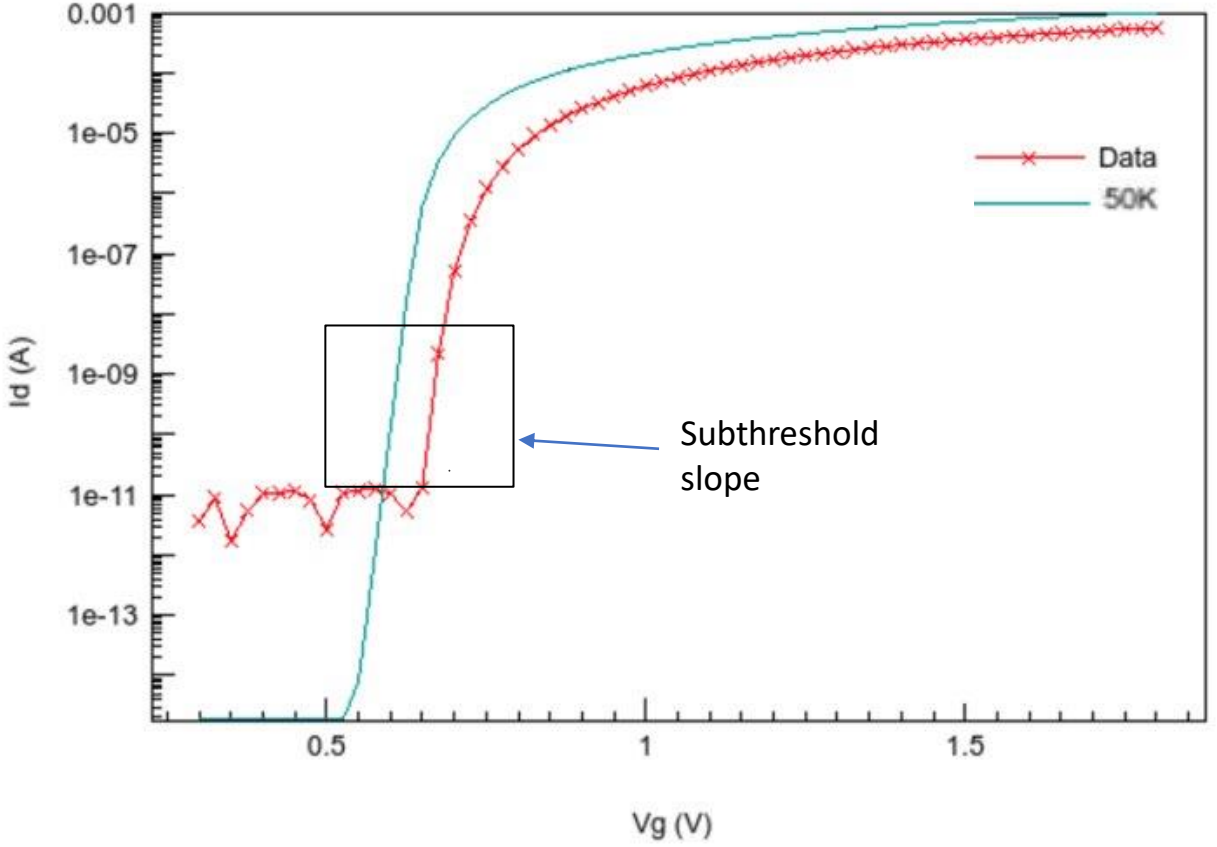
Setting TNOM Value

Adjust temp=tnom and find where the subthreshold slope best fits:

Transfer Characteristics for Vd=1.8V



Transfer Characteristics for Vd=1.8V



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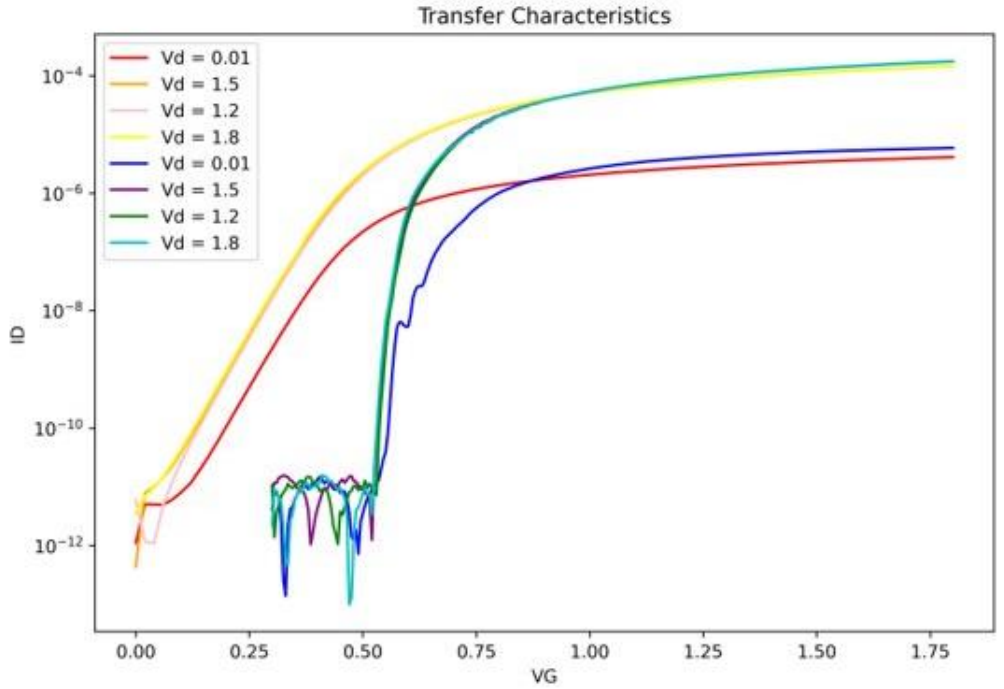
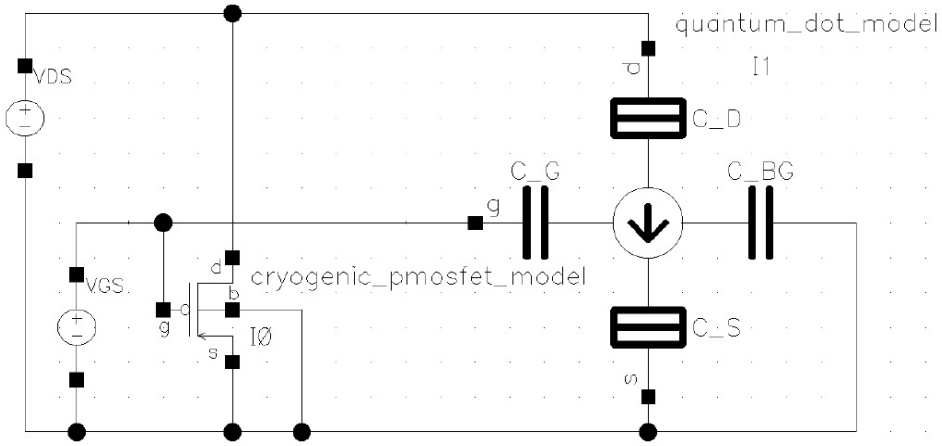
Subthreshold Current Jumps

Some short channel lengths show this effect in our measurement data

This is caused by resonant tunneling via the ionized dopant [15] [16] [19]

These effects are not modeled for the time being, but can be modeled via Verilog wrappers (see S. Bonen presentation and S. Tripathi paper)





Tripathi, S. Pati, et al. "Characterization and modeling of quantum dot behavior in FDSOI devices." *IEEE Journal of the Electron Devices Society* 10 (2022): 600-610.

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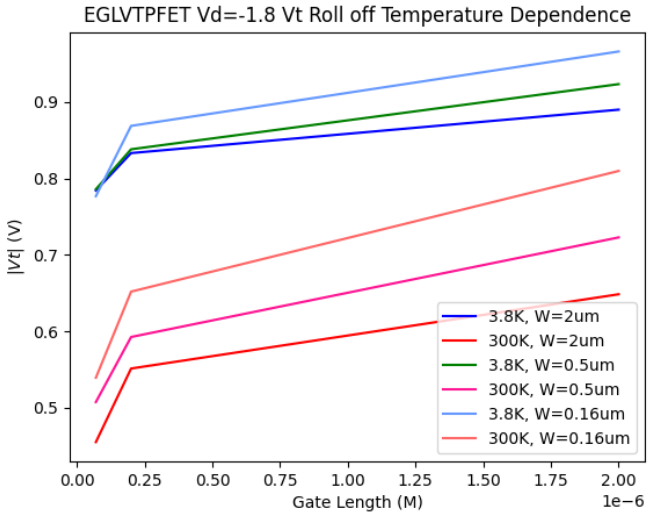
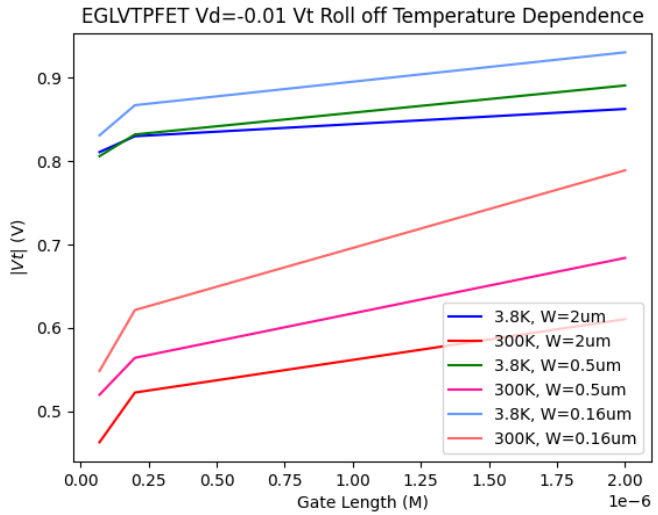
Behavior Changes at Cryogenic Temperatures

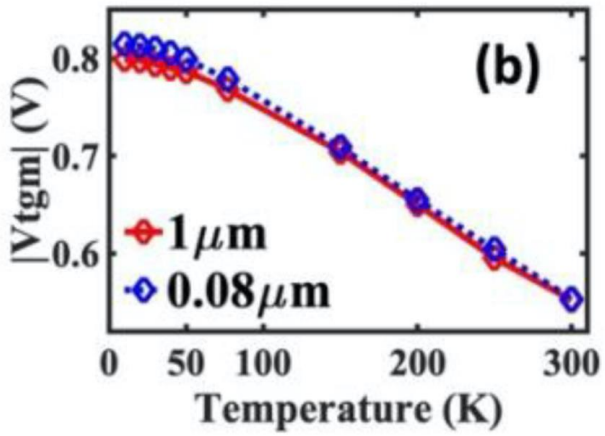
- Electron Mobility [2]
- Phonon scattering, coulomb scattering [3]
- Capacitance effects [4]
- Resistance due to self-heating [5]
- Source drain extension resistance [6]
- Velocity saturation [7][8]
- Work function [7][9]
- Subthreshold slope [10]
- Drain induced barrier lowering [11]
- …etc

Threshold Voltage Expectation at Cryogenic Temperatures

- Increase in Vt as temperature decreases seen in 28nm FDSOI [12]
- Our 22nm FDSOI data reflects this trend, with an average 250 mV difference in Vt across all lengths/widths:







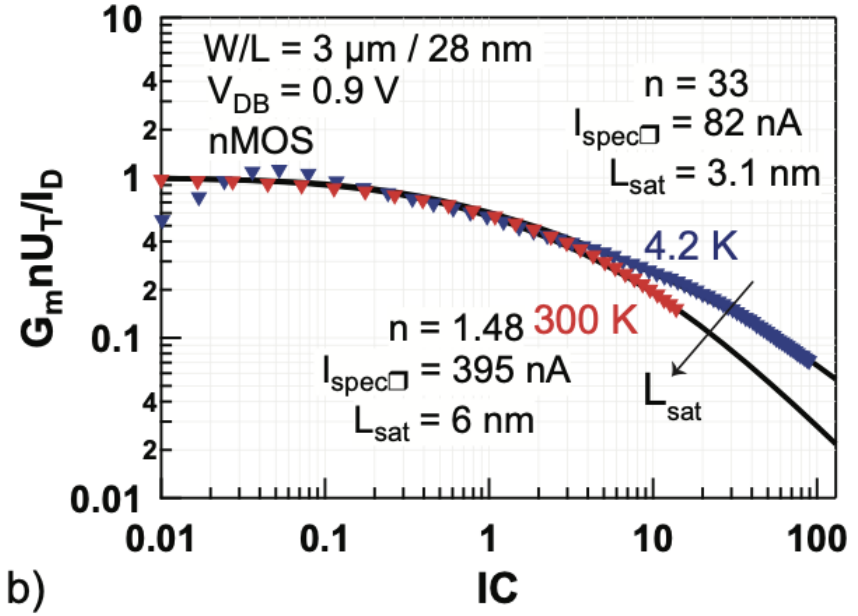
|Vt| vs temperature at Vds=50mV using maximum transconductance method for a 28nm FDSOI pmos device at Vb=0, taken from [12]

Used **fixed current criteria** rather than GmMax to get a smoother roll off across geometries (GmMax method in backup slides)

High drain roll-off usually shows a **bigger difference in Vt because of DIBL**, at cryo we want Vt geometry dependence to be **more linear,** which is seen in the rightmost plot

Velocity Saturation Expectation at Cryogenic Temperatures

Decrease in impact of velocity saturation seen in 28nm FDSOI [7][8]



b) Normalized transconductance efficiency versus the inversion coefficient for nMOS W/L = 3 µm / 28 nm, showing a decreased velocity saturation effect at 4.2 K. [7]

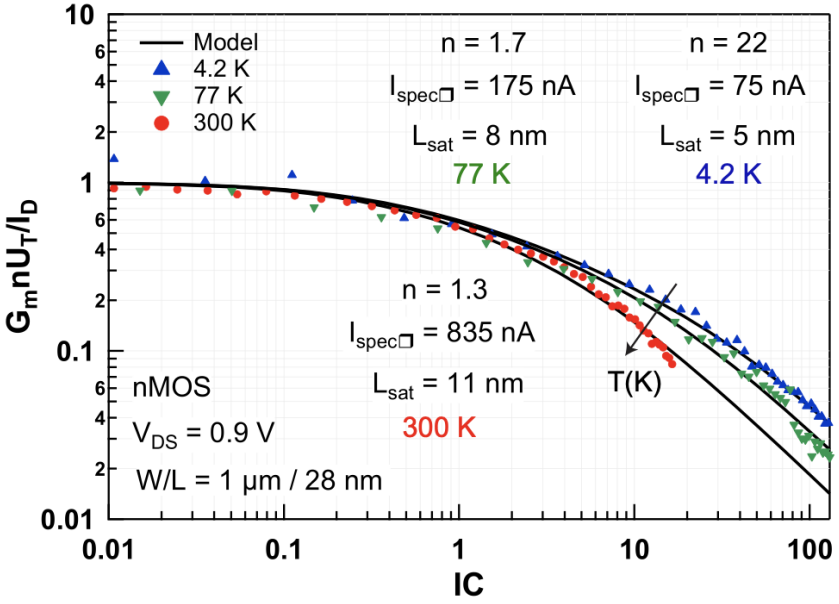


Figure 10: Modeling the normalized transconductance efficiency at 300, 77, and 4.2 K in a short 28-nm FDSOI nMOS in saturation. Model parameters are given in the figure. [8]

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Source/Drain Resistance Expectation at Cryogenic Temperatures

- In 22nm FDSOI a **11-15% decrease** seen in S/D resistance [13]

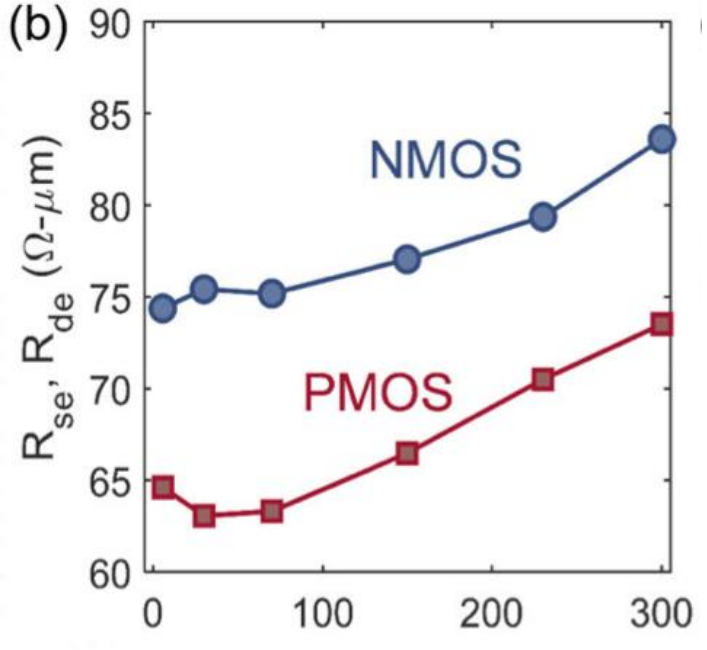
- Improvement in gate resistance:

  - **Prwg** models gate dependence of S/D resistance in BSIM 102.9.6, and as it **increases, overall resistance should decrease** (Our models reflect this)

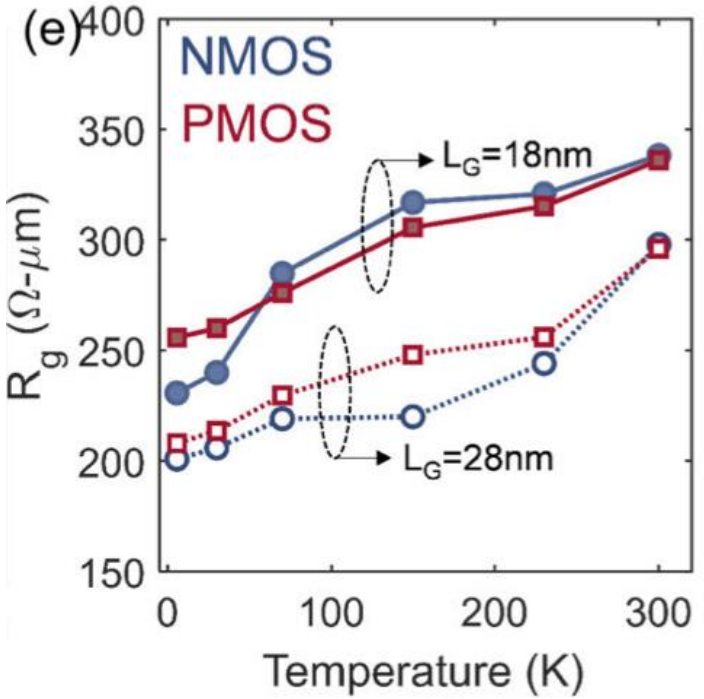
From BSIM-IMG 102.9.6 Manual:

$$R_{source} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RSWMIN(T) + \frac{RSW(T)}{1 + PRWG \cdot V_{gs,eff}} \right) + R_{s,geo}$$

$$R_{drain} = \frac{1}{W_{new}^{WR} \cdot NF} \cdot \left(RDWMIN(T) + \frac{RDW(T)}{1 + PRWG \cdot V_{gd,eff}} \right) + R_{d,geo}$$



Source/drain series resistance (*R*se, *R*de) improve by 15% at 5.5 K [13]



Reduced resistivity of gate metal contact (NiSi) and poly-Si cause gate resistance (*R*ge) reduction at cryogenic temperature. [13]

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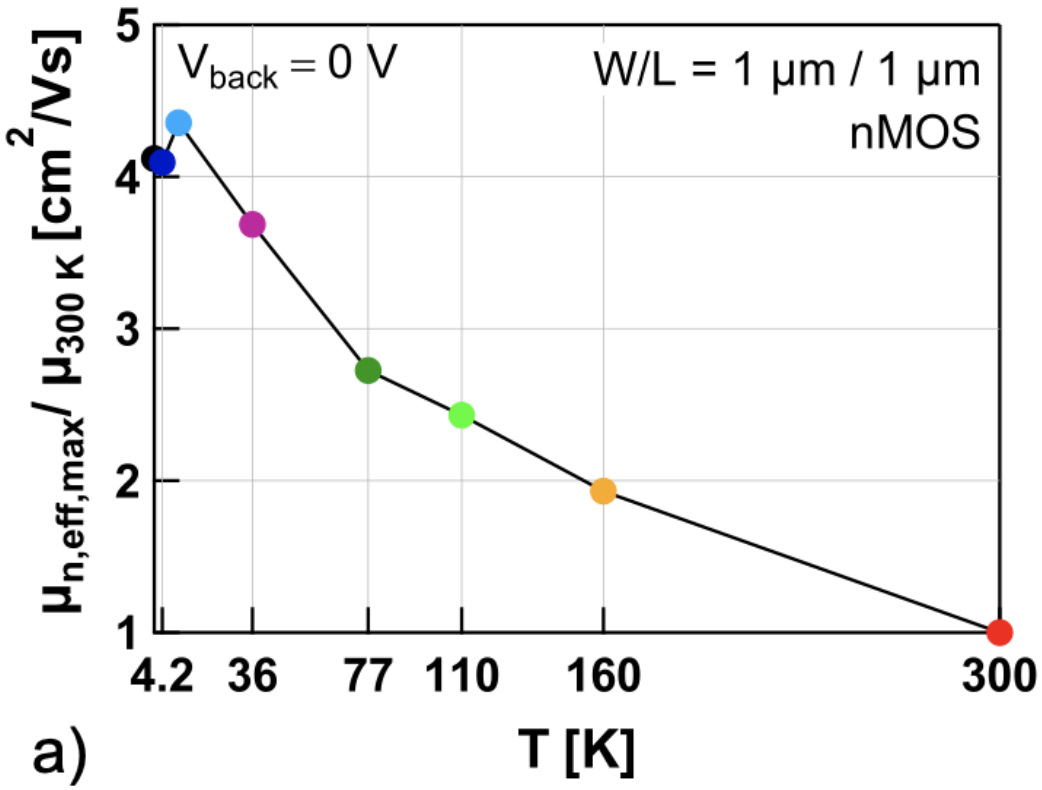
Mobility Expectation at Cryogenic Temperatures

- Effective mobility is made of three main components:
  - Lattice vibration-induced scattering
  - Scattering on impurities (Coulomb and phonon scattering)
  - Surface Roughness Scattering

- At cryogenic temperatures Coulomb Scattering becomes more dominant increasing mobility [2]



Effective Mobility Temperature dependence in 28nm FDSOI [3]

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BSIM-IMG Recommended Strategy as a Basis

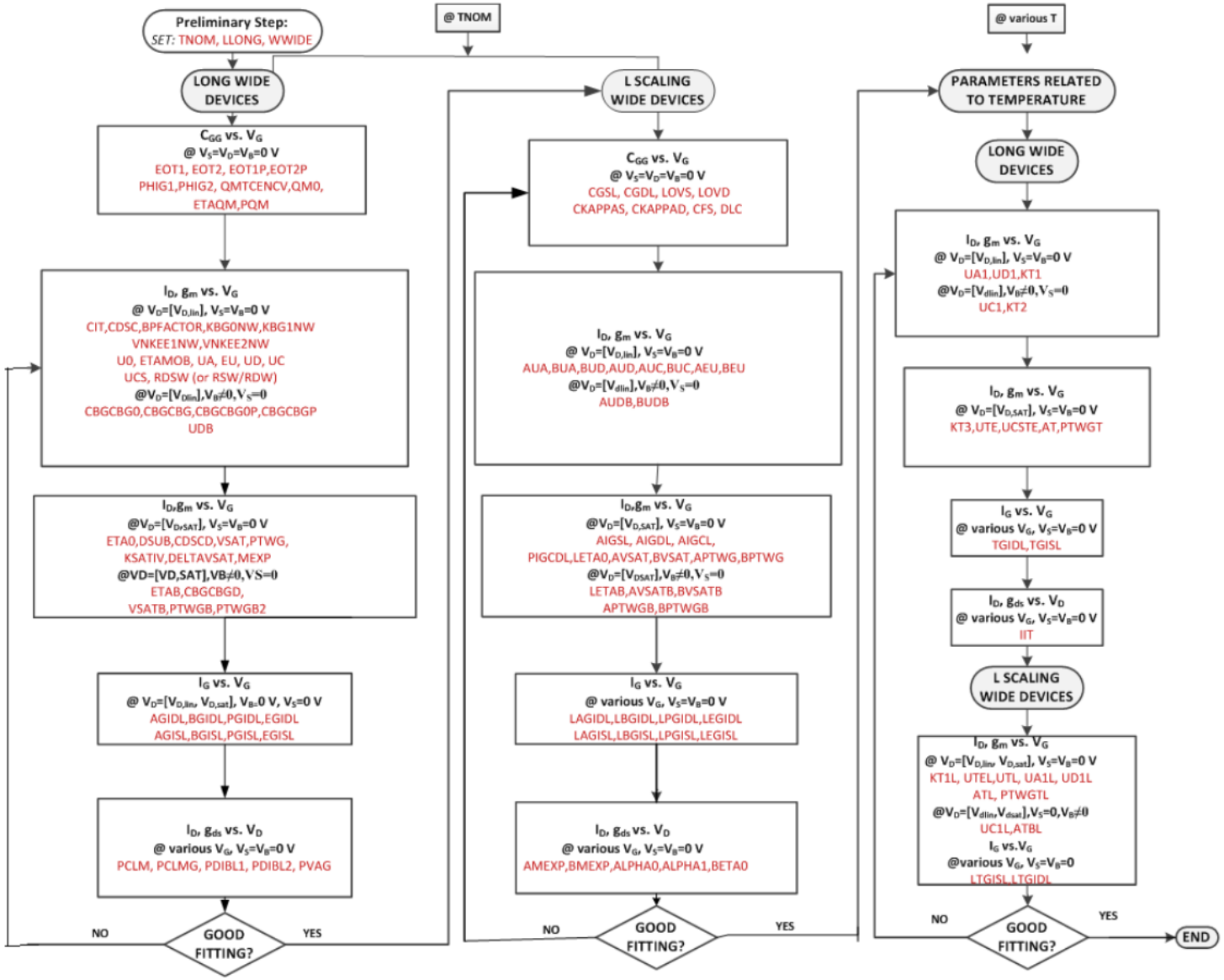

Figure 13: Parameters Extraction Procedure in BSIM-IMG Model.

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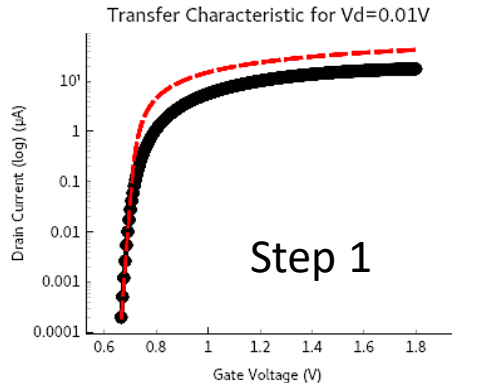
Building an Extraction Strategy

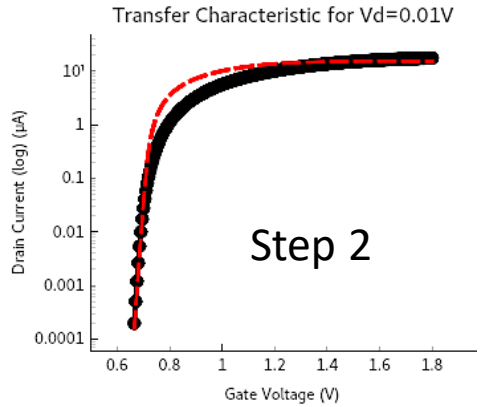
- **Stages:** Contain *groups of isolated parameters* that mainly influence each other
  - **Steps:** Subgroups of parameters that impact v*arious target regions* of the curves within each stage
  - **Loop:** *Repeat Steps* until a good fit is reached

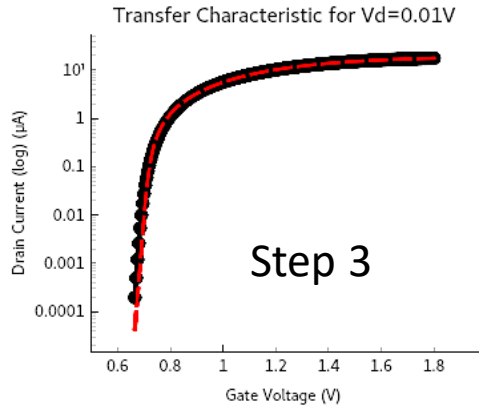
Example: Stage 1
(u0,ua,ud,rdw, rsw, cit, phig1) impact Low Drain Bias curve

Step 1: (phig1, cit) fit to subthreshold region
Step 2: (u0,ua,ud) fit to Ion region
Step 3: (rdw, rsw) fit to threshold voltage region

Loop steps 1-3 until a good fit requirement is met

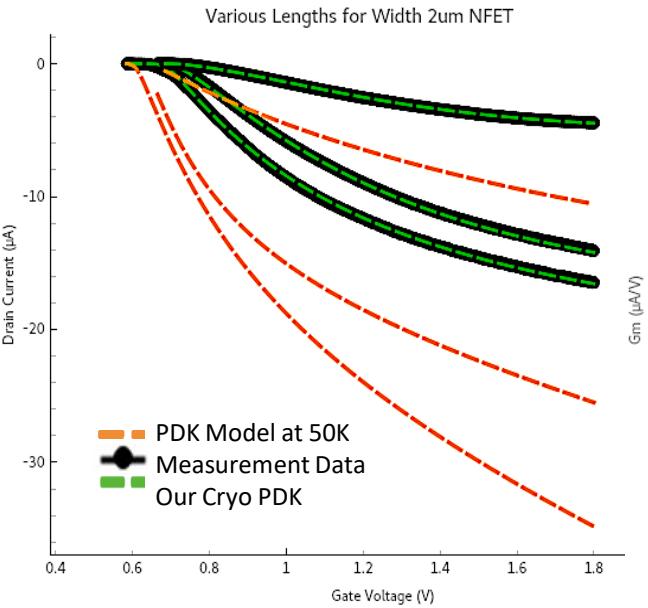


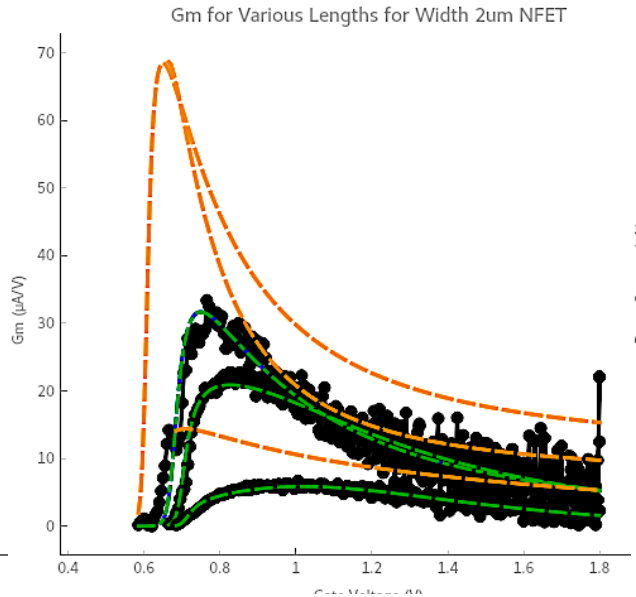


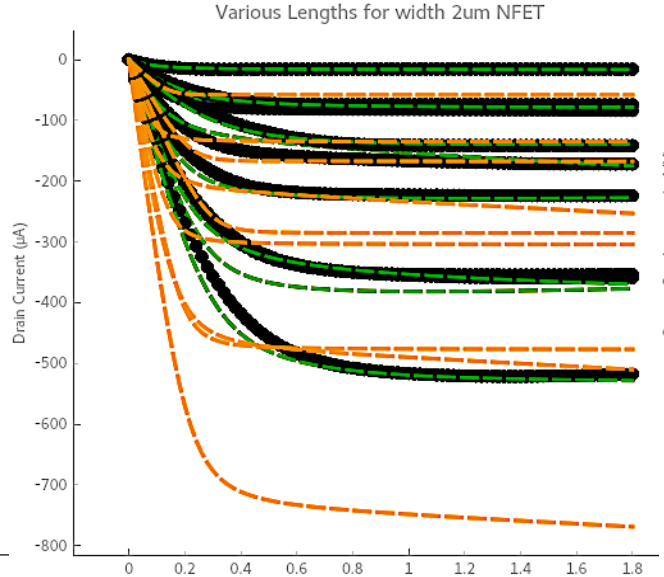


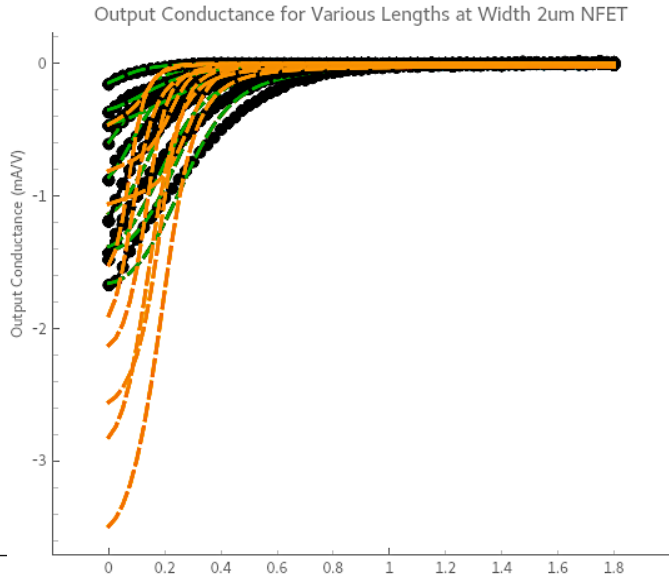
Results of our Cryo PDK:

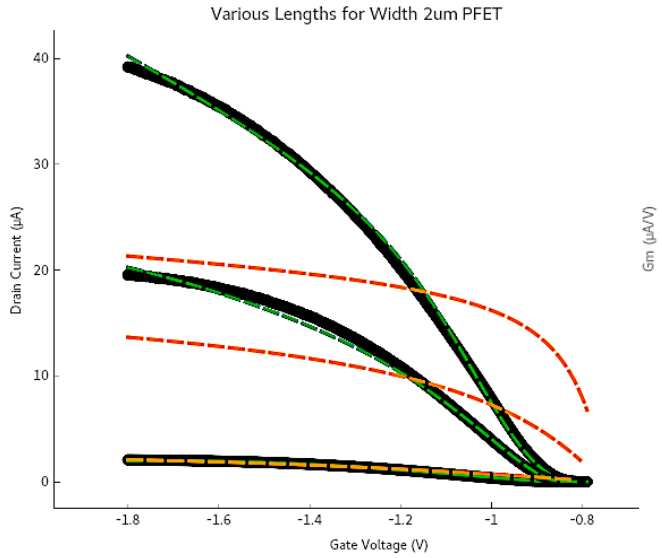
EGLVT Lengths 70-2000nm:

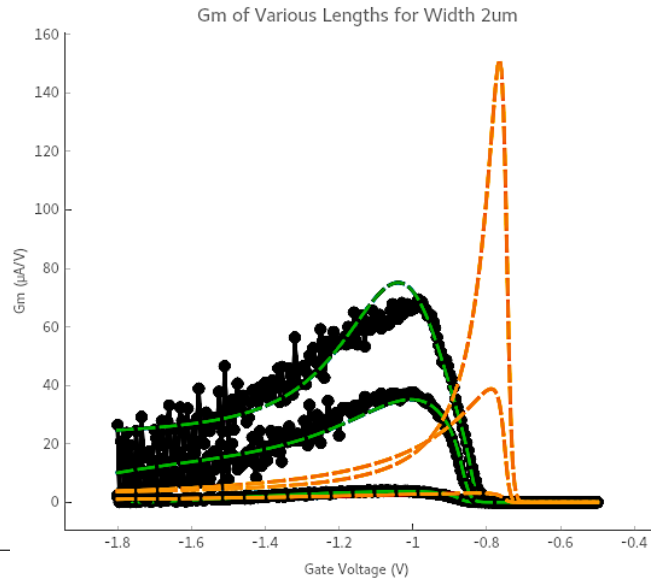


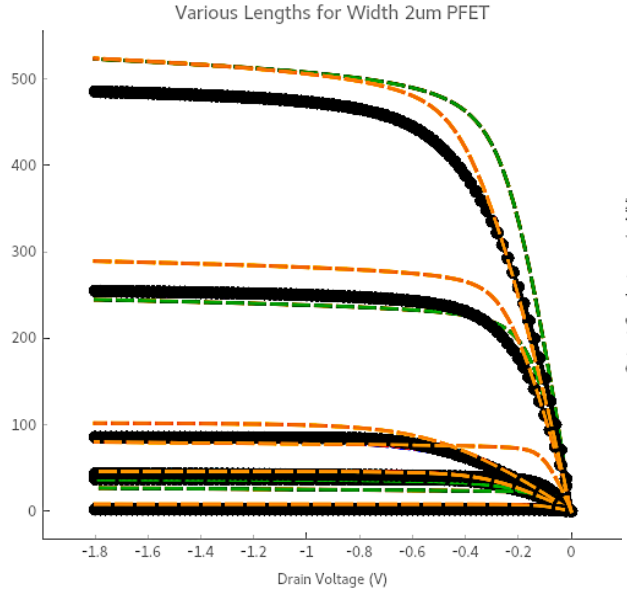


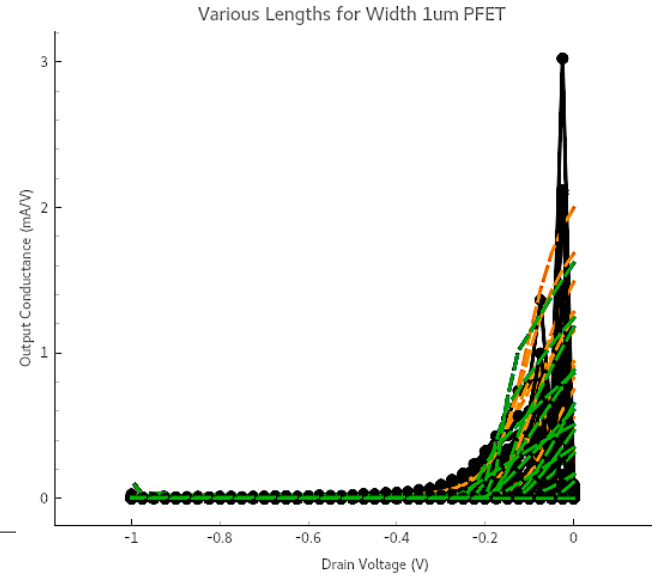












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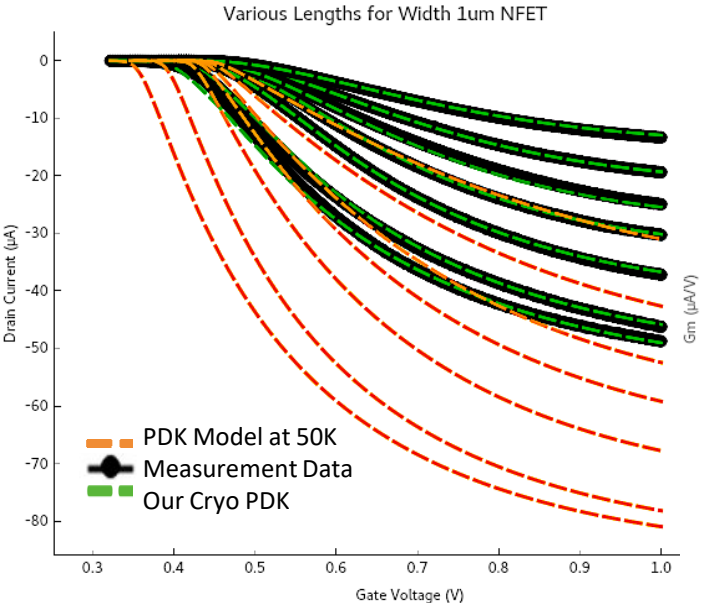
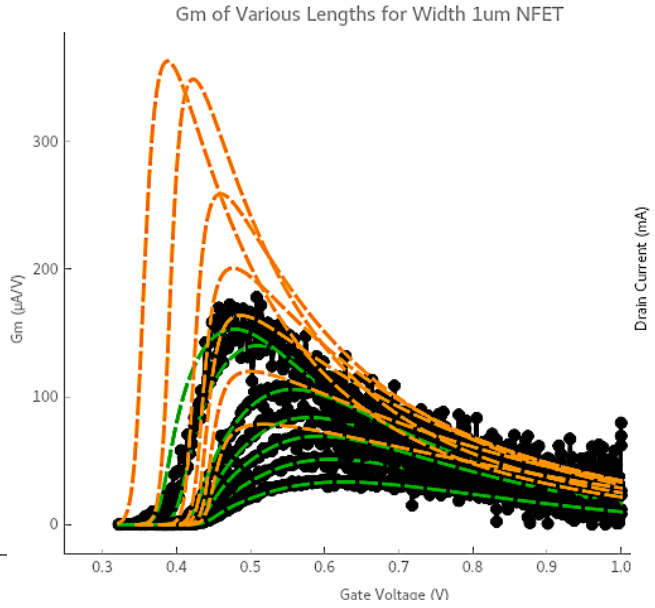
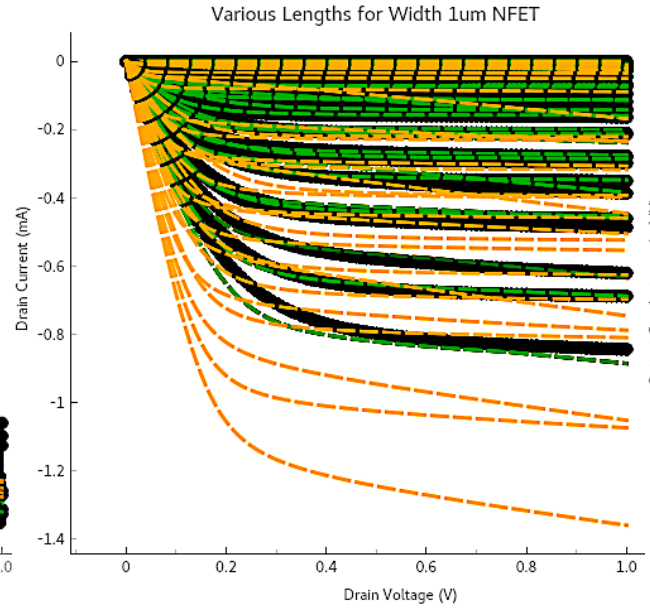
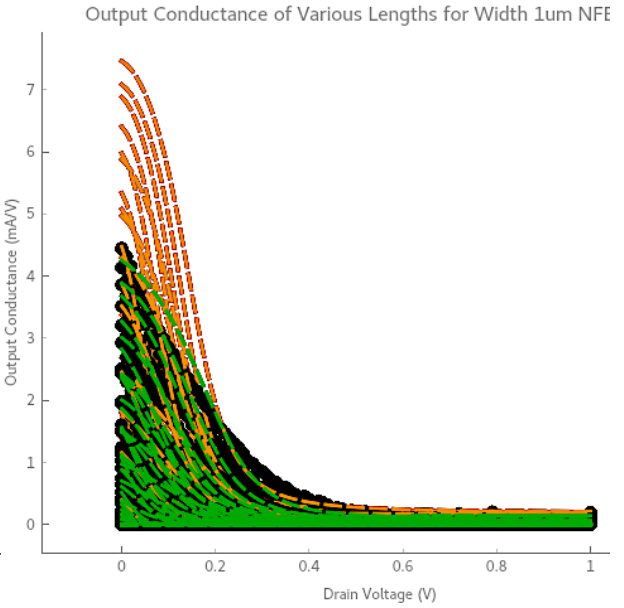
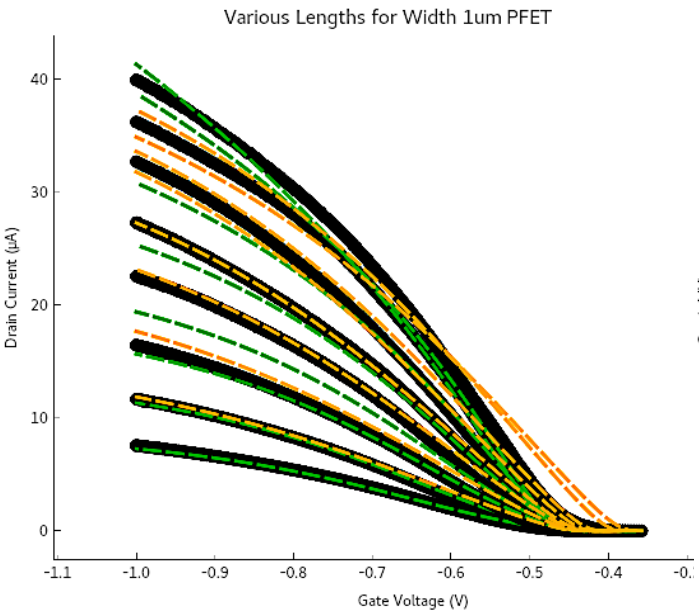
SLVT Lengths 30-500nm:

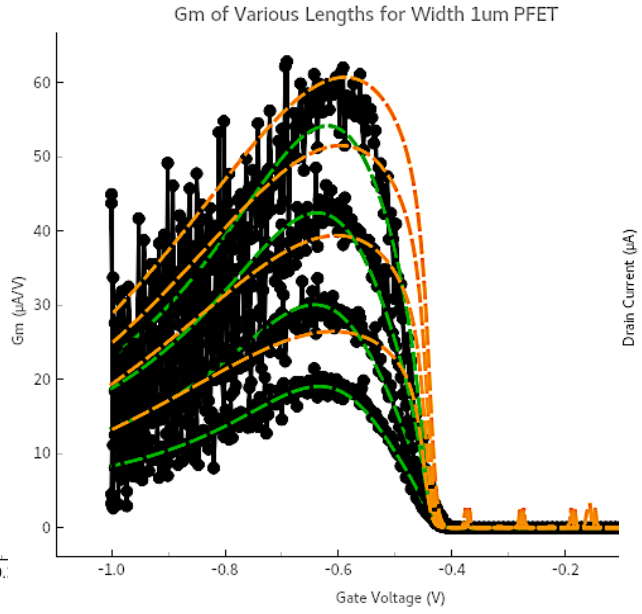


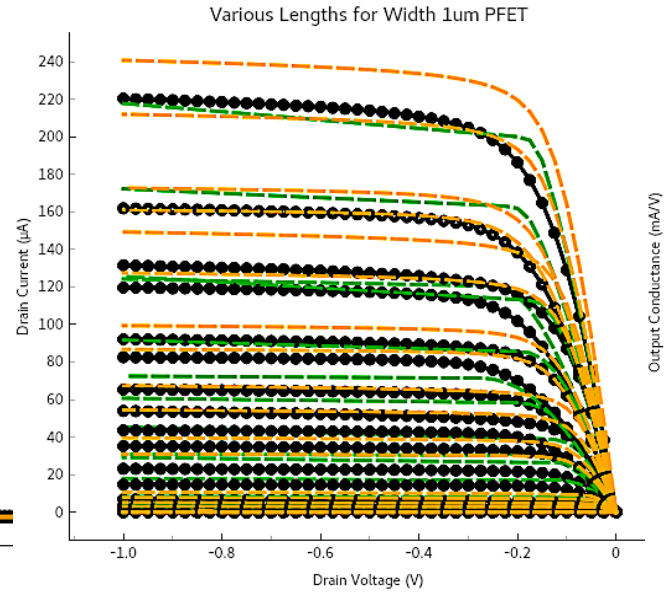


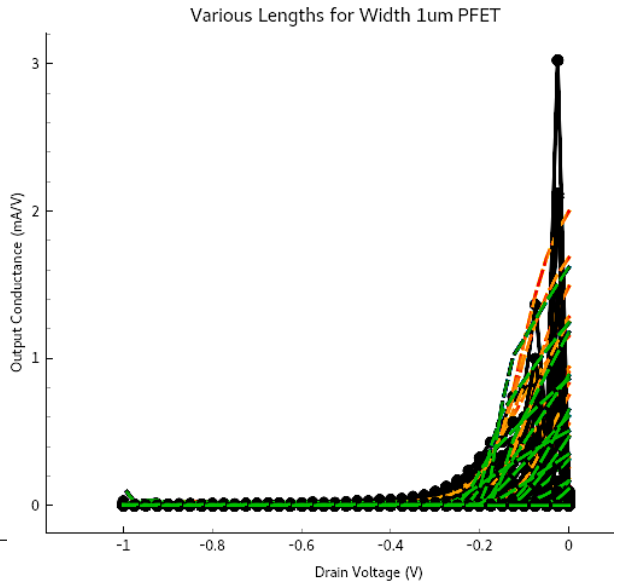












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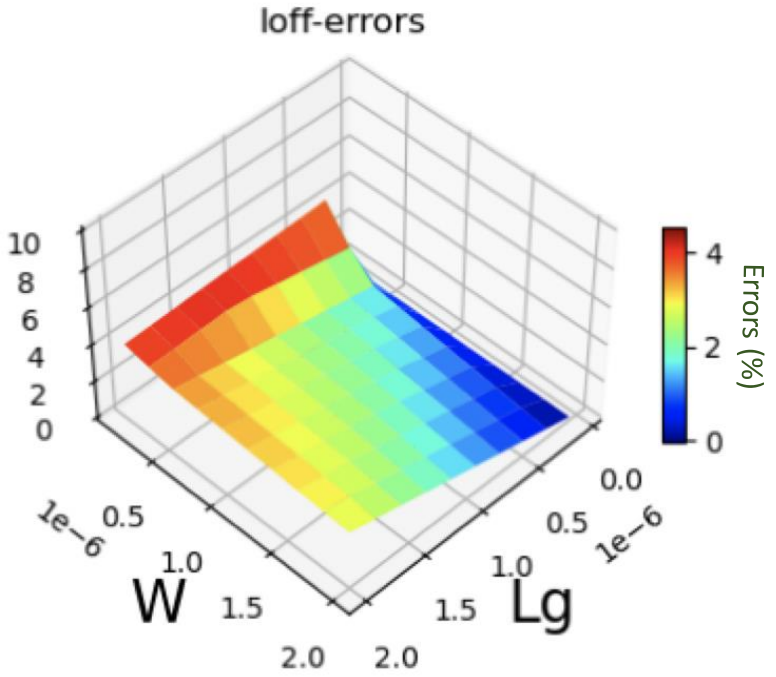
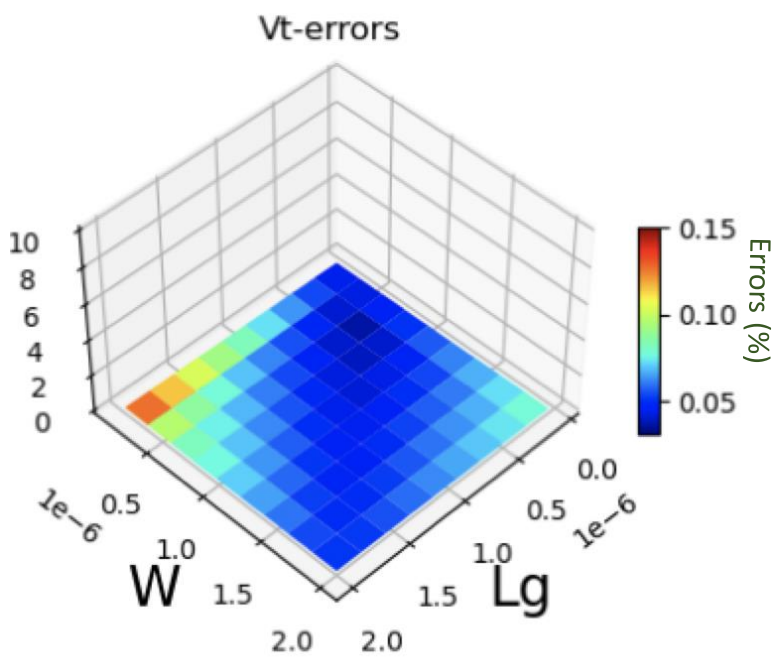
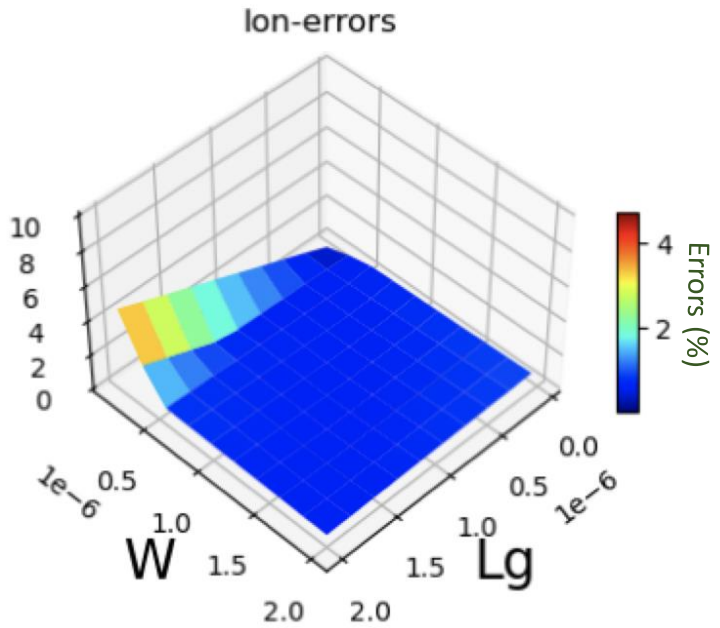
Errors across Figures of Merit for all Lengths and Widths (EG Devices)

Found by taking the percentage error between data simulated using the extracted model and the measurement data (for transfer characteristics):







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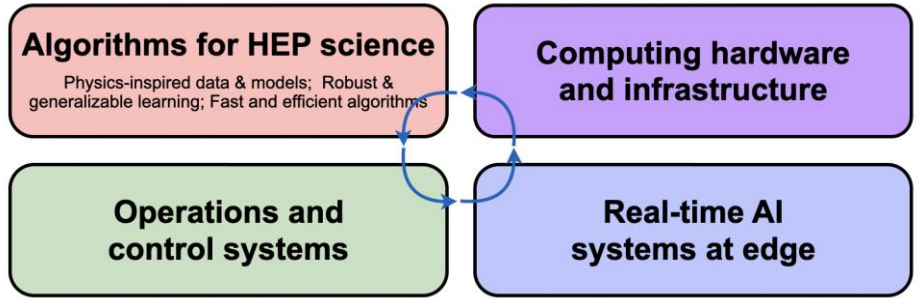
AI/ML Modelling for Extreme Environments

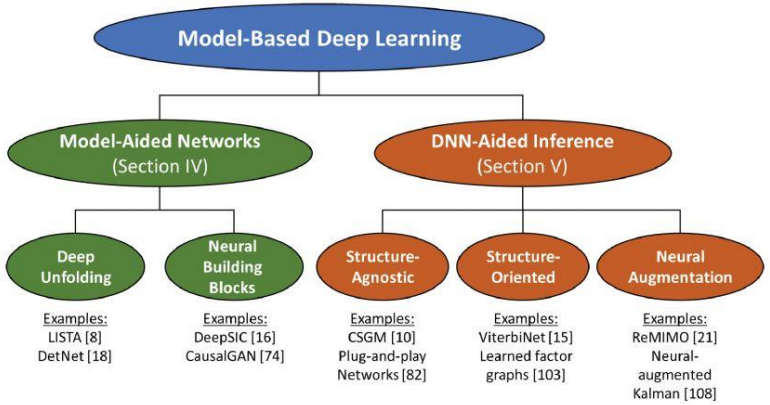


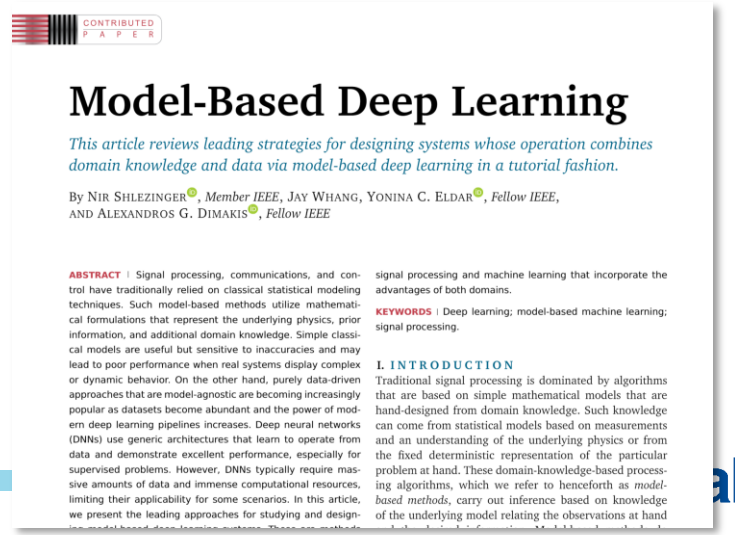
Fermilab has expertise with AI across a wide array of tasks and methods

- Develop robust models, adaptable across domains (temperatures)

With are currently considering 3 scenarios:

1. PDK compatible SPICE models using AI/ML extracted parameter values
   - Use AI/ML to enhance specialized tools, ameliorate difficulties for modelling engineers, rapidly develop models for extreme environments
2. Make a data driven model that bypasses compact models all together
   - This is where most of the work in AI/ML based transistor modeling has been done
3. Collaborate with Synopsys to integrate AI/ML in their tools. Expertise with AI across a wide array of tasks and methods





CONTRIBUTED PAPER

Model-Based Deep Learning

This article reviews leading strategies for designing systems whose operation combines domain knowledge and data via model-based deep learning in a tutorial fashion.

By Nir Shlezinger, *Member IEEE*, Jay Whang, Yonina C. Eldar, *Fellow IEEE*, and Alexandros G. Dimakis, *Fellow IEEE*

ABSTRACT | Signal processing, communications, and control have traditionally relied on classical statistical modeling techniques. Such model-based methods utilize mathematical formulations that represent the underlying physics, prior information, and additional domain knowledge. Simple classical models are useful but sensitive to inaccuracies and may lead to poor performance when real systems display complex or dynamic behavior. On the other hand, purely data-driven approaches that are model-agnostic are becoming increasingly popular as datasets become abundant and the power of modern deep learning pipelines increases. Deep neural networks (DNNs) use generic architectures that learn to operate from data and demonstrate excellent performance, especially for supervised problems. However, DNNs typically require massive amounts of data and immense computational resources, limiting their applicability for some scenarios. In this article, we present the leading approaches for studying and design-

signal processing and machine learning that incorporate the advantages of both domains.

KEYWORDS | Deep learning; model-based machine learning; signal processing.

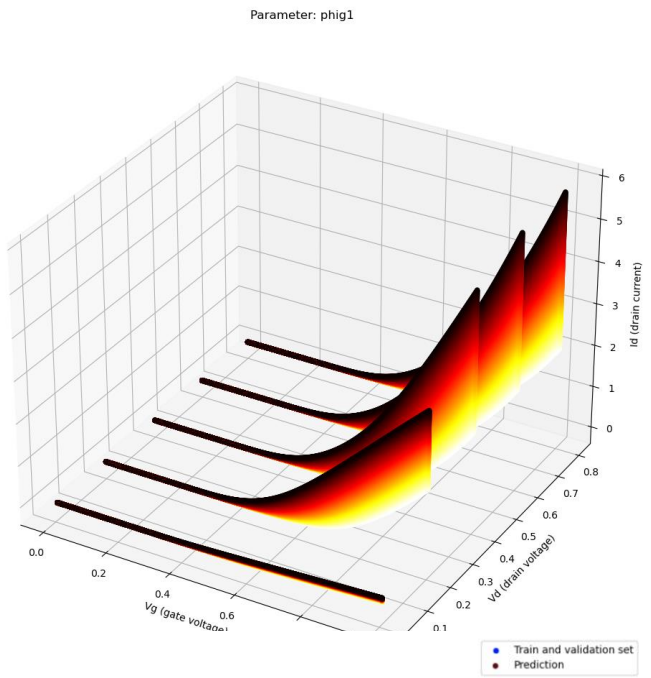
I. Introduction

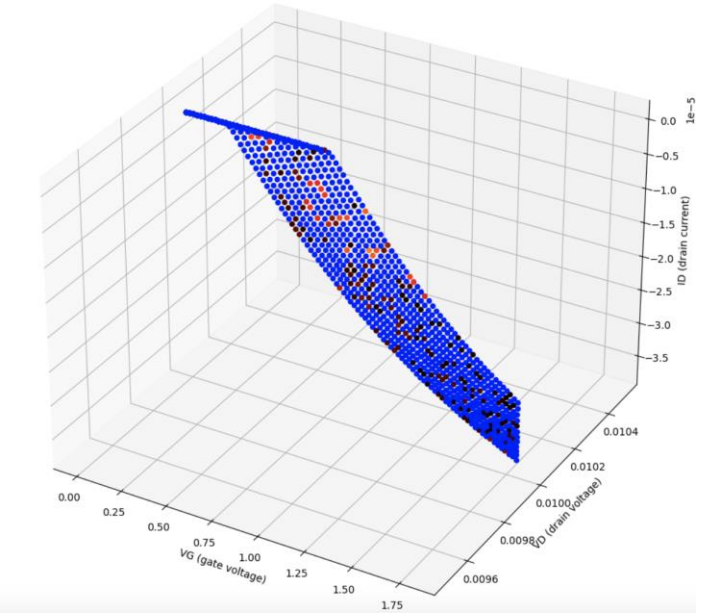
Traditional signal processing is dominated by algorithms that are based on simple mathematical models that are hand-designed from domain knowledge. Such knowledge can come from statistical models based on measurements and an understanding of the underlying physics or from the fixed deterministic representation of the particular problem at hand. These domain-knowledge-based processing algorithms, which we refer to henceforth as *model-based methods*, carry out inference based on knowledge of the underlying model relating the observations at hand

In House ML Algorithm for Cryo-Modeling (In Progress)

Goal: Find optimal value of 16 parameters using machine Learning

- **Inputs:** Drain current that is dependent on gate length (L), width (W), gate voltage (Vg), drain voltage (Vd), and a 39 count parameter set (P)
  - Id = f(L,W,Vg,Vd,P)
- **Outputs:** Optimal values for all 39 parameters that can simulate data using HSPICE as close as possible to the actual measurement data values
- Training the impact of changing a model parameter on drain current. Cadence simulated data from PDK model at 50K
- Starting algorithm that predicts one parameter to the accuracy needed





Future work

- **Complete 4K PDK-compatible models**, including back gate biasing
- Develop 4K static **timing libraries** for standard cell library
- Cryogenic **noise measurements**
- Quantify cryogenic **measurement error**
- **AI/ML** modeling and extraction for cryo-PDK development for extreme environment
- Develop cryo-PDK for **GF 28HV**

Work supported by the U.S. Department of Energy, Office of Science (Microelectronics Codesign), URA Visiting Scholars Fellowship, and Fermilab LDRD.

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"A Single-Channel 18.5 GS/s 5-bit Flash ADC using a Body-Biased Comparator Architecture in 22nm FD-SOI""
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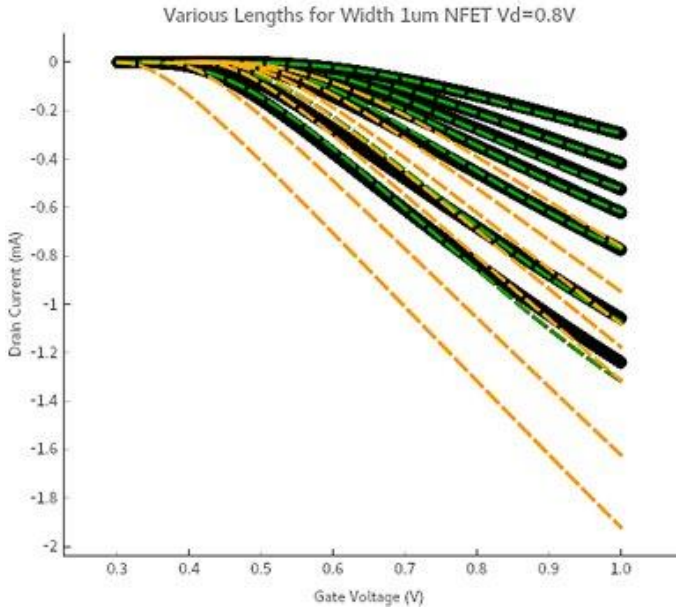
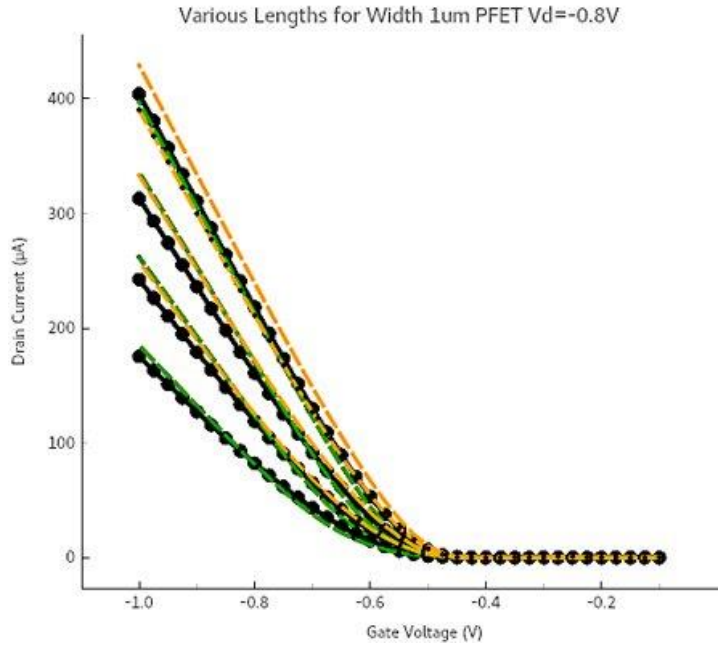
Backups

EGLVT Lengths
70-2,000nm:

Measurement Data
Our Cryo PDK

SLVT Lengths
30-500nm :





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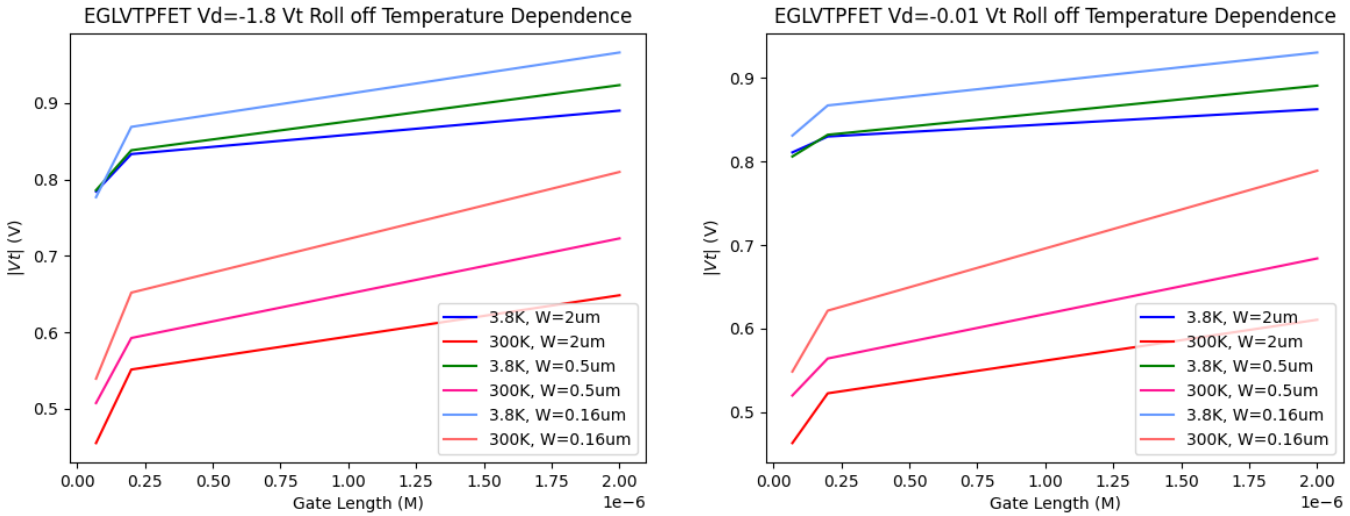
Threshold Voltage Expectation at Cryogenic Temperatures

- Increase in Vt as temperature decreases seen in 28nm FDSOI [12]
- Our 22nm FDSOI data reflects this trend, with an average 250 mV difference in Vt across all lengths/widths:



Used **fixed current criteria** rather than GmMax to get a smoother roll off across geometries (GmMax method in backup slides)

High drain roll-off usually shows a **bigger difference in Vt because of DIBL**, at cryo we want Vt geometry dependence to be **more linear,** which is seen in the rightmost plot

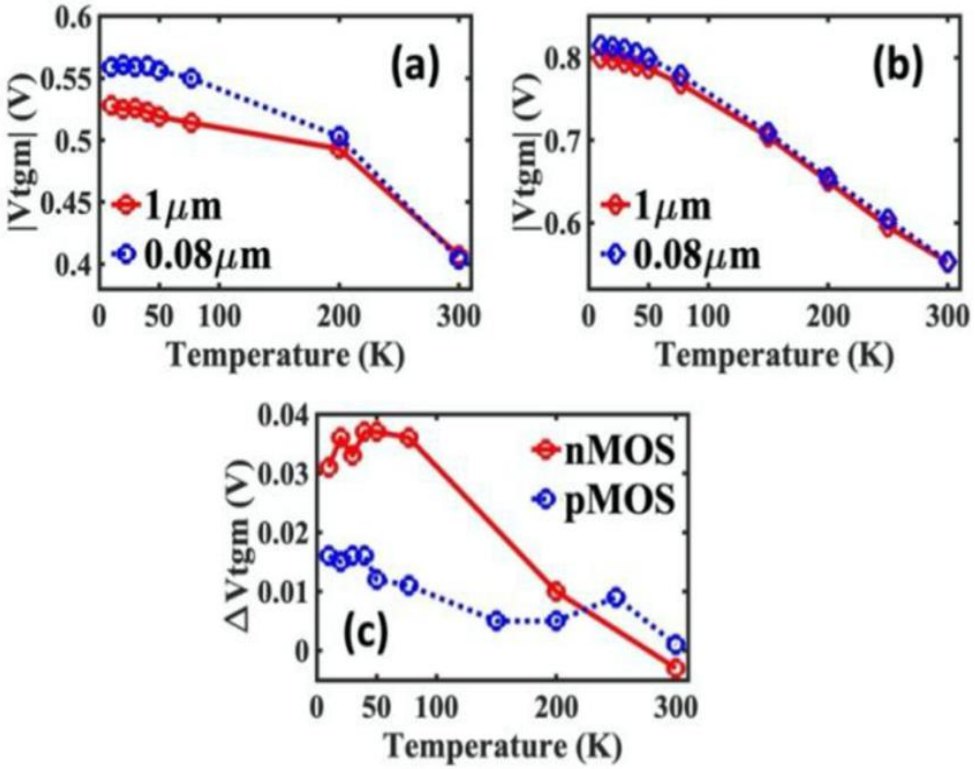


FIGURE 4. **|*Vt*| vs Temperature at |Vds|=50 mV using maximum transconductance method for (a) nMOS and (b) pMOS, (c) Δ*Vt* vs temperature using maximum transconductance method. The back-gate bias (*Vbs*) = 0 V.** [12]

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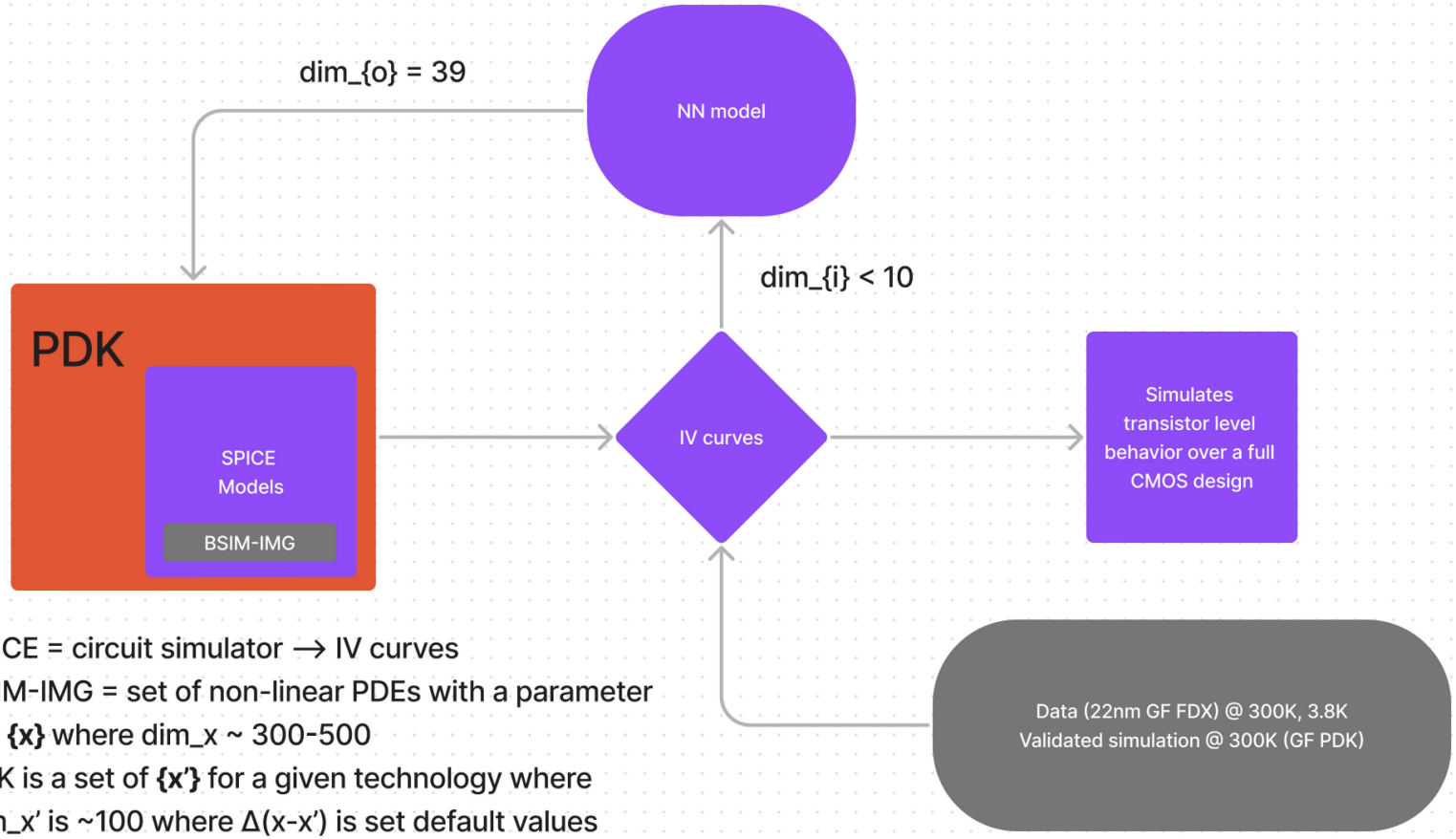
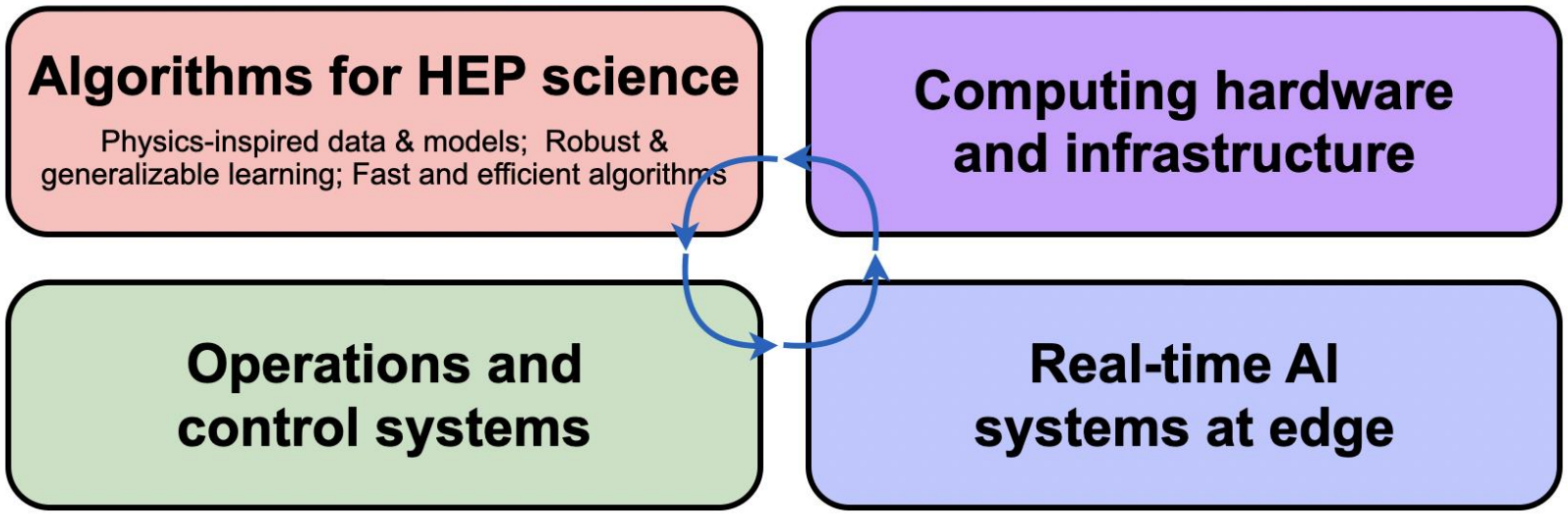
Workflow



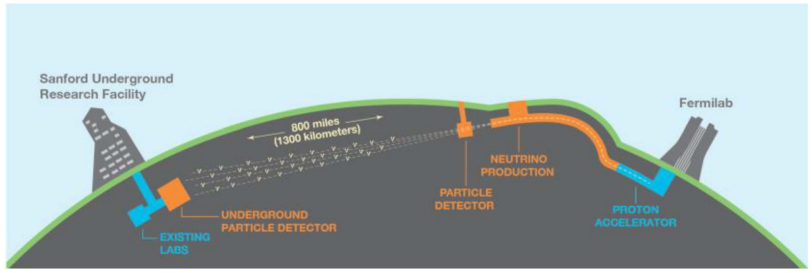
- SPICE = circuit simulator → IV curves
- BSIM-IMG = set of non-linear PDEs with a parameter set **{x}** where dim_x ~ 300-500
- PDK is a set of **{x'}** for a given technology where dim_x' is ~100 where Δ(x-x') is set default values
  - dim_x'' = 39 where x'' are the parameters dependent on T

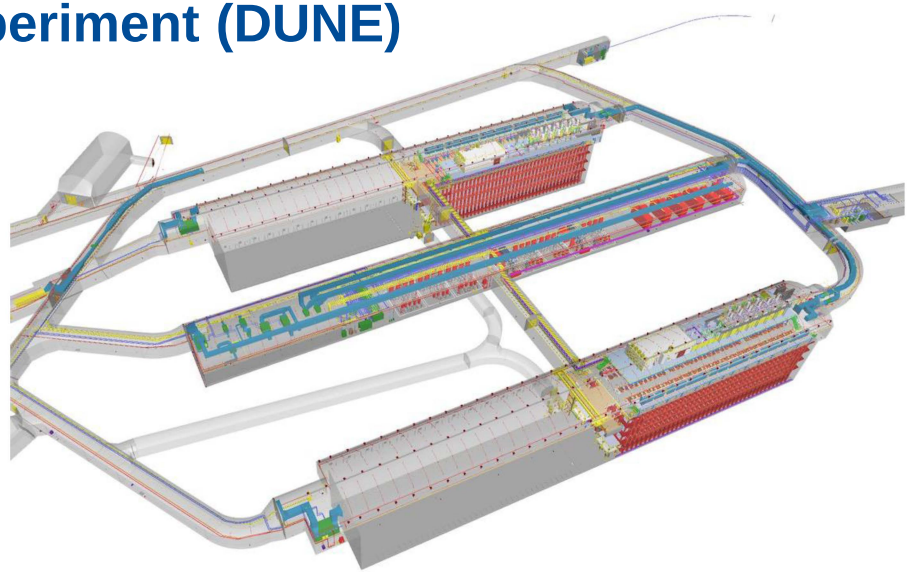
AI at Fermilab

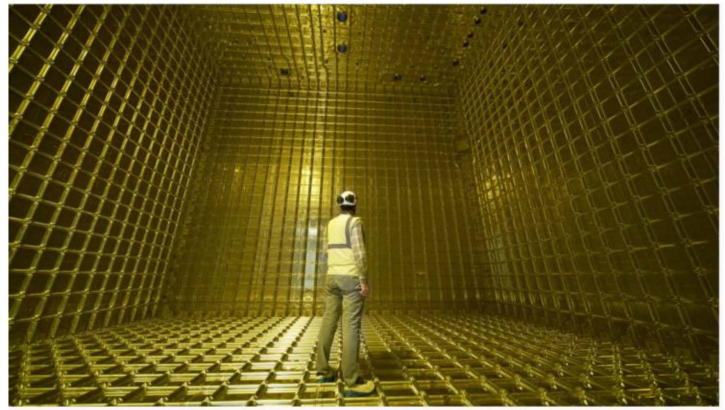
- Expertise with AI across a wide array of tasks and methods
  - Develop robust models, adaptable across domains (temperatures)
- For this project, develop regression and surrogate models
  - Potentially explore inductive bias / physics-informed models based on physics knowledge/PDEs; e.g. BSIM-IMG model

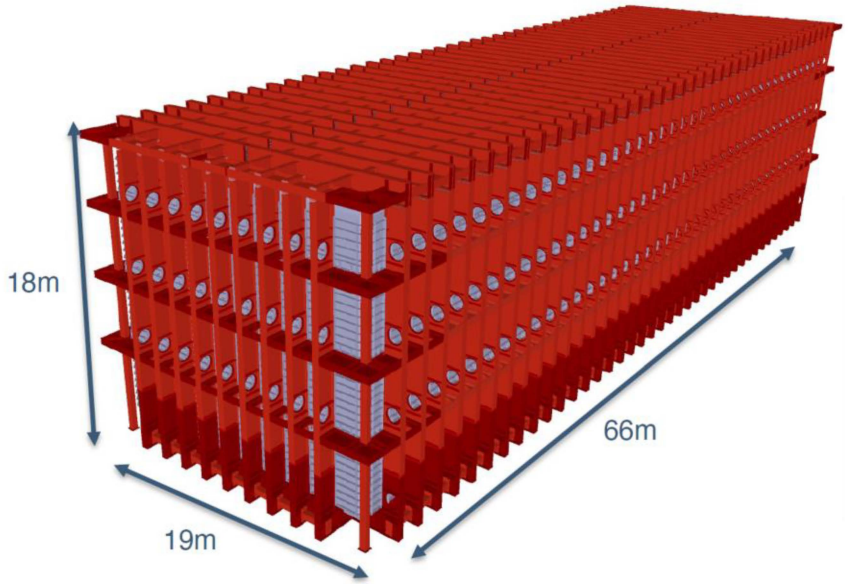


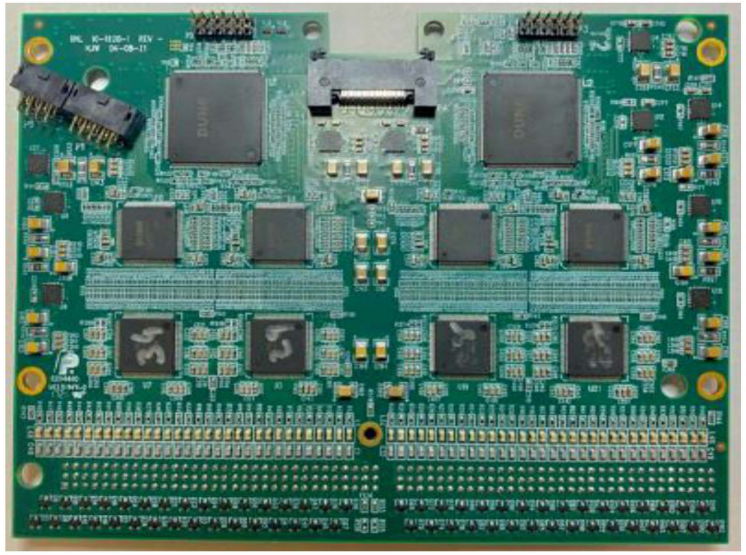
Deep Underground Neutrino Experiment (DUNE)



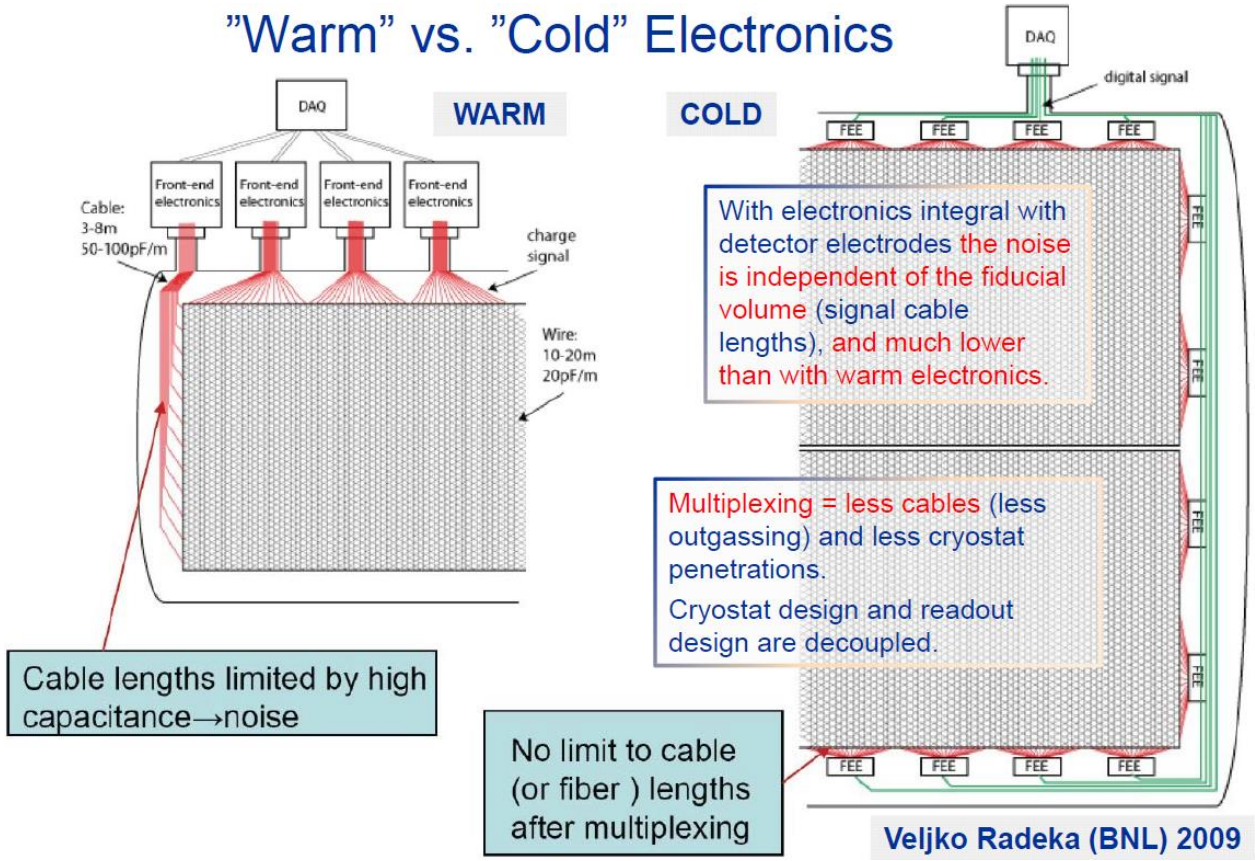








Operation in liquid Argon



Requirements

- Negligible risk of failure due to the hot carrier effect (less than 0.7% channel failure in **30 years of operation**)
- Total power consumption <50 mW/channel.
- Fully functional at both room temperature and liquid argon temperature;
- Both control and data links must operate with negligible error rate over cables up to ~30m in length.

Benefits of operating in liquid Argon:

- The **charge carrier mobility** in silicon is higher and thermal fluctuations are lower at liquid argon temperature than at room temperature. For CMOS electronics, this results in substantially **higher gain** and **lower noise** (by about a factor of two) at liquid argon temperature than at room temperature, which greatly extends the reach of the DUNE physics program.
- Mounting the front-end electronics on the anode plane array (APA) frames also **minimizes the input capacitance**.
- Placing the digitizing and multiplexing electronics inside of the cryostat allows for a **reduction in the total number of feed-throughs** into the cryostat, **reducing the expense and complexity** of the experiment.

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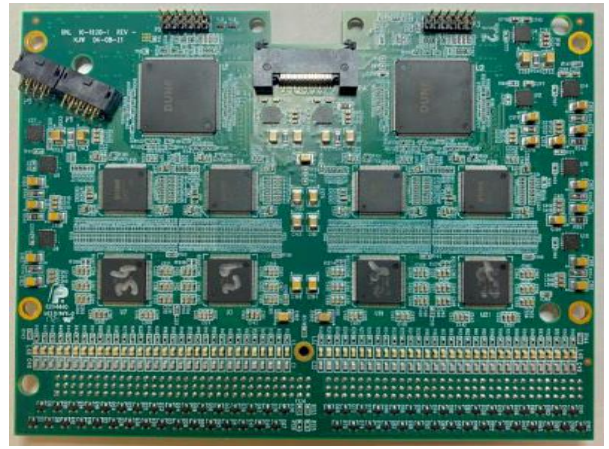
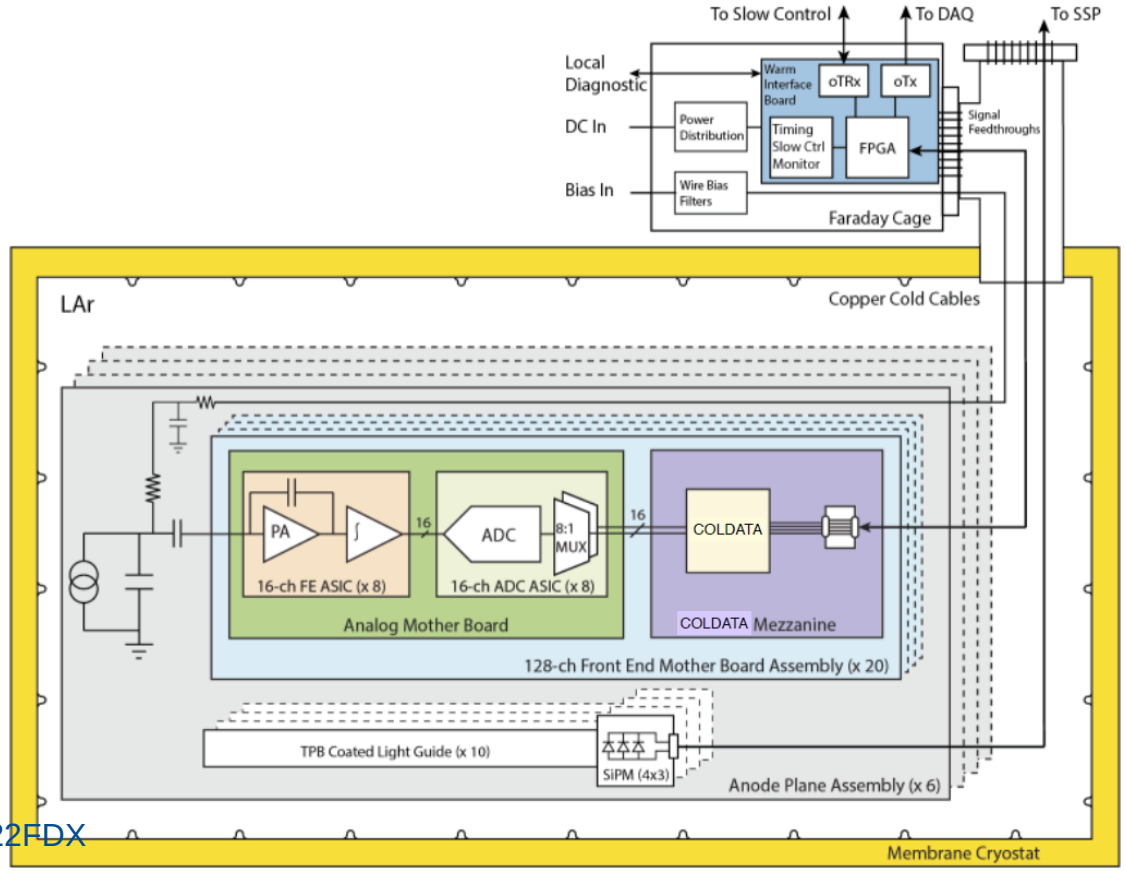
DUNE cryogenic ASICs

- 16-channel front-end ASICs for amplification and pulse shaping (**LArASIC** - BNL);
- 16-channel 12-bit ADC ASICs operating at 2 MHz (**ColdADC** – LBNL+FNAL+BNL);
- 64-channel control and communications ASICs (**COLDATA** – FNAL+SMU)

Element	Quantity
TPC wires (channels)	384K
Anode plane array (APA)	150
Front End Mother Board (FEMB)	3000
FE ASIC	**24000**
ADC ASIC	**24000**
COLDATA ASIC	**6000**



- Large number of components requiring testing and qualification at both roomT and LAr
- Future proposed pixelated readout schemes with >100M channels (<100µW/channel), SiPh for readout and power delivery, chiplet-based or monolithic chips with integrated sensing, computing and communication



Large scientific experiments challenges and requirements:

- Performance (low noise, low power)
- Thermal and system constraints (e.g feedthroughs)
- Reliability (lifetime, SEE)
- Large # channels
- Radiopurity, etc.

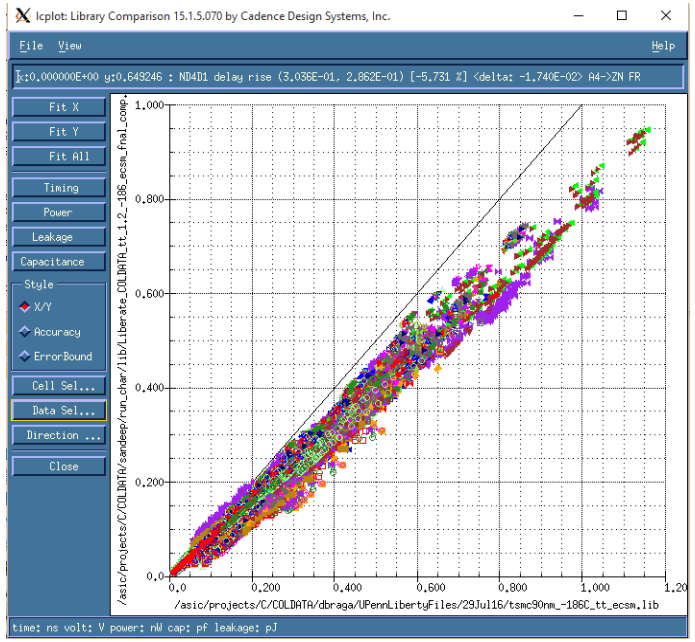
… not too dissimilar to the challenges of scalable quantum computers

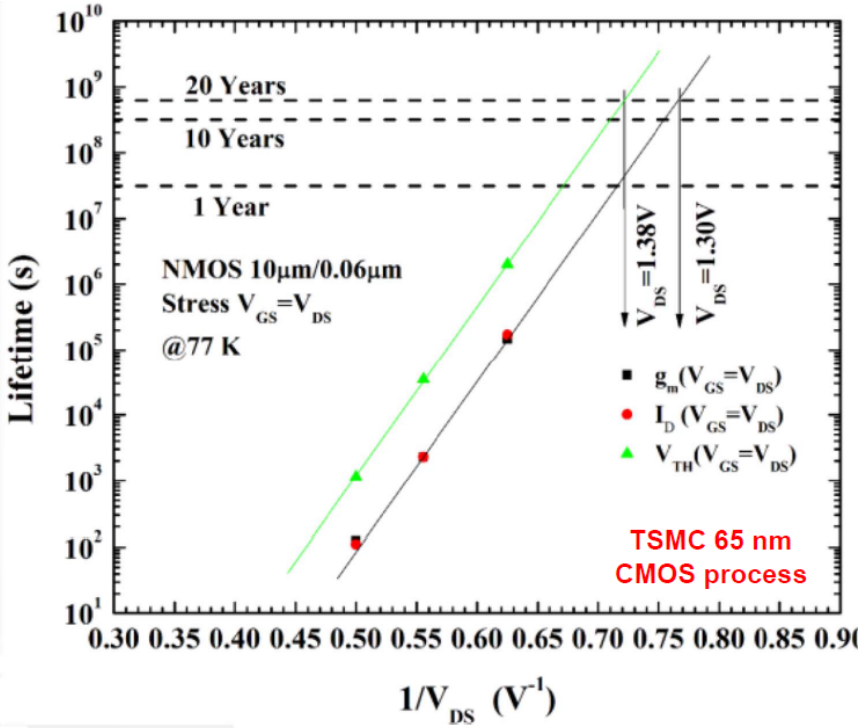
Lifetime studies, modeling, and custom library development

Hot carrier induced lifetime degradation can be avoided by limiting Vds and/or increasing L

→ We derated the nominal supply by 10% and created a custom digital library with increased L (90nm)

The custom library (~230 cells) was characterized for static timing analysis (timing and power across corners) for digital synthesis and place and route.





The predicted lifetime for 130 nm nMOS devices reaches 20 years provided the drain voltages are reduced from the nominal, room temperature value of 1.5 V to a cryogenic temperature value of 1.49 V.

As noteworthy as this prediction is, the 65 nm nMOS device is even more resistant to cryogenic hot carrier degradation. Its nominal, room temperature voltage of 1.2 V is already lower than the maximum allowable cryogenic temperature voltage of 1.3 V.

FERMILAB/SMU: J. R. Hoff, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.59, NO.4, AUGUST 2012

BNL: Shaorui Li, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.60, NO.6, DECEMBER 2013

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Behavior Expectation at Cryogenic Temperatures

Threshold Voltage:

- Increase in Vt as temperature decreases seen in 28nm FDSOI [12]
- Our 22nm FDSOI data reflects this trend, with an average 250 mV difference in Vt across all lengths/widths:

Velocity Saturation:

Higher field needed to reach velocity saturation seen in 28nm FDSOI [7][8]

Source/Drain Resistance:

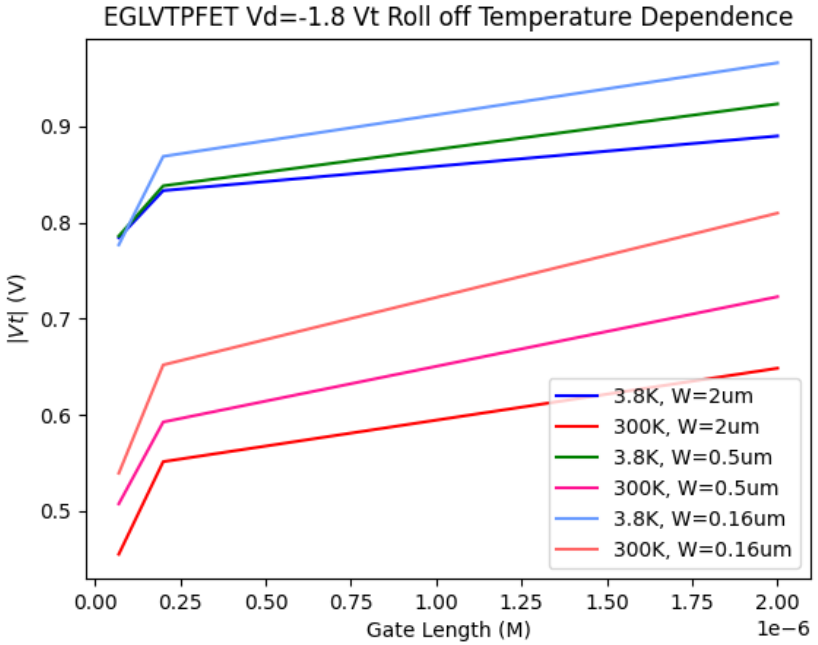
- In 22nm FDSOI a 11-15% decrease seen in S/D resistance [13]
- Prwg models gate dependence of S/D resistance in BSIM 102.9.6, and as it increases, overall resistance should decrease (Our models reflect this)

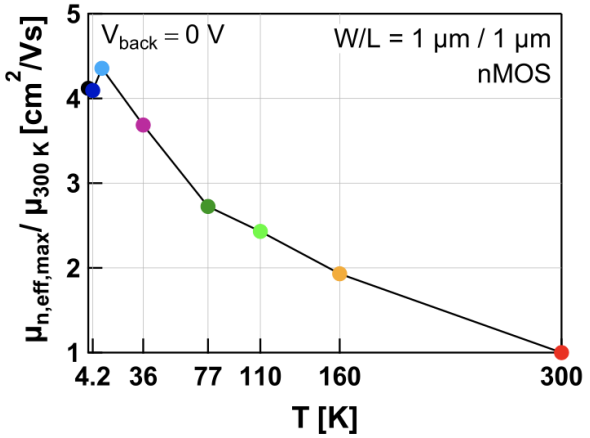
Carrier Mobility:

Effective mobility is made of three main components:

- Lattice vibration-induced scattering
- Scattering on impurities (Coulomb and phonon scattering)
- Surface Roughness Scattering

At cryogenic temperatures Coulomb Scattering becomes more dominant increasing mobility [2]



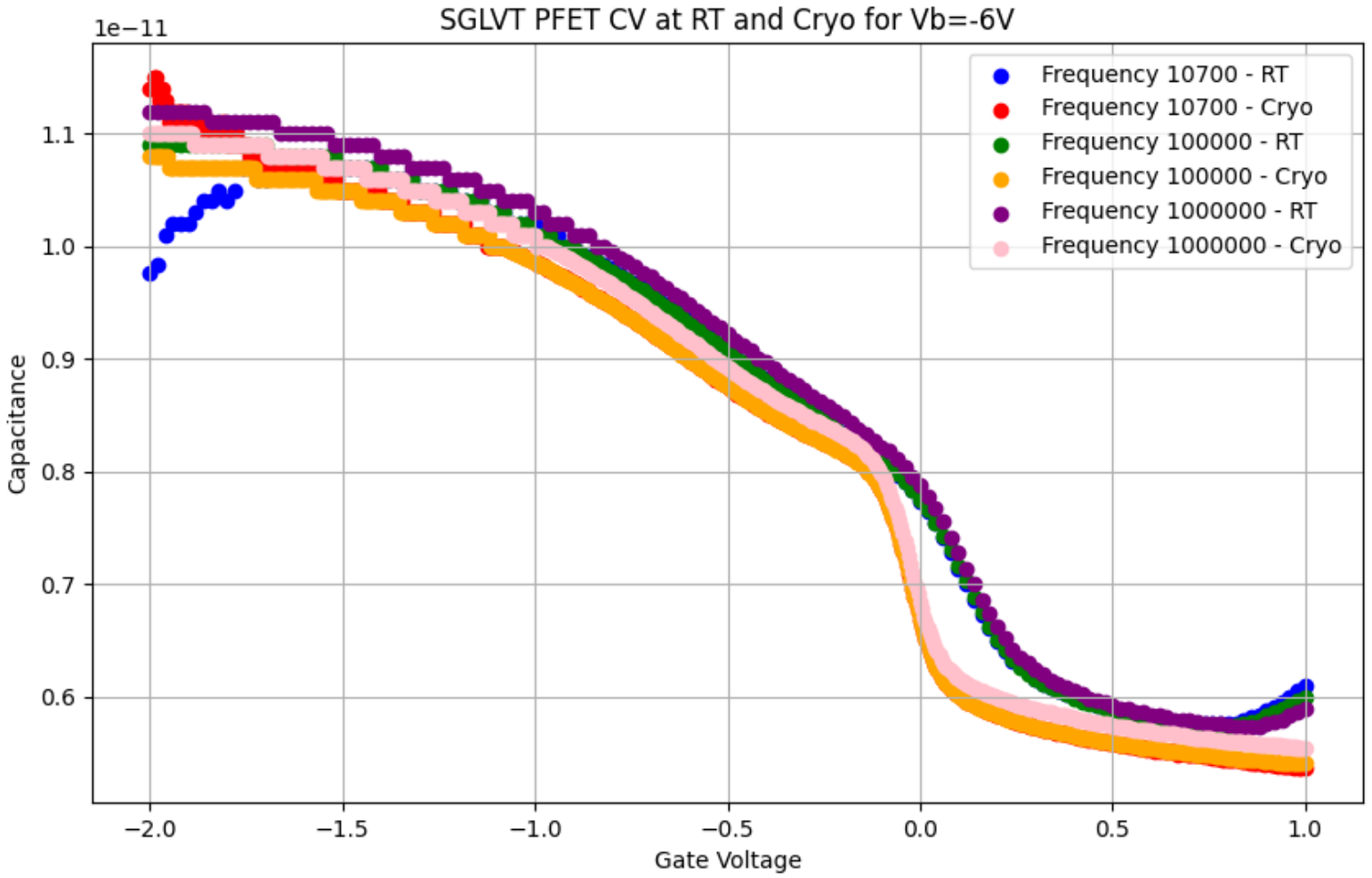


Effective Mobility Temperature dependence in 28nm FDSOI [3]

Fermilab

CV Temperature Dependence

Not a significant change with temperature, so we are not modeling this for now



Fermilab

Conventional Ring Oscillator Delay

Approach 1:

We model $t_{pLH} = \frac{C_L V_{DD}}{2I_p}$ and $t_{pHL} = \frac{C_L V_{DD}}{2I_n}$

For the Long Channel Model, $I_n = \frac{1}{2}\beta_n (V_{dd} - V_{thn})^2$ (derived by assuming that the input switches instantaneously from low to high, and so Vov remains at Vdd – Vthn for the whole transition).

Approach 2:

We model $t_{pLH} = \ln(2)\, R_{eqp} C_L$ and $t_{pHL} = \ln(2)\, R_{eqn} C_L$

And we can derive the resistances as approximately $\approx \frac{3V_{dd}}{I_{DSATn}} \left(1 - \frac{7}{9}\lambda V_{dd}\right)$

Source: Improved_Accuracy_tprop_of_SE_ring_oscillator.pdf

Using EKV Parameters in this Conventional Model

The goal is to measure the drain current of a MOSFET (and thus get a 1st-order estimate of ring oscillator speed) with the particular parameters for low-temp versus high-temp.

I installed SEKV-E using pip3 install sekve.

SEKV-E Documentation: https://moscm.gitlab.io/sekv-e/modules.html

With a little help from Hung-Chi, I was able to reproduce the 28nm FDSOI characterization I found in their earlier paper:

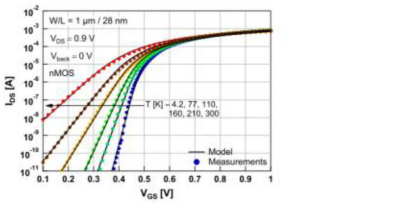
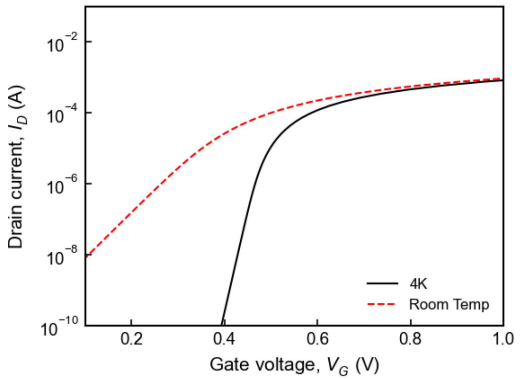


Figure 9: Modeling short 28-nm FDSOI nMOS down to 4.2 K. Model parameters are given in Table 3.

Temperature [K]	n	V_{T0} [V]	$I_{spec\square}$ [nA]	L_{sat} [nm]
4.2	22	0.47	75	5
77	1.7	0.46	175	8
110	1.47	0.45	195	8.5
160	1.38	0.43	335	9
210	1.34	0.41	505	10
300	1.3	0.37	835	11

Table 3: Model parameters for nMOS $W/L = 1\,\mu m/28\,nm$ at $V_{back} = 0$ V and increasing temperatures, corresponding to Fig. 9.



Through some experimentation, I found the values of Id @ Vg = 0.8V for this NFET.

For comparison, I created a similar NFET in our PDK: 1um/28nm length, with VDS=0.9V, whose DC transfer characteristic I simulated at 0 and at -240 C.