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Grid Forming Inverter With Increased Short-Circuit Contribution to Address Inverter-Based Microgrid Protection Challenges

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ABSTRACT Substantial differences in fault levels between grid-tied and islanded modes is one of the primary challenges of microgrid protection. During grid-tied mode, the bulk grid provides significant short-circuit, while during islanded operation the short-circuit magnitude is small due to inverter-based resources limiting their current output close to nominal ratings. Consequently, conventional distribution protection strategies based on overcurrent cannot reliably protect microgrids when operating in islanded mode. Fuses and circuit breakers are particularly affected because of their inverse characteristics. Presently, the absence of affordable solutions for protecting microgrids in islanded mode leads to microgrids shutting down during electrical faults. The contribution of this article is two-fold. The first innovation proposes specific hardware modifications to grid-forming inverters to increase their short-circuit current during electrical faults. The second innovation introduces a novel control strategy designed to preserve control stability margins even when the grid-filter saturates, ensuring sinusoidal output currents under normal and fault conditions. Through experimental results, the inverter with the proposed modifications can provide more than three-times its nominal current during electrical faults. For the prototype testbed, this was sufficient to enable the use of traditional legacy overcurrent protection, achieving the fuse-to-relay and relay-to-relay minimum coordination time for the line-to-ground, line-to-line to ground, and three-phase electrical faults.

INDEX TERMS Microgrid protection, grid-forming inverters (GFMI), distribution protection, saturable inductors, adaptive protection, overcurrent protection.

I. INTRODUCTION

Microgrids have been identified as a critical component of the energy grid of the future. Recently, microgrid deployments have increased significantly both in the U.S. and worldwide [1]. A microgrid is defined as a coordinated group of distributed energy resources (DER) units that supply power to user-end loads via a distribution system with the capability to operate grid-connected or islanded modes of operation. Microgrids allows the use of locally available renewable energy sources such as solar and wind power, and provide advantages of such as continuous power, improved power quality, and increased reliability. A distribution system that adopts microgrids brings generation closer to the load, allowing customers to maintain the power supply in the event of grid electrical faults. However, microgrid resilience can be compromised if they are not properly protected in the event of faults within their own electrical boundaries [2], [3].

To achieve reliable operation, a protection scheme should meet the protection requirements of reliability, selectivity, and speed of operation and sensitivity [4]: Reliability in this context is defined by the accuracy with which the protection system trips during faults, and not trip when no faults are present. Selectivity, also known as coordination, refers to the protection system's capacity to isolate an electrical fault while

minimizing disconnection of system components. Speed of operation denotes the protection system's ability to quickly operate after a fault, and sensitivity capacity of the protection system to detect the electrical faults within its designated protection zone. New protection schemes should consider both cost and the technological maturity of the proposed solution. The cost evaluation should include workforce training requirements. Additionally, technological reediness must be considered to ensure the feasibility of integrating functions that are available in commercial products or that could be quickly developed.

Meeting protection requirements in a cost-effective manner within inverter-based microgrids is particularly challenging due to the significant variance in short-circuit current between grid-tied and islanded modes of operation. For grid-tied microgrids, fuses and overcurrent circuit breakers are deployed within the feeder's laterals as initial protective measures, and these are coordinated with upstream reclosers and backup protection systems to establish a reliable protection scheme. This protection is effective due to substantial short-circuit fault current of the bulk grid. However, for islanded operation, the reduced level of short-circuit is insufficient, which causes delays in the operation of fuses and breakers, thereby compromising the integrity of lateral and feeder protection systems.

Although microgrid protection issues and solutions are known in academia, many real microgrids are using traditional overcurrent protection, inclusive for protecting microgrids in island mode. In real microgrids operating in island, inadequate protection often results in the tripping of the grid-forming inverter during electrical faults, which trips after a few seconds upon the initiation of the fault. Tripping of the grid-forming inverter serves as a protective response from equipment damage as well as safety measure. However, tripping leads to the shutdown of the entire microgrid. Second, fault localization is also a challenge, with the existing protection scheme failing to identify the fault's location. In many real microgrids that cannot afford more sophisticated communication-based protection, this issue makes meeting the protection requirements of reliability, sensitivity, selectivity, speed of operation, unattainable.

The complexity of addressing islanded electrical fault conditions in microgrid development often results in the treatment of electrical faults in islanded mode as secondary contingencies. A practical example of this challenge can be observed in certain real-world microgrid implementations, such as CERTS, Santa Rita Jail, and EPB Control Center Microgrid, and community microgrid in Adjuntas, Puerto Rico, where electrical faults occurring during islanded operation are treated as secondary contingencies, ultimately resulting in the complete shutdown of the entire microgrid [5]. Postfault inception, black starting the microgrid may pose a significant challenge for large microgrids, as it requires identifying and clearing the fault before the microgrid can be re-energized.

Fig. 1 illustrates a protection scheme for a community microgrid in Puerto Rico. The energy storage system (ESS) ac combiner is protected using 400 A overcurrent breaker and a SEL-751 digital relay. This digital relay typically provides voltage, frequency, and current protections for seamless unintentional islanding as well as re-synchronization to the grid. The main distribution panel (MDP) and lateral connections utilize overcurrent breakers and 200 A fuses, positioned before the step-down transformer. Business-level transfer switches and electrical panels are protected with fuses and breakers. Although small breakers at businesses [see Fig. 1(d)] may trip during faults in island mode, large breakers, and fuses in the laterals, the MDP and the ESS ac combiner will not clear faults due to the limited current from the grid-forming inverter. For electrical faults at the feeder or laterals, the ESS would trip to protect itself after few seconds since fault inception, leading to the shutdown of the microgrid. Other microgrids reported in [5], [6], [7] highlight similar challenges within a larger scale, medium voltage microgrid environment.

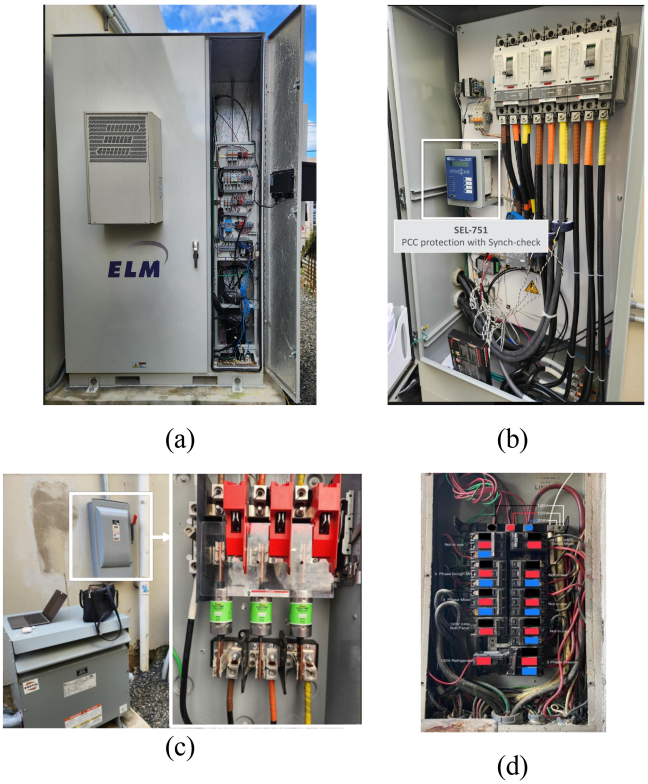

FIGURE 1. Real-world microgrids often use overcurrent protection; faults in island mode can lead to shutdowns. (a) Lithium-ion energy storage with 2, 125 kW inverters. (b) AC combiner with 400 A breakers in series with energy storage inverter and SEL 751 used as protection of point of common coupling. (c) Lateral transformers protected with 200 A fuses. (d) Breakers at end-user electrical panel. Photo credit: Maximiliano Ferrari, Oak Ridge National Laboratory.

While numerous academic publications explore solutions to the challenge of microgrid protection, a seminal paper in the area [7] highlights an ongoing gap. It identifies that despite decades of research, the published work had not led to the development of an economically viable, commercially available relay that effectively addresses the challenges of microgrid protection. Although microgrids are commissioned

at the distribution level, the best microgrid protection solution comes from transmission level protection for microgrid applications. For example, the Illinois institute of Technology campus microgrid uses differential protection [6]. Although these methods are effective, they are very expensive compared to distribution protection. The elevated cost associated with this approach renders it financially impractical for numerous microgrids [7]. For example, achieving coordination for islanded microgrids would require installing communication assisted digital protective relays at every protection node. However, the need for numerous relays, sensor, breakers, communications, and installation can render these commercial solutions economically unfeasible for many microgrid projects. In contrast, grid-tied operations utilize the substantial short-circuit current from the grid to coordinate lateral and feeder level protections through traditional overcurrent distribution methods.

Because of these limitations, only a few real-world microgrids use communication-assisted protection schemes. Line differential protection is present in only 6% and distance protection in 2% of the surveyed microgrids in [6]. This contrasts with overcurrent protection, which is utilized in 49% of the surveyed microgrid sites, primarily for grid-tied protection. In islanded mode, overcurrent protection would only reliably protect microgrids if sufficient electrical fault current magnitudes are available, e.g., synchronous machines are installed. Voltage-based and frequency-based protection is also widely used; however, this protection has important limitations when it comes to coordination as islanded microgrids typically lack inertia.

To address the identified challenges, this study investigates the hardware and control requirements necessary to viably increase the short-circuit capability of grid-forming inverters (GFMI). The goal is to utilize distribution-grade overcurrent protective devices to reliably coordinate protecting in islanded microgrids.

Increasing the short-circuit current GFMI can offer multiple benefits, including the ability to utilize existing distribution protection devices like fuses and inverse-time elements found in relays and reclosers that facilitate the coordination of fuse-protective relays and ensures compatibility between primary and backup protective relays. The proposed method is also cost-effective as it involves overrating only specific components, while most inverter components can maintain their standard power ratings. Additionally, no extra units are required since the energy storage inverter can be engineered to supply the increased fault current. Other benefits include provision of additional ancillary services, enabling greater current injection during grid anomalies to bolster frequency-watt and voltage-var support, as discussed in [8].

This work identified that minimal hardware modifications are needed to significantly increase short-circuit capacity of GFMI. These include overrating semiconductor current rating for electrical fault tolerance and ensuring current transducers (CTs) can accurately measure higher currents for controlling inverter during electrical faults. The proposed modifications enabled the GFMI prototype, originally rated for a 1.0 per unit (p.u.) capacity, to generate more than 3.0 p.u. of short-circuit current for an extended duration, thus facilitating compatibility with existing distribution overcurrent protection by achieving fuse-relay and relay-to-relay coordination. The specific short-circuit current requirements are based on the time-current curves (TCC) of fuses and protective relays. Through experimental analysis, this article advances current knowledge by identifying inverter components that, when overrated, substantially boosts the GFMI's capacity to handle high short-circuit currents.

To minimize costs, this study also demonstrates that it is not required to oversize the inductive grid filter for overloading conditions, given the relatively short duration of electrical faults unlikely to cause permanent damage. However, when currents exceed the filter rated capacity, deep saturation of the magnetic core occurs, introducing nonlinearities that vector control systems must accommodate to ensure stable inverter operation during high-current fault conditions. To tackle this issue, the study introduces a novel adaptive control strategy within the synchronous reference frame, designed to account for the inductor saturation preserving closed-loop stability under both standard and fault conditions. This control also maintaining sinusoidal current output during fault conditions. Importantly, this proposed approach does not necessitate alterations to the ratings of other inverter components, such as dc-link capacitors, gate drivers, and sensors. The main novelties of this article microgrid are summarized in Table 1.

This article is organized as follows. Section II presents a detailed literature review of microgrid protection. Section III presents the experimental methodology and cost analysis for the proposed inverter modifications. Section IV shows the electrothermal modeling comparing losses of normally rated and overrated semiconductors for the prototype and full-scale inverters. Section V shows the impact of increasing the ac short-circuit current on the dc current of the inverter. Section VI addresses the control challenges of inverters with saturable inductors. Section VII proposes a control method to maintain the closed-loop stability during high short-circuit current operation. Section VIII shows the experimental results. Section IX a discussion on the proposed approach and its limitations and Finally, Section X concludes this article.

II. LITERATURE REVIEW: MICROGRID PROTECTION

A. GFL AND GFMI RESPONSE DURING GRID ELECTRICAL FAULTS

Despite these numerous advantages of microgrids, the resiliency of a microgrid may be lost if it is not properly protected against electrical faults [7], [3], [9]. There is a consensus in the literature that one of the main challenges for protecting microgrids arises from the significant variation in electrical fault current, which drastically changes between operating mode of the microgrid. During the grid-tied operation mode, the short-circuit current is very high due to the high utility grid source's inertia. Conversely, in islanded

TABLE 1. State of the Art and Research Novelty

Criteria	State of the Art	Proposed Inverter Modifications
Overcurrent protection	Low short-circuit current of islanded Microgrid may not trigger protective fuses or allow protection coordination during faults [2], [3], [6], [7].	Increased the short-circuit current levels from GFMI, ensuring fuse operation, better selectivity, discrimination, and speed.
Conventional protection elements	Non-current protection elements (Sequences, Voltage, Frequency, Admittance, etc.) increase sensitivity compared with overcurrent. However, these methods are difficult to coordinate and incur in expensive hardware and installation costs [7], [29], [30].	Increased the short-circuit current levels from GFMI leverage widely available and affordable distribution protection based on overcurrent.
Adaptive Protection	Requires communications and may be limited to available settings groups in relays [9], [25].	Requires local information (current), no communication network not needed.
Communication based protection	Differential protection schemes provide selectivity and coordination but incur high costs and complex communication requirements, needing installation at each node [7].	Increased short-circuit contribution allows for the integration of economical overcurrent protection strategies. Selectivity is maintained when properly coordinated with upstream devices.
Current Sources Solutions	Dedicated short-circuit sources for islanded microgrids developed in [37]. This presents cost challenges due to the need for additional units. Not reliable due to potential unit failure. Oversizing the whole energy storage unit proposed in [28]. Which may not be efficient nor cost-effective approach.	Proposed approach is cost-effective identifies specific components for overrating to allow high short-circuit currents. Only semiconductor and current sensor needs overrating. Grid-filter inductor and other components remains at typically rated power.
Power Electronics Control	Stability concerns associated with inverters using saturable inductors are identified in [49], [50].	This work extends previous work by deriving the dq small-signal circuit for inverters with saturable inductors, providing a transfer function for current behavior. Adaptive control developed to maintain stability during faults.

operation, the short-circuit current is very low because of the constrained capacity of inverter-based resources (IBRs). For instance, during grid-tied operation, the short-circuit current ratio ranges from 10 to 50 p.u. In contrast, during islanded operation, the available short-circuit current may drop to as low as 1.2 p.u. [3], [9]. Such a large difference makes coordination of overcurrent distribution protection often unattainable. In islanded operation, fuses are particularly affected because of their inverse characteristics; in some cases, fuses and breakers protecting the lateral feeders would not operate during electrical faults.

To protect the power electronics, commercial GFMI as well as grid-following (GFIs) limit their short-circuit contribution. Table 2 outlines the short-circuit contribution of GFIs, such as photovoltaic (PV) inverters, as referenced in [12], [13], [14], [15]. GFIs are required to comply with standard like IEEE 1547 [10]. However, the short-circuit current contribution of GFMI is not uniformly standardized across manufacturers. For example, commercial energy storage inverters show variability in their short-circuit current limits; some cap their current at 1.5 p.u., while others allow 2.0 p.u., as shown in Table 3 [16], [17], [18], [19], [20]. Additionally, the duration GFMI can sustain fault conditions varies by manufacturers, from 1.5 to more than 2.0 s. Certain inverters shut down at 50% current imbalances while others can handle 100% imbalance, which is crucial during asymmetrical faults. This lack of uniformity further complicates the design of microgrid protection in islanded mode.

Moreover, while inverter manufacturer datasheets typically include the maximum short-circuit contributions and grid-following operation as specified by IEEE standard, they frequently do not provide comprehensive information on the dynamic responses and sequence contributions in grid-forming mode. This omission often leaves a gap in understanding the full capabilities of these systems under various operational conditions. Only few published research fills this gap by offering experimental data on sequence components during faults of different commercial inverter types. These results are compiled in Table 4.

TABLE 2. Short-Circuit Contribution Commercial PV Inverters

Manufacturer	Model [Reference]	Power Rating [kW]	Voltage [V]	Electrical Fault/Nominal Current p.u.
FIMER	PRO-33.0-TL-OUTD [12]	33	480	1.00
ABB	TRIO-27.6-TL-OUTD [13]	28	480	1.02
FIMER	PVS-60-TL [14]	62	480	1.15
SMA	STP 30000TL-US-10 [15]	30	480	1.00
SMA	STP 50-US-40 [15]	50	480	1.06
SMA	STP 12000TL-20 [15]	12	480	1.00

Based on experimental presented in [21], [22], [23], and [24], GFMI inverters can produce negative sequence components, while the presence of zero sequence components depends on the inverter topology or transformer selection. For the zero sequence to be present, a path to ground should be stablished, e.g., delta-wye grounded or 4-wire inverters [21], [22], [23], [24].

TABLE 3. Short-Circuit Contribution Commercial ESS Inverters in Grid-Forming Operation

Manufacturer	Model [Reference]	Power Rating [kW]	Voltage [V]	Current [A] Ratio [p.u.]
OZTEK	OZpcs-RS40 [16]	40	480	Rated: 50 Max: 63 Ratio: 1.3
DYNAPOWER	MPS-125 [17]	125	480	Rated: 150 Max: 213 Ratio: 1.4
SMA	SUNNY BOY STORAGE 2.5 [18]	2.5	208	Rated: 10.5 Max: 19 A Ratio: 1.8
FIMER	REACT2-UNO-5.0-TL [19]	5	208	Rated: 22 Max: 22 Ratio: 1.0
SINEXCEL	PWS1-500K [20]	5	400	Rated: 760 Max: 836 Ratio: 1.1

TABLE 4. Sequence Contribution Energy Storage Inverter and PV Inverter [21], [22], [23], [24]

Inverter Type	Rating kVA	Voltage/ Phases	XFMR	Sequences
ESS	9	208, 3x1ph	No	I_+, I., I_0
ESS	100	480, 3ph	$\triangle Y_{\downarrow}$	I_+, I., I_0
ESS	5.5	208, 1ph	No	I_+, 0, 0
ESS	5	240, 1ph	No	I_+, 0, 0
PV	24	480, 3ph	No	I_+, 0, 0
PV	3.2	208, 1ph	No	I_+, 0, 0

For grid-following inverters, regulatory changes are shaping the requirements for sequence contribution. According to IEEE 1547, 2018 standards [10], during electrical faults, GFI were required to only provide positive sequence. However, more recent regulations, such as IEEE Standard 2800, now require that IBRs generate negative-sequence currents that lead the negative-sequence voltages. This new requirement is designated to mimic the dynamics of synchronous generators and decrease the risk of protection system malfunctions [11].

B. MICROGRID PROTECTION REVIEW

Research highlighted in sources [5], [6], [7] reviews microgrid protection, identifying line differential and adaptive protection as optimal for inverter-based systems. Adaptive protection, while promising for future microgrids, depends on complex programmable logics and necessitates a vast, resilient communication network, which brings the challenge given potential physical and cyber vulnerabilities in communication infrastructure. Moreover, adaptive protection is constrained by the limited number of settings groups available in protective relays, which varies depending on manufacturer and is typically limited between four and seven [26], [27]. Authors concur that line differential protection is the most effective commercially solution for protecting microgrids during islanded operation [7]. Line differential remains effective despite the small electrical fault current from inverter-based resources (IBRs) and changes of fault levels from grid-tied to islanded operation. However, line differential protection costly as it requires a protective relay to be installed at every node within a protection zone, which may not be feasible for many microgrid projects due to the high number of nodes in a microgrid. Additionally, it requires high bandwidth communication and is incompatible with high latency communication technologies [7].

Sequence based protection uses symmetrical components elements of voltage or current to detect and clear asymmetrical electrical faults. However, this approach is challenging in real applications because commercial GFIs are controlled to maximize positive sequence currents and minimize negative sequence currents, and GFMI limit the phase currents during the electrical faults; experimental validation of electrical fault sequence contribution of GFMI and GFI can be found in Table 4. Furthermore, electrical loads and generation are not perfectly balanced in real microgrid applications, therefore, applying this protection method is challenging as the negative sequence varies with the available load and generation. Incremental sequence protection addresses this challenge [29], but coordination is still challenging in low impedance network. An admittance protective relay has been proposed for microgrid protection in grid-tied and islanded modes of operation. However, coordinating these protective relays can be difficult in microgrids with a relatively small distribution line.

Achieving high protection selectivity though these methods require the installation of protective relay, sensors, and breaker at every protection node, which may be prohibitive for most microgrid project. Recently, a wavelet transformation approach was introduced [31], [32]. Nevertheless, these techniques demand a high sampling frequency and may not be suitable for microgrids characterized by short distribution lines.

Other suggested methods are based on advance signal processing and artificial intelligence (AI) [33], [34], [35]. These schemes extract information about the electrical fault signatures to train an AI-based scheme to distinguish and identify the electrical faults. However, these methods have the drawback of requiring large datasets for training purposes which are typically unavailable and may be affected by bias or data errors. AI and Wavelet transformation-based methods are currently in the research stage, characterized by low Technology Readiness Levels (TRL). Additionally, commercial protection relay systems do not incorporate protective elements to support the implementation of this method. Newer approaches propose modifying the control loops of the IBR to inject pre-defined harmonics into the microgrid during the electrical fault condition [36]. These new methods are focused on the detection algorithm and do not address the coordination challenges. Furthermore, they have very low maturity to be applied in real microgrid project. Other authors have proposed installing a dedicated electrical fault current source or by installing larger DER units such as flywheels or synchronous condensers [28], [37]. Although this approach would enable

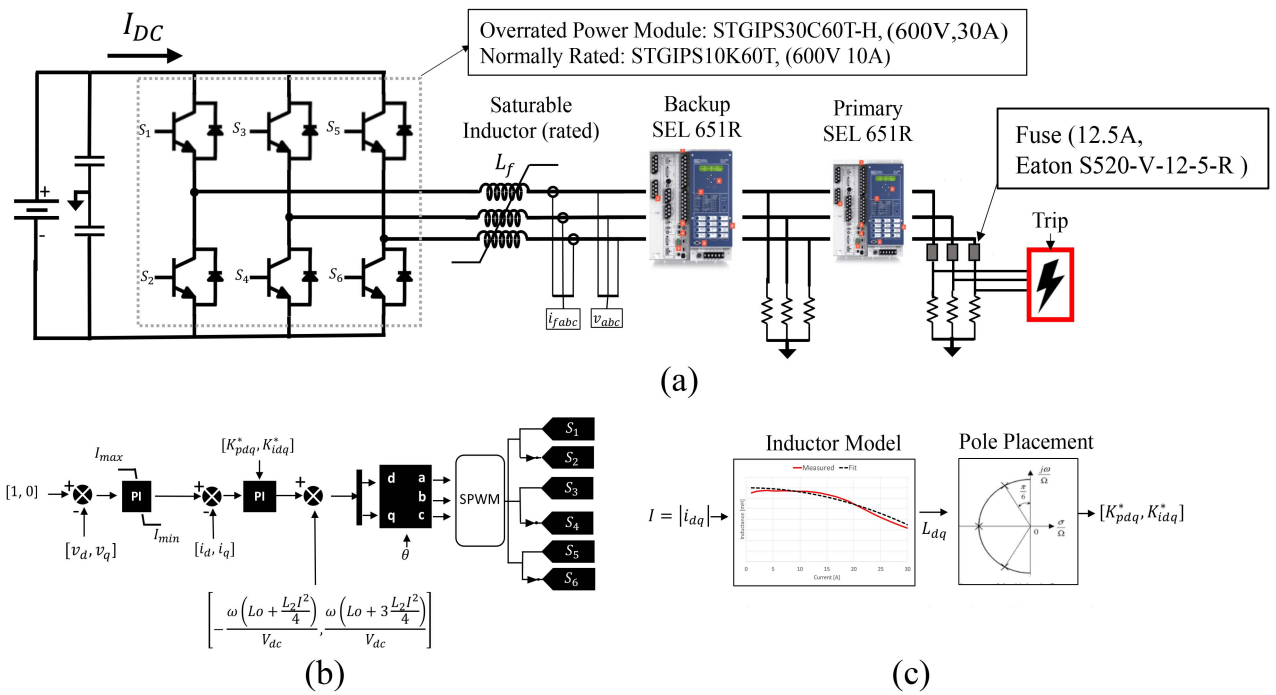

FIGURE 2. **Prototype testbed block and control diagram for evaluating ac faults in three-phase grid-forming. (a) Hardware components including VSI, inductive grid-filter, backup and primary overcurrent digital relays and fuses. (b) Cascaded control with decoupling terms considering saturation of grid-filter inductors. (c) Pole placement based on Butterworth polynomial maintains stability when the grid-filter inductor saturates. In practical application, the neutral is formed through a delta-wye grounded transformer or/and a zigzag grounding transformer.**

the adoption of traditional overcurrent protection, it can be cost prohibitive as an additional or unit must be installed.

III. SYSTEM DESCRIPTION AND METHODOLOGY

Fig. 2 shows the circuit and control block diagram of this study. The prototype inverter design consists of a 4-wire two-level voltage-source inverter (VSI) connected to the grid through an inductive grid filter [38]. In this work, is assumed that a stiff dc-source is established in the dc-side of the inverter, consequently, the dynamics from the dc input are neglected in this paper. The neutral of the system is formed by connecting the mid-point of the dc-link capacitors.

To safely increase the short-circuit current from the inverter, this study proposes to replace the semiconductor, rated at 10 A, 600 V, with a 3X current overrated semiconductor, 30 A, 600 V. The power devices, manufactured by ST semiconductors, are power modules that include the gate-driver in the same package. These devices are easily interchangeable as they come in the same 25-pin SDIP. Although in real application it is good practice to slightly overrate the semiconductor power rating, in this research, the semiconductor current rating is significantly overrated to three-times the nominal rated current to accommodate the overcurrent current condition during electrical faults. The current transducer (CTs) was also overrated to measure higher currents to maintain control during electrical faults. The CT was also overrated from 15 to 50 A during the electrical fault state. The rest of the inverter components remained at the rated power, including the dc-link capacitors, grid filter inductors, voltage sensors and other required circuity.

Fig. 2 also shows the cascaded vector control in the fundamental reference frame applied in this research. The external loop regulates the magnitude of voltage at the point of connection of the inverter v_{abc}, while the internal loop regulates the inverter current i_{abc}. The angle θ is artificially generated integrating the angular speed $\omega = 2\pi f$, where f is the desired frequency, in this article $f = 60$ Hz. The saturation limits $[I_{\max}, I_{\min}]$ determine the maximum allowable current during balanced three-phase electrical faults. For unbalanced electrical faults, the inverter does not regulate the negative sequence, and the phase electrical fault current is determined by the circuit impedance and dc-link voltage. However, in practical applications cycle-by-cycle current limiters, or virtual impedance, are applied to limit the maximum current during the electrical faults and inrush events, e.g., motor start, transformer magnetization, faults etc. [39], [40].

This diagram also shows the proposed adaptive control that considers the grid-filter saturation to maintain stability during short-circuit electrical faults. This adaptive control calculates in real-time the controller gains $[K^*_{pdq}, K^*_{idq}]$ based on the remaining inductance of the grid-filter inductor. Adaptive control becomes necessary to maintain stability during the electrical faults, when the core of the grid-filter inductor deeply saturates due to the high short-circuit current. The proposed controller calculates the remaining inductance using the phase current flowing through the inductors and a second

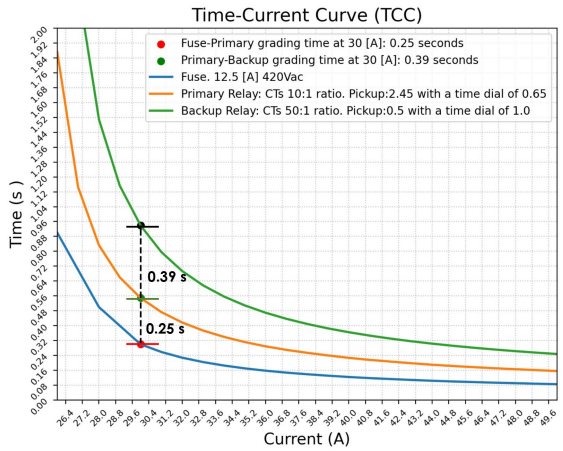

FIGURE 3. TCC curves for the 12.5A fuse. SEL 651R protective relay used as inverse time overcurrent primary and backup protection. Primary relay: CTs: 10:1 ratio. Pickup 2.45, time dial 0.65. Backup relay: CTs: 50:1 ratio. Pickup 0.5, time dial 1.00. Fuse, S520-V-12-5-R rated at 12.5 A, 600 V.

order polynomial fit equation of the saturable inductor. This approach utilizes a fit function to estimate the remaining inductance based on the operating current, and the Butterworth polynomial to optimize the closed-loop eigenvalue locations. The proposed adaptive control calculates in real-time controller gains [K^*_{pdq}, K^*_{idq}], and there is no need to switch controllers during normal operation or during the electrical fault events.

The protection devices in the hardware testbed include two Advanced Recloser Control SEL 651R and a fuse is an Eaton S520-V-12-5-R rated at 12.5 A, 600 V. The SEL 651R was used as a protective relay as inverse time current only and the recloser control capability was not enabled. The fuse protects the resistive three-phase loads at the end of the line. Fuse-protective relay and protective relay-relay coordination are evaluated to determine if full protection coordination is achievable in an islanded system. To maintain coordination, the fuse-protective relay grading margin was set to 0.25 s, and the protective relay-to-relay margin was set to be greater than 0.3 s, see Fig. 3.

Although there are no specific reports addressing the cost breakdown of silicon based GFMI inverters according to the authors' best knowledge, we can refer to the breakdown presented in [41] for an approximate cost of the cost implications of overrating the inverter components. Fig. 4 shows the inverter breakdown cost for an outdoor rated inverter. The breakdown reveals that the cost of passive components (29.6%) and mechanical components (33.1%) significantly outweighs the cost of the power module (5.9%) and integrated circuits (5.7%). Consequently, overrating the silicon power module is unlikely to have a significant impact on the overall cost of the inverter.

For reference, according to Infineon, doubling the cost of the silicon IGBT module results in a nominal current that triples [42], the same relationship stands for the ST modules

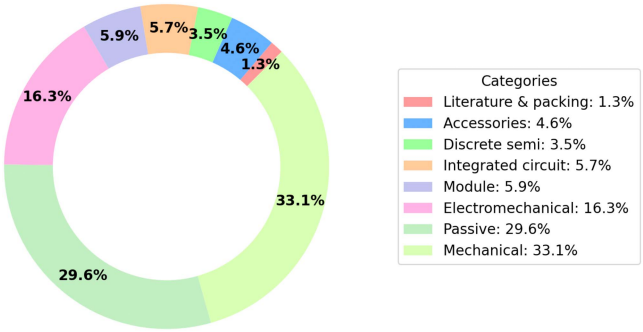

FIGURE 4. Cost breakdown for inverter [41].

TABLE 5. Switching and Conduction Power Losses [45]

	SWITCHING	CONDUCTION
IGBT	$\frac{1}{T_o}\sum(E_{on}+E_{off})\frac{i}{I_{nom}}\frac{V_{dc}}{V_{nom}}$	$V_{CE}(T_{IGBT},i)\,i\tau(t)$
DIODE	$\frac{1}{T_o}\sum(E_{rec})\frac{i}{I_{nom}}\frac{V_{dc}}{V_{nom}}$	$(V_{To}(T_{diode})+r_T(T_{diode})i)i\tau'(t)$
$\tau(t)$	$\frac{1}{2}(1+m\sin(\omega t+\emptyset))$	$\frac{1}{2}(1-m\sin(\omega t+\emptyset))$

used in this study. For wide bandgap semiconductors, these relationships do not hold true, and an estimation using silicon carbide semiconductors is conducted in [43]. The cost associated with oversizing hardware components is minimal when compared with the cost required for the integration of line differential or other protection methods at each protection node, which can amount to tens of thousands of dollars per node. Detailed financial analysis pertaining to line differential protection implementation costs is shown in [44].

IV. ELECTROTHERMAL MODELING

In this section, we will develop an electro-thermal model to estimate the IGBT and diode junction temperature [46]. This model will be used in subsequent sections to analyze the dynamic behavior of the semiconductor's junction temperature during the normal operation as well as during electrical faults. Table 5 summarizes the equations to calculate losses of the IGBTs and their anti-parallel diodes. Switching losses happen during the turn ON and turn OFF transients and are proportional to the switching frequency $1/T_o$, the collector current i, and blocking voltage $V_{\rm dc}$. The conduction loss can be calculated with the saturation voltage drop V_{CE} and the collector current i, multiplied by the instantaneous duty ratio τ. For this study, τ corresponds to sinusoidal pulsewidth modulation.

Fig. 5 shows the Foster thermal network used to model the thermal circuit for the IGBT and diode. A four-layer model was chosen because it provides a better dynamic response compared to a single layer network [45]. Fig. 6 presents the information for both the normally rated and the semiconductor with overrated current rating used in this study. Because not all values were disclosed in the semiconductor

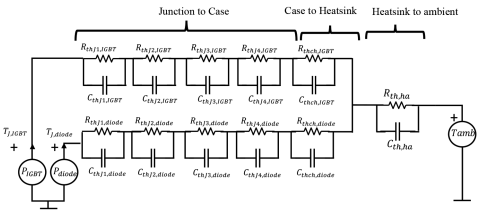

FIGURE 5. Foster thermal network of IGBT and diode.

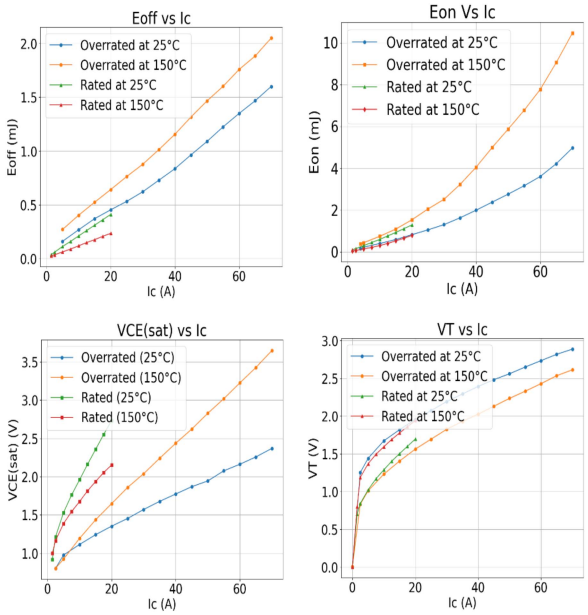

FIGURE 6. Electrothermal data of power used in this study [46].

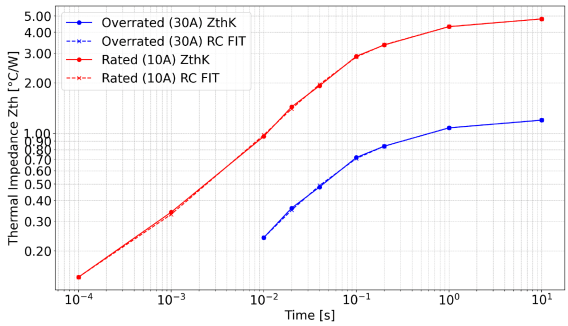

FIGURE 7. Estimated thermal impedance and fit using foster RC network for the prototype 10 A / 600 V module and 30 A / 600 V module.

datasheet, some electrothermal values were estimated and validated using similar devices and then validated using the manufacturer's simulator, ST PowerStudio, for accuracy [47].

As shown, the following parameters are sensitive to the collector current: V_{CE}, V_T , E_{on}, E_{off}. During high current operation, the increased collector current influences these parameters rapidly increasing the conduction and the switching losses, which further increases the junction temperature. The overrated module has lower V_{CE} compared to the normally rated device, which would translate to lower conduction losses which are dominant at high currents. The thermal impedance of the rated and overrated device is shown in Fig. 7. The curve fitting was done by minimizing the root mean square error. The accumulative percentage error is 2.2% for the 30 A device and 1.1% for the 10 A device.

Fig. 8 presents the estimated power losses using the developed electrothermal model. Fig. 8(a)–(d) shows the results for both the normally rated and overrated module during normal operation (currents lower than 10 A), and Fig. 8(e)–(h) for currents higher than 10 A. Fig. 8(a) shows that the overrated power module has significantly lower conduction losses for the IGBT. Fig. 8(a) and (d) show that the switching losses and conduction losses are similar for the rated and overrated semiconductor. Fig. 8(d) shows that the junction temperature for the overrated device is significantly lower because of the lower losses and lower thermal impedance, which is shown in Fig. 6. Thus, replacing the normally rated semiconductor with an overrated semiconductor improves the efficiency of the inverter and may reduce cooling requirements.

Fig. 8(b) shows the results for high-current operation during electrical faults (>10 A). The projections for the normally rated device simulation show an exponential increase in the conduction losses as well in the IGBT junction temperature. As shown in Fig. 8(h), at high currents the normally rated device quickly overheats while the overrated device remains at lower temperature for high current operation, as expected.

Fig. 9 illustrates the scalability of our proposed method. This figure provides a comparison involving devices used in a full-scale inverter. The comparison is made between a normally rated device at 50 A, 1200 V and an overrated device rated at 150 A, 1200 V. Both devices employ the same Econo3 package. The results show that overrating the current rating allow high current operation as devices with a higher current rating exhibit reduced total losses, as it is expected. These lower losses, coupled with better thermal impedance, leads to lower junction temperatures. Similarly to the devices used in the inverter prototype, during normal operations, the overrated device has lower power losses and junction temperatures, improving the inverter's efficiency and reducing its cooling needs.

V. DC-LINK CURRENT DURING FAULTS

An important consideration when designing inverters with increased short-circuit current capabilities is understanding the implications in the dc current during faults. To address this question, Fig. 10(a)–(c) shows simulation results for line to ground (LG), line-to-line to ground (LLG), and 3-phase faults (3-ph) considering typical configurations for microgrids: 3-wire with delta-wye transformer and the 4-wire inverter systems with and without grounding transformer. As shown in Fig. 10(a) and (b), the use of delta-wye grounded, or grounding transformers significantly mitigates the dc current magnitude and fluctuations for faults to ground (LLG and LG). With these transformer configurations, I_{dc} remains relatively low

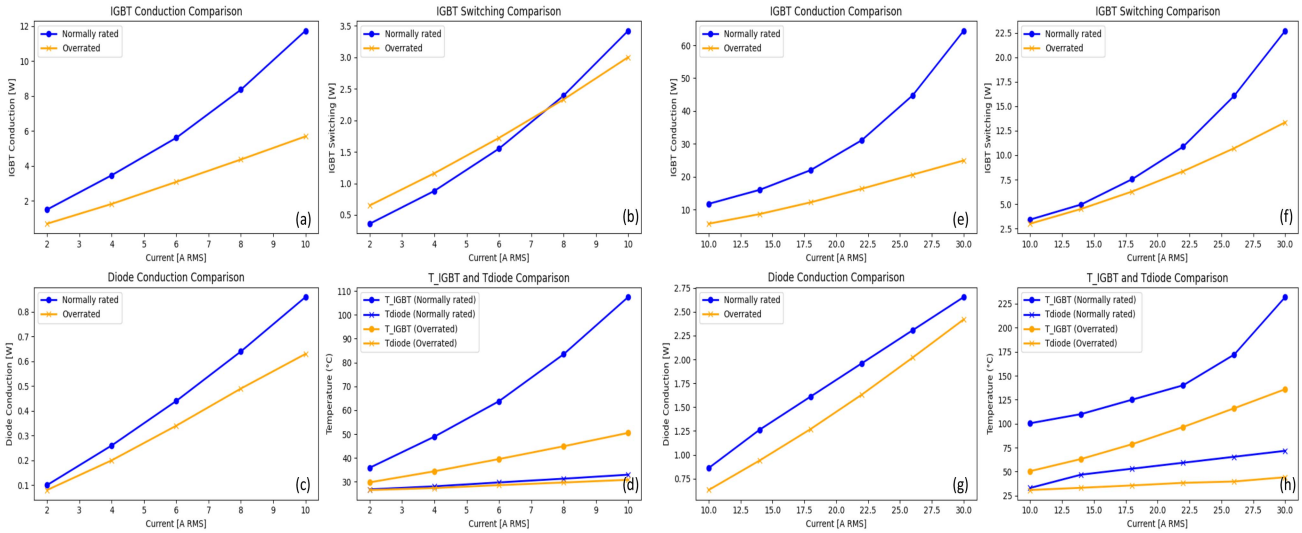

FIGURE 8. Simulated loss comparison between normally rated and overrated semiconductor. (a)–(d) For normal operation; currents lower than 10 A. (e)–(f) Fault operation, currents higher than 10 A. $V_{DC} = 400$ V, $PF = 1$, $M = 1$, $F_{sw} = 10$ kHz.

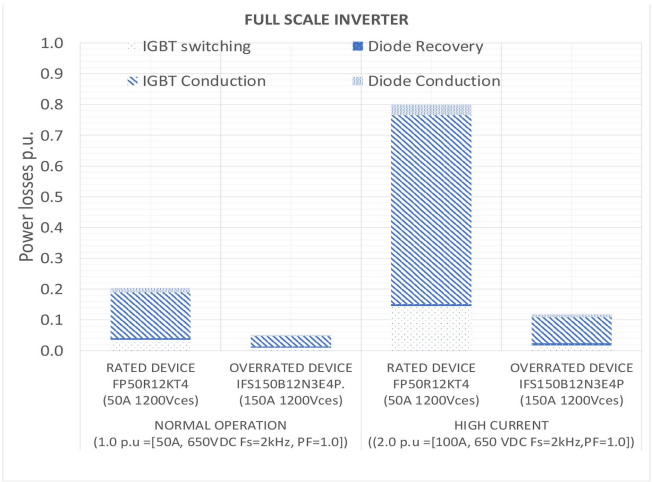

FIGURE 9. Conduction and switching losses for semiconductor for full-scale inverters.

compared to the ac current and has a single polarity. Grounding transformers or/and delta-wye grounded transformers are typically found in microgrids to stablish the ground and they provide a path for the zero sequence, present during ground faults. In 4-wire inverter configurations, dual polarity oscillations in the dc current I_{dc} occur due to the flow of neutral current through the mid-point of the dc-link capacitor present during phase imbalances caused by LG and LLG faults. For 3-ph fault the dc current is almost zero, see Fig. 10(c). This occurs because during a low-impedance 3-phase fault the ac voltage is very small, then, a small amount of power needs to be transferred from the dc side to de ac side to produce a large short-circuit current. This result is independent of the transformer type. These simulations result indicates that substantial ac currents do not necessarily translate to large dc currents, primarily because the zero-sequence current is effectively managed within the wye-grounded or grounding circuit configurations, which are common practice in microgrids.

Although additional dc current is required to have increased the short-circuit current, lithium-ion batteries have low internal resistance and high energy density, which enables them to deliver substantial bursts of current when required [48]. However, the current burst from the battery is brief as fault must be cleared as quickly as possible and the inverter should inject current for only few seconds.

VI. VECTOR CONTROL WITH SATURABLE INDUCTORS

This section presents the operation of a GFMI considering saturable inductors. Experimental results showed that overrating the grid filter to accommodate the overloading condition is not required because the electrical fault current magnitude is relatively short would not produce permanent damage if interrupted quickly. However, at currents that exceed the rated current, the core of the inductive grid filter saturates. This saturation introduces nonlinearities that must be accounted for in the vector control to maintain stable operation. To address this challenge, this work also proposes a novel control method in the *dq* synchronous reference frame considering saturable inductors to maintain closed-loop stability during normal operation as well as the electrical fault conditions.

The employment of conventional vector control in saturable inductors brings considerable issues regarding the current control performance. This is because traditional vector controllers are developed considering linear and constant inductance. However, systems with saturable inductors result in inductances that are unsymmetrical and nonlinear [48], [49], [50]. Neglecting the inductor saturation at high-current operation can make the closed-loop unstable. The following sections present the control challenges introduced by

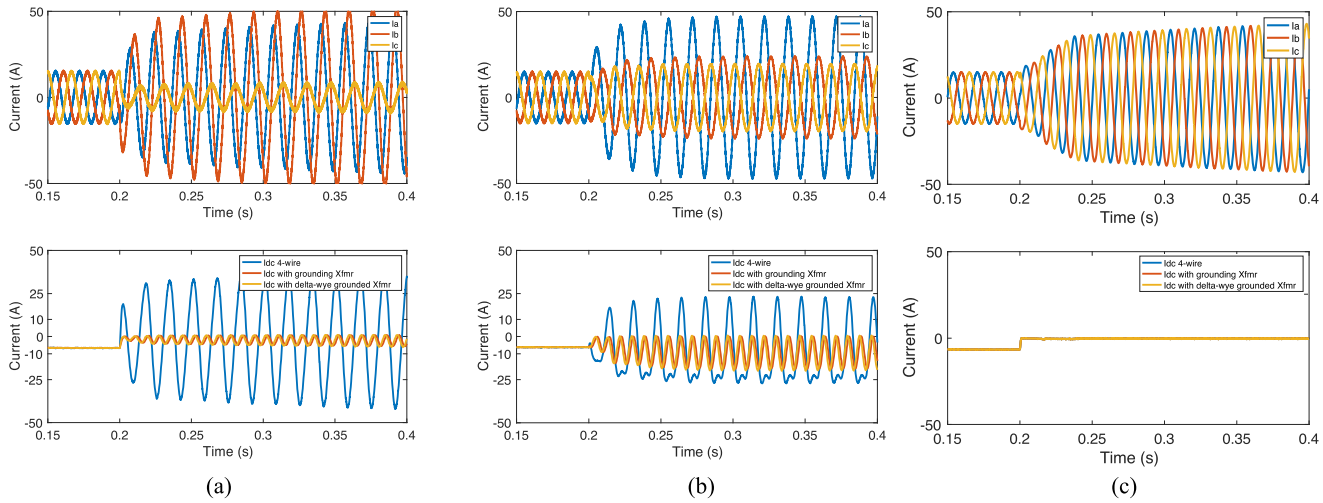

FIGURE 10. **DC current magnitudes during a LLG (a), LG (b), and 3-phase (c) fault with a 3X short-circuit current. When using delta-wye grounded, or grounding transformers (zigzag transformers), achieving large AC currents does not necessarily result in a correspondingly large I_{dc}current.**

saturable inductors, derives the small-signal model and decoupling terms for the vector control, and presents a control method to tune the current controllers to maintain stability during the normal and electrical fault conditions.

A. MODELING SATURABLE INDUCTORS

In saturable inductors, as the operating current increases, the rate at which flux increases with each increment of current significantly decreases [49], [50]. This physical phenomenon is called saturation of the magnetic core. In Fig. 9 the measured inductance-current characteristics of the ferrite inductors used in this paper's experimental setup is shown. The inductor cores were characterized using a DPG10 Power Choke Tester. As shown in Fig. 9, due to the core saturation, the available inductance decreases as the magnitude of the current increases. The inductance of the ferrite core drops until it reaches 0.6 mH at 35 A, which is a reduction of about 45% the initial inductance 1.1 mH.

Equation (1) is used in the literature to describe the nonlinear inductor in a polynomial form [50], where i is the instantaneous current flowing through the inductor ($i = I \sin \omega t + \delta$), and L_o is the inductance at zero current, and L_n a constant term that can be adjusted to fit the saturation characteristics of the inductor. This fit equation will be used later in this paper to derive the vector control considering saturable inductors

$$L_s = L_o + L_2 i^2 + L_4 i^4. \tag{1}$$

For validating the fit equation, the even, second-order polynomial is used for the ferrite core. The parameters of the even order polynomial L_o, L_2 are needed to be specified to fit the measurements presented in Fig. 11. The fit method minimizes the root mean square error (RMSE) using the reduced gradient nonlinear engine in Excel. For the ferrite core, the estimated value of L_o, L_2 are 1.1 and –0.4 mH. With these values, a good

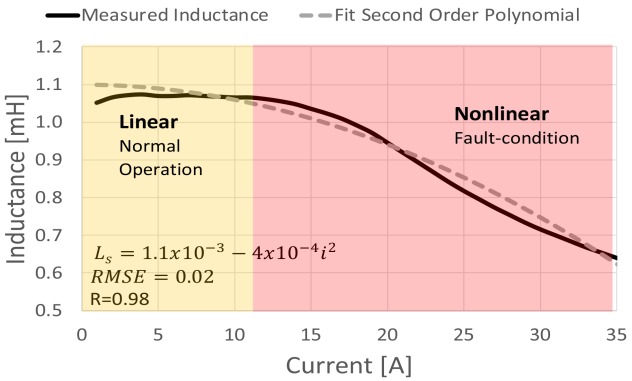

FIGURE 11. **Experimental characteristic of the nonlinear inductor used in this work. Inductor characterized at room temperature using DPG10 power choke tester.**

fit is obtained considering a second-order polynomial with a RMSE of 0.02 and the correlation R is 0.98 ohms.

B. CURRENT WAVEFORMS QUALITY

Fig. 12 presents the open-loop response of a three-phase inverter employing saturable inductors during normal conditions and high-current operation. At the nominal current, the three-phase currents are sinusoidal with a fundamental at 60 Hz. However, during high-current operation (>10 A), the inductance of each phase varies with the associated phase current, leading to introduction of a fifth and seventh harmonics. In the dq reference frame, these harmonics are present as a sixth harmonic, see Fig. 13.

From a control perspective, the inductance value is critical as it determines the poles of the system which are required to effectively tune the integral and proportional gains. Because this work operates in closed-loop for normal and electrical fault conditions, it is important to account for nonlinearities

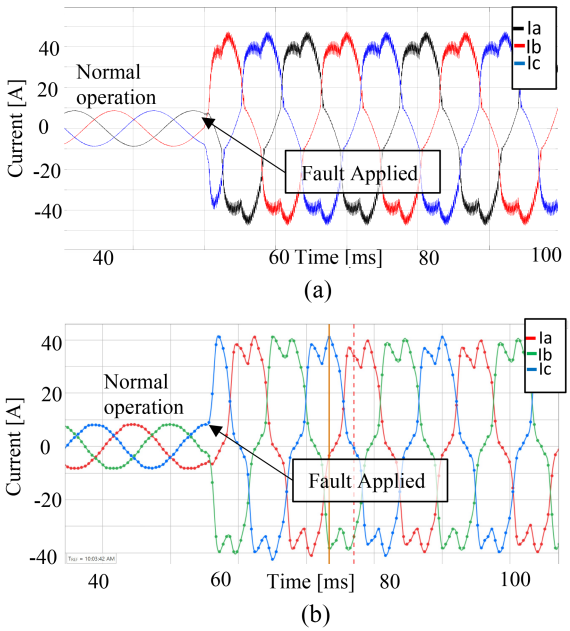

FIGURE 12. Open-loop response of inverter using saturable inductors. (a) Simulated waveforms. (b) Experimental waveforms captured from SEL 651R.

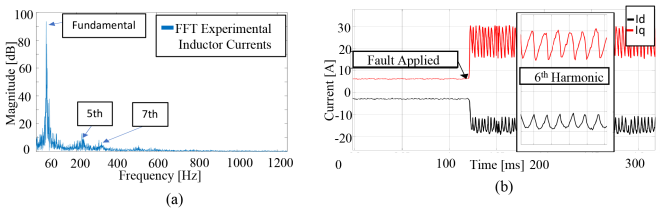

FIGURE 13. Open-loop response of inverter using saturable inductors. (a) Fast-Fourier transform of experimental currents. (b) Control signals in synchronous reference frame.

of the inductance to guarantee the closed-loop stability during normal and electrical fault conditions. As will be shown in following sections, the proposed control reduces the harmonics and makes the current sinusoidal during fault conditions.

C. CONTROL STABILITY

Fig. 14 shows the effects of not retuning the controller gains when the inductors are deeply saturated. The gains of the proportional integral (PI) controller remained constant and the time delay was captured by a first-order Padé approximation and set as 200 us to account for the delays of the analog to digital converter input, the digital output card, and the field programmable gate array (FPGA) processing time. Notice that for the nominal inductance, the open-loop transfer function meets the stability criteria of phase margin greater than 40° and a gain margin of 8 dB.

Fig. 14 shows that in a conventional vector controller with fixed controller gains, the inductor saturation reduces both the phase and gain margin of the open-loop transfer function,

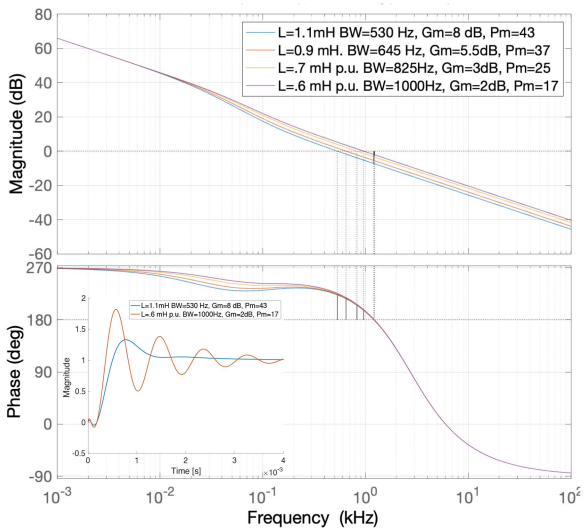

FIGURE 14. Bode plot for different inductance values due to core saturation effect of the ferrite core. Controller gains (K_p=0.06, K_i=10).

which affects the stability of the closed-loop control. The step response, which is included in the same figure, shows an undamped response when the inductance is nominal. However, with a deeply saturated inductor, the step response is undamped with high overshoot. Eventually, for deeper saturation, the closed-loop control would become unstable.

D. VECTOR CONTROL WITH CORE SATURATION

This section derives the small-signal model in dq of the three-phase inverter considering the nonlinearities of the inductor. The objective is to analytically obtain the current transfer function and the decoupling terms to properly tune the controller considering the effects of the core saturation. The flux linkage λ in a three-phase converter can be described as follows [49]:

$$\lambda_{abc} = L_{abc} i_{abc}. \tag{2}$$

The current controller for the three-phase inverter is implemented in the synchronous reference frame. Then, the inductor matrix in the abc-frame needs to be transferred to the dq-frame. Replacing the inductance estimated by (1) to (2)

$$\lambda_{abc} = \begin{bmatrix} L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} & 0 & 0 \\ 0 & L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} & 0 \\ 0 & 0 & L_o + \sum_{n=1}^{\infty} L_{2n} i_a^{2n} i_c^{4} \end{bmatrix} \tag{3}$$

where i_a=I sin(θ), i_b=I sin($\theta - \frac{2}{3}\pi$) and i_c=I sin($\theta + \frac{2}{3}\pi$).

The elements of the abc-frame inductor matrix in (3) are nonlinear and relate to the instantaneous current flowing through the inductor. To linearize the equations, the following assumptions are made. The first assumption is that the three-phase current is balanced without a zero-sequence component. The second assumption is that the currents only contain positive sequence fundamental frequency components. The flux linkage can be expressed in the synchronous reference frame as follows:

$$\lambda_{dq} = T_{abc/dq} L_{abc} T_{dq/abc} i_{dq}. \tag{4}$$

Solving (4) for a fourth-order polynomial, the flux linkage equations are given by the following:

$$\lambda_d = i_d \left(Lo + 3\frac{L_2 I^2}{4} + 5\frac{L_4 I^4}{8} + I^4 L_4 \cos\frac{6\omega t}{16} \right) + i_q I^4 L_4 \sin(6\omega t)/16 \tag{5}$$

$$\lambda_q = i_q \left(Lo + \frac{L_2 I^2}{4} + \frac{L_4 I^4}{8} - I^4 L_4 \cos\frac{6\omega t}{16} \right) - i_d I^4 L_4 \sin(6\omega t)/16. \tag{6}$$

Equations (5) and (6) are nonlinear coupling terms between the direct and quadrature axis. However, these terms can be linearized on the known operating point current since the magnitude of the cross-coupling terms are very small comparing with the dc equivalent inductance. With this approximation, the flux linkage equations are given by the following:

$$\lambda_d = i_d \left(Lo + 3\frac{L_2 I^2}{4} + 5\frac{L_4 I^4}{8} + I^4 L_4 \cos\frac{6\omega t}{16} \right) \tag{7}$$

$$\lambda_q = i_q \left(Lo + \frac{L_2 I^2}{4} + \frac{L_4 I^4}{8} - I^4 L_4 \cos\frac{6\omega t}{16} \right). \tag{8}$$

The equivalent flux linkage can be further simplified by adopting a second-order polynomial. The second-order polynomial provides a very good approximation as was shown in Fig. 9

$$\lambda_d = i_d \left(Lo + 3 * L_2 I^2/4 \right) \tag{9}$$

$$\lambda_q = i_q (Lo + L_2 I^2/4). \tag{10}$$

These equations show that there are no coupling terms between the direct and quadrature axis components. The equivalent d-axis inductance is only related to $3L_2I^2/4 + Lo$ and the q-axis equivalent inductance to $Lo + L_2I^2/4$. The next section will apply this approximated inductance in the dq synchronous reverence control of a three-phase power converter.

E. VECTOR CONTROL CONSIDER CORE SATURATION

This section derives the small-signal model of the inverter of Fig. 15, which considers the saturation of the grid filter inductors. The three-phase voltage source converter is connected to the point of common coupling through the grid filter. The equations of the three-phase inverter with connection to the grid, with the average state model and the external elements

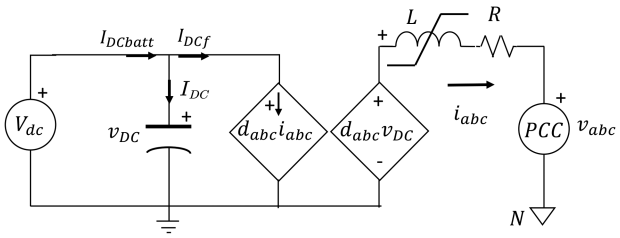

FIGURE 15. Inverter schematic in the abc frame considering nonlinear inductor.

of the circuit are given by the following:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} - \begin{bmatrix} v_N \\ v_N \\ v_N \end{bmatrix} \tag{11}$$

$$\frac{d}{dt} v_{\mathrm{dc}} = \frac{1}{C}\left(I_{\mathrm{DCBATT}} - I_{DCf} \right). \tag{12}$$

The inductor voltage is related with flux linkage for a three-phase inductor as follows:

$$\vec{v}_{abc} = \frac{d}{dt}\vec{\lambda}_{abc} = L\frac{d}{dt}\vec{i}_{abc}. \tag{13}$$

Based on the circuit of Fig. 15, we can write the following:

$$L\frac{d}{dt}\vec{i}_{abc} = \frac{d}{dt}\vec{\lambda}_{abc} = \vec{v}_{abc} - r\vec{i}_{abc} - \vec{d}_{abc} v_{\mathrm{dc}} + \vec{v}_N. \tag{14}$$

Assuming a balanced system, the zero sequence can be neglected

$$\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\vec{\lambda}_{dq} + \frac{d}{dt}\vec{\lambda}_{dq} = \vec{v}_{dq} - r\vec{i}_{dq} - \vec{d}_{dq} v_{\mathrm{dc}}. \tag{15}$$

The current loop transfer function is derived by the small-signal model, which applies small variations around the operation point. Considering a second-order polynomial for the nonlinear inductor

$$\tilde{i}_d = \frac{-\tilde{d}_d V_{dc} + \omega \tilde{i}_q L_q}{(sL_d + r)} \tag{16}$$

$$\tilde{i}_q = \frac{-\tilde{d}_q V_{dc} - \omega \tilde{i}_d L_d}{(sL_q + r)} \tag{17}$$

where the q- and d-axis inductances are defined as follows:

$$Ld = Lo + 3\frac{L_2 I^2}{4} \tag{18}$$

$$Lq = Lo + \frac{L_2 I^2}{4}. \tag{19}$$

Equations (16) and (17) show that the d and q channels are coupled by the terms $\omega\tilde{i}_q L_q$ and $\omega\tilde{i}_d L_d$; these terms are inconvenient to independently control the d and q channels. A way to simplify this is to introduce decoupling terms.

The decoupling terms are introduced in Fig. 16 to eliminate the coupling between channels, and this results in a first-order transfer function with a pole defined by the point of operation

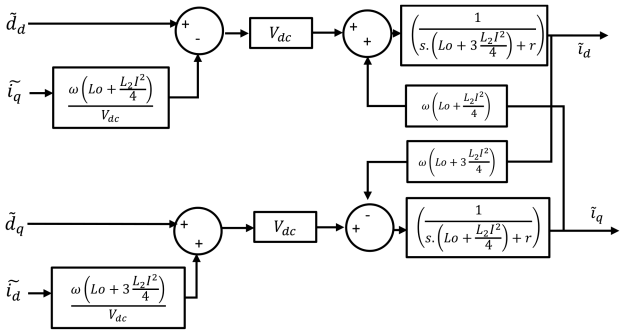

FIGURE 16. Small-signal model of the inverter in *dq* coordinates including decoupling terms considering saturable inductors.

and the passive elements of the grid filter. Equations (18) and (19) show the current to duty cycle transfer function considering the effects of the saturation of the grid filter. Equations (20) and (21) show the current to duty-cycle transfer function considering the saturable inductors. The current I in the equation is related to the peak current only, which can be seen as the operating point of the approximate linearization

$$\frac{\tilde{i}_d}{\tilde{d}_d} = \frac{V_{\rm dc}}{(sL_d + r)} = \frac{V_{\rm dc}}{\left(s\left(Lo + 3\frac{L_2I^2}{4}\right) + r\right)} \tag{20}$$

$$\frac{\tilde{i}_q}{\tilde{d}_q} = \frac{V_{\rm dc}}{(sL_q + r)} = \frac{V_{dc}}{\left(s\left(Lo + \frac{L_2I^2}{4}\right) + r\right)}. \tag{21}$$

VII. PROPOSED CONTROL CONSIDERING GRID-FILTER INDUCTOR SATURATION

Increasing the short-circuit capacity of an inverter without overrating the grid-filter inductor to accommodate this current leads to inductor saturation. As previously discussed, saturation of the inductor reduces the available inductance, severely impacting closed-loop stability. This section introduces a novel method to adapt the current control gains to accommodate the effects of saturable inductors. The primary goal of this control is to maintain stability margins while also minimizing unwanted oscillations during electrical faults, where high short-circuit current is injected. This control is different from proposed control algorithms for controlling inverters during faults [39], [40], which primarily focuses on current limitation. Our approach is for maintaining system stability and it is designed to be complementary and could work alongside with current limiters.

This section presents the method to calculate the control gains considering the saturable inductors. The proposed method consists of retuning the integral and proportional gains considering the available inductance in the grid filter. Then, the Butterworth polynomial is adopted to optimize the closed loop eigenvalue locations [51], [52]. This Butterworth polynomial locates the eigenvalues uniformly in the left-half s-plane on a circle with radius ω , with its center at the origin. The Butterworth polynomial receives as inputs the inductance value $\mathbf{L_{dq}}$, the system delay $\boldsymbol{\alpha}$, and the desired bandwidth for the current controller $\boldsymbol{\omega}$, which is typically 8 to 10 times smaller than the switching frequency. The third-order Butterworth polynomial can be expressed as follows:

$$s^3 + (1 + 2\zeta)\,\omega s^2 + (1 + 2\zeta)\,\omega^2 s + \omega^3 \tag{22}$$

where ω_o is the bandwidth of the current controller, which is set ten times lower than the switching frequency, and ζ is a constant that influences the damping response. The time delay is captured by a first order Padé approximation, where $\alpha = 0.5T_s$ and T_s is the maximum delay time

$$e^{-s(D)T_s} \approx \frac{1 - \alpha\, s}{1 + \alpha\, s}. \tag{23}$$

The open-loop transfer function of the current loop can be expressed as follows:

$$T_{idq} = \beta\left(\frac{1 - \alpha\, s}{1 + \alpha\, s}\right)\left(K_p + \frac{K_i}{s}\right)\left(\frac{V_{dc}}{sL_{dq} + R}\right) \tag{24}$$

where β is the gain for the current sensor, K_p the proportional gain, K_i the integral gain, R the inductor resistance and L_{dq} are the d-axis and q-axis inductances defined in (18) and (19). By comparing the coefficients in the Butterworth polynomial (22) with the denominator of the closed-loop transfer function (25), the controller gains K_p and K_i (26), (27) are obtained

$$G_{id} = \frac{\left(V_{dc}\,(\alpha - \mathrm{s}) * \left(K_i + K_p \mathrm{s}\right)\right)}{\left(\begin{array}{l} s^3 L_{dq} + s^2 r + s\alpha r - s\beta K_i V_{dc} + \\ s^2 L_{dq}\alpha - s^2\beta K_p V_{dc} + s\beta K_p \alpha V_{dc} + K_i \beta \alpha V_{dc} \end{array}\right)} \tag{25}$$

$$K_i = \frac{\omega^3 L_{dq}}{\beta\alpha V_{dc}} \tag{26}$$

$$K_p = \frac{\omega^2 L_{dq}\,(1 + 2\varsigma) + \beta K_i V_{dc} - \alpha r}{\beta\alpha V_{dc}}. \tag{27}$$

Fig. 17 shows the Bode plot of the current open loop transfer function (24). The constant ς is set to one, and the bandwidth of the controller is set to $\omega = 2\pi$ 600 rad/s. The Bode plot shows the efficacy of the proposed controller, which guarantees the phase margin greater than 40° and the gain margin above 8 dB for all operating points.

This provides a solution to the challenges presented previously in the Bode plot of Fig. 14, where it was shown that phase and gain margins changed when the inductor saturates. The step response shows that overshoot is constant for all operation points, even when the inductor is deeply saturated. The proposed controller is computationally lightweight and can be easily implemented in the same inverter microcontroller.

VIII. EXPERIMENTAL RESULTS

The experimental results are divided into the following three sections.

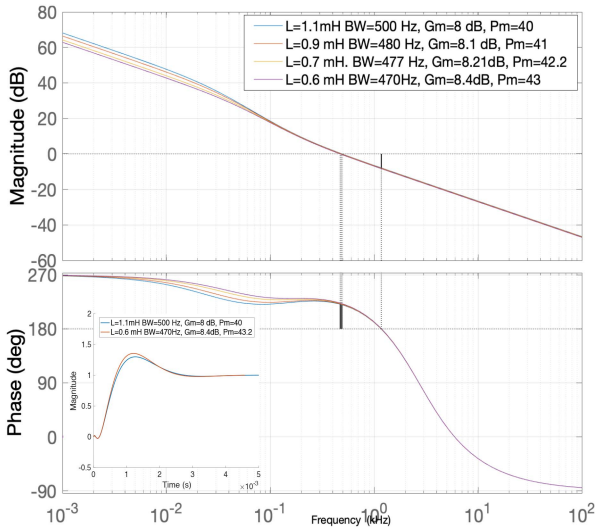

FIGURE 17. Bode plot for different inductance values due to core saturation effect of the ferrite core. PI gains calculated using the proposed controller which considers the core saturation.

1) The first section builds on the findings detailed in [46], highlighting the limitations of normally rated semiconductors when subjected to high short-circuit current conditions.
2) Following this test, a semiconductor with overrated current rating is tested to show that it can safely provide high short-circuit current. For this first section, the inverter current control is disabled to decouple its dynamics, and the inverter operates in open loop control. The second section addresses a comparison between the proposed control that consider the core saturation against a fixed PI controller during the electrical fault conditions.
3) The third section presents a coordination study using the proposed energy storage inverter. The fuse-protective relay coordination tests are divided as follows:
    a) fuse-blowing scheme;
    b) primary backup coordination;
    c) backup protective relay coordination.

A. NORMALLY RATED DEVICE

The initial test evaluates the short-circuit constraints of an inverter equipped with a normally rated semiconductor (10 A, 600 V). The inverter operates in open-loop control to disregard the dynamics of current control, which will be addressed in subsections J and K. The inverter is set to provide [12.5, 15, 20, and 30] A_{RMS}, or in per unit, [1.25, 1.5, 2.0, and 3.0] p.u. The maximum permissible short-circuit current is regulated by the saturation block of the voltage controller [i_{max}, i_{min}] shown in Fig. 2.

As demonstrated in Fig. 18(a) and (b), the normally rated device is capable of handling electrical fault currents of 12.5 A_{RMS}, with a minimal temperature increase in the IGBT junction of $(\Delta T) = 45\,^{\circ}C$ compared to its prefault state. Fig. 18(c) and (d) reveal that the normally rated device can sustain twice its rated current, 20 A_{RMS}, but this result in a large temperature swing is 120 °C. With this temperature increase, the device would surpass its maximum operating temperature of 150 °C if the junction's initial temperature is greater than 30 °C . Finally, the inverter was set to provide an electrical fault current magnitude 30 A_{RMS}. Fig. 18(d), shows the device experienced a catastrophic failure after 0.15 s.

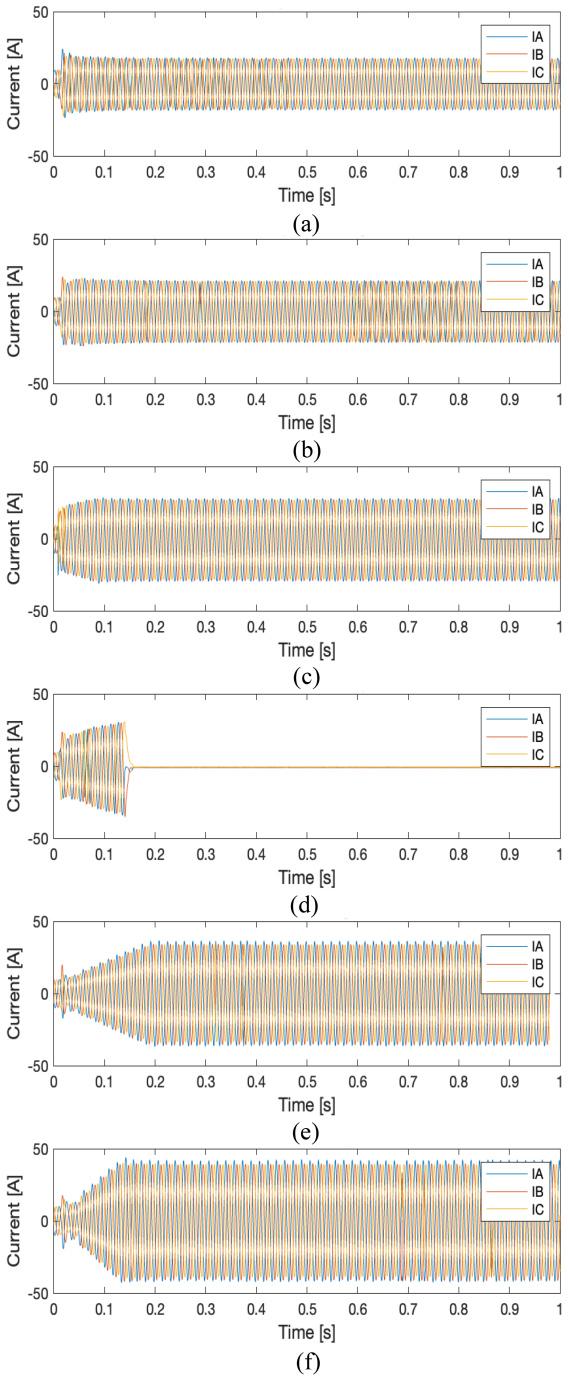

FIGURE 18. Experimental results displaying inverter currents during three-phase faults. The normally rated device rated at 10 A, 600 V, providing the following short-circuit current: (a) 1.25 p.u. (b) 1.5 p.u, (c) 2.0 p.u. (d) 3.0 p.u. Overrated device, rated at 30 A, 600 V, providing the following fault current: (e) 2.5 p.u. (f) 3.0 p.u.

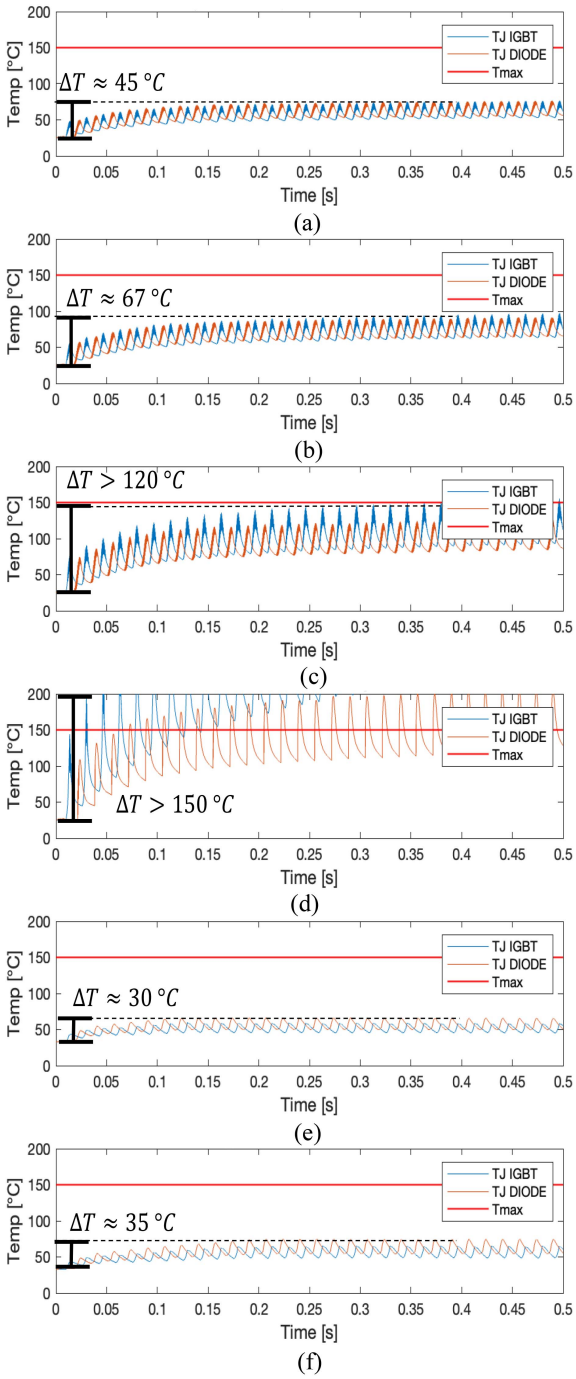

FIGURE 19. Simulated temperature response using 4-layer Foster network for the following short-circuit current: normally rated device providing the following fault current: (a) 1.25 p.u. (b) 1.5 p.u, (c), 2.0 p.u. (d) 3.0 p.u. Overrated device providing the following fault current: (e) 2.5 p.u. (f) 3.0 p.u.

Fig. 19(d) illustrates that the device quickly exceeds its maximum junction temperature, leading to a permanent damage.

B. OVERRATED DEVICE

The experiments with the normally rated device revealed that while it can handle 2.0 p.u. of its rated current, the initial junction temperature must be lower than 30 °C, which is not a realistic constraint for real applications. To increase the inverter's capability to handle high short-circuit currents, the normally rated semiconductor is substituted with one that has three-times higher current rating. This allows for a greater current output during fault conditions. All other inverter components continue to operate at their rated power levels. Fig. 18(e) and (f) display the experimental results using the overrated semiconductor, where the inverter handles electrical faults currents of [19], [29] A_{RMS}. Figure 19(e) and (f) show the corresponding simulated thermal response. The results illustrate that the semiconductor with the higher current rating successfully manages large short-circuit while maintaining the safety margins. Specifically, it can handle a 2.0 p.u. fault current magnitude with a maximum temperature rise $(\Delta T) = 30\,^{\circ}\text{C}$, and a 3.0 p.u. electrical fault current magnitude with a maximum $(\Delta T) = 35\,^{\circ}\text{C}$. An interesting aspect of these experiments is that while the semiconductor is overrated to accommodate higher currents, the other inverter components are kept at their rated values. This method indicates that increasing the short-circuit current handling capacity can be achieved without the need for a complete redesign of the entire inverter system. For the prototype testbed and the selected fuses, 3.0 is the minimum current required for achieving coordination, see Fig. 3.

C. EXPERIMENTAL RESULTS TRADITIONAL CONTROLLER WITH SATURABLE INDUCTORS

This section presents experimental results that compare the dynamic response of the proposed control, which accounts for inductor saturation, to a conventional control with fixed PI gains. To evaluate the stability of the controls, three types of electrical faults were evaluated: LG, LLG, and three-line (3L) electrical faults. This section presents experiments using the prototype inverter that is equipped with an overrated semiconductor device and a normally rated grid-filter inductor.

Fig. 20 presents the experimental results for and inverter using a conventional current controller with fixed PI gains, while Fig. 21 shows the experimental results for the inverter with the proposed controller that considers inductor saturation. The controller with fixed PI shows oscillatory behavior when the electrical fault is applied. This is because inductor saturation limits the available inductance, therefore the phase and gain margin of the current control, diminishes the stability margin and causing overshoots and oscillations when its rated current is exceeded. Fig. 20(c) displays severe oscillations when three-phase electrical faults are applied. Additionally, as shown in Fig. 20(a) and (b), the controller is ineffective at regulating the inverter current. The control signals in Fig. 20(a) and (b) also reveal the presence of a negative sequence current with a frequency of 120 Hz is during asymmetrical electrical faults. This negative sequence is introduced due to the severe unbalance in the voltage caused by the asymmetrical electrical faults.

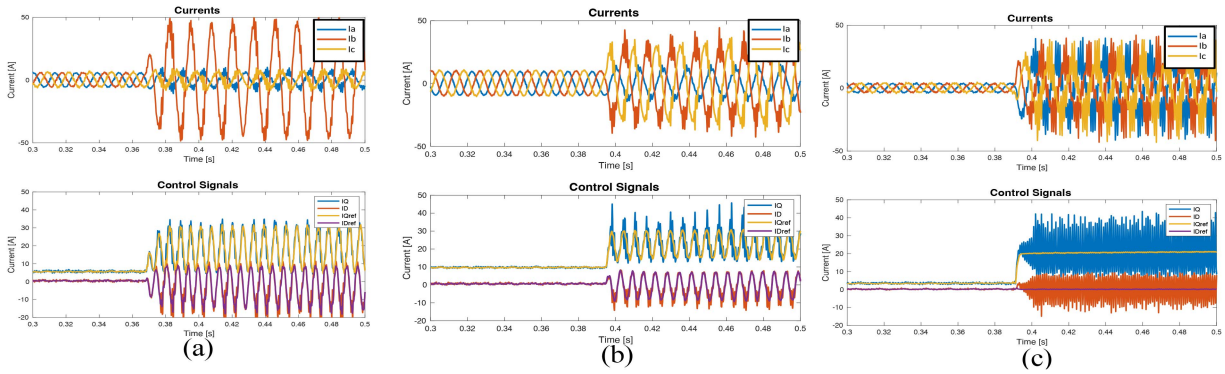

FIGURE 20. Experimental results of inverter under faults using fixed PI gains. (a) Line to ground faults. (b) Line-to-line to ground. (c) Three-phase faults.

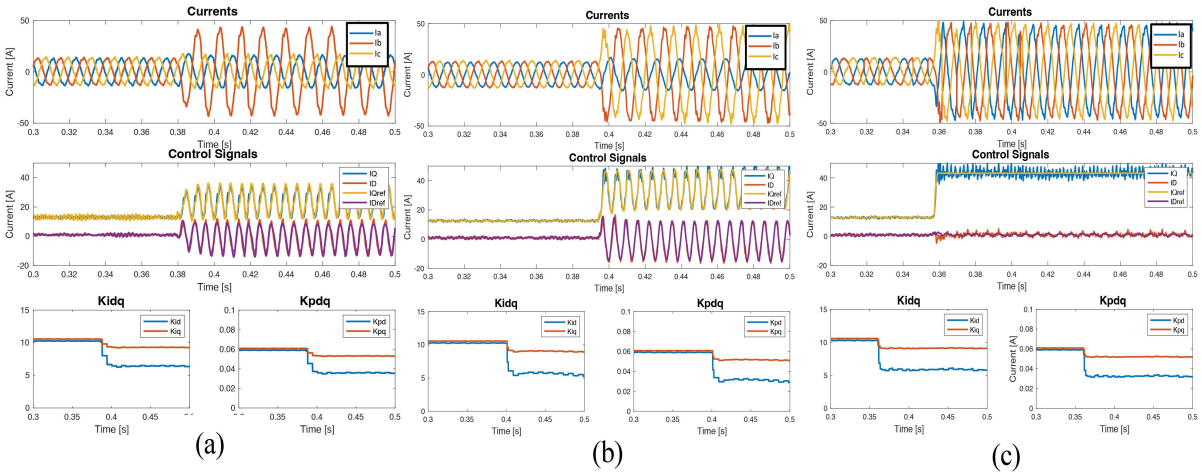

FIGURE 21. Experimental results of inverter under faults using proposed controller that considers inductor core saturation. (a) Line to ground faults. (b) Line-to-line to ground. (c) Three-phase faults.

D. EXPERIMENTAL RESULTS WITH THE PROPOSED CONTROLLER WITH SATURABLE INDUCTORS

Fig. 21 illustrates the performance of the proposed controller that accounts for the grid-filter saturation during for the LG, LLG, and 3L electrical faults. The controller's proportional and integral gains of the current controller are dynamically adjusted based on the available inductance to meet the stability criteria during both high current and normal operation. The proportional and integral gains are determined using (26), (27) and programmed in the same FPGA that hosts the inverter control. The experimental results demonstrate a smooth transition during normal operation states to electrical fault conditions, with mitigated oscillations during high short-circuit current operation. The 120 Hz oscillations correspond to the negative sequence introduced by the voltage unbalance during asymmetrical electrical faults.

E. COORDINATION STUDY: MINIMUM GRADING TIME

Table 6 showcases the impact of various short-circuit currents on the protection coordination between protective relays and fuses within the prototype testbed. For short-circuit currents of 1.25 p.u., neither the fuse nor the primary or backup protective relays act withing 10 s. A similar result was obtained for short-circuit currents of 2.0 p.u. However, at currents exceeding 3.0 p.u., the fuse melts in 0.26 s, effectively maintain coordination with the primary and backup relays, which trip in 0.6 and 0.85 s, respectively. This demonstrates that 3.0. p.u. of short-circuit current is sufficient for maintain proper coordination in the prototype testbed. Although it is possible to modify the protective relay's setting to trip at lower currents, this would make maintaining the grading margins very narrow. For fuse and protective relay, the recommended minimum coordination time interval is 7.2 cycles (0.12 s), for protective relay to relay is 12.2 cycles (0.20 s), as specified in the standard IEEE Std. 242- 2001 [53].

TABLE 6. Protection Coordination for Multiple Short-Circuit Currents

Electrical fault current (p.u)	Fuse melting time (s)	Trip time of primary protective relay (s)	Trip time of backup protective relay(s)
1.25	>10	>10	>10
2.0	>10	>10	>10
3.0	0.26	0.56	0.9

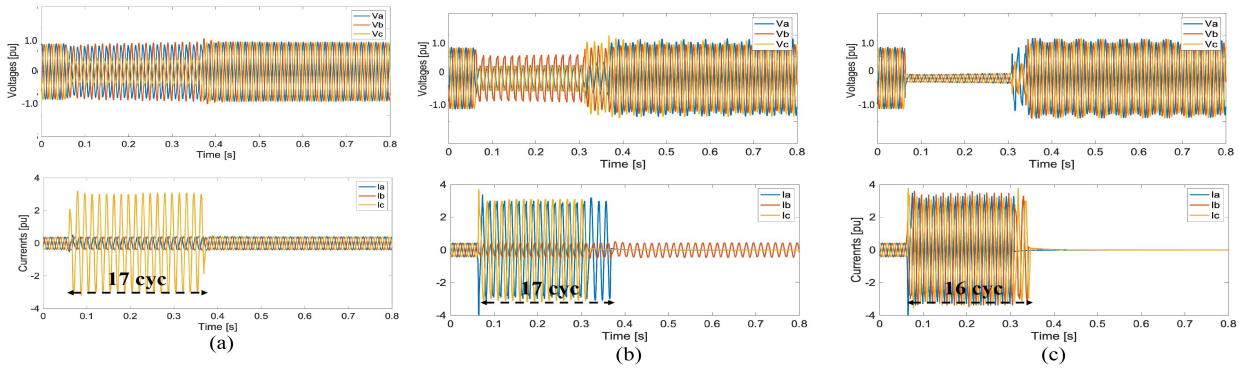

FIGURE 22. Experimental event with proposed inverter hardware modifications and control that considers grid-filter saturation. File collected from SEL 651R relay (128 samples per cycle). Clearing times of the fuse for the following faults (a) line to ground. (b) Line-to-line to ground. (c) Three-phase.

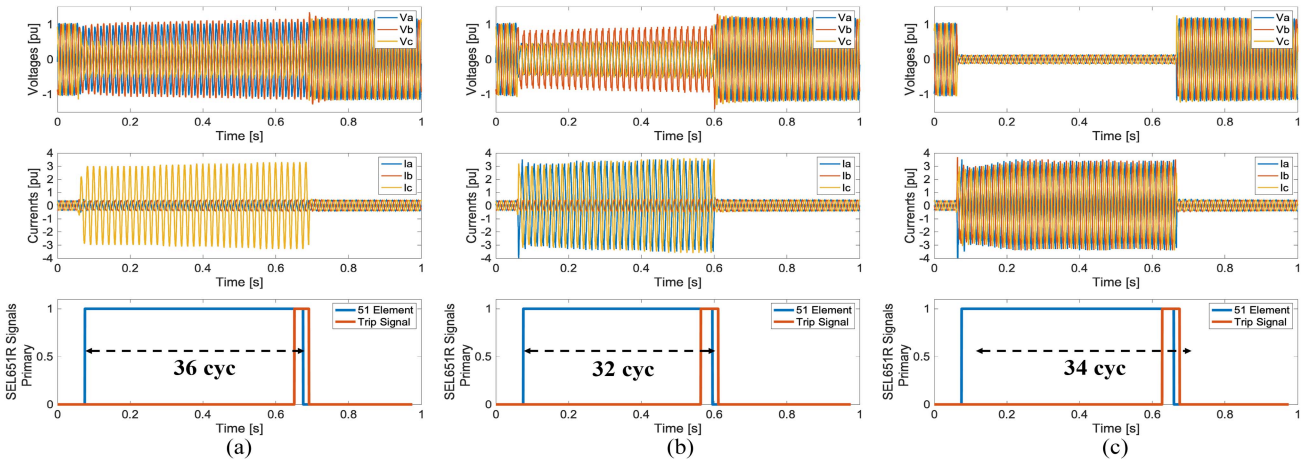

FIGURE 23. Experimental event with proposed inverter hardware modifications and control that considers grid-filter saturation. File collected from SEL 651R relay (128 samples per cycle). Clearing times of the primary relay for the following faults. (a) Line to ground. (b) Line-to-line to ground. (c) Three-phase.

F. FULL COORDINATION STUDY: LG, LLG, 3L ELECTRICAL FAULTS

Fig. 22 shows the experimental results of electrical fault current recorded by the SEL 651R. The SEL captured files are also included as Supplementary material. These events captured the overcurrent event and the clearing time for the fuses located at the end of the power line. Fig. 22(a) shows the results for a LG electrical fault in phase c. For the LG electrical fault, the fuse is blown in 17 cycles. Fig. 22(b) shows the LLG electrical fault applied at the end of the power line. The electrical fault is cleared first in phase-c in 14 cycles and then in phase-a at 17 cycles. This difference in time can be explained by different fuse melting times. Finally, Fig. 22(c) shows a 3L electrical fault was applied at the end of the power line. Like the LLG electrical fault, the fuse melting times are different, and the 3L electrical fault becomes an LLG electrical fault after 14 cycles. The electrical fault was finally cleared in all phases after 16 cycles. As shown, the proposed modifications to the inverter allowed providing enough current to blow the fuses for the LG, LLG, and 3L electrical faults.

Fig. 23 shows experimental results for fuse-relay coordination. For this test, it is assumed that the fuses fail to blow when the electrical fault is applied, and the primary protective relay must isolate the event. As shown, the primary protective relay maintained the coordination and effectively cleared the LG, LLG, and 3L electrical faults.

Fig. 24 shows experimental results for the primary protective relay to backup protective relay coordination. This experiment tested the backup protective relay when neither the fuse nor the primary protective relay cleared the electrical faults. As shown, the backup relay effectively cleared all electrical faults maintaining the coordination in the test system. Table 7 summarizes the tripping time in cycles for all the tests.

The coordination study demonstrates that the proposed modifications to the inverter provide high and sustained short-circuit current to enable the fuse-protective relay and protective relay-relay coordination, which is a promising step to enable adopting legacy overcurrent protection for islanded microgrids. Although the speed of the protection is slower that it would be achievable in grid-tied operation, the full

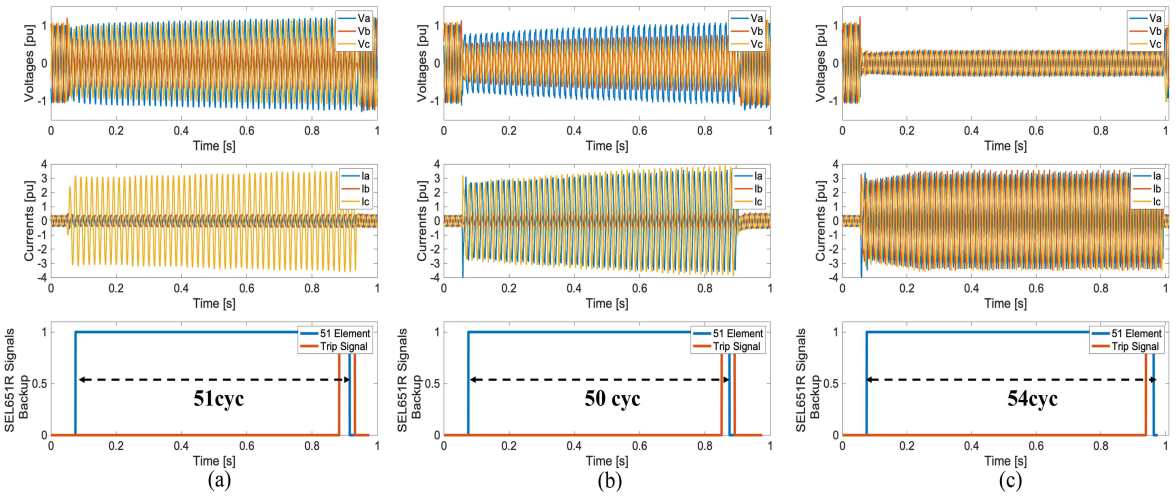

FIGURE 24. Experimental event with proposed inverter hardware modifications and control that considers grid-filter saturation. File collected from SEL 651R relay (128 samples per cycle). Clearing times of the backup relay for the following faults. (a) Line to ground. (b) Line-to-line to ground. (c) Three-phase.

TABLE 7. Summary Protection Coordination Study

Fault Type	Fuse melting time (cycles) [a,b,c]	Trip time of primary protective relay (cycles)	Trip time of backup protetcive relay(cycles)
LG	[0,0,17]	36	51
LLG	[17,0,14]	32	50
3-Phase	[15,16,16]	34	54

coordination was possible in less than one second, which is an acceptable coordination time. The short-circuit power available in islanded mode is significantly lower than in grid-connected mode, reducing the potential damage from faults and allowing for more lenient protection response times under islanded conditions.

IX. DISCUSSIONS

Numerous methodologies for microgrid protection have been documented in academic research; however, overcurrent protection is still being used by community, commercial, and utility microgrids to protect microgrids. This trend suggests that alternative strategies, despite their efficacy, may be hindered by their cost or complexity when integrating into real microgrid systems. This article advocates for an increase in the output current of grid-forming inverters, which are commonly paired with energy storage systems, to utilize mature and affordable distribution overcurrent protection schemes. The proposed modifications are research and development oriented, focused on future inverter generations rather than retrofitting existing installations. The paper's aim is demonstrating the technical and economic viability of increasing the short-circuit current output of grid-forming inverters.

A notable result of this article is that although the semiconductor and current sensors must be overrated to manage higher currents, the other inverter components could remain at their rated specifications. This allows for an increase the short-circuit current capacity without a full redesign of the entire inverter system. In the prototype testbed, at least three per unit of current was required to achieve the minimum coordination time interval. Nonetheless, depending on the time current curves of the protective devices, additional short-circuit current may be needed. However, as shown in Fig. 19(f), the overrated semiconductor had a small temperature increase when supplying short-circuit current, indicating it has the thermal capacity to handle additional current if required.

For the prototype testbed, the protection coordination between fuses and backup protection can take up to a second. Although this time may be considered long for protection, it is important to highlight that the available short-circuit power is significantly lower compared to grid-tied operation. A lower short-circuit power diminishes the potential destructive effects of faults, which allows for the more relaxed response times of protection mechanisms in islanded conditions.

Settings groups in the primary and backup relays can be employed to account for the delayed operational response of fuses, ensuring effective protection coordination for both islanded and grid-tied modes of operation. Finally, it is important to highlight that the required short-circuit current magnitude is depends on the inverse time-current characteristics of selected fuses and upstream protective relays.

X. CONCLUSION

In response to the challenges of protecting inverter-based microgrids, this article proposes a grid-forming inverter designed to provide high-current magnitude contribution during the electrical faults. Experimental results using a prototype inverter showed that increasing the current from grid-forming inverters would enable leveraging legacy distribution protection devices in islanded microgrids. Through experimental results, this article showed that that few modifications are needed for the inverter to provide more than three-fold of short-circuit current. This current proved to be the minimum

current in the test system to allow full protection coordination in the test system while maintaining grading margins between fuses and protective relays. The minimum current to achieve coordination would depend on the inverse time characteristic of the selected fuses for lateral protection.

This work also addressed the challenges of controlling inverters with deeply saturated inductors, which is necessary when operating the inverter at high-current using a normally rated inductor. An online method to adapt the proportional and integral gains based on the available grid-filter inductance was derived and validated in hardware. Additionally, this work analytically derived the current transfer function and decoupling terms considering saturable inductors. The proposed modifications to the inverter provided sufficient electrical fault current magnitude to enable fuse-protective relay coordination in microgrids operating in islanded mode. The proposed modification increases the fault current magnitude, paving a path forward to reliable use conventional and affordable distribution overcurrent protection in islanded microgrids.

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