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Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems

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Abstract

Due to the increasing importance of artificial intelligence (AI), significant recent effort has been devoted to the development of neuromorphic circuits that seek to emulate the energy-efficient information processing of the brain. While non-volatile memory (NVM) based on resistive switching, phase-change memory, and magnetic tunnel junctions have shown potential for implementing neural networks, additional multi-terminal device concepts are required for more sophisticated bio-realistic functions. Of particular interest are memtransistors based on low-dimensional nanomaterials, which are capable of electrostatically tuning memory and learning behavior at the device level. In this Perspective, a conceptual overview of the memtransistor is provided in the context of neuromorphic circuits. Recent progress is surveyed for memtransistors and related multi-terminal NVM devices including dual-gated floating-gate memories, dual-gated ferroelectric transistors, and dual-gated van der Waals heterojunctions. The different materials systems and device architectures are classified based on the degree of control and relative tunability of synaptic behavior, with an emphasis on device concepts that harness the reduced dimensionality, weak

electrostatic screening, and phase changes properties of nanomaterials. Finally, strategies for achieving wafer-scale integration of memtransistors and multi-terminal NVM devices are delineated, with specific attention given to the materials challenges for practical neuromorphic circuits.

1. Introduction

The field of artificial intelligence has experienced massive growth due to innovations in algorithms and the increased computational power of complementary metal-oxide-semiconductor (CMOS) technology. The proliferation of digital data acquisition and communication has further accentuated the need for rapid local data processing to enable timely decision-making. Although the miniaturization of individual devices has slowed, commercially available graphics processing units (GPUs) have sustained the growth in computation power that is necessary for training deep neural networks (DNNs) with increasing complexity.[1-4] However, current machine learning and artificial neural network (ANN) algorithms continue to rely on CMOS chips that use the von Neumann architecture,[5] where data must be constantly shuttled between the processing and memory units. With large amounts of data, this architecutre leads to poor scaling of computational time and energy consumption due to limited bandwidth that is often referred to as the von Neumann bottleneck.[6] To circumvent this intrinsic limitation of CMOS technology, increasing effort has been devoted to neuromorphic computing approaches that attempt to emulate the energy-efficient information processing in biological neural networks.[7] Neuromorphic circuits aim to take advantage of the parallel, low-power, and fault-tolerant processing of the brain by mimicking the functions of neurons and synapses in highly interconnected networks.[8]

Synapses greatly outnumber neurons in both the brain (~10^{15} synapses versus ~10^{11} neurons) and fully connected ANN architectures, making them critical elements for neuromorphic hardware implementations. Biological synapses can either enhance or inhibit the transmitted signal between neurons. The level of transmission is determined by the strength of the synaptic connection, which is updated during learning. Consequently, artificial synapses should not only store

an analog weight but also possess a physical mechanism to update the weights based on simple protocols. In solid-state electronic devices, the synaptic weights are often represented using different conductance states, where the conductance range and weight update rules are constrained by materials properties. For most ANN applications, non-volatile memory (NVM) and time-independent linear and symmetric weight update rules are sufficient. However, bio-realistic synaptic functions are complex and temporally influenced, requiring more complicated learning rules such as short-term and long-term plasticity,[9, 10] paired-pulse facilitation,[11] spike-time dependent plasticity (STDP),[12, 13] spiking-rate dependent plasticity (SRDP), heterosynaptic plasticity,[14] and metaplasticity.[15] Like synapses, bio-realistic neuron behavior is also highly diverse, which has motivated the development of mathematical neuron models with varying levels of complexity.[16-20] Often highly simplified cases such as the perceptron[21] are sufficient for ANNs, resulting in many neuron models being designed to imitate only the ability of the neuron to integrate incoming signals and fire output spikes after reaching a predefined threshold.

While biological neurons and dendrites can achieve an extremely large number of synaptic connections in three dimensions, the physical realization of neuromorphic circuit architectures has thus far been constrained by the planar and rigid nature of integrated circuits. For ANN architectures, fully connected one-dimensional layers of perceptrons called multi-layer perceptrons (MLPs)[22] can be implemented in a planar geometry using crossbar arrays. Although MLPs and other DNNs using back-propagation and gradient descent-based supervised learning algorithms have shown success for select AI applications, they fail to incorporate many features of biological neural networks and require large amounts of computationally intensive matrix multiplication.[23] In contrast, bio-realistic spiking neural networks (SNNs) are an emerging architecture that rely on temporally coded spikes to transmit information and are typically trained using STDP-based unsupervised learning rules.[24, 25] Despite their inferior performance for pattern recognition, SNNs are more energy-efficient than ANNs due to their temporally dependent and sparse spiking

behavior, and are well-suited for event-driven applications.[25, 26] Importantly, SNNs also provide opportunities for additional bio-realistic functionality such as reinforcement learning and other reward-based learning rules. Other network models that are optimal for particular problems, such as recurrent neural networks (RNNs) for natural language processing, convolutional neural networks (CNN) for image recognition, and reinforcement neural networks for robotic applications are also relevant, and often come with unique requirements at the device and circuit level.[3, 4, 27-29]

Due to its technological maturity, silicon was the first platform used for exploring neuromorphic computing[30], and the semiconductor industry remains interested in developing in-memory[31] using CMOS-based field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs).[32, 33] SpiNNaker,[34] TrueNorth,[35] and Loihi,[36] are large-scale examples of spike-based neuromorphic hardware that seeks to take advantage of the unique characteristics of SNNs at the hardware level.[34, 36] However, these CMOS-based examples suffer from high power consumption due to the von Neumann bottleneck, with an extreme example being the GPU-based training of a neural architecture search (NAS) model consuming over 650,000 kWh of power.[37] Consequently, emerging NVM technologies are considered to be a promising alternative due to lower power consumption and smaller footprints.[38] In crossbar array implementations, each NVM node between rows and columns acts like a synapse. The output current from each node is summed along the rows and columns before feeding into the neurons that are further connected with the same or another set of crossbar synapses. In this manner, crossbar arrays of NVM elements can be used to directly map ANN weights to device conductance states, enabling parallel operations for analog vector-matrix multiplication (VMM).[39] The fundamental switching mechanisms, materials science, and applications of NVM devices have been extensively reviewed elsewhere,[40] including implementations based on nanomaterials,[41] organic electronics,[42] van der Waals layered materials,[43] phase-change materials,[44] ferroelectric and multiferroic materials,[45] Mott insulators,[46] spintronics,[47] memristors,[6, 38] and other inorganic synaptic transistors.[48]

Among these NVM options, memristors have attracted significant recent attention due to their small footprint, fast switching time, low power consumption, and capability for multi-state storage. Furthermore, memristors can implement bio-inspired functionality such as STDP due to the underlying similarities between ionic motion in biological synaptic channels and the correlated drift and diffusion of electrons, defects, vacancies, and ions in memristive systems. However, memristors are simple two-terminal devices, and typically require an additional element like a transistor to select individual nodes. An NVM device with gate-tunable memory not only integrates selection functionality at the device level but can also use the gate electrode to influence the switching behavior and achieve on-demand learning rules. In a single two-terminal device, this level of tunability is not possible because switching mechanisms involving resistance state changes are intimately tied to underlying physical processes such as electron transport, ion migration, phase change, thermal transport, and spin flipping processes. Despite these limitations, some progress has been made in tailoring the switching behavior of two-terminal memristors by controlling material stoichiometry or using multi-layered structures. For example, Ag islands in an oxide matrix can disperse under an applied electric field and regroup due to surface tension, resulting in a bio-realistic delay and relaxation response.[49] Nevertheless, even if a memristive system can display a bio-realistic response and desired learning rules for a specific data-centric problem, a memristor-based circuit offers limited additional reconfigurability at individual nodes due to the two-terminal architecture. In this context, nanomaterials are capable of alternative device architectures where the underlying resistive switching can be coupled to additional control parameters such as electrostatic gating and photoexcitation.[41, 50] In particular, two-dimensional (2D) materials not only allow anisotropic in-plane conductivities and multi-terminal geometries but also present opportunities for van der Waals heterojunctions with other low-dimensional nanomaterials.[51]

Three-terminal gate-tunable memristors, also known as memtransistors, are promising device prototypes that exploit the weak electrostatic screening of low-dimensional nanomaterials.

Typically, memtransistors are based on Schottky barrier tuning at metal-semiconductor interfaces using vacancy/ion transport, charge trapping, or ferroelectric domain switching. Other switching mechanisms, such as those found in phase-change materials, have also been explored. In addition to their intrinsic resistive switching, the channels are atomically thin and therefore can be strongly tuned using electrostatic gating. Electrostatic gating not only allows for control of the channel conductance through the field effect, but it can also be used to directly influence the switching mechanism of the NVM state. Therefore, by combining NVM with gate tunability in a single device, memtransistors simplify addressability in crossbar arrays and efficiently enable tunable learning rules and bio-realistic functions such as heterosynaptic plasticity, continuous learning, neuromodulation, and multi-temporal plasticity.

Figure 1 summarizes the areas of interest for memtransistors including materials synthesis, devices, architectures, and applications. In the following sections, we will first review concepts and mechanisms underlying memristors, memtransistors, and related devices such as dual-gated synaptic transistors, and how these mechanisms are influenced by material defects. We will also explore how defects can be engineered during the materials synthesis process. We will then discuss recent experimental demonstrations of gated memory devices and memtransistors based on 2D materials, van der Waals heterojunctions, and related material systems. Initial attempts to integrate memtransistors and related devices in scaled circuit architectures will be delineated, with a specific focus on the opportunities enabled by the ultrathin nature of 2D materials. Finally, we will outline the remaining challenges and opportunities for moving from individual memtransistor devices to full neuromorphic circuits and systems, such as requirements for wafer-scale integration, opportunities for realizing novel bio-inspired functions, and the need to develop new software and neuromorphic architectures to fully take advantage of the unique properties of memtransistors.

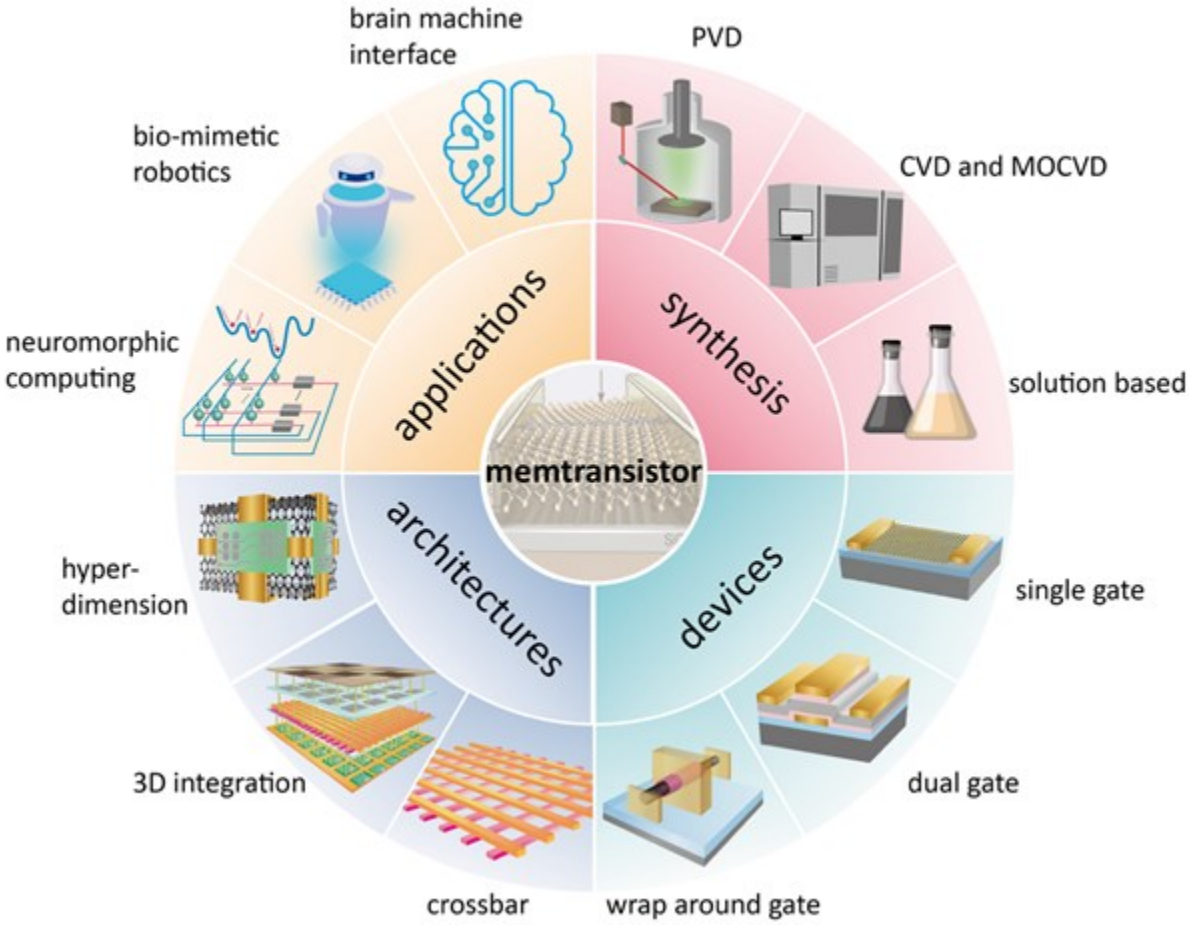

Figure 1. Summary of memtransistor synthesis, device structures, architectures, and neuromorphic applications. Synthesis methods include physical vapor deposition (PVD), chemical vapor deposition (CVD), metal-organic chemical vapor deposition (MOCVD), and solution-based processing to realize materials suitable for memtransistors. Memtransistor device structures can be designed with different gating schemes to enable new device functions. Connecting multiple memtransistors in crossbar arrays and/or three-dimensional (3D) integration can further facilitate applications in neuromorphic computing, bio-mimetic robotics, and brain-machine interfaces. The memtransistor schematic at the center is adapted with permission.[52] Copyright 2018, Springer Nature. The 3D integration schematic is adapted with permission.[53] Copyright 2017, Springer Nature.

2. Memtransistor Fundamentals

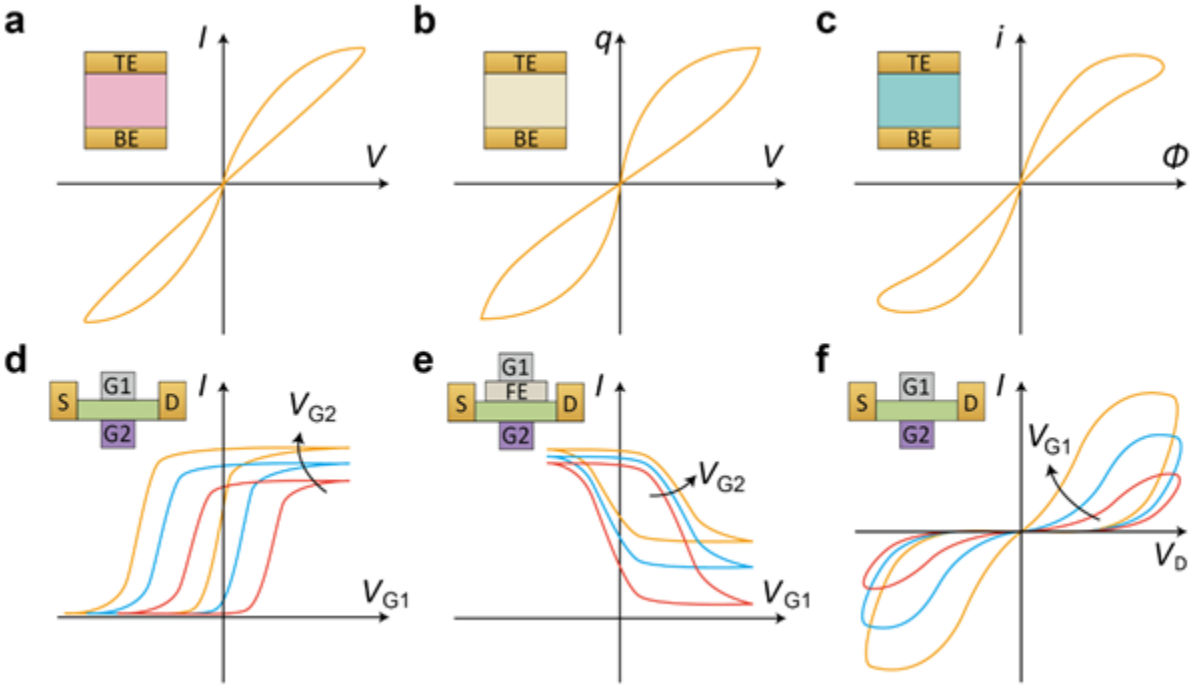

Figure 2. Current-voltage (I-V) characteristics of two-terminal memristive systems, multi-terminal memtransistors, and related device concepts. (a) Memristor. (b) Memcapacitor. (c) Meminductor. (d) Dual-gated synaptic transistor. (e) Dual-gated ferroelectric field-effect transistor (FeFET). (f). Dual-gated memtransistor. (d-f) The arrow shows how the device behavior changes under increasing gate voltage bias (V_{G2}). TE and BE stand for top electrode and bottom electrode, respectively. S, D, G1, and G2 stand for source electrode, drain electrode, gate electrode 1, and gate electrode 2, respectively. FE stands for ferroelectric dielectric.

The prototypical memristor[54, 55] consists of a metal/insulator/metal stack, whose current-voltage (I-V) characteristic displays a pinched hysteresis loop[56, 57] (**Figure 2a**). The resistance of the device is controlled by the migration of defects, dopants, or ions, which modulate the conductance through the formation and rupture of a filament or by modifying the Schottky barriers at the

contacts. Depending on the switching mechanism, different types of volatile and non-volatile memristive behavior have been observed such as bipolar, unipolar, threshold, complementary, and diffusive resistive switching.[41, 58-60] The concept of memristive systems has also been extended to meminductors and memcapacitors,[61] which show similar pinched hysteresis loops for charge-voltage and current-flux curves, respectively, and are mainly used to pursue hardware implementation of spiking neurons and neuristors (Figure 2b-c).[62] Furthermore, higher-order memristive systems include more than two coupled internal state variables with intrinsic dynamical behavior, with second-order and third-order memristors having been demonstrated experimentally.[63-66]

The memistor[67] is distinct from but related to the memristor in that it is a combination of "memory" and "resistor" but consists of three terminals. The third terminal is used as a gate to modulate the formation and rupture of the conductive filament, which was first demonstrated with copper electroplating of a graphite rod.[67] Due to the recent interest in using NVM for neuromorphic circuits, three-terminal devices like memistors have gained traction as a means of decoupling the write and read terminals in the network. One simple way to create the circuit equivalent of a memistor is by connecting two memristors in parallel using independent source terminals and a common drain terminal.[68] However, a more compact approach to achieve the same response is to engineer memristor materials and device geometries so that only a single third terminal is needed for modulation of the resistive switching. For example, in a three-terminal TiO_2 memristor realized using angled evaporation of metals, an applied voltage at a third terminal was shown to modulate the resistance between the first two terminals by a factor of 20. Similar multi-terminal memristor schemes have also been explored in oxide nanowires to understand resistive switching mechanisms,[69] and in planar films of Ag nanoclusters to demonstrate heterosynaptic plasticity.[70] Three-terminal memistors have also been studied in Ta_2O_5,[71-73] TiO_2,[68] $SrTiO_3$,[74] and Ag/Cu atomic switches,[75] often with the addition of a gate dielectric to reduce the leakage currents from the third

terminal (**Figure 3a**). However, while memistors can show continuous conductance states with a wide dynamic range,[76] the additional terminal increases the device footprint and fabrication complexity, limiting their suitability as synaptic elements. As suggested by Zidan,[77] one possibility is to use memistors as a selector element in memristor crossbar arrays. Because of their exceptionally high off-state resistance and non-volatile switching, memistors would enable fine control over individual nodes while consuming less power compared to conventional selectors.

In addition to memistors, three-terminal transistors with integrated memory have also been developed for neuromorphic applications.[48] The earliest transistors for synaptic emulation (i.e., synaptic transistors) were fabricated using conventional CMOS technology, namely floating-gate flash memory.[78] More recently, floating-gate transistors based on 2D semiconductors such as monolayer MoS_2 and graphene have been explored (Figure 3b) due to their improving scaling potential and the ultrafast speed of charge tunneling through the van der Waals barrier.[79-82] Similarly, synaptic transistors based on interface charge trapping have been explored in a variety of contexts due to their potentially lower power consumption per synaptic weight update operation.[83-86] In particular, charge trapping carbon nanotube[87] and MoS_2[88] synaptic transistors have been demonstrated and used to implement STDP protocols for SNNs. Nanomaterial-based devices are highly advantageous in this regard due to the high surface area and large curvature that results in increased access to interfacial and other midgap trap states. Additionally, the reduced charge screening of nanomaterials allows for greater electrostatic control via dual-gated and self-aligned device architectures.[89, 90] While dual-gated synaptic transistors have been demonstrated using CMOS platforms, they typically require complicated structures such as fin field-effect transistor (FinFET) or gate-all-around (GAA) structures to achieve full electrostatic control.[91] In contrast, a simple lateral structure is sufficient for full electrostatic control over 2D materials. For example, dual-gated MoS_2 synaptic transistors have been demonstrated with oxide bilayer charge trap memory using $Al_2O_3/HfO_2/Al_2O_3$ stacks.[92] Dual-gated MoS_2 synaptic transistors have also been

realized with floating-gate memory using hBN as a tunnel barrier and either metal[93] or graphene[94] as the floating gate. Sweeping the top gate in these synaptic transistors typically leads to a transfer curve with a large hysteresis window, which is dependent on the magnitude of the voltage sweep. Applying a back-gate voltage then shifts the threshold voltage and also changes the size of the hysteresis window via doping/de-doping of the channel (Figure 2d), enabling multi-level weight storage and tunable learning curves[94] for neuromorphic applications. Charge trapping memory can also be programmed using the source and drain contacts, to obtain a two-terminal charge-trapping memristor (i.e., memflash). This concept has been demonstrated in both silicon CMOS[95, 96] and van der Waals heterojunction[97, 98] floating-gate devices. However, gate-tunable memristive behavior is difficult to achieve in these cases since the tunneling primarily occurs underneath the metallic contacts, which screen the electric field from the gate electrode.

Another strategy to achieve gate-controlled NVM is by using ferroelectric gate dielectrics in ferroelectric FETs (FeFETs).[45, 99] For example, ZnO transistors with a Pb(Zr, Ti)O_3 ferroelectric dielectric have been used as synaptic devices in a Hopfield neural network,[100] and IGZO transistors with a $HfZrO_x$ ferroelectric dielectric have been used in multi-layer perceptrons.[101] FeFETs with ultrathin channels can also be implemented in dual-gated structures for tunable memory.[102] However, unlike dual-gated charge-trapping or flash memory, the effect of the additional gate in FeFETs is more complicated due to electrostatic coupling, and thus additional constraints often need to be addressed to obtain large on/off ratios (Figure 2e.). In a demonstration of a dual-gated SnO transistor with a ferroelectric P(VDF-TrFE) polymer,[103] the threshold voltage remained relatively unaffected by the back-gate voltage since the ferroelectric polymer layer was largely screened by the 30-nm-thick channel. In contrast, in a dual-gated FeFET with a few-layer MoS_2 or black phosphorous channel and the same P(VDF-TrFE) ferroelectric layer, the channel showed a strong electrostatic interaction with the bottom and top gates, resulting in an on/off ratio exceeding 10^3.[104]

Gate-tunable synaptic responses have also been achieved with electrolyte-gated transistors (EGTs) that are modulated by ionic electric double layers (EDLs) and organic electrochemical transistors (OECTs) that are modulated by redox reactions.[42, 105] However, electrolyte-based NVM suffers from poor retention times due to ionic relaxation, although the integration of OECTs with diffusive Ag-oxide memristors (Figure 3c) can enhance the state stability and enable parallel operation of crossbars.[106] Li-ion-based synaptic transistors based on solid-state electrolytes have also shown promise due to linear and symmetric learning behavior for low-power analog computation.[107] For example, dual-gated Li-ion-intercalated MoS_2 synaptic transistors (Figure 3d) have demonstrated neuristor behavior with independently controlled responses from the electrolyte and dielectric gates.[108] Electrolyte gating also enables the integration of multiple gate terminals with spatially and temporally coupled signals, which is particularly well-suited for niche neuromorphic applications such as sound localization. The non-rectilinear channel geometries in electrolyte and ion-gel-based materials have further been used to demonstrate heterosynaptic plasticity in MoS_2 synaptic transistors[109-111] and OECT synaptic transistors[112] in addition to homeostatic plasticity in EGT synaptic transistors.[113, 114]

The memtransistor is also a three-terminal device based on the memristor. Unlike a memistor or a synaptic transistor, the gate electrode in the memtransistor is used to modulate the resistive switching behavior rather than drive it. While synaptic transistors and memistors possess hysteresis and pinched loops in their transfer curves, a memtransistor (Figure 2f) has a gate-tunable pinched hysteresis loop in the output characteristics (I_D-V_D) that can be achieved without gate-bias hysteresis in the transfer characteristics (I_D-V_G). Therefore, single-gated memtransistors incorporate the intrinsic resistive switching behavior of memristors while also achieving a similar node selection function as previously described in dual-gated synaptic transistors. Furthermore, in a dual-gated four-terminal memtransistor, the node selection and tuning functions can be concurrently achieved with no additional circuitry,[115] and differently configured gates can be used to realize bio-mimetic

functions.[116] In the following section, we will review recent experimental progress for memtransistors, which have been primarily implemented using 2D materials and van der Waals heterojunctions.

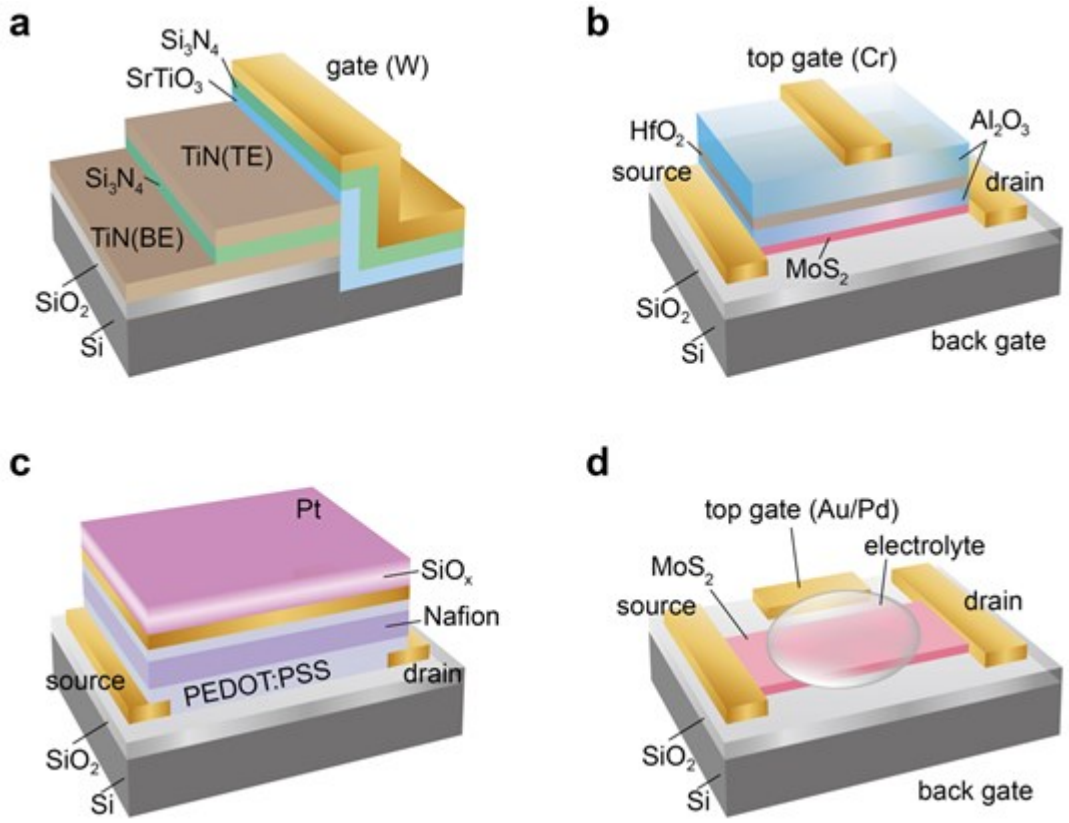

Figure 3. Device architectures for gate-tunable memory devices. (a) Three-terminal memristor based on Si_3N_4 and $SrTiO_3$. Adapted with permission.[74] Copyright 2018, IEEE. (b) Dual-gated MoS_2 charge trapping memory device possessing tunable hysteresis. Adapted with permission.[92] Copyright 2015, American Chemical Society. (c) Ionic floating-gate memory device consisting of an organic electrochemical transistor and diffusive memristor for parallel operation of the crossbar array. Adapted with permission.[106] Copyright 2019, The American Association for the Advancement of Science. (d) Dual-gated MoS_2 synaptic transistor with an electrolyte top gate and a Si/SiO_2 back gate and dielectric stack. Adapted with permission.[108] Copyright 2019, American Chemical Society.

3. Memtransistor Materials, Mechanisms, and Architectures

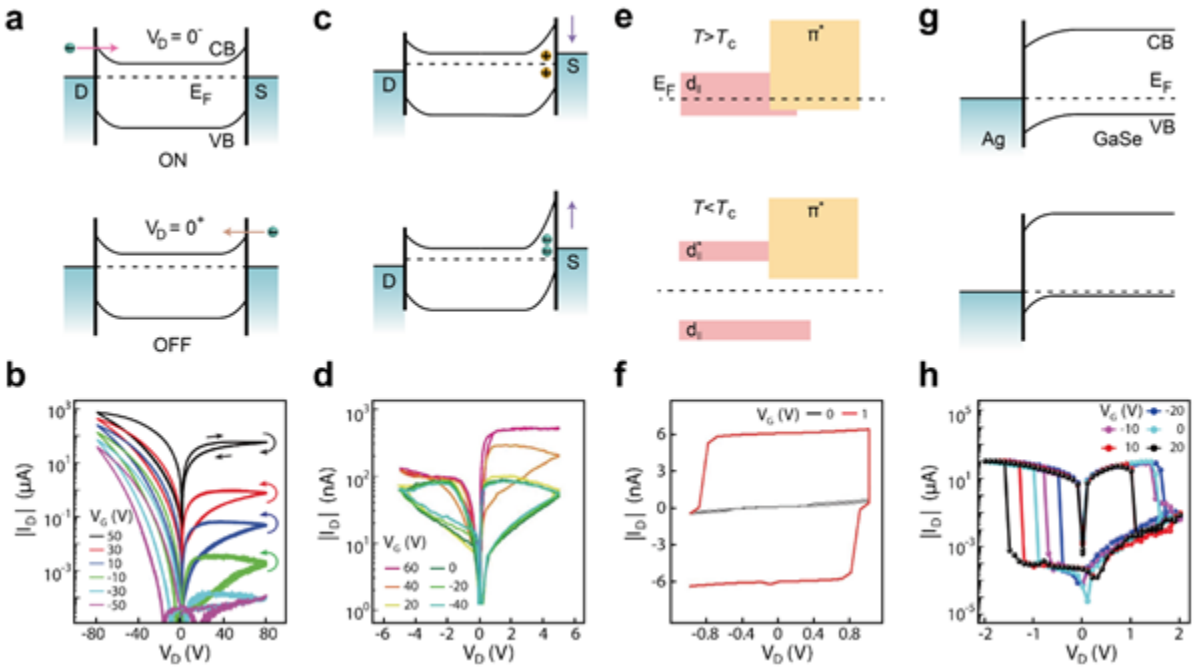

Figure 4. Band diagrams and I-V characteristics of memtransistors and related memory devices. (a-b) Band diagram of a monolayer polycrystalline MoS_2 memtransistor[117] showing switching of the dominant Schottky contact in the OFF and ON states (top) and corresponding I_D-V_D characteristics (bottom) at different gate voltage biases (V_G). Arrows show the direction of the curves. Reproduced with permission.[52] Copyright 2018, Springer Nature. (c-d) Band diagram of an α-In_2Se_3 ferroelectric memtransistor (top) showing Schottky barrier modulation via in-plane ferroelectric polarization and corresponding I_D-V_D characteristics (bottom) showing gate tunability. Reproduced with permission.[118] Copyright 2019, Wiley. (d-e) Change in VO_2 band structure during the Mott metal-to-insulator transition (top) and corresponding I_D-V_D characteristics of the VO_2 memtransistor (bottom) showing gate tunability of the Mott transition. Reproduced with permission.[119] Copyright 2021, Wiley. (f-g) Schottky barrier modulation associated with the filament formation mechanism in a GaSe memtransistor (top) leading to I_D-V_D characteristics (bottom) with gate-tunable resistive switching. Reproduced with permission.[120] Copyright 2019, Elsevier.

3.1. MoS_2 Memtransistors

Resistive switching in bulk materials relies on vacancy or ion migration to modulate the Schottky barrier height or to form and rupture conductive filaments in memristors. Using 2D materials, this mode of resistive switching has also been achieved in thin vertical memristors and atomristors.[41, 43, 121, 122] Although some control over device characteristics can be realized with thickness and stoichiometry control, these two-terminal memristors achieve essentially the same NVM synaptic functions as conventional metal-oxide memristors, and have limited gate tunability due to the vertical structure that results in strong screening by the electrodes.[43, 123, 124] In contrast, planar memristive behavior in 2D semiconductors was first demonstrated using polycrystalline, sulfur-deficient MoS_2 grown by chemical vapor deposition (CVD), where the planar geometry enabled strong gate tunability.[125] Different types of switching behaviors were observed for different grain boundary topologies, and the sulfur-deficient stoichiometry was found to be essential for resistive switching. The MoS_2 memtransistor response was then made considerably more reproducible by employing multiple grain boundaries in the channel to avoid the discrete dependence on single grain boundary topologies.[117, 126] A diverse range of *in-situ* measurements, such as cryogenic charge transport,[117] electrostatic force microscopy (EFM),[117, 125, 126] Auger electron spectroscopy,[127] and Kelvin probe force microscopy (KPFM),[127] have provided further insight into the underlying switching mechanism, consistently implicating lateral field-driven defect motion. At a device level, resistive switching in polycrystalline MoS_2 with Ti/Au contacts originates from modification of the Schottky injection[127] in a manner analogous to certain interface switching mechanisms in bulk memristors (**Figure 4a**). It should be noted that the Schottky injection can be modulated by defect migration and/or charge trapping at MoS_2 grain boundaries or neighboring dielectrics, and charge trapping has also been used to demonstrate gate-tunable memristive behavior.[128]

Measuring the I_D-V_D characteristics at different gate biases reveals the gate-tunable nature of the memristive switching, where each resistance state is non-volatile (Figure 4b). At gate biases lower than the threshold voltage, a positive bias at the drain switches the device from a high-resistance state (HRS) to a low-resistance state (LRS), whereas a negative bias switches from LRS to HRS, signifying bipolar resistive switching. Varying the gate voltage not only modulates the current level and switching ratio (I_{LRS}/I_{HRS}) but can also qualitatively change the switching behavior such as inverting the switching direction of the resistance state at high positive gate bias[115] (Figure 4a). These initial MoS_2 memtransistors showed tunable synaptic behavior in long-term potentiation and depression, multi-state memory, and indirect spike-timing-dependent plasticity, albeit at relatively high voltages due to the large device dimensions.[52, 115, 129] More recently demonstrated MoS_2 memtransistors with smaller grain sizes (1-3 μm) and thinner (20 nm) high-k gate dielectrics operate at substantially lower voltages (< 1V) and powers (~20 fJ), and recent work suggests that the operating voltage and switching speed of MoS_2 memtransistors can be further scaled with smaller channel lengths.[52, 130] The planar nature of memtransistors also opens the possibility for surface functionalization. For example, a Nb_2O_5 interfacial layer between the MoS_2 channel and the Al_2O_3 gate dielectric was used to create a larger Schottky barrier, resulting in improved linearity and an increased number (>200) of distinct conductance states.[131]

In 2D memtransistors, the open planar geometry in conjunction with spatially localized switching has been used to demonstrate novel forms of heterosynaptic plasticity through the integration of additional terminals on the 2D channel.[117, 132] Similarly, shared terminals to multiple MoS_2 memtransistors[127] can achieve symmetric heterosynaptic plasticity. The semiconducting nature of the MoS_2 channel also lends itself to additional gating schemes that have not been explored in previous oxide-based memory devices. For example, photo-induced modulation of the Schottky injection increases the switching ratio by two orders of magnitude beyond what has been achieved using only electrostatic gating.[133] Optical illumination can further provide concomitant and

independent short-term and long-term plasticity in MoS_2 memtransistors, where photons act as additional synaptic inputs with only short-term memory.[134] Triple-gated MoS_2 memtransistors based on electrical, optical, and ionic liquid gates have further revealed diverse synaptic behaviors such as reverse and anti-Hebbian STDP, metaplasticity, and homeostatic regulation.[135] In general, the 2D nature of memtransistors allows diversification of the input signals and memory mechanism, which is useful for implementing more complex bio-realistic functions.

3.2. Ferroelectrics

Schottky-barrier-based resistive switching has also been realized in 2D materials without vacancy or ion migration by using the van der Waals α-In_2Se_3 semiconductor as a ferroelectric channel.[118, 136, 137] In lateral α-In_2Se_3 devices, the in-plane polarization switching of the ferroelectric domains is controlled via the drain voltage, resulting in modulation of the Schottky injection (Figure 4c). In these optoelectronically-active devices, the ferroelectric switching is largely decoupled from photogenerated electron-hole pairs, enabling the read current to be either the dark current or the photocurrent (Figure 4d). Furthermore, in the case of thin flakes, drain-induced ferroelectric switching can be additionally modulated using the field effect of the gate electrode. In other words, electrostatic gating can be used to directly switch the in-plane polarization (IP) via coupling with the gate-switchable out-of-plane polarization (OOP). This coupling between IP and OOP polarization enables multi-terminal heterosynaptic plasticity that can be generalized to other ferroelectric van der Waals materials. Although many ferroelectric switching channel devices suffer from incomplete polarization, this issue can be mitigated for 2D ferroelectric semiconductors since they allow dual gating schemes that provide stronger electrostatic control.[138] For example, applying pulses at additional modulatory terminals has been shown to increase the switching ratio of α-In_2Se_3 memtransistors by over an order of magnitude.[137] Although these devices suffer from poor

switching speed (~seconds) due to the need for in-plane polarization switching and relatively large (~1μm) device channel lengths, ferroelectric resistive switching materials are intrinsically capable of much faster switching speeds (~10 ns) due to low levels of atomic displacement.[139]

3.3. Ion and Vacancy Migration

The general concept of gate-tunable memristive switching has also been explored beyond the van der Waals material family. For example, Schottky barrier tuning based on hydrogen ion migration has been exploited for gate-tunable memristive behavior in zinc oxide thin films.[140] In addition to interface-mediated mechanisms that typically exhibit soft switching, filament-based hard-switching has also been explored in memtransistor designs. In particular, methylammonium lead iodide ($MAPbI_3$) perovskite memtransistors have shown gate-tunable resistive switching behavior.[141, 142] Memristive behavior in $MAPbI_3$ is driven by the migration of I^- vacancies that form conductive channels, thus exploiting what is usually a degrading ion migration effect in photovoltaic applications.[143] Similar to 2D material-based memtransistors, light can be used as an additional input with these devices typically displaying photoinduced carrier and ion migration.[142] Gate-tunable filamentary switching has also been demonstrated in memtransistors based on GaSe nanosheets.[120] In GaSe memtransistors, a positive drain voltage bias leads to migration of Se^{2-} ions to the drain contact, inducing the formation of a conductive filament consisting of p-type Ga vacancies, which can then be broken by reversing the voltage direction (Figure 4e). Unlike MoS_2 memtransistors, the I-V characteristics of GaSe memtransistors exhibit prototypical hard-switching behavior that involves an abrupt increase in current (to LRS) after passing a SET voltage, and a similarly abrupt decrease in current (to HRS) after passing a RESET voltage in the reverse direction (Figure 4f). In this case, the effect of the gate voltage is to tune the SET/RESET voltages while also modulating the readout (drain) current by a factor of 100 through field-effect gating of the channel.

Gate tunability of the switching voltage threshold has also been achieved in TiO_x memristors[144] and $Cu_{2-\alpha}S$ memristors, but with weaker field-effect modulation.[145, 146] These examples illustrate that thinner materials provide the most effective gate modulation by allowing for independent control over the volatile channel conductance states and non-volatile memristive states. As the size of the neuromorphic memtransistor circuits increases, the requirement for low off-current becomes more stringent,[77] suggesting that larger bandgap 2D semiconductors with larger resistive switching ratios will be required.

3.4. Phase-Change Materials and Other Mechanisms

Another class of memristive devices involves a phase change such as a metal-to-insulator (MIT) transition or a current-induced crystal phase change. For example, vanadium oxide undergoes a Mott MIT transition at 341 K that can be stimulated electrically or thermally (Figure 4g).[119] Polycrystalline VO_2 thin films have been used for low-power memtransistors, where the MIT-based resistive switching is sharply tuned with only a small gate voltage bias of 1 V (Figure 4h). This system also exhibits significantly faster switching speeds (35 ns) compared to other memtransistors of comparable channel length, since switching does not rely on atom or charge migration. However, while the transition from insulator to metal in VO_2 can theoretically be achieved with even faster switching speeds (< 1 ps), the relaxation back to the insulating state has so far been limited to tens of nanoseconds.[147] Additionally, the switching behavior in VO_2 memtransistors is especially complicated due to the intermixing of the dielectric and the channel materials that leads to the formation of a $VSiO_x$ interlayer. Recently, dual-gated phase-change memory (PCM) memtransistors have also been demonstrated,[116] where the gate voltage was not used to tune the switching ratio, but instead to introduce short-term plasticity for sequential learning and homeostatic regulation.

Finally, organic and polymer-based memtransistors have been realized based on UV-gated charge trapping[148] and ion exchange.[149]

3.5. Van der Waals Heterojunctions

The ability of 2D materials to form diverse heterostructures through van der Waals bonding enables heterojunction memtransistors, especially those based on barrier-type mechanisms. **Figure 5a** shows a vertical device based on graphene/WSe_2/WO_{3-x} exhibiting gate-tunable resistive switching (Figure 5b) via electrostatic control of the graphene/WSe_2 Schottky barrier height.[150] Due to its similarity to a graphene-silicon barristor[151], this device can be viewed as an integrated barristor and oxide memristor. Although the gate does not directly interact with the channel, gate-modulated synaptic learning is achieved by controlling the relative distribution of fields at the interface, which is determined by the gate-controlled Fermi level in the graphene layer. Similar concepts have also been shown in graphene/$ReSe_2$ heterojunctions,[152] graphene/InN nanowires,[153] and hBN/graphene/MoS_2 heterojunctions.[154] Volatile reconfigurable synaptic devices have further been explored in BP/SnSe heterojunctions (Figure 5c) that are capable of excitatory or inhibitory synaptic behavior depending on the electrostatically controlled configuration of the junction (Figure 5d).[155] Beyond Schottky barrier control, van der Waals heterojunctions also can be used to engineer well-defined charge-trapping interfaces, such as those found in floating-gate synaptic transistors.[80-82] Recent work has further shown that floating-gate van der Waals heterojunctions can achieve ultrafast (10 ns) writing with moderate (10 s) refresh times (Figure 5e-f).[79] Since carefully designed flash memory devices with lateral offsets are capable of programming, erasing, and reading with only two terminals, a third gate terminal can then be used for modulatory purposes. For example, Figure 5g-h shows a MoS_2/hBN flash memory device with gate-tunable memristive hysteresis.[156] These devices possess fast writing (~50 ns) and non-volatile memory in addition to improved training

for pattern recognition via gate-tunable learning. A summary of device metrics for demonstrated memtransistor devices is provided in **Table 1**.

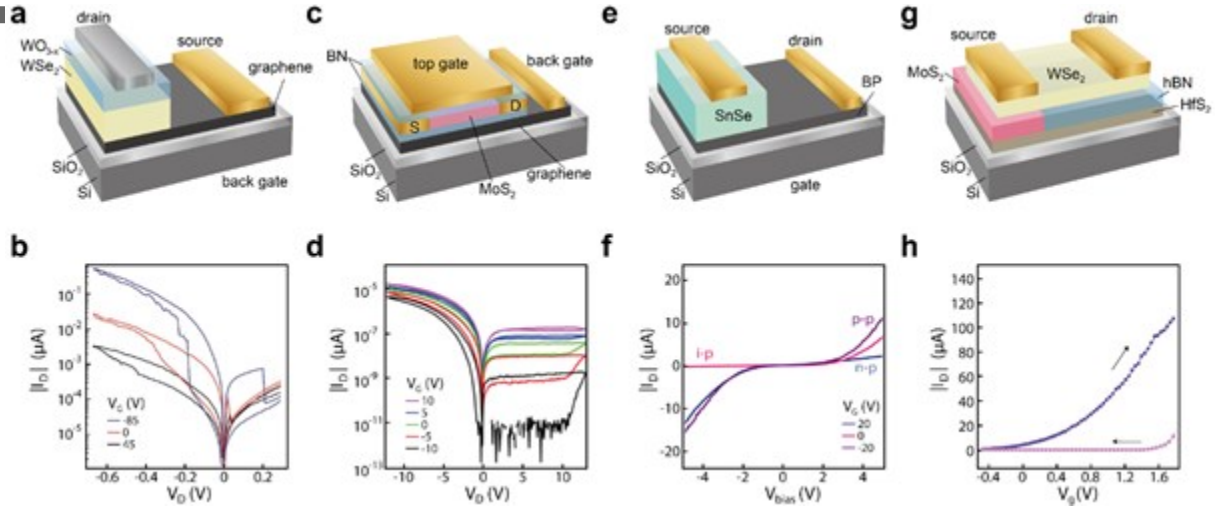

Figure 5. Device architectures and I-V characteristics of van der Waals heterojunction memtransistors and related devices. (a-b) WO_{3-x}/WSe_2/graphene synaptic barristor (top) showing gate tunable memristive characteristics (bottom) based on Schottky barrier modulation. Adapted with permission.[150] Copyright 2018, Wiley. (c-d) Schematic of a MoS_2/hBN van der Waals heterojunction (top) that shows bottom gate-tunable I_D-V_D characteristics (bottom) of a memtransistor. An additional top floating gate was used to strongly modulate the switching behavior to achieve heterosynaptic functionality. Adapted with permission.[156] Copyright 2020, American Chemical Society. (e-f) Schematic (top) and I-V characteristics (bottom) of a bottom-gated BP-SnSe heterojunction artificial synapse. The heterojunction can be reconfigured between p-p, i-p, and n-p junctions based on the gate voltage bias, allowing for a highly tunable synaptic response. Adapted with permission.[155] Copyright 2017, American Chemical Society. (g-h) MoS_2 semi-floating-gate van der Waals memory device with ultrafast writing time (100 ns) and long refresh time (10 s), and transfer curves in the on (blue) and off (purple) states. Adapted with permission.[79] Copyright 2018, Springer Nature.

Table 1: Summary of Device Metrics for Demonstrated Memtransistor Devices

Channel Material	Dielectric Material	Proposed Mechanism	Operating Voltage (V)	Switching Ratio	Conductance States	Endurance	Retention (min)*	Switching Energy (J)	Speed (s)	Ref
MoS_2	SiO_2	Schottky	40	~100	>11	>500	>1500	$\sim 3\times10^{-9}$	10^{-3}	[117]
MoS_2,	Nb_2O_5/ Al_2O_3	Schottky	10	~40	>200	>200	>16	$\sim 6\times10^{-12}$	10^{-2}	[131]
MoS_2	Al_2O_3	Schottky	0.5	~5000	>100	>150	>800	$\sim 2\times10^{-14}$	10^{-2}	[130]
α-In_2Se_3	SiO_2	Ferroelectric	4	~100	2	>40	>15	$\sim 8\times10^{-7}$	4	[118]
α-In_2Se_3	SiO2	Ferroelectric	4	~5000	6	>1000	>3000	$\sim 8\times10^{-10}$	2	[137]
GaSe	SiO_2	Filamentary	1.5	~1000	2	>5000	>160	$\sim 1.5\times10^{-5}$	10^{-1}	[120]
$MAPbI_3$	Al_2O_3	Filamentary	5	~100	2	>1000	>160	$\sim 5\times10^{-9}$	10^{-2}	[141]
VO_2	$VSiO_x$/ SiO_2	Mott MIT	0.5	~3	>20	>6000	>500	$\sim 2\times10^{-13}$	3.5×10^{-8}	[119]
Pentacene	PVN/ SiO_2	Charge trapping	10	~5000	>50	N/A	>16	$\sim 4\times10^{-5}$	2×10^{-6}	[148]
Graphene/ WSe_2/WO_{3-x}	SiO_2	Schottky	1	~100	>30	>1000	>16	$\sim 10^{-10}$	10^{-2}	[150]
hBN/ graphene /MoS_2	SiO_2	Filamentary	8	~5000	10	>50	N/A	N/A	N/A	[154]
Graphene/ $ReSe_2$	SiO_2	Filamentary	4	~10000	>5	>250	>160	N/A	N/A	[152]
MoS_2	SiO_2	Charge trapping	12	~100	>30	>500	>16	7.3×10^{-15}	5×10^{-8}	[156]

**The listed retention times and endurance are experimentally demonstrated. Device retention times can be extrapolated from the experimental data, and are often significantly longer (~few years).*

4. Integration into Neuromorphic Circuits and Systems

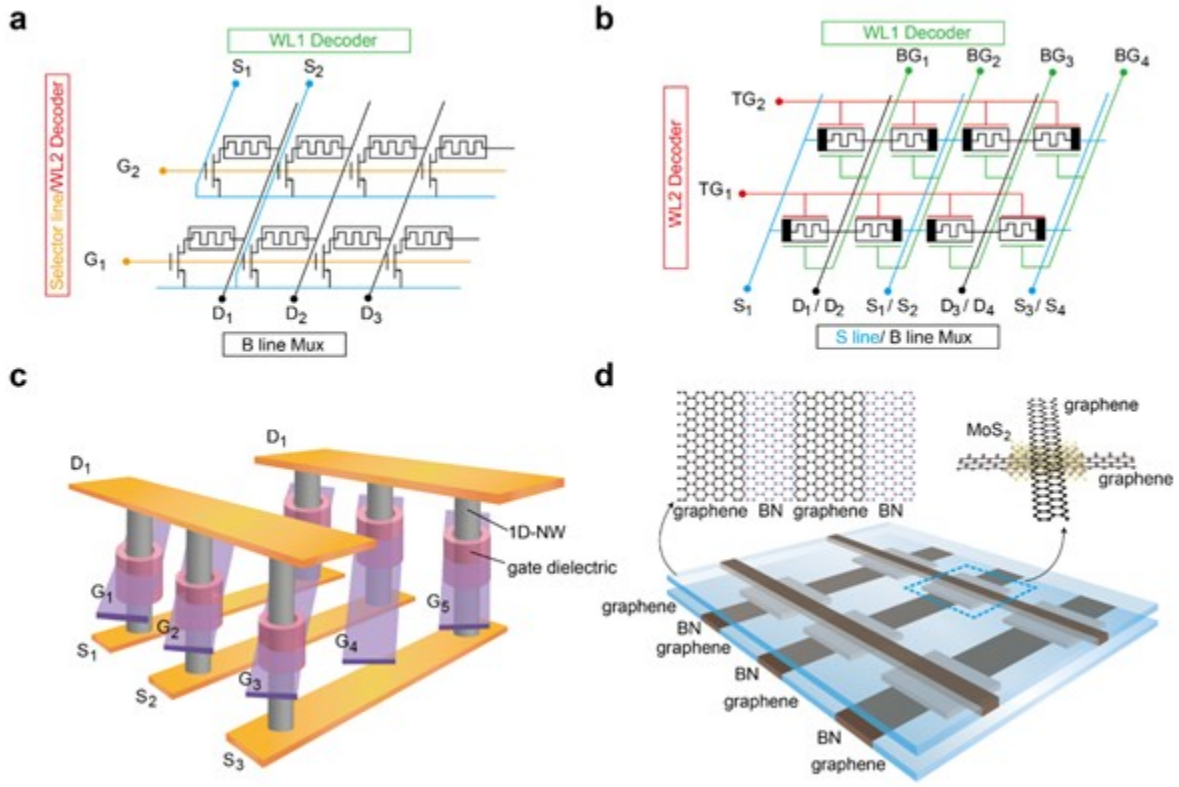

Figure 6. Crossbar integration strategies for memtransistors and related memristive systems. (a) Schematic of a traditional one-transistor-one-memristor (1T1M) crossbar array where a transistor at each node minimizes the sneak current between neighboring memristors. Reproduced with permission.[115] Copyright 2020, Wiley. (b) Schematic of the dual-gated memtransistor crossbar array where an additional transistor is not needed. Reproduced with permission.[115] Copyright 2020, Wiley. (c) Schematic of a proposed gate-all-around vertical nanowire memtransistor crossbar array. High device density with strong electrostatic control can be realized in this geometry. (d) Schematic of an all-2D graphene/MoS_2/graphene crossbar array using lateral stitching based on a bottom-up growth technique.

Two-terminal memristor-based crossbar arrays are widely employed for in-memory computing due to their small footprint, low power, and design simplicity.[58] The memristor crossbar paradigm has been explored extensively for neuromorphic computing algorithms that require high parallelism including vector-matrix multiplication for ANNs, SNNs, and CNNs.[40, 58] **Figure 6a** shows a typical crossbar array architecture using a 1T1M configuration, where the transistor serves as a switch to minimize the sneak current and crosstalk between neighboring memristors.[115] However, while the simplicity of two-terminal memristors is desirable for scaling reasons, it also results in certain intrinsic limitations. In particular, when using passive NVM in crossbar arrays, each node needs to be individually addressed to minimize the crosstalk and sneak-path current between the neighboring nodes during the read and write operations.[157] Typically, this addressability constraint requires an additional electrical component at each node. For example, in the one-selector-one-memristor (1S1M) design, the selector is a diode, a threshold switch, or an intrinsic Schottky barrier built within the memristor.[59, 158] However, the sneak current in the 1S1M scheme still scales with crossbar array size, and special biasing protocols are needed to access individual nodes. Alternatively, each node can be integrated with a transistor[77] in a one-transistor-one-memristor (1T1M) design, resulting in a reduced sneak current that is determined by the off-current of the transistor.[159] Overall, 1T1M designs lead to increased footprint and complexity due to the integration of two disparate technologies.

Compared to memristors, memtransistors possess an intrinsic selector, but the additional terminals also present integration challenges. Some early efforts have already begun to integrate memtransistors into crossbar arrays at the hardware level. For example, Lee *et al.* demonstrated a 10 x 9 crossbar array (Figure 6b) using dual-gated four-terminal MoS_2 memtransistors as a synaptic element, where a symmetric and linear weight update rule was achieved by gate-tunable learning.[115] Dual gating also allows two desired functions simultaneously: (1) sneak current suppression using one of the gates in a manner similar to the 1T1M architecture; (2) gradual tuning

of the long-term potentiation behavior by the second gate. This control of synaptic learning enables *in-situ* modification of weight update rules during training in dynamical neural networks. In addition, while a large Schottky barrier in memtransistors in the sub-threshold regime enables a wide dynamic range of synaptic learning,[115] a small Schottky barrier makes the resistive switching direction more sensitive to the gate voltage bias. This latter principle was utilized by Yuan *et al.* for memtransistors using MoS_2 grown by chemical vapor deposition on sapphire substrates. In this case, tuning the gate voltage allowed for switching between LTP and LTD responses without changing the polarity of drain bias pulses in a manner that is analogous to biological systems. The shapes of the LTP and LTD learning curves were further varied from sub-linear to super-linear curves by using time-varying pulsing schemes, thus enabling the SNNs to demonstrate continuous learning.[160] Feng *et al.* have also demonstrated a single-gated 10 x 10 memtransistor crossbar array for ANN applications while achieving a record switching energy (20 fJ/bit) and operating voltage (0.42 V) through careful grain boundary engineering and device scaling.[130] Their architecture uses a shared-drain (bit line) layout to achieve a cell size of 4.5 F^2 ($F = 4\lambda$ = minimum half-pitch), which compares favorably to 1M (4 F^2) and 1T1M (7 F^2) structures. These authors further hypothesized that the use of an overlapping source line could further reduce the cell footprint to 3 F^2. While memtransistor crossbars have thus far been limited to small-scale demonstrations, these proof-of-concept studies suggest that there are no fundamental barriers to wafer-scale implementation.

Novel crossbar array architectures also hold promise for realizing the scalable integration of memtransistors. Figure 6c shows a crossbar array composed of one-dimensional (1D) memtransistors that consists of etched mesas of bulk memristive materials, or organic/inorganic nanowires. GAA structures in 1D and vertical memtransistors are advantageous over other gating schemes because the strong electrostatic control of the 1D channel results in high current densities. The vertical orientation also allows for overlapping word/bit and selector lines, further improving lateral scalability. Figure 6d shows another potential crossbar array, this time realized using 2D

materials that are grown and integrated via a bottom-up approach. Recently, different combinations of 2D materials including semiconductors, insulators, and semimetals have been grown and stitched together either with covalent bonds or by using overlapping van der Waals gaps in the lateral plane.[161-164] With the small lattice mismatch between hBN and graphene (1.7%), purely 2D lateral growth of hBN-graphene heterostructures has also been reported,[165-168] which could potentially enable all-2D integrated memtransistors. In this scheme, a "stripe-by-stripe" hBN-graphene superlattice would serve as the contact layer for a crossbar array based on 2D materials. The switching layer consists of an array of the 2D mesa, which can be precisely patterned from a single monolayer 2D sheet. An all-2D crossbar array of memtransistors built with bottom-up growth and transfer techniques has the potential to incorporate both vertical and lateral heterostructures while providing ultimate scalability.

These all-2D arrays are of high interest due to their many desirable properties, including atomic thickness, pristine interfaces, high in-plane thermal conductivity, and a wide range of controllable bandgaps. These properties make them ideal candidates for building three-dimensional (3D) circuits.[169] For 3D integration, mobility degradation restricts the vertical scaling limit of bulk channel materials such as Si and GaN, whereas 2D materials retain high mobilities at ultra-thin thicknesses.[169] 3D integration using stacked memory and computing has been explored for neuromorphic computing,[26] and memtransistors as crossbar elements in this context are particularly promising since 1T1M designs are difficult to scalably integrate in a 3D manner.[60] **Figure 7a** illustrates a schematic of this concept in which multiple computing and memory elements, including CMOS circuitry, FETs, memtransistor crossbar arrays, sensors, and photodetectors, can be stacked. Such 3D integrated circuits have been experimentally demonstrated by Shulaker *et al.* using CMOS devices, conventional memristors, and CNT thin-film transistor (TFT) sensors.[53] These circuit architectures take advantage of the high bandwidth and dense interconnections enabled by 3D integration to create a computing ecosystem that is capable of massive data collection, local data

storage, in-memory computing, analog-to-digital data conversion, and fast weight update speed. Figure 7b illustrates a stacking scheme using an all-2D memtransistor crossbar (Figure 6d) to form a 3D integrated circuit. Due to the high vertical integration density, stacking 2D material memtransistor crossbars has the potential to achieve exceptionally high overall integration density, which partly compensates for the inherently larger footprint of lateral memtransistors compared to vertical memristors. Besides achieving high device density, carefully tailored 3D designs can be used for other purposes such as networks with high interconnectivity. For example, Figure 7c shows a staircase-like stacking of conventional oxide memristors that is purposely designed for parallel kernel operations in a CNN that are too complex to be realized in simple crossbar arrays.[170] Since selection devices are challenging to integrate into 3D designs, this architecture relies on stacking mismatch to reduce the sneak current by minimizing the overlap of the shared electrodes among devices.

One issue with 3D integration is that high-density vertical interconnects not only increase perturbations in accessing individual nodes but also degrade the bandwidth and speed of data communication. To prevent these deleterious effects while maintaining a high density of memristive devices, Strukov *et al.*[171] demonstrated a CMOS and crossbar integrated 3D system (Figure 7d, left plot), where each device in a rotated crossbar array is uniquely connected to two vias (blue and red dots in the right plots of Figure 7d represent two vias from the lower and upper wire levels). The rotation of crossbars provides a multiplicative factor that allows the high-density crossbars to be addressed by CMOS circuitry built at a larger lithographic scale. A similar scheme can be used to stack layers of 2D memtransistors, enabling high bandwidth and low communication latency between memtransistor and CMOS platforms without sacrificing high device density.

Integrating memtransistors in three-dimensional (3D) circuits can also enable additional data communication channels in the vertical direction for feedback loops and control lines between

different layers of neural networks[53, 171]. For example, Shulaker *et al.* deposited thin inter-layer dielectrics followed by etching and filling to fabricate high-density metal interlayer vias (2 µm pitch) that connected CNT sensing and logic with an RRAM crossbar array. Similar high-density interconnects could be used in a memtransistor crossbar array for *in-situ* rewiring of the gate terminal. One possibility is to use the gate terminal to implement evolving synaptic connectivity patterns into the hardware so that both synaptic learning and neural connectivity can be tailored to realize desired neuromorphic functions. This strategy is analogous to the continuous topographic mapping architectures and recurrent loop architectures that are common in biological neural models such as the mammalian visual system.[172] In general, the addition of the gate terminal increases the number of state variables available without sacrificing the capability of 3D integration. Consequently, memtransistors are ideally suited for exploring hardware implementations of highly interconnected neural networks that underlie complex bio-realistic synaptic behavior.

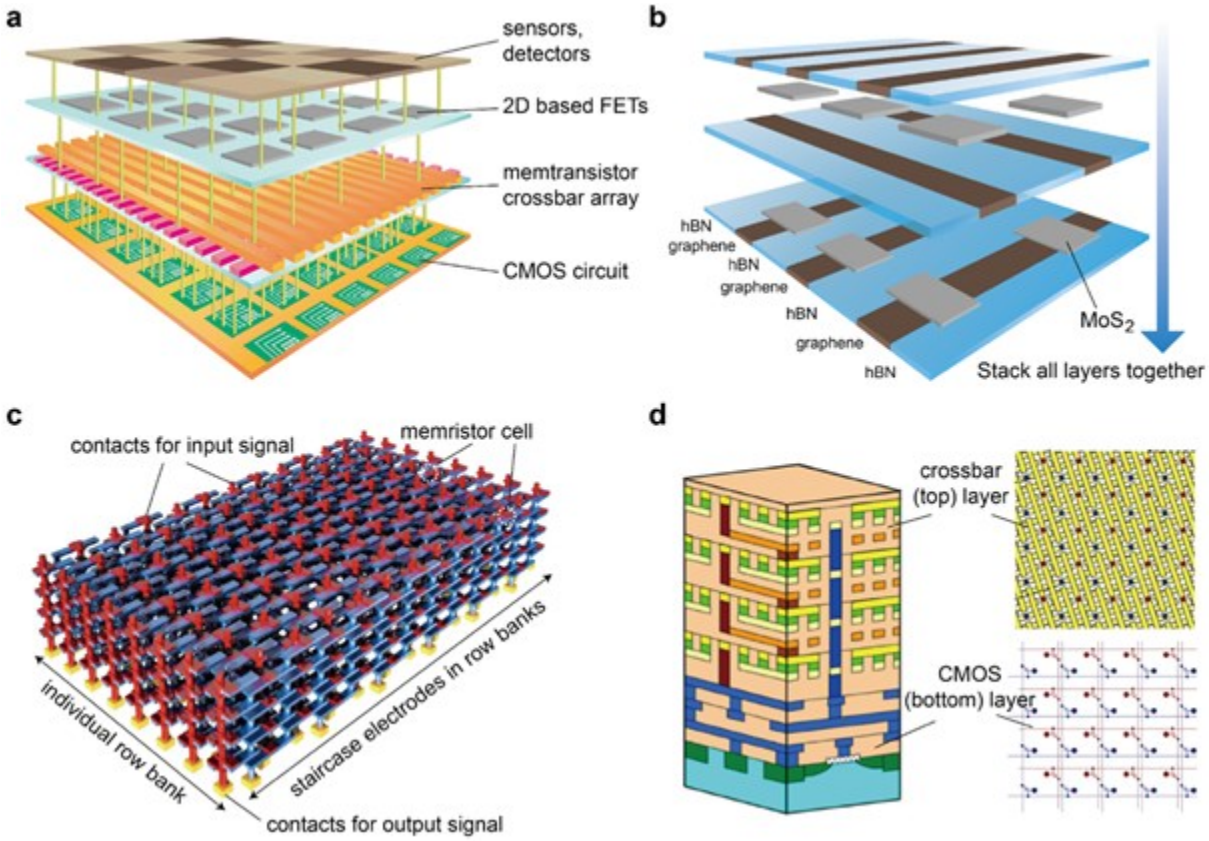

Figure 7. Three-dimensional integration strategies for memtransistors and related memristive systems. (a) Schematic of a proposed 3D integration of memtransistor crossbar arrays with other semiconductor technologies including sensors and CMOS digital circuits. Adapted with permission.[53] Copyright 2017, Springer Nature. (b) Schematic showing 3D stacking of an all-2D memtransistor crossbar array. (c) Schematic of 3D circuits composed of high-density staircase output electrodes (blue) and pillar input electrodes (red). Reproduced with permission.[170] Copyright 2020, Springer Nature. (d) Schematic of a 4D address topology for circuits with stacked multi-layer crossbar arrays. Reproduced with permission.[171] Copyright 2009, National Academy of Sciences.

5. Remaining Challenges and Future Outlook

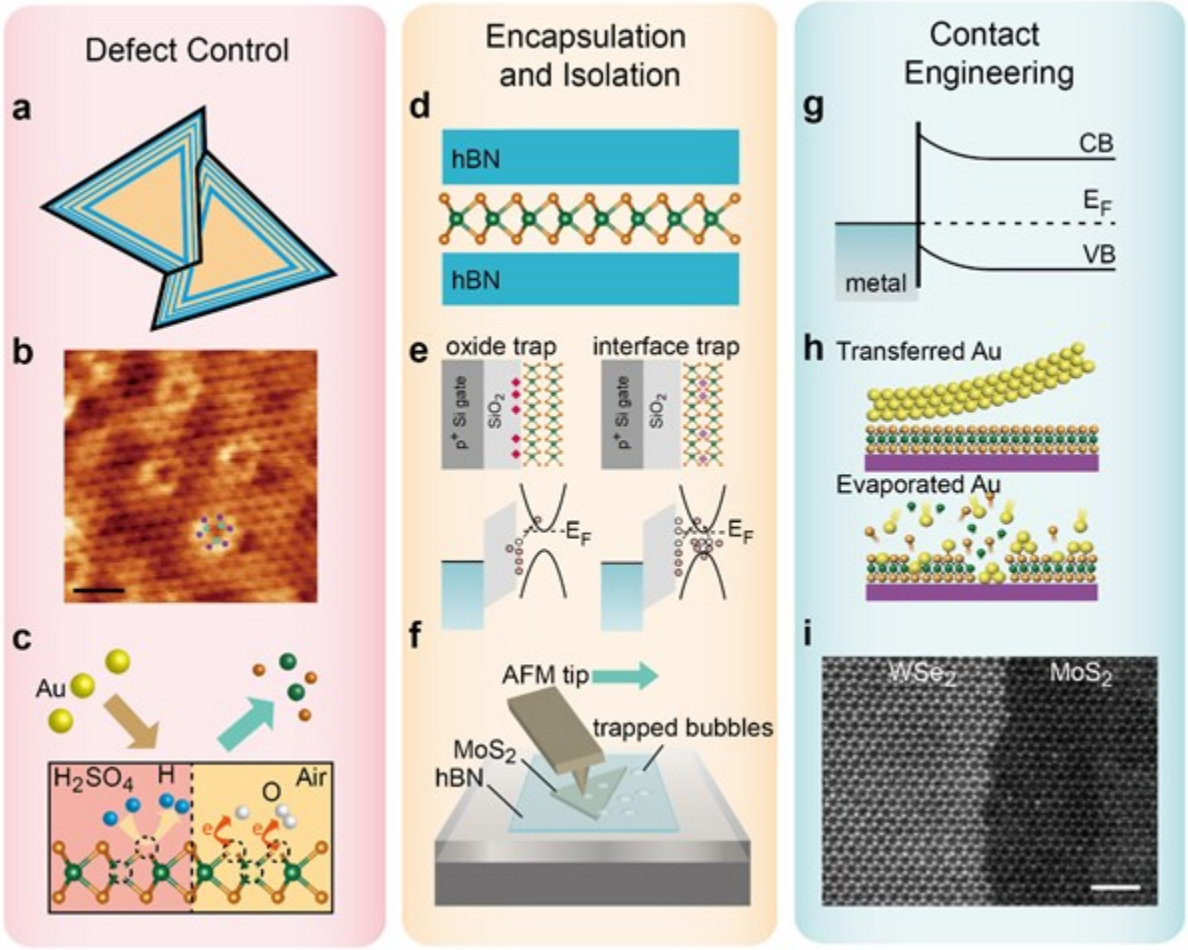

Figure 8. Remaining challenges and future outlook for memtransistors in neuromorphic circuits and systems. (a) Schematic showing grain boundary formation in monolayer MoS_2 during CVD. Reproduced with permission.[173] Copyright 2015, Wiley. (b) Scanning tunneling microscopy (STM) image of a single sulfur vacancy in monolayer MoS_2. The scale bar is 1 nm. Light blue dots represent Mo atoms and purple dots represent S atoms. Reproduced with permission.[174] Copyright 2020, Springer Nature. (c) Methods for defect engineering MoS_2 include ion irradiation, chemical modification, and annealing. Reproduced with permission.[175] Copyright 2018, American Chemical Society. (d) Schematic showing hBN encapsulation of monolayer MoS_2. Reproduced with permission.[176] Copyright 2019, American Chemical Society. (e) Charge trapping and other mechanisms of hysteretic memory in gated MoS_2 devices.[177] (f) Nano-Squeegee for forming clean van der Waals interfaces using contact-mode atomic force microscopy. Adapted with permission.[178] Copyright 2018, American Chemical Society. (g) Schematic showing the Schottky barrier formation between metal electrodes and semiconductors with memristive properties.[179] (h) Schematic of transferred versus evaporated contacts for 2D materials showing pristine atomic surface and degraded surface, respectively. Reproduced with permission.[180] Copyright 2018, Springer Nature. (i) Schematic showing the lateral stitching growth for a lateral WSe_2-MoS_2 heterojunction. A single 2D layer with metallic and semiconducting materials stitched together may allow greater electrostatic control of the tunable Schottky barrier in dual-gated architectures. Reproduced with permission.[161] Copyright 2015, American Association for the Advancement of Science.

In this Perspective, recent progress has been surveyed for memtransistors as building blocks for neuromorphic hardware applications. In addition, related devices with tunable NVM states were delineated including floating-gate memristive systems and phase-change devices. For synaptic applications, high endurance and retention are required due to repeated readout during inference.

Large dynamic ranges with low noise and fast switching speeds are necessary due to the large number of weight updates performed during training. A large dynamic range is also beneficial for achieving a large number of continuous, multi-level states, and for reducing the effect of device-to-device variability and noise. Power consumed during each weight update step is another critical parameter. In particular, lower operating voltages and write times during the weight update and low readout currents during inference are desirable to minimize energy consumption. Furthermore, especially for non-filamentary devices, tradeoffs exist between the programming voltage and other performance metrics (e.g., higher voltage enables a larger dynamic range and faster switching speed) that can be tailored specifically to desired applications. While neural networks are fairly robust against variation due to the large number of connections present, excessive stochasticity will lead to degraded network performance, thus motivating efforts to improve device-to-device uniformity. Although the existing literature on memtransistors is still largely in the exploratory phase, initial reports on disparate materials systems including polycrystalline monolayers, ferroelectric α-InSe, Mott materials, van der Waals heterojunctions, and Schottky-barrier-based 2D memtransistors have already shown significant improvements in key performance metrics. In particular, for Schottky-barrier-dependent MoS_2 memtransistors, scaling down channel lengths and using high-k dielectrics resulted in significantly improved device operating voltage and switching ratio.[130] Detailed characterization and optimization of these memtransistor systems will help further understand and improve device metrics and uniformity.

Advances in 2D material growth and defect control will facilitate the implementation of memtransistors into wafer-scale architectures. Early MoS_2 memtransistors have relied on randomly oriented grain boundaries, which presents challenges for device scaling. While the majority of existing growth efforts have focused on wafer-scale growth of 2D materials with large grain sizes for traditional electronics and optoelectronics, memtransistors that exploit grain boundaries[173, 181, 182] and sub-stoichiometric defects[174, 175] necessitate growth efforts specifically designed to achieve

smaller and uniform grain sizes with controlled stoichiometry (**Figure 8a-c**). Computational modeling and *in-situ* atomically resolved microscopy of defect dynamics under applied electric fields will also facilitate a better understanding of memtransistor switching mechanisms.[183] Studies on helium-beam-modified MoS_2 memtransistors, [184] plasma-treated MoS_2 memtransistors,[185] and air-treated GaSe memtransistors[120] suggest that post-growth defect engineering is also a promising avenue for exploration. Data-driven approaches such as machine learning[186, 187] are also likely to aid in the identification of optimal stoichiometries, defect densities, and electrical contacts for high-performance memtransistors. Additionally, ongoing research on the direct growth of lateral van der Waals heterostructures will be highly beneficial for realizing 2D heterojunction-based memtransistors.[161, 165, 188, 189] Finally, exploring alternative low-cost synthesis methods based on solution processing, such as MoS_2 percolating networks[190] and printed lead halide perovskite memtransistors,[142] may be useful for biosensing and wearable electronics. Liquid phase exfoliation of layered materials is also showing promise for spiking neuron applications due to the intrinsic volatile switching behavior originating from thermally activated electrical discharge due to the large curvature at the edges of 2D nanosheets.[191] This low voltage (~2 V) switching has been observed in a diverse range of 2D materials (e.g., MoS_2, WS_2, $ReSe_2$, and InSe) prepared in multiple solvent systems, thus paving a way for additive manufacturing of memristive systems.

In resistive switching devices, multiple competing and interacting memory mechanisms are often at play, and this issue is further compounded in memtransistors due to the complexity introduced by additional gate terminals and dielectric interfaces.[177] Therefore, an improved understanding of switching behavior is needed through *in-situ* analyses, simulations, and device modeling.[192, 193] At the device level, encapsulation layers,[176] interface control,[178, 194] and heterostructure assembly[195] are particularly useful methods to control the properties of all-surface 2D materials and to engineer heterojunctions (Figure 8d-f). In memtransistors involving Schottky barrier modulation, contact engineering and van der Waals heterojunction formation are also

promising for achieving desired behavior, but have yet to be fully explored (Figure 8g-i**)**.[179, 196-200] For 2D materials specifically, emerging schemes of transferred contacts,[180, 201] edge contacts,[202, 203] and ion-permeable contacts[204] can further be explored to enable improved control. Additionally, the use of tunnel barriers and interfacial layers with well-defined charge trapping states can yield gate-controlled Schottky barriers that underlie memtransistor characteristics. Lastly, electric-field-induced or ion-induced phase transitions in 2D materials, such as MoS_2[132, 205] and $MoTe_2$,[206-208] in addition to moiré ferroelectricity in 2D material heterostructures[209] are of potential interest as alternative memtransistor switching mechanisms.

Memtransistors also present key challenges and opportunities at the circuit and software levels. High-yield integration of 2D materials with existing fabrication technology remains an ongoing challenge. Additionally, while extensive research has been conducted on the design and protocols for large-scale memristor-based crossbar arrays,[58, 159] memtransistors have been limited to a few small-scale demonstrations. However, compared to conventional memristor circuit architectures like 1T1M crossbar arrays or four-terminal synaptic transistors, three-terminal memtransistors can be scalably incorporated into 3D architectures for ultra-high-density integration. Memtransistors can also be dual-gated, solving the long-standing issues of sneak current in memristor crossbar arrays, while simultaneously enabling tunable learning for dynamical neural networks. Another promising use of memtransistors is to emulate bio-realistic synapses through additional gate tuning,[116, 160] such as reconfigurable STDP behavior[52, 115, 130, 160] for improved SNN learning.[210, 211] Incorporation of long-term memory at the memtransistor gate terminal through ferroelectric dielectrics or charge trapping is also a possibility and would provide a second layer of nonvolatile memory that is independent of the memristive behavior. In general, realizing the full potential of memtransistors for network-level applications will require the exploration of concepts that take full advantage of the high tunability at the device level, such as using multiple state variables for reinforcement learning[36] or using gate-terminal tuning to mitigate device variability effects. Ultimately, the diverse

set of potential functionalities in multi-terminal memtransistors, including independently expressed long-term and short-term plasticity,[212, 213] heterosynaptic functionality,[117, 137], and neuromodulation,[116] has the potential to drive neuromorphic computing hardware toward increasing levels of bio-realism that represent the next frontier of artificial intelligence.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Author Contributions

X.Y. and J.H.Q. contributed equally to this work. All authors wrote the manuscript and discussed the results at all stages.

Conflict of Interest

The authors declare no conflict of interest.

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Table of Contents Entry

Recent progress and ongoing challenges for memtransistors are reviewed in the context of neuromorphic computing in solid-state circuits and systems. Gate-tunable learning and bio-realistic functions in multi-terminal synaptic devices are compared for memtransistors and related floating gate and ferroelectric memories, suggesting opportunities for new architectures that are suitable as hardware accelerators for artificial intelligence algorithms.

Keywords: memristors; gate-tunable; non-volatile memory; van der Waals materials; artificial intelligence

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Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems

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Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems

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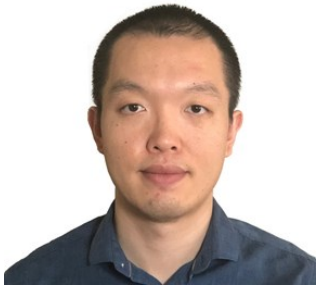

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