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ABSTRACT

We report an N_2 based annealing treatment to passivate interface traps (D_{it}) in n- and p-type 4H-SiC. The process has the potential to replace the commonly used hazardous and expensive gas nitric oxide (NO). N_2 postoxidation annealing reduces D_{it} in both the upper and lower halves of the 4H-SiC bandgap, with a greater impact at the valence band edge. N_2 annealing at 1500 °C is observed to be more effective in passivating traps and positive fixed charges than NO annealing for p-type devices, whereas for n-type devices, the opposite is true. The breakdown voltages for these devices are found to be lower than that of NO annealed devices. X-ray photoelectron spectroscopy has been performed to estimate the nitrogen areal density at the interface. D_{it} is measured as a function of nitrogen areal densities in the near interfacial regions for the different processes. Theoretical analysis through density functional theory is consistent with the measured D_{it} profiles by showing the generation of additional states near the valence band edge due to increased nitrogen concentration. In addition to reporting the effect of N_2 annealing on both n- and p-type 4H-SiC, this work correlates the nitrogen areal densities at the interface to the D_{it} and explains the difference in D_{it} characteristics with nitrogen areal density between n- and p-type interfaces.

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I. INTRODUCTION

Silicon carbide (4H-SiC) is one of the leading wide bandgap semiconductors for high-power, high-temperature applications.[1] Compared to silicon, 4H-SiC metal–oxide–semiconductor field effect transistors (MOSFETs) have much lower power dissipation, making them ideal for low-noise and high-efficiency all-electric vehicle drives, fast-charging stations, solar inverters, and much more. While these devices significantly improve the energy efficiency of next-generation power systems, 4H-SiC also offers additional functionality in the form of integrated circuits (ICs) at high temperatures (>300 °C). Lateral complementary metal–oxide–semiconductor (CMOS) IC technology in 4H-SiC is highly desired for large-scale integration due to its strong noise immunity and low static power consumption.[2] Both n- and p-channel MOSFETs that can operate at high temperatures are required for this technology. Nevertheless, despite significant advances, the high density of interface states (D_{it}) at the 4H-SiC/SiO_2 interface inhibits 4H-SiC MOSFETs from realizing their full potential, by causing high channel resistance and low mobility.

Extensive gate passivation research has been conducted over the last decade to passivate D_{it} in 4H-SiC.[3–13] Some passivation methods such as wet oxidations[14] were only effective in reducing traps near the valence band edge (E_V), but not effective for passivating traps near the conduction band edge (E_C). Out of all passivation methods, postoxidation annealing in nitric oxide (NO) at high temperature turned out to be the most effective and the standard process for reducing D_{it} both near E_C and E_V.[12,15,16] However, the disadvantages of using NO annealing, both economically and environmentally, cannot be ignored. Furthermore, NO annealing is known to cause threshold voltage instability[17] and create oxide hole trapping[6] in 4H-SiC MOSFETs. To find alternative solutions for toxic and expensive NO, earlier research,[5] and more recently, Tachiki and Kimoto[18] demonstrated that high temperature (1400–1600 °C) annealing in flowing nitrogen gas produces promising results for 4H-SiC MOSFET processing.

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In particular, that work shows that nitrogen annealing provides a higher reduction of D_{it} near E_V as compared to D_{it} passivation near E_C.

We report physical measurements that correlate the nitrogen areal density of the near interfacial regions with D_{it} and try to explain the difference in D_{it} characteristics for the n- and p-type 4H-SiC/SiO_2 interfaces. For this purpose, postoxidation annealing at high temperature (1400–1500 °C) in flowing N_2 gas is conducted and D_{it} measurements are reported in comparison to NO. Nitrogen annealing is found to be more effective than NO annealing in reducing D_{it} near the valence band, while the opposite is true close to the conduction band edge, which is consistent with Ref. 18. N_2 also decreases the positive fixed charge at the interface of p-type 4H-SiC and SiO_2, as evidenced by the flatband voltage comparison between processes. The oxide breakdown voltage for the devices made with 1500 °C N_2 annealing was similar to that of NO annealed devices. Critical to this study are (1) the comparison of x-ray photoelectron spectroscopy (XPS) measurements of the actual areal density of nitrogen at the interface for different annealing processes and (2) density functional theory (DFT) calculations that show the generation of additional energy states near E_V due to higher nitrogen concentration.

II. EXPERIMENTS AND METHODS

In this work, metal–oxide–semiconductor (MOS) capacitors were fabricated on p-(N_A–$N_D = 6.2 \times 10^{15}$ cm^{-3}) and n-type (N_D–$N_A = 2.0 \times 10^{16}$ cm^{-3}) epitaxial layers on 4° off-axis (0001) Si-face oriented p- and n-type substrates, respectively. The oxide is grown thermally in a dry atmosphere at 1150 °C, at flowing oxygen

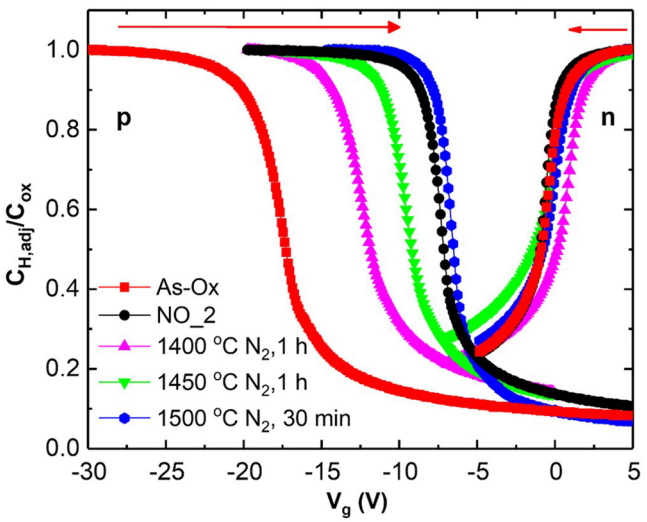

FIG. 1. High frequency CV curves for p- and n-type MOS capacitors for different processes. Interface state passivation and fixed charge reduction are associated with N_2 annealing for both p- and n-type capacitors, lowering the flatband voltages as a result. The oxide thickness ranges from ∼65 to 70 nm and for p-type 4H-SiC and ∼55 to 60 nm and for n-type 4H-SiC. The capacitors have a circular shape with a diameter of 500 μm.

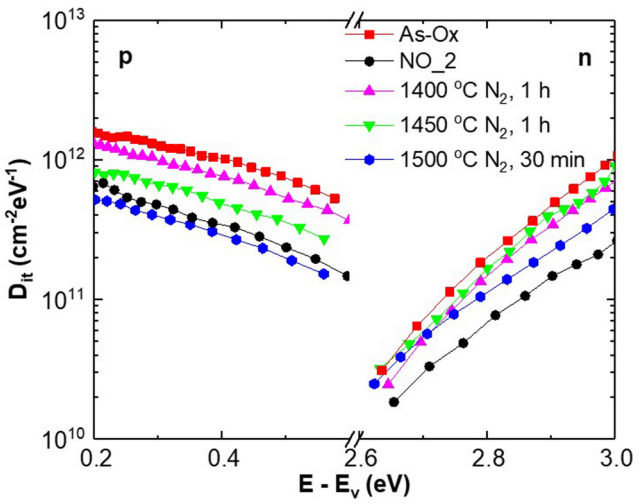

FIG. 2. Shallow D_{it} profiles of p- and n-type MOS capacitors extracted from simultaneous high frequency (100 kHz)-low-frequency CV measurements. As-Ox represents oxidation at 1150 °C without any POA, and NO_2 represents oxidation at 1150 °C and POA at 1175 °C NO for 2 h. 1500 °C, 30 min N_2 POA passivates more traps near the valence band edge (E_V) than NO annealed devices. The opposite is true near the conduction band edge (E_C).

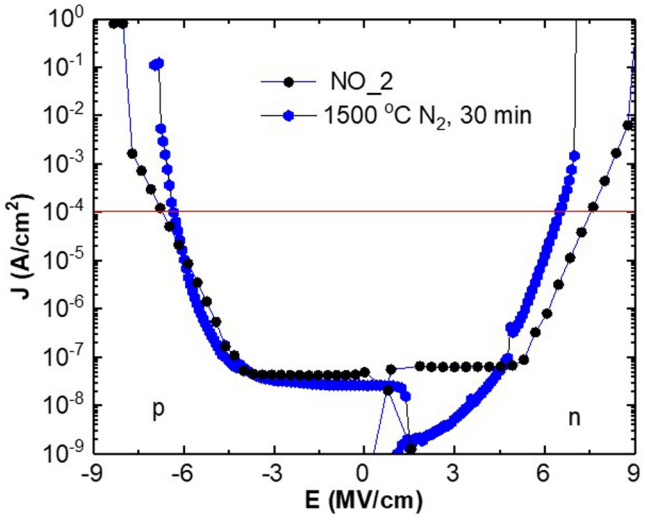

FIG. 3. Current density (J)–electric field (E) characteristics of the devices made with 1500 °C, 30 min N_2 POA and compared to 1175 °C, 2 h NO annealed devices. Horizontal red line denotes the breakdown current density of 10^{-4} A/cm^2. Both p- and n-type capacitors have a comparable breakdown field with NO annealed devices. The thickness for p-type capacitors is ranging from ∼65 to 70 nm and that for n-type ones is ∼55–60 nm and with a circular gate diameter of 500 μm.

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gas at a rate of 500 SCCM, and some samples were subsequently subjected to postoxidation annealing (POA) for comparative studies of D_{it}. The thicknesses of the gate oxides for the n- and p-type capacitors were found to be ~55 and ~65 nm, respectively, by the capacitance–voltage (CV) method. The various samples are labeled according to the process as follows. "As-Ox" represents a sample without any POA. Samples called "NO_2" were annealed in nitric oxide (NO) at 1175 °C for 2 h with a flow rate of 500 SCCM. For high-temperature N_2 annealing, selected oxidized samples were annealed in flowing ~99.99% N_2 at high temperatures (1400 °C, 1 h; 1450 °C, 1 h; and 1500 °C, 30 min or 1 h) at a flow rate of 3000 SCCM in a ceramic furnace. It is seen to increase the oxide thickness by ~5 nm after N_2 annealing. After POA, ~50 nm thick aluminum (Al) was evaporated on top of the samples to form gate metal on all the capacitors. Simultaneous high frequency (100 kHz)–low-frequency CV (HI-LO CV) measurement was performed to extract interface trap densities (D_{it}) for each process and compared at room temperature (27 °C) with reference to 1175 °C, 2 h NO annealing.

For XPS measurements, the SiO_2 dielectric layer was removed using buffered oxide etchant (BOE) 6:1 (6 parts by volume of 40% ammonium fluoride and 1 part by volume of 49% hydrofluoric acid, Sigma-Aldrich). Earlier measurements have shown that the buffered oxide etch does not remove interfacial nitrogen within the accuracy of the elemental probes, ~10%. The XPS measurements were carried out using a monochromatic Al Kα x-ray source (K-Alpha, Thermo Scientific Inc.) with a flood gun for charge compensation. Spectra were calibrated against C1s from SiC (283.4 eV). During measurements, x rays with a spot size of 200 μm were focused on each sample and the normal direction of the sample surfaces was pointed to the analyzer.

III. RESULTS AND DISCUSSION

A. Electrical analysis

High frequency (100 kHz) CV curves are obtained for capacitors using different methods. Figure 1 shows the results for n- and p-type capacitors under different N_2 annealing conditions, compared with "As-ox" and "NO_2." For p-type capacitors, the CV curves clearly move to the right with the increase in the N_2 annealing temperature, reducing the flatband voltage due to the passivation of deep interface states and fixed charges. For 1500 °C

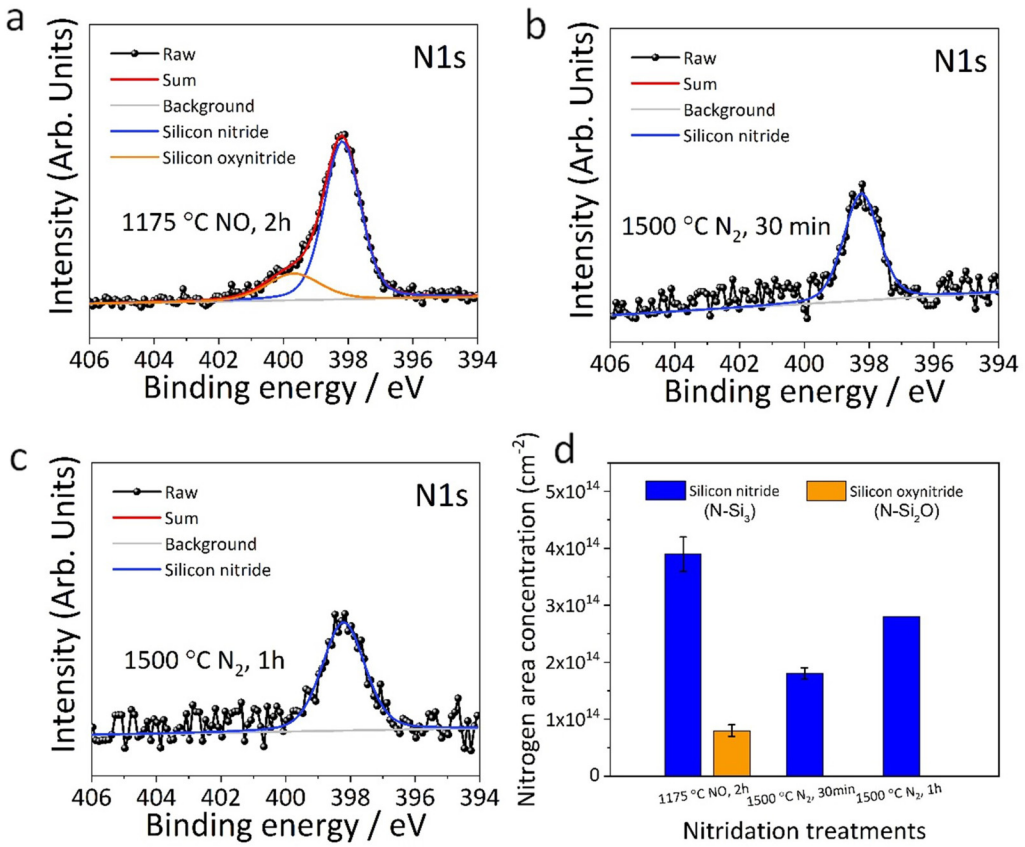

FIG. 4. (a)–(c) N1s spectra of BOE-etched SiO_2/SiC MOS structures after nitridation treatments including 1175 °C, 2h NO POA, 1500 °C, 30 min N_2 POA, and 1500 °C, 1 h N_2 POA, respectively, and (d) the corresponding nitrogen area concentrations.

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TABLE I. XPS measurement data showing the amount of nitrogen at the interface for different processes.

Nitridation conditions	N1s binding energy of silicon nitride ($N\text{-}Si_3$) (eV)	N1s binding energy of silicon oxynitride ($N\text{-}Si_2O$) (eV)	N area concentration of silicon nitride ($N\text{-}Si_3$) (10^{14} cm^{-2})	N area concentration of silicon oxynitride ($N\text{-}Si_2O$) (10^{14} cm^{-2})
1175 °C, 2 h NO	398.2	399.7	3.9 ± 0.3	0.8 ± 0.1
1500 °C, 30 min N_2	398.2	…	1.8 ± 0.1	…
1500 °C, 1 h N_2	398.2	…	2.8 ± 0.1	…

annealing, the flatband voltage for p-type becomes less than NO annealing, which is definitely advantageous. On the other hand, with the increase in the annealing temperature, CV curves in n-type devices move slightly left and the 1500 °C process yields a similar flatband voltage as NO_2. Hysteresis increased with annealing temperature. Depending on the processes, the value of ΔV_{fb} (difference in flatband voltage) ranges from 0.2 to 0.7 V between the opposite directional CV sweeps.

Using simultaneous HI-LO CV measurements, shallow D_{it} profiles were extracted for states near the valence (E_V) and conduction band (E_C) edges as shown in Fig. 2. For p-type capacitors, a consecutive reduction in D_{it} is visible with the increase in the N_2 annealing temperature, which is consistent with the decrease in V_{fb}. Among all the processes, 1500 °C, 30 min N_2 yielded the minimum D_{it} value close to Ev. A lower D_{it} using N_2 annealing could be a combined effect of higher temperature and lower nitrogen concentration at the p-type interface. However, for n-type capacitors, D_{it} near Ec was lower for NO annealing compared to N_2, which is consistent with Ref. 18.

Current–voltage (I–V) characteristics were obtained to find the breakdown voltage of the capacitors fabricated with 1500 °C, 30 min N_2 annealing and were compared with the 2 h NO annealed samples as shown in Fig. 3. For both n- and p-type capacitors, the breakdown voltage was found to be lower than that of the NO annealed samples. The lower breakdown in the N_2 curves might be due to the possible crystallization at higher temperatures. High-temperature N_2 annealing, indeed, made the surface rougher as seen from AFM. For N_2 annealed samples, the rms roughness is seen to be ~2.6 nm, whereas for samples without annealing, the roughness is ~1 nm. The value of the conduction band offset (barrier height) of the n-type capacitors is calculated, using Fowler–Nordheim tunneling, to be 2.42 and 2.26 eV for NO and N_2 annealed capacitors, respectively, using the effective mass of electrons in oxide (m_{ox}) 0.35 m, whereas for p-type capacitors, they are found to be 2.1 and 2.9 eV taking m_{ox} for holes as 0.4 m. Here, m is the electrons' rest mass in vacuum.

B. XPS analysis

To understand the interfacial chemistry of the high-temperature N_2 annealed samples, x-ray photoelectron spectroscopy (XPS) was performed and compared with NO annealed samples. Figure 4 shows the N1s XPS spectra and the corresponding N areal density calculated using the method in Ref. 19 as shown in Table I. XPS measurement data show the amount of nitrogen at the interface for different processes. Both NO POA at 1175 °C and N_2 POA at 1500 °C gave rise to the formation of silicon nitride ($N\text{-}Si_3$ configuration) as indicated by N1s peaks at 398.2 eV (blue peaks), while

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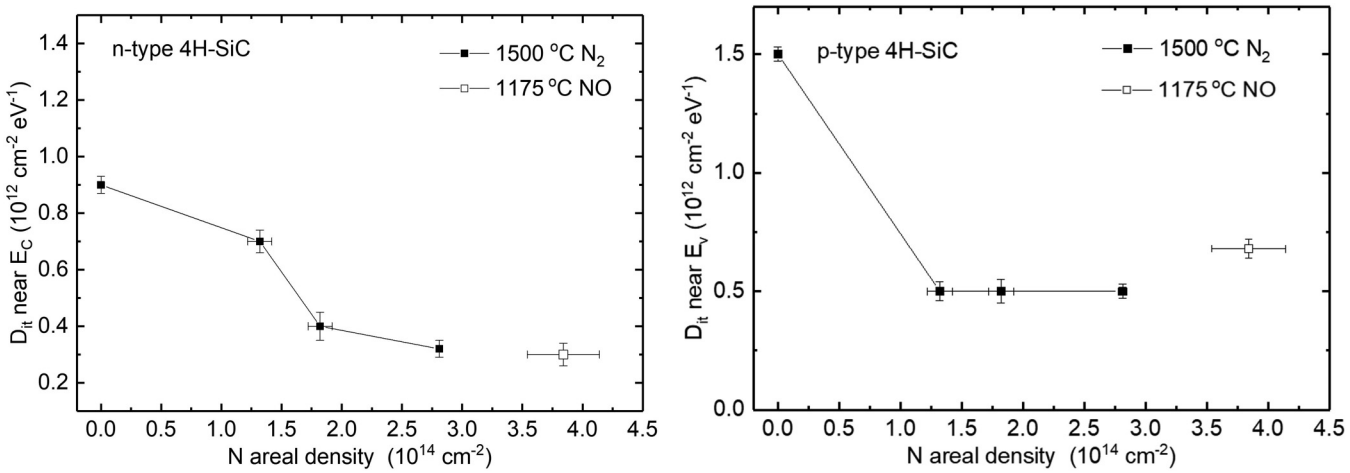

FIG. 5. D_{it} near the conduction (left) and valence (right) band edge vs nitrogen concentration at the interface. Here, the 1400 °C N_2 annealed sample is assumed to be the zero-nitrogen point, because the concentration of nitrogen at the interface for this sample is well below the XPS detection limit (<10^{13} cm^{-2}).

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the NO process also resulted in the formation of silicon oxynitride (N-Si_2O configuration) as indicated by the N1s peak at 399.7 eV (orange peak).[20] The total N area density due to NO POA is ~4.0×10^{14} cm^{-2}, which is consistent with Ref. 19. The N areal density increased with further N_2 POA at 1500 °C and reached 2.8×10^{14} cm^{-2} at 1 h, which is ~40% lower than that resulting from NO POA. Combined with the D_{it} results in Fig. 5, we can conclude that N-uptake by either process effectively reduces the interface trap density for both n-type and p-type SiO_2/SiC devices. However, when the N areal density $\geq 1.8 \times 10^{14}$ cm^{-2}, there can be negative correlations between N-uptake and the interface trap density for p-type devices, as explained later.

C. D_{it} vs nitrogen at the interface

The values of D_{it} near the E_C (at 3.0 eV) and E_V (at 0.2 eV) are plotted with respect to the nitrogen amount at the oxide–semiconductor interface as shown in Fig. 5. Here, the 1400 °C N_2 annealed sample is assumed to be the zero-nitrogen point, because the concentration of nitrogen at the interface for this sample is well below the XPS detection limit. It can be noted that with the increase in nitrogen, the value of D_{it} near E_C reduces continuously and reaches near saturation at 3×10^{14} cm^{-2}, whereas for the p-type interface, at least 1×10^{14} cm^{-2} nitrogen density is required for the reduction in D_{it}. However, the value of D_{it} increases near E_V with the increased amount of nitrogen that can be seen from the 1175 °C NO point of the right-hand side of Fig. 5. The higher D_{it} with NO annealing compared to N_2 might be due to the effect of lower temperature annealing or associated with the additional generation of states near the valence band edge as suggested from the DFT calculations.

D. Theoretical analysis

To gain atomic level insight on the changes in the interfaces upon nitridation, we analyze the electronic properties of model systems using first principles calculations within the density functional theory (DFT). These systems correspond to nitrided 4H-SiC/SiO_2 interfaces that are perfectly coordinated (i.e., no dangling bonds), assuming the N-Si_3 configuration (where N binds to three Si atoms) previously found as prevalent in these systems.[21] Nitridation has been shown to remove interfacial traps by passivating the Si-dangling bonds emerging at the SiO_2/4H-SiC interface because of silicon density reduction when transitioning between the semiconductor and oxide.[22,23] Computational descriptions of these interfaces employed 3×3-unit cells of the 4H-SiC (0001) with different atomic arrangements near the interface, as illustrated in Fig. 6. Atomic cores are described with projector augmented wave (PAW) pseudopotentials, and exchange-correlation energy is parameterized by the Perdew–Burke–Ernzerhof (PBE) functional.[24,25] The self-consistent field was obtained through integration over the Brillouin zone in a $6 \times 6 \times 1$ Monkhorst-Pack k-point grid,[26] as well as energy cutoffs were set to 60 and 500 Ry for wave functions and charge density, respectively. Atomic positions in the model interface supercells were determined through a structural relaxation until forces were lower than 0.01 eV/Å before band structures were obtained, employing the Quantum Espresso software.[27]

Figure 6 shows the band structures near the valence band for interfaces with different nitrogen areal densities (1.3×10^{14}, 2.7×10^{14}, and 4.0×10^{14} cm^{-2}), comparable to those attained experimentally and nearly two orders of magnitude larger than

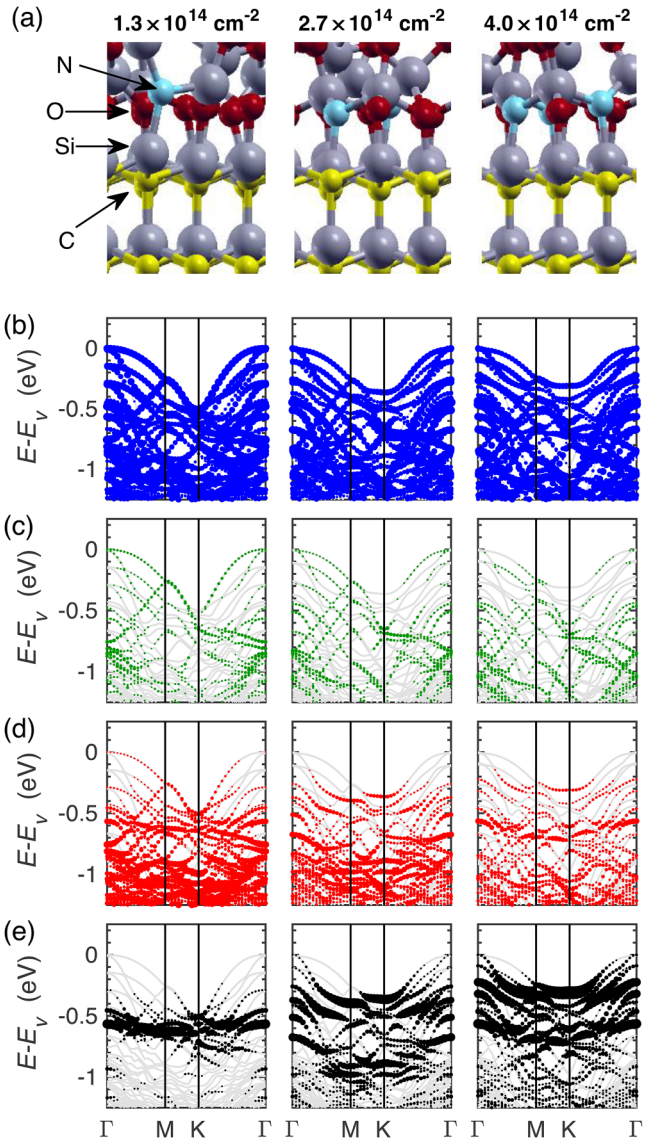

FIG. 6. Geometric and electronic structure of 4H-SiC/SiO_2 model interfaces with different nitrogen areal densities. (a) Geometric configuration of the different interfaces. Band structures (gray lines) near the valence band edge for these different interfacial models are presented with decomposition onto localized atomic orbitals denoted in color for the different elements of atoms near the interface: (b) carbon layer (blue); (c) top silicon layer in SiC (green); (d) oxygen states (red); and (e) nitrogen states (black) adjacent to the interface. Different columns denote the cases with different N areal densities (from left to right): 1.3×10^{14}, 2.7×10^{14}, and 4.0×10^{14} cm^{-2}.

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interface trap densities. To facilitate the comparison, Bloch states of the system (gray lines) are projected onto localized orbitals corresponding to atoms (C, Si, O, and N) residing near the interface. The results reveal the presence of states formed with nitrogen orbitals near the valence band edge. This feature, which is not observed near the conduction band edge (not shown here), is attributed to the lower electronegativity of nitrogen with respect to that of oxygen. Moreover, the energy position of these interface states moves closer to the band edge as the N areal density increases. Hence, these interface states originating from nitrogen may become active during device operation for p-type devices as nitridation levels reach their highest values.

These results suggest that nitridation may not be as beneficial for holes as it is for electrons because of the emergence of N-related interfacial states near the valence band edge. They also provide a qualitative explanation of the D_{it} uptick near the valence observed for the NO process (Fig. 5), as this yields a significantly higher N concentration. We note that model systems in this work focus on Si_3–N coordination; however, further atomistic studies may be needed to characterized other configurations (e.g., with different and less prevalent coordination of N such as Si_2–N–O or Si–N–O_2 or N-related defects) to assess the impact of nitridation on p-type devices.

IV. SUMMARY

The effect of high-temperature N_2 postoxidation annealing in 4H-SiC n- and p-type MOS interfaces is investigated. 1500 °C N_2 annealing substantially reduces the positive fixed charge and interface traps near the valence band edge to a greater extent than for NO annealing, whereas for the n-type structures, similar D_{it} levels are attained. The D_{it} vs N areal density (measured by XPS) for n-type interfaces shows that the D_{it} passivation requires at least $1.8 \times 10^{14}\,cm^{-2}$ nitrogen for substantial reduction and continues to decrease up to $\sim 4 \times 10^{14}\,cm^{-2}$ (the NO value). On the other hand, approximately $1.3 \times 10^{14}\,cm^{-2}$ nitrogen density shows a major reduction for the D_{it} reduction of the p-type interface, with essentially no further reduction at greater N incorporation. Our data show that while D_{it} in n-type structures is continuously reduced by increased nitridation, p-type ones exhibit an initial improvement, which degrades at $4 \times 10^{14}\,cm^{-2}$ concentration of N. This increase in D_{it} for p-type structures with a high N content is attributed to the formation of N-related states near the valence band as observed in first principles calculations. The results from this work show that while N_2 annealing yields D_{it} comparable to NO annealing, breakdown field degradation and the emergence of N-related states near the valence band edge may demand further studies toward the realization of p-type 4H-SiC devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Suman Das: Data curation (lead); Formal analysis (equal); Investigation (lead); Writing – original draft (lead). **Hengfei Gu:** Data curation (equal); Writing – original draft (equal). **Lu Wang:** Data curation (equal). **Ayayi Ahyi:** Project administration (equal); Writing – review & editing (equal). **Leonard C. Feldman:** Project administration (equal); Writing – review & editing (equal). **Eric Garfunkel:** Resources (equal). **Marcelo A. Kuroda:** Formal analysis (equal); Resources (equal); Software (lead); Writing – review & editing (equal). **Sarit Dhar:** Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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