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Detuned synchronized waveform averaging for reducing distortions due to sample interleaving

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Disclaimer

This work performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344.

Title

Detuned synchronized waveform averaging for reducing distortions due to sample interleaving

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Abstract of the Invention

This invention introduces a method for optimally detuning the ratio of analog-to-digital (ADC) sample rate and trigger rate during waveform averaging to minimize the deleterious effects from sample interleaving. A prescription is described for determining the optimal detuning factor for the ADC or trigger rate in any scenario, depending on the number of ADC cores used and the limited tuning resolution of the clock rates for a specific implementation.

Uses of the Invention (List past uses, current uses and potential uses for your invention including LLNL, Government and Commercial Uses)

Pulse shaping, repetitive waveform characterization,

Potential Licensees (list keywords for appropriate companies to contact concerning your invention)

Test and measurement

Patent Search Terms (list keywords for an effective patent search)

Waveform Averaging, Analog-to-Digital Conversion, Sample Interleaving

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Technology Background and Description of Prior Art

Please describe the current state of the science, technology, and prior art related to your invention. In your description, please consider the following:

- What is the technical problem, challenge, or goal?
- What have others done to address the technical problem or achieve the goal? Please provide a few specific examples including references/citations.
- What are some of the disadvantages or limitations of the prior art?
- How does your invention overcome the limitations of the prior art?

High fidelity characterization of repetitive signals—with the goal of determining the common signal shared across multiple repeating waveforms—is critical for various applications, including telecommunications and optical pulse shaping. With digital waveform averaging, multiple digitized waveforms are temporally aligned, and the corresponding values from each waveform are averaged. This approach reduces the root mean square deviation of uncorrelated error as the square root of the number of averaged waveforms. The result is a high signal-to-noise ratio (SNR) measurement of the common waveform on the repetitive signal-under-test.

While digital waveform averaging is effective at reducing uncorrelated error, it cannot distinguish the common waveform of interest from correlated errors, i.e., noise and distortion that is common across all waveforms. One source of correlated error can arise in the digitization process itself as a result of non-idealities in the sample interleaving process used in high-speed analog-to-digital converters (ADCs). Sample interleaving is a widely used technique to achieve high-sample rate digitization by employing multiple sub-sample rate ADC cores in parallel. The ADC cores of sample interleaved ADCs synchronously sample the same input signal, but with the sampling clock of each core delayed, or phase shifted, with respect to each other. In this way, each core samples a unique point in time on the input signal, so that when the samples from each core are interleaved together, the result is a digitized signal with a higher effective sample rate. Though effective at achieving high sample rates, this interleaving technique also comes with some drawbacks. If mismatches in gain or offset exist between the ADC cores, or if the phase shifted sample times of each core do not fall at uniform sampling intervals, sample interleaving artifacts, or spurs, can arise, distorting the signal. When digitizing a repetitive signal-under-test, if the waveform repetition rate and the sample rate of the ADC are synchronized, these interleaving artifacts can become correlated across the repeating waveforms and will therefore not be mitigated by waveform averaging.

One method to avoid correlating the sample interleaving artifacts with the repeating waveforms is to run the ADC sample rate asynchronously with the waveform repetition rate. If the ADC and signal clocks randomly drift with respect to each other during the waveform averaging, or if the clock frequencies happen to be detuned (for example, due to different crystal oscillator temperatures) then the interleaving artifacts will vary across the different waveform captures and thus become decorrelated. However, there are drawbacks to not synchronizing the waveform and sampling clocks. Simply relying on drift in the clocks, or random detuning, is not always sufficient to guarantee the two clocks are asynchronous; it is possible that they may drift in phase with each other during waveform averaging long enough to correlate the interleaving artifacts. Additionally, asynchronous waveform sampling can

lead to increased trigger jitter as well as inconsistent sampling points across waveforms, and therefore may not be an option in some applications.

In this invention we introduce a technique for optimally detuning the ADC and signal clocks while maintaining synchronization between the two. This technique maintains synchronization between the two clocks, but with optimal detuning applied the interleaving artifacts are maximally decorrelated across waveforms. By maintaining synchronization, we can keep the associated benefits of lower trigger jitter and consistent sampling point.

Detailed Description of the Invention

Please describe your invention in detail, including descriptions and referenced drawings of a few specific embodiments. In your description, please consider the following:

- Identify and describe the main components, features, and/or functionalities of your invention, including physical properties, e.g. geometries, dimensions, choice of materials, etc.
- Describe how the invention operates, including how the main components, features, and/or functionalities operate in relation to each other.
- What is new or novel about your invention?
- Does your invention use or combine features/functionalities already known in the art? If so, why would the combination not be obvious?

This invention consists of a signal source, a sample interleaved ADC, a trigger system, a clock generation block, and a synchronized waveform averaging block. The signal source generates a signal under test consisting of repeating waveforms, which is sent to the ADC for digitization. The ADC captures and digitizes a certain number of waveforms from the repetitive input signal. The synchronized waveform averaging block digitally overlaps the captured waveforms using information from the trigger system, and the corresponding points on each waveform are averaged to reduce the uncommon noise and distortion present on the signal. Depending on the trigger system, consecutive waveforms may be captured and averaged or non-consecutive waveforms may be captured and averaged. The period between overlapped signal data is typically constant and is called the trigger period. The inverse of the trigger period is called the trigger rate. For ideal waveform averaging, the trigger period should be an integer multiple of the waveform period. The novelty of this invention is that the ratio of the trigger repetition rate and the ADC sample rate are set in such a way as to maximally decorrelate the sample interleaving artifacts during waveform averaging. This maximal decorrelation can be achieved by using the clock generation block to set the ratio of the trigger repetition rate and the ADC sampling rate so that the number of ADC samples per trigger period is relatively prime compared with the number of ADC cores. With such an optimal ratio, each point on the waveform will be sampled by all the ADC cores during waveform averaging, so any distortion induced by interleaving artifacts will be maximally averaged out.

We can illustrate this maximal decorrelation configuration mathematically. Let f_T indicate the trigger repetition rate and f_S the sample rate of the ADC, so that the number of ADC samples per trigger period is $N = f_S/f_T$. Let M indicate the number of cores making up the sample interleaved ADC. The ideal configuration is for N and M to share no common factors, i.e. for N and M to be relatively prime. If N and M are not relatively prime, but instead share a greatest common divisor, $\gcd(N, M) > 1$, i.e. $N = n \times \gcd(N, M)$ and $M = m \times \gcd(N, M)$, then $N \times m = M \times n$, and thus, after m trigger captures, the pattern of ADC cores mapped to waveform sampling points will repeat. Since $m < M$, not all ADC cores will get the chance to sample every point on the waveform before the pattern repeats. In the worst case, when N is a multiple of M, then $M = \gcd(N, M)$, and $m = 1$, so the pattern repeats every trigger period, maximally correlating the interleaving artifacts during averaging. In the optimal case, when N and M are relatively prime, then $m = M$, and only after M trigger periods, or after all ADC cores sample every point on the waveform, will the interleaving pattern repeat. The interleaving artifacts due to

mismatch of the ADC cores will therefore be maximally decorrelated and will be maximally reduced after averaging.

The ADC clock and signal clock must be phase locked in order that the ratio of ADC sample rate and trigger rate is constant in time. The system can be optimized to maximally decorrelate the interleaving spurs by adjusting this ratio. The optimal ratio can be configured by adjusting the ADC clock or the signal clock (or both). For example, in a situation where a tunable sample rate ADC is being used to characterize a signal with a fixed repetition rate, then it would be the ADC sample rate that would be adjusted. In the case of a user-controlled signal source in which the repetition rate is tunable, it may be more convenient to change the signal clock. In either case, it is generally desired (or required) to keep the sample rate of the ADC and the repetition of the signal as close to their original or nominally designed values as possible. If we call the nominal ADC sample rate and trigger repetition rate $f_{S,nom}$ and $f_{T,nom}$, respectively, then the nominal number of samples per trigger period $N_{nom} = f_{S,nom}/f_{T,nom}$. The goal is to find the nearest integer N_{opt} to N_{nom} which is coprime with the number of ADC cores, M. We define $N_{opt} = N_{nom} + \Delta N$. The ADC sample rate and/or trigger repetition rate would then need to change by a factor of $\Delta N/N_{nom}$ (or less) to maximally decorrelate the interleaving spurs.

The task of optimizing the system reduces to the problem of finding the nearest integer N_{opt} to a number N_{nom} which is coprime to an integer M. This problem is related to a function in number theory called the Jacobsthal function. The Jacobsthal function for an integer M is defined as the smallest integer $g(M)$ such that any sequence of consecutive integers of length $g(M)$ is guaranteed to contain a number coprime with M. In our case, the smallest change in the number of ADC samples per trigger period, ΔN, would be equal to $g(M)/2$, so that the smallest relative change in ADC sample rate or trigger repetition rate would be equal to $\frac{g(M)}{2\times N_{nom}}$. In practice, the number of ADC cores in a high-speed ADC is typically no greater than 256. The largest Jacobsthal function for $M \leq 256$ is 10 (corresponding to $M = 210$), which means the closest coprime integer to N_{nom} is guaranteed be no greater than 5 integers away. Moreso, it is common for the number of ADC cores to be a power of 2. In this case, any odd number will be coprime with M, and therefore, the closest coprime integer to N_{nom} will be no greater than 1 integer away. By finding this smallest ΔN for a particular system, we can ensure that the ADC sample rate and/or signal repetition rate will deviate minimally from their nominal values.

In most applications, the sample rate of the ADC, $f_{S,nom}$, is many factors faster than the trigger repetition rate, $f_{T,nom}$. To operate in the first Nyquist zone, the ADC sample rate must be at least double the maximum frequency content of the signal under test. Moreso, many applications use an ADC with a sample rate multiple factors above Nyquist to benefit from oversampling gain on SNR. With the highest frequency features of a waveform lying within the waveform period, and the trigger period being at least as large as the waveform period, it is therefore common for the ADC sample rate to be multiple factors faster than the trigger repetition rate. Additionally, for many applications, for instance optical pulse characterization, the duty cycle of the signal content relative to the waveform period is typically small leading to an even larger ratio of ADC sample rate to trigger repetition rate. The higher the sample rate of the ADC relative to the trigger repetition rate, the larger the number of ADC samples per trigger period, N_{nom}. With the optimal minimum ΔN bounded by 5 in realistic sample interleaving ADCs (because $g(M) \leq 10$ for the number of cores $M \leq 256$), and just 1 for most practical applications (with M a power of 2), this means the percentage change of the ADC sample rate and/or waveform repetition rate is bounded and will typically be small. In the case that the number of ADC samples per trigger

period is not large enough, so that the fractional change in the ADC sample rate and/or waveform repetition rate is too large, the trigger period can be chosen to be a larger multiple of the waveform period. Using a longer trigger period comes at the cost of longer averaging time for the same number of averages, but in applications where fidelity is more important than averaging time, it is a viable option.

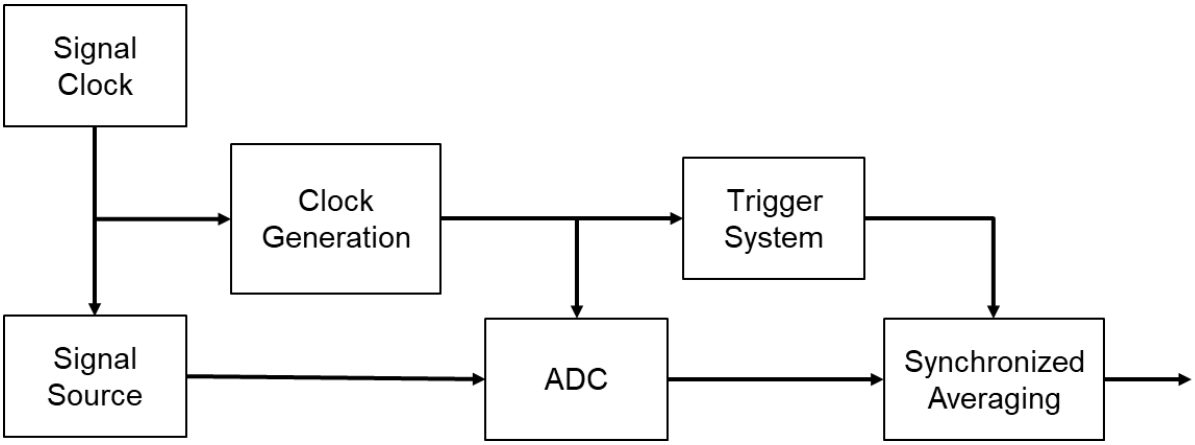
For an example of optimally adjusting the ratio of ADC sample rate to trigger repletion rate, consider a system with a nominal ADC sample rate of $f_{S,nom} = 1\ GSps$ and a nominal trigger repetition rate $f_{T,nom} = 1\ MHz$ equal in this case to the waveform repetition rate. The nominal number of ADC samples per trigger period is $N_{nom} = 1000$. For a sample interleaving ADC with $M = 16$ cores, the ratio N_{nom} and M are not relatively prime, since they share a common factor of 8. The interleaving pattern would therefore repeat after only 2 waveforms, which would result in the even order spurs coherently averaging and thus distorting the final averaged waveform. Since M is a power of 2, we only need a ΔN of 1 to maximally decorrelate the interleaving spurs (e.g. $N_{opt} = 1001$). We therefore need to change the ADC sample rate or the waveform repetition rate by just one part in a thousand, or 1k ppm. If, for instance, the system can tolerate a variation from the nominal of just 100 ppm, then the trigger rate can be chosen to be one tenth of the waveform repetition rate, with $f_{T,nom} = 100\ kHz$. In this case, $N_{nom} = 10{,}000$, $N_{opt} = 10{,}001$, and the necessary fractional change in clock rate is just 100 ppm.

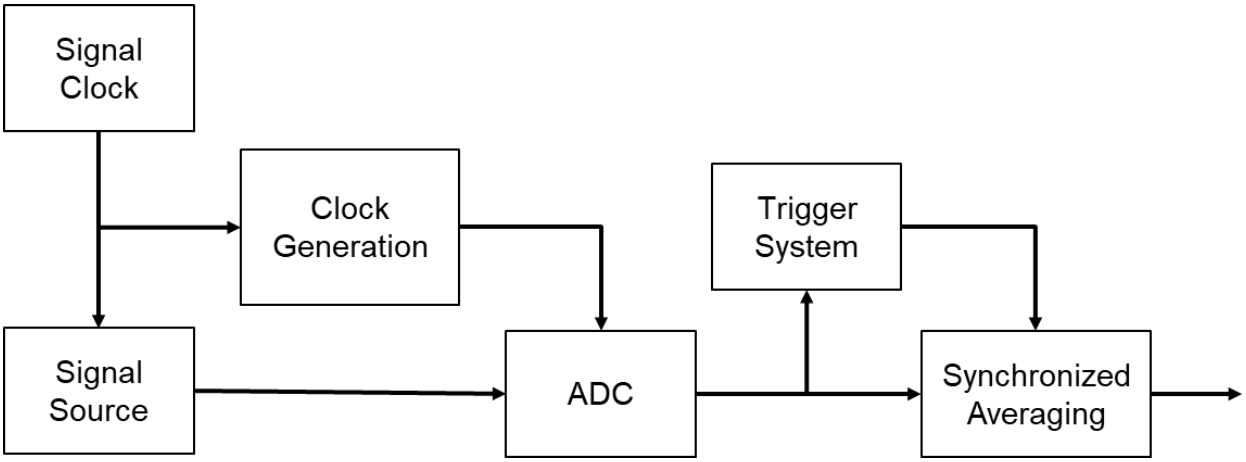
In one example implementation, the waveform repetition rate of the signal under test is kept fixed (perhaps locked to a low noise quartz oscillator) and the ADC sample rate can be controlled by accepting a variable external reference clock over a certain capture range (e.g. 10 MHz +/- 1k ppm). The sample rate of the ADC is locked to this external reference clock either directly or as a multiple of the reference clock via a phase locked loop and can be tuned by adjusting the frequency of the external reference clock. For instance, if the nominal ADC sample rate is 1 GSps and the nominal external reference clock acceptance frequency is 10 MHz, the ADC sample rate can be tuned to 1.001 GSps by using a 10.01 MHz external reference clock input to the ADC. To optimally configure this system to maximally decorrelate the sample interleaving artifacts, first the optimal ADC sample rate must be determined based on the calculations above. A clock generator which is phase locked to the signal clock must then provide an external reference clock within the capture range of the ADC external clock input. The clock generator can be phase locked to the signal clock by accepting an external clock from the signal source. The clock generator must then tune the external reference clock frequency from the nominal value for the ADC by the same proportional amount that the ADC sample rate must be tuned. As an example, the clock generator may consist of a fractional-N frequency synthesizer which generates the new optimally tuned external reference clock from a nominal reference clock of the signal source.

In practice, the resolution with which the clock generator can tune the ADC or signal reference clock is limited. The minimum resolution will impact the options for selecting a possible number of ADC samples per trigger period. As an example, consider an implementation in which the ADC sample rate is tunable, with a nominal sample rate of $f_{S,nom}$, and the trigger repetition rate is fixed at $f_{T,nom}$. Also, suppose the clock generator has finite tuning resolution such that the possible ADC sample rates are $f_S = f_{S,nom} \times \frac{k}{D}$ with D fixed and k a selectable integer. For $N = \frac{f_S}{f_{T,nom}}$ to be an integer, the possible values of integer k are limited to step sizes of $\Delta k_{min} = \frac{f_{T,nom} \times D}{\gcd\,(f_{S,nom}, f_{T,nom} \times D)}$. Therefore, the possible values of N are limited to step sizes of $\Delta N_{min} = \frac{f_{S,nom}}{\gcd\,(f_{S,nom}, f_{T,nom} \times D)}$. Ideally, $\Delta N_{min} = 1$, corresponding to

$\gcd(f_{S,nom}, f_{T,nom} \times D) = f_{S,nom}$. In this case, there are no restrictions on possible values for N, and the ADC sample rate can be kept close to the nominal value (to within $1/N$ if the number of ADC cores is a power of 2). This scenario can be guaranteed for any trigger rate if D is an integer multiple of $f_{S,nom}$. An ADC and clock generator can be designed together with this relationship. In the case that $\Delta N_{min} > 1$, then only a subset of possible integers N can be achieved. An achievable optimal N which is both relatively prime with the number of ADC cores and as close as possible to N_{nom} can be found by first finding the nearest achievable integer to N_{nom}: $N_0 = round\left(\frac{N_{nom}}{\Delta N_{min}}\right) \times \Delta N_{min}$. If N_0 is relatively prime with the number of ADC cores, then N_0 is the optimal value for N, with the ADC sample rate tuned to the new optimal value of $f_{S,opt} = N_0 \times f_{T,nom}$. If N_0 is not relatively prime with the number of ADC cores, then ΔN_{min} can be added to or subtracted from N_0 until an integer relatively prime to the number of ADC cores is reached. In the case that ΔN_{min} is even and the number of ADC cores is a power of two, then there is no possibility of tuning the ADC sample rate to a value which results in N relatively prime with the number of ADC cores. In this case, the optimal value for N will be one that minimizes the $\gcd(N, M)$.

As an example, consider an implementation with an ADC composed of 16 ADC cores and nominal sample rate $f_{S,nom} = 5\ GSps$, a fixed trigger rate $f_{T,nom} = 960\ Hz$, and a clock generator with a minimum tuning resolution of 1ppm ($D = 1{,}000{,}000$) used to tune the ADC sample rate. In this case, the nominal number of sample points per trigger period is not an integer, with $N_{nom} = 5{,}208{,}333.\overline{3}$. Because of the finite tuning parameter D, the possible values of N are limited to ΔN_{min} =125. To find the optimal ADC sample rate, we start by finding the nearest achievable integer to N_{nom}, which in this case is $N_0 = 5208375$. Since N_0 is relatively prime with the number ADC cores, this is the optimal value for N, corresponding to an optimal ADC sample rate $f_{S,opt} = 5.00004\ GSps$, a change of less than 10 ppm from the nominal value.


Signal Clock
Clock Generation
Trigger System
Signal Source
ADC
Synchronized Averaging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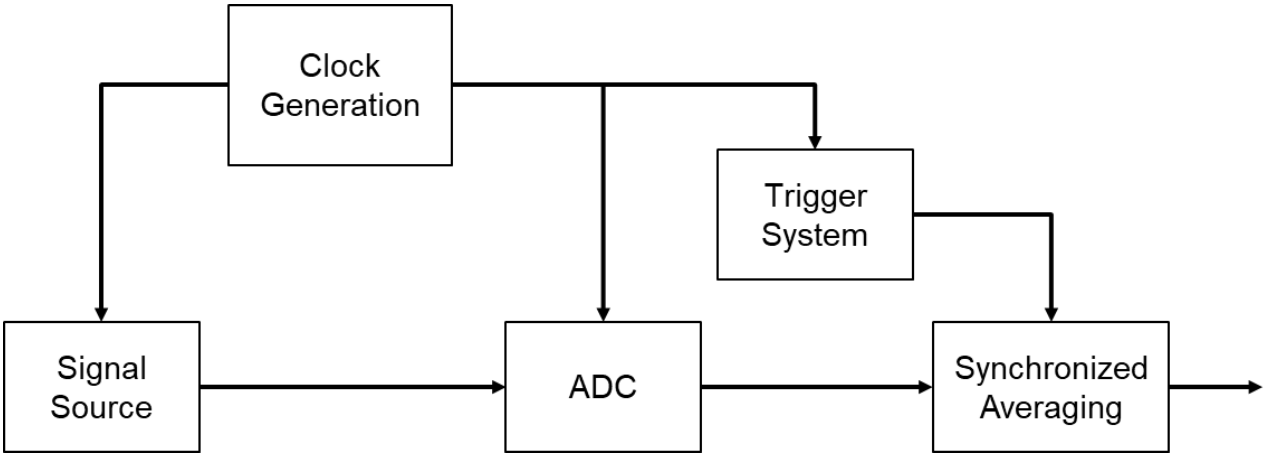
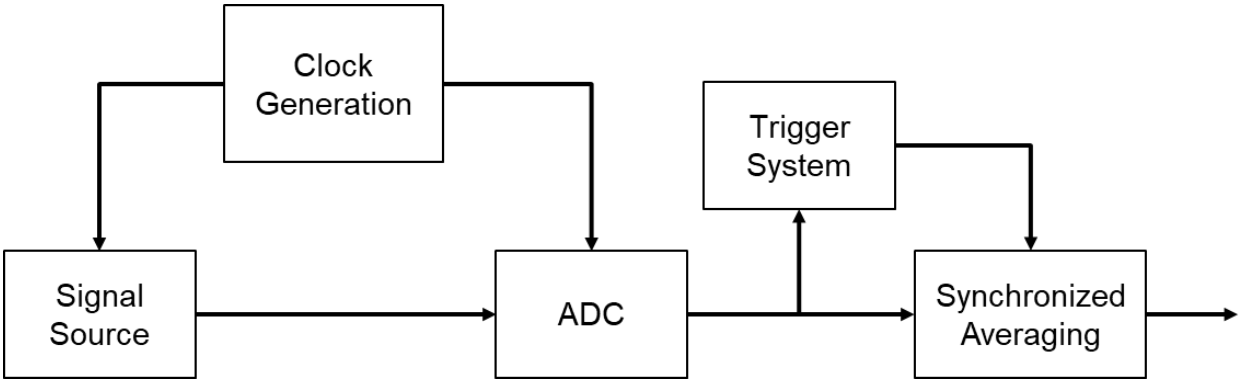

Clock Generation
Trigger System
Signal Source
ADC
Synchronized Averaging


Clock Generation
Trigger System
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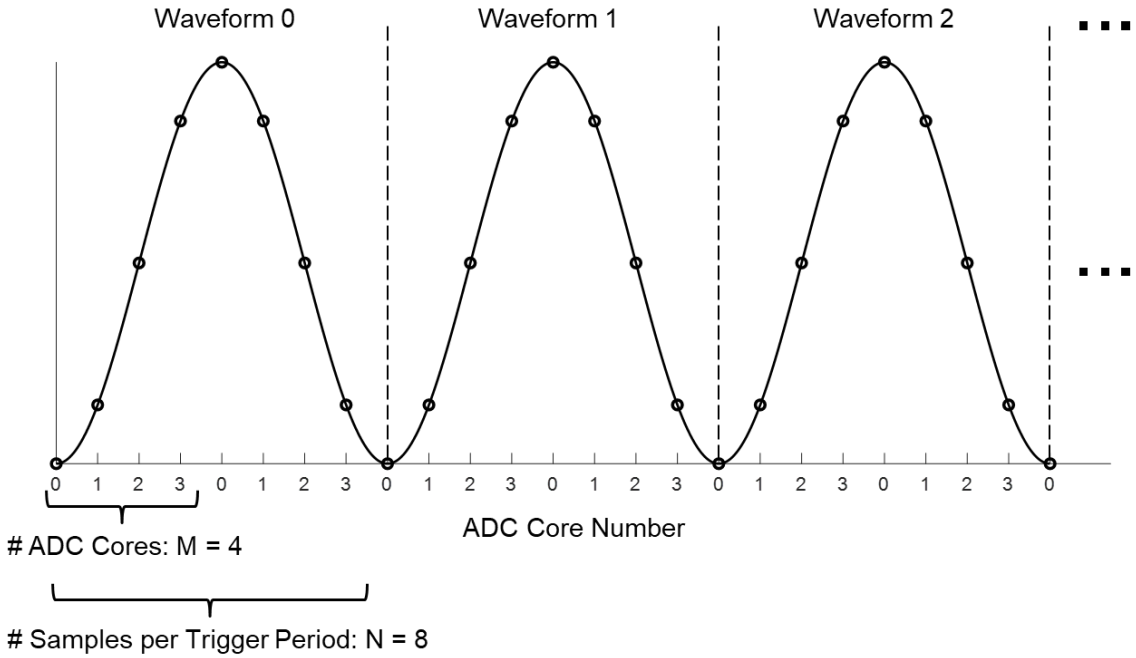
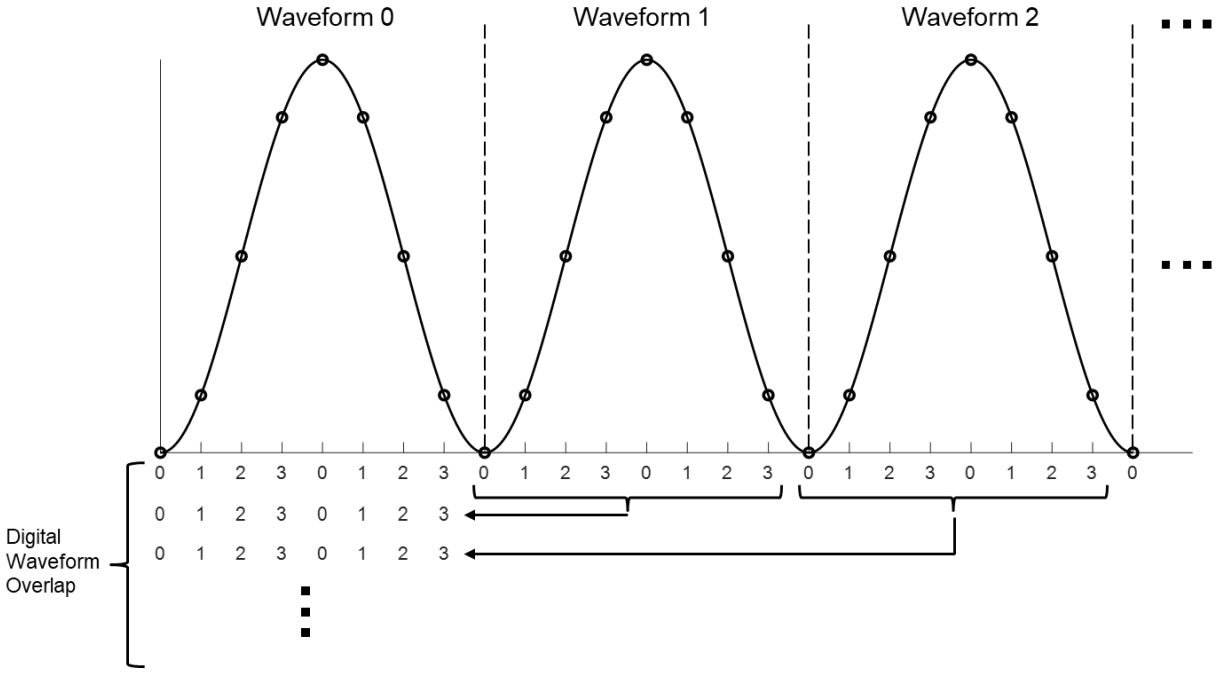
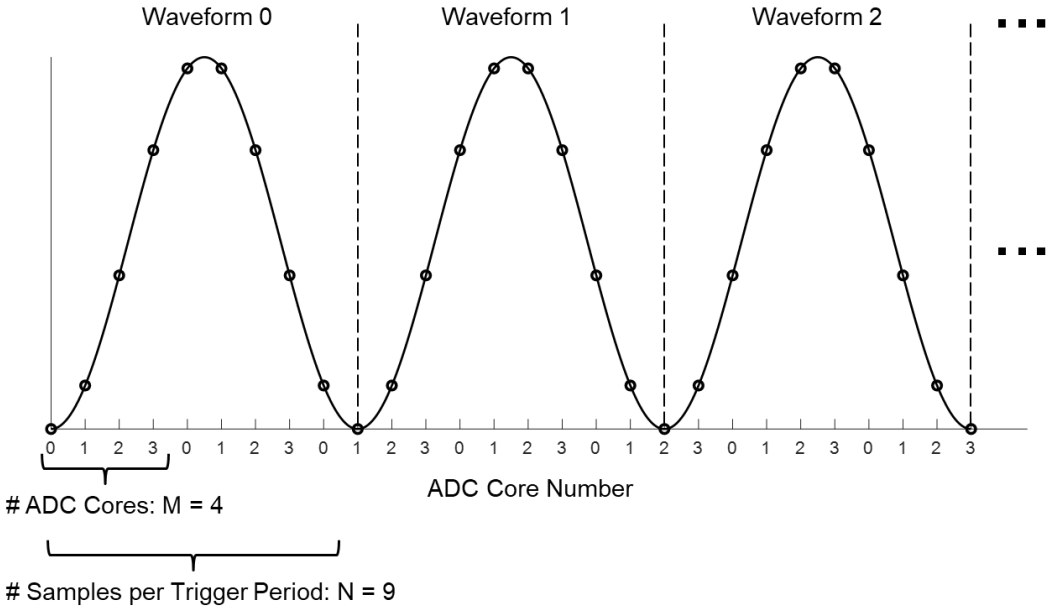
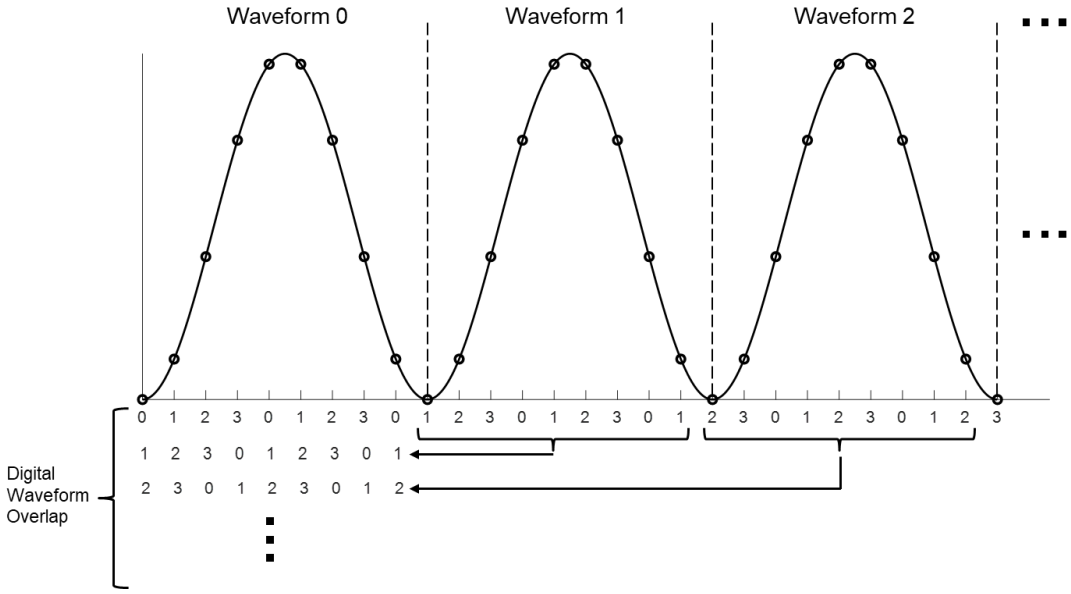

Waveform 0
Waveform 1
Waveform 2
0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0
ADC Core Number
ADC Cores: M = 4
Samples per Trigger Period: N = 8


Waveform 0
Waveform 1
Waveform 2
0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0
0 1 2 3 0 1 2 3
0 1 2 3 0 1 2 3
Digital
Waveform
Overlap


Waveform 0
Waveform 1
Waveform 2
0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3
ADC Core Number
ADC Cores: M = 4
Samples per Trigger Period: N = 9


Waveform 0
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0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3
1 2 3 0 1 2 3 0 1
2 3 0 1 2 3 0 1 2
Digital
Waveform
Overlap