CONF-941061--24

Monolithic Circuits for the WA98 Lead Glass Calorimeter*

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Abstract

Two monolithic circuits developed for readout of a 10000 element lead glass calorimeter are described. The first contains 8 channels with each channel comprising a charge integrating amplifier, two output amplifiers with gains of one and eight, a timing filter amplifier and a constant fraction discriminator. This IC also contains a maskable, triggerable calibration pulser and circuits needed to form 2 by 2 and 4 by 4 energy sums used to provide trigger signals. The second IC is a companion to the first and contains 16 analog memory channels with 16 cells each, eight time-to-amplitude converters and a 24-channel analog-to-digital converter. The use of the analog memories following the integration function eliminates the need for delay cables preceding it. Characterizations of prototypes are reported, and features included to ease integration of the ICs into a readout system are described.

I. INTRODUCTION

A lead-glass electromagnetic calorimeter which will be used as the photon detector of CERN experiment WA98 is being built by a collaboration of the University of Münster, Kurchatov Institute for Atomic Energy (Moscow), GSI (Darmstadt), University of Lund, and Oak Ridge National Laboratory. The readout electronics, which are being developed by ORNL, rely heavily on custom integrated circuits to reduce the cost and volume of the electronics on a per channel basis and to provide increased functionality compared to readout electronics previously used by the collaboration. The calorimeter consists of approximately 10000 blocks of TF1-type lead glass. This system has been described earlier [1], so only a brief description will be included here. Each glass block, or "tower," is read out by a type FEU-84 photomultiplier tube (PMT) which is equipped with a Cockcroft-Walton-type high-voltage synthesizer base [2]. A glass block with accompanying PMT and base is known as a module. For mechanical reasons, modules are arranged in 4 by 6 element arrays and are known as "supermodules". 416 supermodules are arranged into two walls that are placed above and below the experiment centerline.

The readout electronics for lead glass calorimeters used in WA98's predecessors consisted of charge-integrating ADCs preceded by delay cable which was needed to provide the 300-400 ns of level-1 trigger delay required in WA98 so the ADCs could be gated properly. For the new calorimeter it was desired that the electronics could eliminate the need for the voluminous delay cable. Additionally, it was decided that the electronics should provide (1) 10+3 bits digitization of the integrated anode charge, (2) plus timing information with at least 200-ps electronics resolution, (3) maskable calibration pulsers for the amplitude and timing channels, (4) means for monitoring PMT outputs, and (5) a tower-cluster trigger with adjustable energy threshold. Goals for the system's performance were: full scale for energy measurements corresponding to 40 GeV, less than 300-ps walk from the timing channel over a 50 MeV to 5 GeV range, and trigger threshold settable between at least 1 and 20 GeV. The calibration pulser was required mainly to verify operation of each channel, but should also allow measurement of the relative gain of the two overlapping gain ranges and some check of system linearity. There should be an interface that allows downloading of control information to the electronics. The hardware and software should collect all energy and timing data, perform zero-suppression of empty channels, format the resulting data, and place it in a global memory accessible via VME.

II. MEASUREMENT TECHNIQUE AND IMPLEMENTATION

For a collider experiment in which the charge arrives with a fixed phase relation to the bunch crossing clock, an integrator followed by an analog memory can be used to store samples which can be double correlated after the receipt of a trigger to give the delta charge. Since the analog memory clock is a multiple of the bunch crossing clock, and the trigger is synchronous as well, there is a fixed time relation between the event and the samples needed for correlation. It was realized that the same process could be used for an asynchronous fixed target experiment by artificially introducing a clock for the analog memory.

* Research sponsored by the U.S. Department of Energy and performed at Oak Ridge National Laboratory, managed by Martin Marietta Energy Systems, Inc. for the U.S. Department of Energy under Contract No. DE-AC05-84OR21400.

The principle of the energy measurement is to integrate the anode current and sample that output at a fixed frequency. The samples are stored in a switched-capacitor analog memory unit (AMU) pending receipt of a positive trigger decision from logic elsewhere in the experiment. The AMU cycles repetitively, overwriting the oldest sample with the newest until receipt of a trigger stops additional write cycles and initiates a readout cycle. In the readout cycle, a sample recorded before the event (the "pre-" sample) is digitized by the ADC, another one recorded following the event (the "post-" sample) is also digitized, and both results are sent to the data acquisition system. The integrator output is sampled by the AMU every 50 ns by this system. The AMU is 16 cells deep, so the trigger must be received in less than 800 ns after the event, otherwise the pre-sample would have been overwritten. The sampling and correlation process is shown in Fig. 1. The system is designed such that multiple pre- and post-samples can be digitized if desired, for example, to provide improved noise rejection.

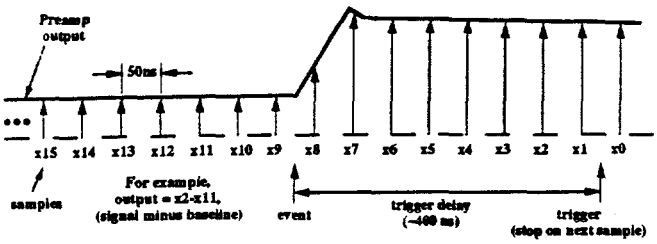

Fig. 1. Sampling and correlation using analog memory.

The timing channel consists of a timing filter amplifier, a constant-fraction discriminator (CFD) and a time-to-amplitude converter (TAC). The CFD was used in order to provide walk of < ±300 ps over a dynamic range in pulse height of 100:1, which corresponds to a photon energy range of 50 MeV to 5 GeV in actual operation. This range was chosen to cover the minimum photon energy of interest for timing (50 MeV) up to the maximum energy at which any discrimination of photons from hadrons and muons is possible in WA98 (5 GeV) for the 25-meter distance from the target to the lead-glass detector. The TAC channels are operated in common-start mode, in order to avoid having channels dead due to an uninteresting pulse occurring since a reset but prior to the trigger. This requires delaying each CFD output so it can stop the associated TAC. Since the trigger formation time is approximately 400 ns, the delay must be similar and be very stable so as to not add significant error to the measurement.

The tower cluster trigger circuits first provide some shaping of the anode pulses and then form a set of non-overlapping 2 x 2 sums of the shaped signals from all towers. These 2 x 2 sums are then combined into a set of overlapping 4 x 4 sums in order to provide full trigger coverage for photons, even if they should land near edges of modules or of the 2 x 2 regions themselves. Each 4 x 4 sum is input to a discriminator with a programmable threshold, and the outputs of the discriminators are logically OR'ed together to provide a trigger output.

Initially, it was desired that the structure of the readout electronics physically correspond to the basic mechanical unit, the supermodule (24 PMT channels). Integrated circuits were developed to process the signals from 8 PMTs as that lead to a reasonably sized chip and meant that a SM would need an integer number of chips. Since this architecture lead to needless (and expensive) duplication of control functions (many of the controls are the same for all 10000 channels) and many multi-pin connectors for trigger sum formation, it was decided to construct circuit boards that would service 6 SMs. This was dubbed the "super-duper" module (SDM), and its architecture has been previously described elsewhere [1].

All the signal processing up to and including the digitization is performed by a pair of application specific integrated circuits (ASICs). The "Preamp" ASIC contains the integrators, CFDs and the trigger sum circuits, while the AMU, TAC and ADC functions are performed by the "ATA" ASIC. One pair of these ASICs process the signals from eight photomultipliers, and therefore, three pairs of these chips make up the supermodule electronics. Both ASICs are implemented in the 1.2-micron N-well CMOS process of ORBIT Semiconductor. The die sizes are 3.7 mm x 4.1 mm for the Preamp chip and 3.7 mm x 5.3 mm for the ATA chip. Both ASICs were fabricated in one dedicated wafer run at ORBIT. Sixteen wafers were diced and packaged, yielding approximately 2550 of each chip. Preliminary tests indicate a yield of about 60%. Both ASICs use 5V DC operation and are packaged as 84-pin PLCCs. Power dissipation is approximately 0.2 W for the ATA chip and approximately 0.5 W for the Preamp chip. These ASICs are described in the following two sections.

III. PREAMP ASIC

The Preamp ASIC includes eight energy channels consisting of charge-integrating amplifiers followed by x2 and x8 amplifiers that drive the inputs of two AMUs (on the ATA ASIC) which in turn feed two ADCs thus providing the dynamic range needed. There are also eight timing filter amplifiers each followed by a constant fraction discriminator. Each channel has a maskable, triggerable calibration pulser and is also connected to a multiplexer used for observation of the input anode signal. Setup of the Preamp ASIC is performed using a serial bus that loops through all chips on an SDM board. This serial bus loads values for three 6-bit DACS controlling CFD threshold, trigger sum discriminator threshold and calibration voltage, the eight-channel calibration pulser mask, the enables for the timing and energy calibration functions, and the inspection multiplexer address plus enable. A block diagram of the Preamp ASIC is shown in Fig. 2, while a simplified schematic of the input network, integrator, amplifiers and CFD of a single channel is shown in Fig. 3.

All three opamps used in the energy channel are simple two-stage designs with PMOS input stages which allow the inputs to operate near the negative supply voltage. The amplifiers are operated with a ground reference of 1.25 V. This was chosen for several reasons which involve making the

best use of the single 5-V supply. The 1.25-V ground reference allows a reasonable match between the output amplifiers' output range (1.25 V to nearly 5 V) and the ADC which has a linear input range extending from an adjustable lower limit to an upper limit near 5 V. The feedback FET of the integrator biases the input to 1.25 V. The input protection diodes on the ASIC limit the input to the integrator to 1.25 V plus the diode forward voltage. Therefore the maximum input that can be processed linearly is about a -1.5-V (30 mA into 50 ohms) pulse from the PMT. This is acceptable, since the PMT can linearly supply that current. Essentially, the sum of the input signal plus the input range of the ADC must be less than 5 V, and increasing one means the other must decrease.

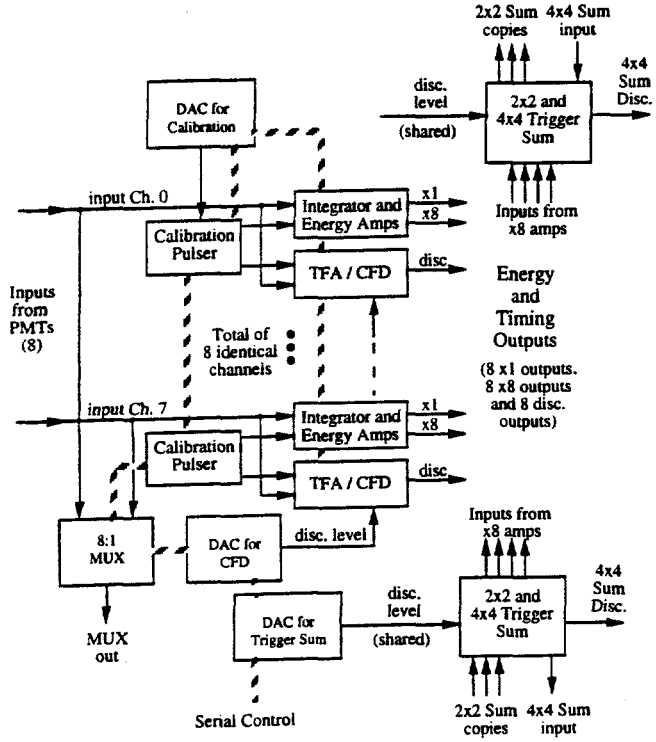

Fig. 2. Block diagram of the Preamp chip.

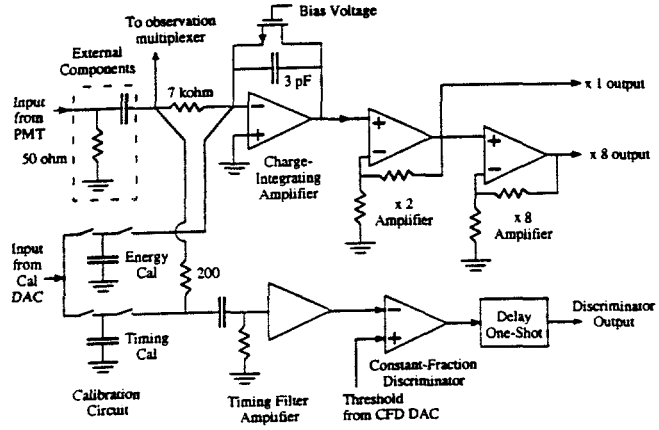

Fig. 3. Simplified schematic for one-channel of Preamp chip.

The integrator uses a long channel MOSFET (W = 1.2 μm and L = 100 μm) as a feedback element. This device is biased as needed to set the decay time of the integrator. The integrator actually only integrates a small fraction of the input charge since most is diverted through the 50-Ω line termination resistor. In fact, if the integrating amplifier is not sufficiently fast, the charge deposited on the amplifier input capacitance will not be completely integrated and will, instead, discharge through the 7-kΩ and 50-Ω resistors. The anode pulses from the FEU-84 PMTs are observed to have a nearly Gaussian shape, with 10-ns rise and 10-ns fall (10% to 90% amplitude), and a small-amplitude tail extending to nearly 300 ns after the event. The amplifier used for the integrator was designed to have sufficient bandwidth to collect most of the charge passed through the 7-kΩ resistor. The amplifier must also have sufficient slew-rate so that it will not slew even in response to the largest possible input pulse, since slewing would change the proportion of charge integrated, resulting in nonlinearity. To reduce the requirements for the integrating amplifier, some shaping is done by tapping the 7-kΩ resistor and adding capacitance to ground. With the Gaussian-shaped pulse from the PMT, the integrating amplifier has about a 30-ns risetime. It has a slew-rate greater than 100 V/μs.

An on-chip calibration circuit is provided to allow functional testing of the energy and timing channels plus a means to determine the relative gains of the two energy outputs. Crude linearity testing of the energy channel may also be done. Any combination of the 8 input channels may be exercised simultaneously, but only one mode (timing or energy) may be selected for the IC.

As shown in Fig. 3, the calibration circuit consists of two capacitors and four CMOS switches. Two of the switches are controlled by the charge signal. This allows charging the capacitors to the voltage output by the calibration DAC. This is normally done when the ATA chip is reset following readout. Once the charging switch is opened, either discharge switch can be closed as needed. This requires either an energy or timing enable, a channel enable and a calibration trigger.

It is not practical to fabricate a large enough capacitor to develop a full-scale energy output upon discharging into 50 Ω, therefore the two much smaller capacitors are used. The energy calibration capacitor is discharged directly into the inverting input of the integrating amp. As it may be charged to a maximum of 1.25 V (with respect to the inverting input), it needs to be only twice as large as the feedback capacitor to produce a near full-scale output.

For the timing circuit, it was decided that it was necessary only to develop a pulse sufficiently large enough to reliably trigger the CFD. The 200-Ω resistor was added to increase the size of the voltage pulse at the intput of the CR network, and had a negligible effect on the timing circuit. Because the input to the IC is ac coupled, charge deposited on the input node by the timing calibration circuit may only be removed by the integrator and this produces an abnormal energy output. Thus the two calibration circuits may not be used simultaneously.

The constant fraction discriminator schematic is shown in Fig. 4. On-chip, lumped-element CFD shaping is used. The filter amplifier is auto-zeroed when the system is reset after

every readout cycle, and therefore no walk adjustment is needed. The circuit is optimized for the 10-ns rise/fall times of the FEU-84 PMTs used, and was designed to minimize the number of adjustments required. The output delay is adjusted (for all eight CFDs) by an external potentiometer, and the threshold for the arming discriminator is set using one of the on-chip, six-bit DACs. This threshold determines only whether the arming discriminator (a leading-edge type) will fire; the actual timing output derives from the zero-crossing discriminator. The walk is observed to be ±250 ps over the entire 100:1 dynamic range of -15 mV to -1.5 V for which the discriminator is designed. Over limited dynamic ranges of 6:1, walk less than 100 ps has been observed. Since the measured timing resolution of a module is dt(rms) ~ 280 ps at 2-3 GeV for electrons, it is expected that the CFD performance should be more than adequate. The CFD is described in greater detail by Simpson [3].

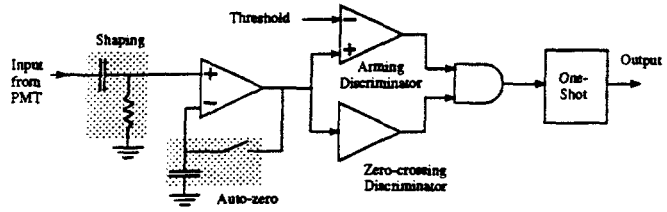

Fig. 4. CFD one-channel circuit block diagram.

The trigger tower summing scheme was developed to provide a selective trigger which favors electromagnetic over hadronic showers, provides a good lower energy cutoff and maintains high efficiency for electromagnetic showers independently of their point of incidence on the lead-glass detector [1]. The resulting scheme first forms one set of non overlapping 2 x 2 tower sums which completely tile the detector, and then uses each 2 x 2 sum as the index to a 4 x 4 sum having it as its upper-left element. The scheme shown in Fig. 5 indicates how eight adjacent lead-glass blocks are serviced by one Preamp chip and how outputs from each channel are fed into two 2 x 2 summing circuits. Four copies are made of the output of each 2 x 2 summing circuit, and these become inputs to four different 4 x 4 summing circuits. Note that some 4 x 4 inputs come from off-chip, and that some copies of each 2 x 2 sum must be in turn sent off chip. When the chips are tiled, each 2 x 2 sum participates in four 4 x 4 sums and, each 4 x 4 sum correspondingly has four 2 x 2 sums input to it.

The current-mode summing circuit used in the Preamp ASIC is shown in Fig. 6. The 2 x 2 sum is formed by shaping and summing the appropriate four x8 outputs. This voltage pulse is converted to a current pulse, which is mirrored to make four copies. These currents are routed to the appropriate 4 x 4 sum inputs, which may be on-chip, off-chip, or even on another SDM. Summing takes place in a diode-connected MOSFET which converts the current pulse back to a voltage. This voltage is then compared to the sum trigger threshold, which is set by another of the on-chip, 6-bit DACs. Current mode operation was chosen for the trigger sum circuits since some signal routes may be long and have sufficient parasitic capacitance which would make driving fast voltage mode pulses difficult. Also, copying and summing signals may be accomplished very easily using current mode circuits.

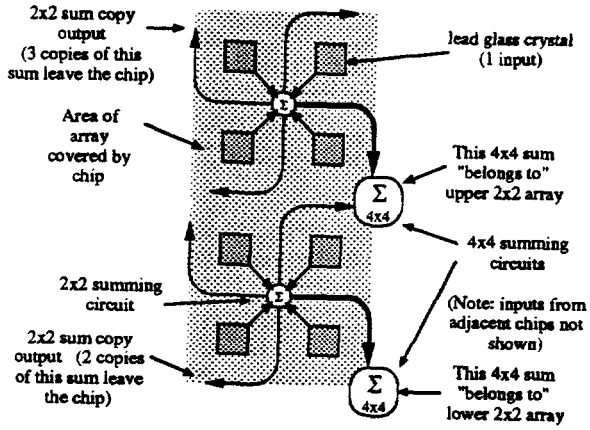

Fig. 5. Lead-glass trigger sum concept.

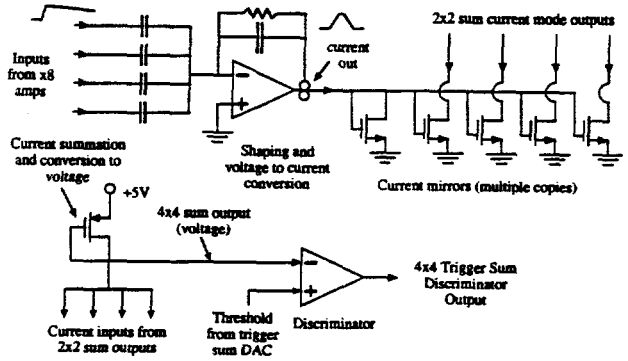

Fig. 6. Trigger sum simplified circuit diagram.

To facilitate the testing of both the prototype chips and the production run, a test fixture was developed that is equipped with numerous multiplexers and buffers. These are used to direct a pulser into any of the inputs and to allow viewing any output with an oscilloscope without having to reconnect cables. Additional mutiplexers are used to monitor bias voltages with a DVM. Multiplexer addresses are controlled with shift registers in series with the ones internal to the chip under test. A simple program running on a pc uses a digital input/output card to supply the serial data and to verify its transmission through the chip. The pc is also used to control the pulser, oscilloscope and DVM via a IEEE-488 card. For the production test, the procedure is completely automated by letting the instruments make measurements such as risetime and output levels, and having the program compare the results against minimum and maximum values.

IV. ATA ASIC

The ATA ASIC contains a 16-channel AMU, an 8-channel TAC and the 24-channel Wilkinson-type 10-bit ADC. The AMU has one input for each of the eight x1 integrator outputs and the eight x8 integrator outputs and provides intermediate

storage of integrator samples during the level-1 trigger delay. The 8-channels of the TAC are started in common by the trigger signal and are stopped individually by the delayed CFD outputs. This ADC has as its inputs the 16 AMU outputs and the 8 TAC outputs. The ADC, operating under the control of the SDM state machine (an EPLD), first digitizes simultaneously the 16 "pre-" samples from the AMU, and subsequently digitizes the 16 "post-" samples from the AMU as well as the 8 TAC values.

The AMU is a voltage-write, voltage-read type as shown in Fig. 7. The pipeline has 16 cells that are used for storage, plus one dummy cell on each end that were added to alleviate end effects. The AMU samples every 50 ns with 25 ns allowed for sampling the analog input and 25 ns allowed for changing addresses and address settling. The "write" switches were designed to allow settling of the stored voltage to 10 bits in 25 ns for the 1 pF storage capacitors. The nominal readout time is 5 μs, but the readout amplifier is capable of settling to 9-bits in 500 ns. The AMU cells are 50.4 μm wide by 167 μm in height. The readout amplifier and reset switches are 762 μm wide by 167 μm tall, thus a 18-cell pipeline requires an area 1669 μm by 167 μm. The read and write addressing of the cells are completely independent, meaning the AMU is capable of simultaneous write/read operation. This capability is not used in the present application, where, instead, the writing is stopped at receipt of a valid trigger, and readout followed by digitization is started.

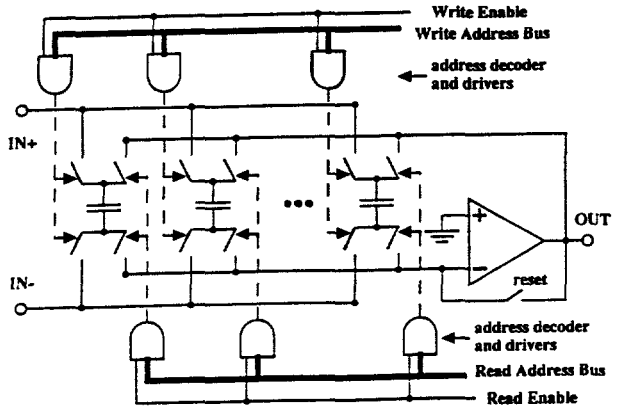

Fig. 7. Analog memory schematic.

Before the AMU, TAC and ADC blocks were combined into the ATA chip, six channel prototype versions of each were fabricated and tested. For the AMU prototype, the typical memory "gain" was 0.956, while cell-to-cell pedestal variations of 3.8-mV rms were measured for a single pipeline of the prototype AMU, using addressing driven by a gate array. This corresponds to less than one LSB for 10-bit operation. The measured integral nonlinearity was ±0.05% over a 4.5-V operating range when a 5-V DC supply was used.

The TAC range was chosen to be 200-ns full-scale. The linear output range extends over 4V for a 5-V DC supply. The noise has only been measured to date using a 10-bit ADC. All events (for > 10000 counts) fell into one ADC channel for this measurement, indicating that at the ±2 sigma level, the rms noise is 50 ps or less. The TAC resets to better than 1 LSB (out of 10-bits) in 50 ns. The pitch of the TAC layout is 167 microns, to match that of the AMU and the ADC and thus make the overall ATA chip layout regular. A schematic diagram of a one TAC channel is shown in Fig. 8.

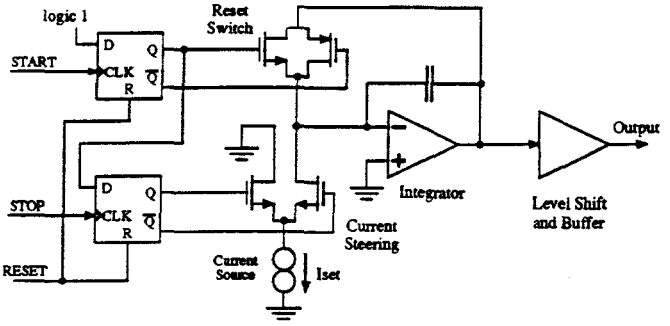

Fig. 8. TAC one-channel circuit block diagram.

The ADC is a multichannel Wilkinson-type architecture with 10-bit counters. The ramp generator and clock are shared by all 24 channels. The clock is operated at 80 MHz nominally, but has been tested successfully up to 170 MHz. The full-scale range is 4.5 V, again operating from a single 5-V DC supply. The integral nonlinearity over the full range is 0.2%, and the measured differential nonlinearity is 33%, for an rms of 0.6 channels. The design allows a straightforward extension to 12 bits, faster clocks, and more channels.

V. RESULTS

Both the Preamp and ATA chips have been tested and found to be fully functional. With the FEU-84 PMTs connected to the Preamp chip inputs, and the Preamp and ATA both functioning, typical post-sample minus pre-sample pedestals were about -1 channel while the pedestal variation was less than one channel for the x1 integrator output and about 2.5 channels for the x8 output. Installation of the SDM boards is ongoing at the WA98 experiment and further results will be reported when available.

VI. REFERENCES

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