Intelligent, grid-friendly, modular extreme fast charging system with solid-state DC protection

Final Report

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1 Introduction and Objectives

The development of electric vehicle (EV) charging infrastructure is crucial for the widespread adoption of electric transportation. However, implementing such infrastructure is a complex task that requires consideration of factors such as space limitations, adherence to industry standards, grid capacity, and other technical and policy issues. This project seeks to create a framework for the efficient design of compact medium voltage (MV) extreme fast charging (XFC) stations for EVs. The station design involves the use of a solid-state transformer (SST) that connects to the MV distribution network, delivering power to a shared DC bus. This innovative approach eliminates the need for a step-down transformer to provide low-voltage service by connecting directly to the MV distribution network. Eliminating the low-frequency transformer not only reduces the system footprint and losses but also eliminates inrush currents during grid black-start. Additionally, placing power electronics directly on the distribution system allows for high-bandwidth filtering and power factor correction. The inclusion of a shared DC bus enables multiple charging dispensers and DC storage/generation units to connect, forming a DC microgrid. This setup facilitates power sharing with minimal conversion stages. The project showcases a DC distribution network protected by intelligent solid-state (SS) DC circuit breakers (DCCB) capable of isolating the smallest section of the faulted circuit much faster than existing mechanical solutions.

1.1 Objectives

The objective is to design and deploy a 1MVA XFC station that connects directly to the power distribution system, operating at 13.2kV. This XFC station comprises a solid-state transformer (SST) that supplies power to a shared DC bus. Multiple EV charging dispensers and DC storage/generation units connect to this bus (refer to Figure 1). The shared DC bus naturally allows power sharing between all generators/loads, with minimum number of conversion stages. The resulting DC distribution network is protected using novel intelligent SS DCCB capable of isolating the smallest section of the faulted circuit much faster than existing mechanical solutions. Each vehicle interfaces with the DC bus through an EV charging dispenser, which is an isolated DC/DC converter. The integrated energy management platform enables the utility to take control actions, including curtailing power to the station and managing power ramp rates.

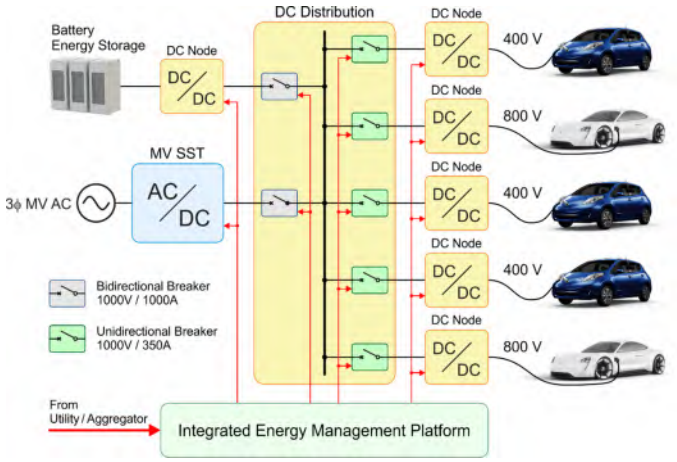


Figure 1: Key components of the proposed XFC Station: MV SST, DC distribution network, and dispenser (DC node) that contains the dc/dc converter and vehicle interface.

1.2 Approach

The scope of this project is to design, prototype, and test the proposed MV XFC station and then deploy it in the field. The key focus was on the design and demonstration of two novel components that make up the proposed system: the SST and the SS DCCB. For each system, the team developed innovations that reduce system cost and improve system efficiency and reliability. The team then finalized, packaged, and tested the SST, dispensers, SS DCCB, DC distribution network protection scheme, and integrated energy management system; and tested the integrated system in the laboratory environment prior to system deployment. The integrated $1MVA$ XFC was shipped to the demonstration site.

2 System Overview

Figure 1 shows the overall system architecture of the proposed SST based XFC station. A three-phase, 13.2 kV medium voltage AC mains feed is connected to the XFC station. The station consists of four subsystems namely SST, AC switchgear, DC switchgear, and DC nodes. The subsystems are introduced in the following paragraphs.

SST: The SST is the AC/DC power stage which is rated for 13.2kV input AC and 750V DC output at 1MVA of power level. The input of the power stage is connected to the differential mode (DM) choke, common mode (CM) choke, and dv/dt filter while the output is connected to the DC-link capacitor bank. The AC side of SST is connected to the grid through AC switchgear and DC side is connected to the DC nodes through DC switchgear along with the pre-charge circuit. The SST has a central controller (CCon) which receives data from the grid voltage sensors, grid current sensors, neutral point voltage sensor, LV bus voltage sensor, and load current sensor. The CCon regulates the LV bus voltage at 750VDC and controls the AC and DC switchgears for start-up and protection.

AC switchgear: The AC switchgear is used to connect and disconnect to the grid during startup, shut-down and in case of any fault condition. It has been implemented with three-phase mechanical breakers or solid state breakers (SSB) which is controlled by the CCon of the SST. In case of any fault, the SST needs to be isolated before the current rises above the maximum capacity of the SST. Therefore, the AC switchgear is the primary protection device of the system, since it can isolate the XFC station from the grid.

DC switchgear: The DC switchgear consists of IGCT based DC solid state breakers, which isolates the SST from LV DC distribution bus using main breaker or individual DC node by opening the node breaker. The breakers are controlled by SST CCon during normal operation. If the current through any breaker exceeds the threshold, then the corresponding breaker opens, and the information is relayed back to the SST CCon.

DC node: The DC node is a power electronic converter which charges the EV battery and can be either isolated or non-isolated type. According to IEC61851-23, the EV battery is required to be galvanically isolated from the supply or grid. As the high-frequency transformers of the SST provide isolation between AC grid and LV DC distribution system, non-isolated DC/DC converters can be used instead of much more complex isolated converters when there will be only one node at the 750VDC bus. When there will be multiple nodes installed to charge multiple vehicles, isolated DC/DC converters will have to be used. In the presented configuration, the multiphase synchronous buck converter (MSBC), a non-isolated topology, has been used at the DC node for demonstration purpose, which interfaces the 750V LV bus to the battery

and controls the charging current according to the vehicle requirement. The DC node has a controller that controls the DC/DC power stage, communicates with the EV, and performs protection action in case of any fault at the DC node.

Integrated Energy Management Platform: The central controller of the SST and the DC node controllers communicate using the Resilient Information Architecture Platform for the Smart Grid (RIAPS) [1]. The station operator can use a graphical user interface (GUI) based supervisory control and data acquisition (SCADA) platform to startup/shutdown the SST, start/stop DC node for EV charging, monitor the system parameters, and provide the subsystem components' status.

3 Solid State Transformer Design

3.1 Converter Topology

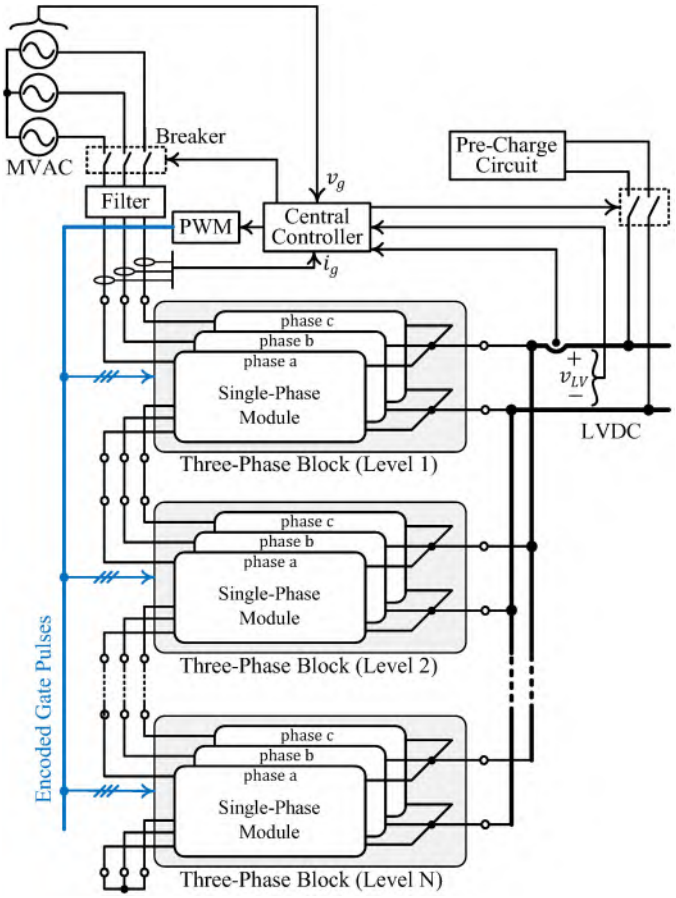


Figure 2: A three-phase SST configuration using ISOP connected single-phase modules (SPMs); a pre-charge circuit is used for soft start-up.

Figure 2 shows the overall system topology of the SST. The system rating is given in Table 1. To achieve this rating, $n = 6$ single-phase modules (SPMs) per phase are cascaded in input-series, output-parallel (ISOP) configuration. By utilizing six cascaded H-bridges, a sufficient number of voltage levels can be achieved to significantly reduce the filter size. The active front ends (AFEs) of the SPMs are Y-connected where the neutral point is floating and is monitored by a neutral voltage monitoring sensor. The filters, AC breakers, and grid sensors are connected at the medium voltage AC (MVAC) side of the SST, which is 13.2kV line-line in the system in question.

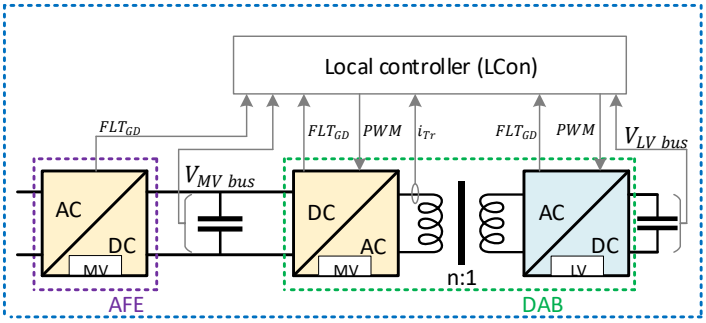


Figure 3: Single phase module (SPM) diagram

The structure of each SPM is shown in Fig. 4. Each SPM consists of a MV AC/DC stage as the active front end (AFE), MV DC link capacitor bank, dual active bridge (DAB) DC/DC converter, and LV bus capacitor bank. The DAB comprises of a MV DC/AC stage; a high frequency transformer (HFT), which provides the galvanic isolation between the input and the output and allows the system to be connected in the ISOP configuration; and a LV AC/DC stage. The ratings and parameters of an SPM are provided in Table 2.

Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are used in all power stages of the SST, enhancing the system efficiency and reducing the filter size by leveraging the higher switching frequency operational capability. For LV DC/AC power stage, a simple H-bridge was constructed with commercially available half bridge power modules. More on the structure of the power stage will be presented later in this report. The LV DC bus negative rail is grounded to the protective earth (PE) which helps provide a path for common mode current. The AC side neutral point (N in Fig. 2) is kept floating which is very close to the PE potential during regular operation. However, the neutral point voltage is monitored for any abnormal condition and the system is shut down if it goes above a threshold value.

3.2 Converter Control

The modular SST converter structure is shown in Fig. 2. Each SPM connects to one phase of the MVAC supply through the AFE and is hence subject to a double-line frequency power pulsation. If DC current and voltage are drawn by the DAB converter, the MV DC bus requires a large capacitor which serves as an energy buffer to compensate the instantaneous difference between the AC and DC power flows through the AFE and the DAB stages, respectively. In addition to the higher cost and size in comparison to their LV counterparts, large MV capacitors and the corresponding stored energy pose a critical challenge from safety perspective, specially for cabinet/enclosure design considering arc hazards and/or fires originating from electrolytic or oil filled capacitors typical at high power levels. To avoid large energy storage element on the MV DC bus, the DAB stage is designed and operated to process AC power in the same way as in the

Table 1: System parameters

Rated power	1 MVA
Rated real power	975 kW - 1000 kW @ 0VAR
Rated reactive power	222 kVAR
Nominal voltage	13.2 kV L-L RMS
Nominal frequency	60 Hz

Table 2: Single phase module parameters

Nominal MV DC link voltage	2.15 kV
Nominal MVAC voltage	1.27 kV
Nominal LV DC voltage	750 V
Rated real power	54.17 kW
DAB switching frequency	20 kHz
AFE switching frequency	5/10 kHz
MV DC link capacitor	275 μF
Leakage inductor of DAB HFT	137 μH
LV DC bus capacitor	37.8 mF

AFE stage. The DC terminals of SPMs are all tied together in a three-phase block. Due to the phase shift of 120 degrees between the phases of the three-phase power supply, the ripples generated by each phase cancel out when the three phases are combined at the DC terminals and constant DC output is obtained.

A central controller is responsible for maintaining the LV DC output by dynamically regulating the grid current. The central controller is also responsible for soft start-up of the system using a grid-side breaker and a pre-charge circuit. The control structure involves dynamic control of the grid current through the AFE stages to regulate the LV DC bus voltage while the DAB regulates the MV link voltage of the SPM [2]. The voltage and power balancing constraints between the SPMs is eliminated through this decentralized control, and the communication requirements get substantially simplified. This control design takes advantage of a clear separation in time-scale between the MV DC link and LV DC bus voltage regulation loops, with the former achieving a significantly faster control response than the latter.

3.2.1 DAB stage control

The control system block diagram for the MV DC link voltage regulation is shown in Fig. 5. The reference v^*_{MV} was dynamically generated by the LV DC bus voltage v_{LV} which is assumed constant within the frequency range of interest as

$$v^*_{MV}(s) = K_v H_{ref}(s) v_{LV}(s);\ H_{ref}(s) = \frac{\omega_{ref}}{s + \omega_{ref}}, \tag{1}$$

where K_v and ω_{ref} denote the constant voltage scaling factor and the bandwidth for the reference generation,

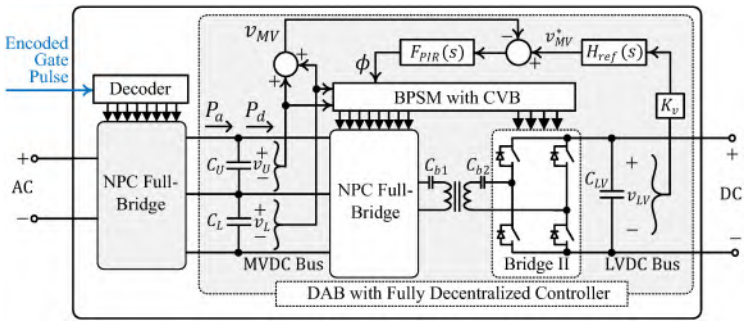


Figure 4: A single-phase module (SPM) with decentralized controller for the DAB stage.

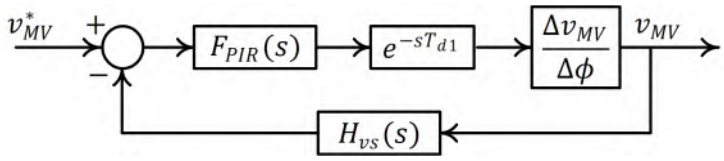


Figure 5: Control block diagram of the DAB stage of a SPM

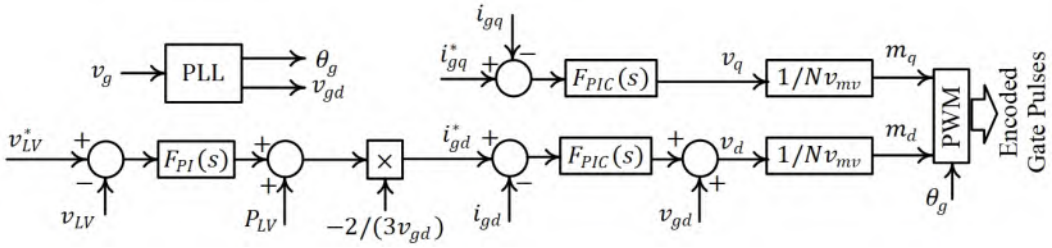


Figure 6: Control block diagram of AFEs

respectively. The compensator is designed as

$$F_{PIR}(s) = K_{pd}\left[1 + \frac{1}{sT_{id}}\right] + \frac{K_{pd}}{T_{rd}} \frac{\omega_{bd}\{s\cos(2\omega_0 T_e) - 2\omega_0 \sin(2\omega_0 T_e)\}}{s^2 + \omega_{bmv}s + (2\omega_0)^2}, \tag{2}$$

where $T_e = T_{d1} + T_{vs}$, K_{pd} denotes the proportional gain, T_{id} is the integral time-constant, and T_{rd} is the time-constant for the resonant compensation at the double line-frequency $2\omega_0$ with a bandwidth of ω_{bd}. The controller implementation takes into account a delay of one and a half samples, which corresponds to $T_{d1} = 1.5T_{s1}$. The variable ϕ defines the phase shift generated by a closed-loop compensator between the two bridges utilizing double phase shift modulation.

3.2.2 Active front end (AFE) control

The control system block diagram for the LV DC bus voltage regulation is shown in Fig. 6. Dual loop voltage regulation is employed here where the outer loop proportional-integral (PI) compensator, $F_{PI}(s)$ generates the real power reference. For the inner loop control, two PI compensators, $F_{PIC}(s)$ are used in the dq reference frame to regulate the d-axis and q-axis currents to follow the real power and reactive power references, respectively. Finally, from the modulation indexes, three-phase unipolar PWM signals are generated and sent to the first AFE stages of each phase. Each AFE delays the PWM signals by $\frac{1}{2\times n\times F_s}$ and sends the signals to the subsequent AFE. Thus, interleaving between the AFEs is achieved which reduces the ripple and minimize the total harmonic distortion (THD) of the grid current.

To start up the system, first the LV DC bus is charged to the nominal voltage by a pre-charge circuit. Then, all the DABs are started up to establish the MV DC link voltages to the nominal value. Finally, the AC breakers are closed, pre-charge is disconnected, and AFEs start operating to regulate the LV DC bus. No current limiting resistors are required on the grid side in this start-up process, unlike the traditional methods.

3.3 Single Phase Module Design

The main building block of the SST are the SPMs that are cascaded in input-series, output-parallel (ISOP) configuration, allowing connection to the MVAC supply on the input and high current LVDC at the outupt.

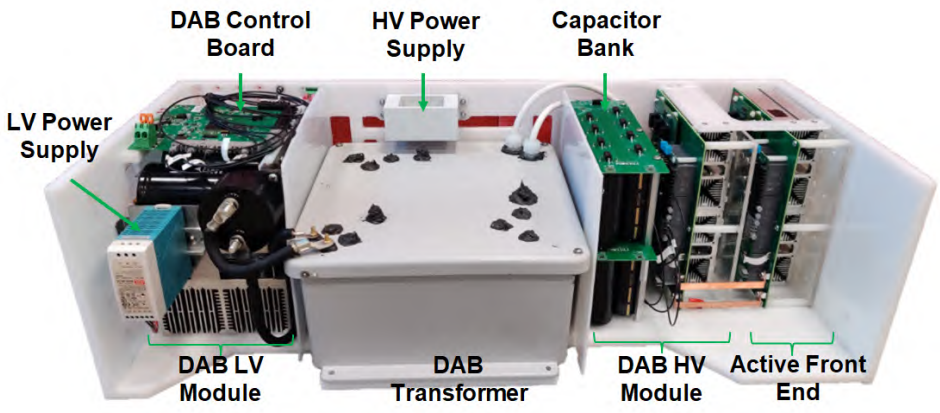


Figure 7: Single phase module hardware assembly showing, from left to right, the DAB and the AFE

In total there are 18 SPMs that make up the SST, whith each SPM concsiting of an AFE and DAB stage. Figure 7 shows the hardware assembly of an SPM with parameters given in Table 2.

From left to right, Fig. 7 shows the low voltage DAB module which connects to the DC bus on left side on the right and the high frequency transformer, which provides the galvanic isolation between the DC output and the MVAC input of the SST. On the right of the transformer, are two identical power stages, one serving as the AFE and the other serving as the high voltage module of the DAB. These identical modules use non isolated TO-247. Also visible is the MV capacitor bank, whose size reduction was enabled by the processing of the second order harmonic by the DAB.

3.3.1 DAB low voltage power stage design

The DAB low voltage power stage design is shown in Fig. 8. The DAB LV stage uses 1.2kV SiC modules from Rhom in a full bridge configuration, mounted on a heatsink. Above the devices is a gate driver and an interface board that provides a link to the DAB controller. Above the gate driver sit the electrolytic and film capacitors with a total capacitance of 37.8mF. The DAB control board sits on top of the capacitors. The control board implements the distributed control of the DAB that enables the DAB to operate as a DC transformer. The control board received voltage feedback from the HV and LV side of the DAB and actuates the PWM signals for both he LV and HV switches that make up the DAB. The connection between the HV side of the DAB and the control board, which is references to the ground, is achieved using optical fibers, thus ensuring that the isolation between the HV and LV sides is maintained. On the back of the module sits a blocking capacitor, which blocks any DC offset that could saturate the high frequency transformer; and the power supply that provides power to the LV control circuitry and powers the HV auxiliary power supply.

3.3.2 AFE and DAB High voltage power stage design

One of the primary barriers to the adoption of SiC MOSFETs in high-power MV applications are the associated costs and availability of the SiC devices. SiC MOSFETs remain expensive, and for power modules with integrated isolation, a costly Direct Bonded Copper (DBC) substrate is required to ensure low thermal impedance and galvanic isolation between the device (die) and the heatsink. In the proposed system, for the MV DC/AC stages, affordable and accessible non-isolated SiC MOSFETs in the TO-247 package have been utilized. However, standard screw-based installation methods hinder the isolation between the SiC MOSFETs and the heatsink, presenting a significant challenge. To address this issue, a structure with high-voltage isolation is proposed using discrete non-isolated devices and an electrically isolated, thermally

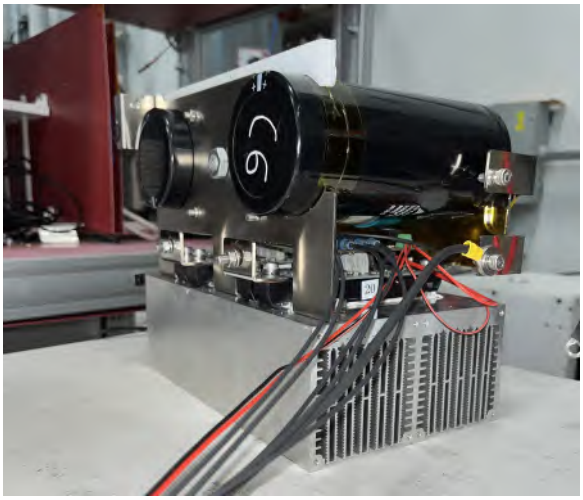


Figure 8: DAB low voltage power stage design

conductive substrate [3]. This approach employs a double-sided cooling method to clamp the devices and utilizes high-temperature rubber for resilience. Additionally, local decoupling ceramic capacitors can be employed to minimize the commutation loop. Figure 9 shows the mechanical assembly of the system. the TO-247 devices are mounted against the Aluminium Nitrite interface , which is used as a electrically isolating, thermally conductive substrate. The devices are held in place with a rubber buffer that maintains pressure on the devices and ensures good thermal conductivity between the device and the heatsink. The figure also shows the placement of the local DC capacitor, which ensures that the commutation loop of the circuit is relatively short.

The power stage uses a full bridge topology, with each full-bridge switch using a series connection of three $1.2kV/16m\Omega$ SiC MOSFET devices. This allows each SPM to operate with a 2.15kV DC bus on the high votlage side. Voltage sharing among the series-connected devices is achieved using the hybrid active and passive clamping circuit, shown in Fig. 9 and described in [4]. Compared to the passive solution, the proposed hybrid solution has no requirement to fully charge and discharge the flying capacitors resulting in reduced power loss and capacitor size. The HV stage of the DAB uses an identical design as the AFE.

The fully assembled power stage is shown in Figure 10. The power stage consists of the mechanical assembly of the heat-sinks, devices, and the Aluminium Nitrite substrate (shown in detail in Fig. 9), and three printed circuit boards that control the power stage. These are: the power board, gate driver board and the local interface board that communicates with the central controller in the case of the AFE stage and with the DAB controller in the case of the HV DAB stage. As pointed out earlier the two stages are identical.

3.4 DAB Transformer design

The DAB isolation transformer provides the galvanic isolation between the LVDC side of the system to which the vehicle chargers are connected the MVAC supply. Due to the ISOP connection of the SPMs, the potential difference between the input and the output of the transformer, will reach the line-to-neutral voltage of the system, assuming that the MVAC feed neutral voltage remains close to the ground potential. As a result, for the 13.2kV system in question, the transformer isolation needs to exceed 8kV. Considering a safety margin, the team has determined that the partial discharge (PD) inception voltage of the isolation transformer must exceed 15kV. The transformers were sourced from an external vendor, who provided an oil-filled solution. The team performed PD testing on all 20 samples received from the vendor, and determined that the PD performance for 18 units exceeded 15kV, with a PD inception voltage ranging

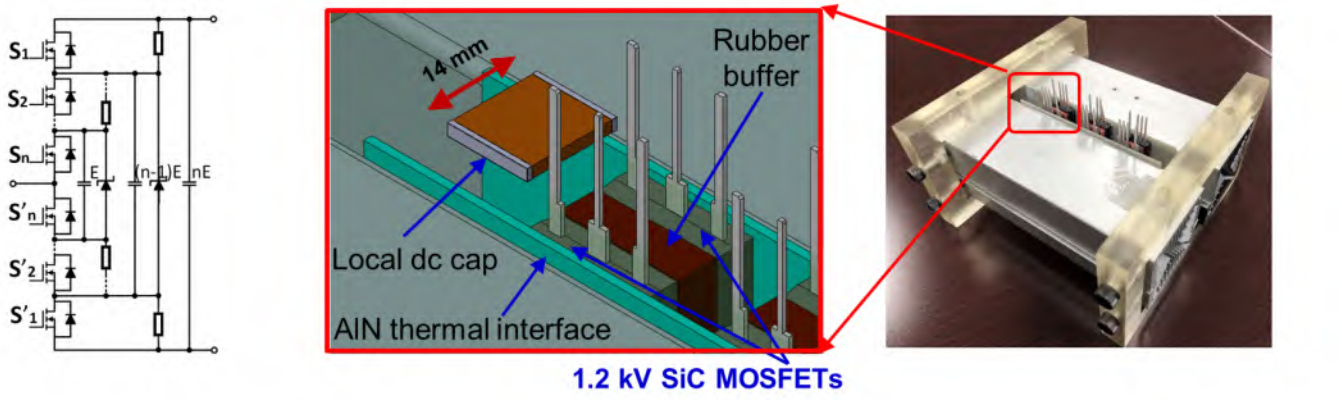


Figure 9: Components that make up the AFE

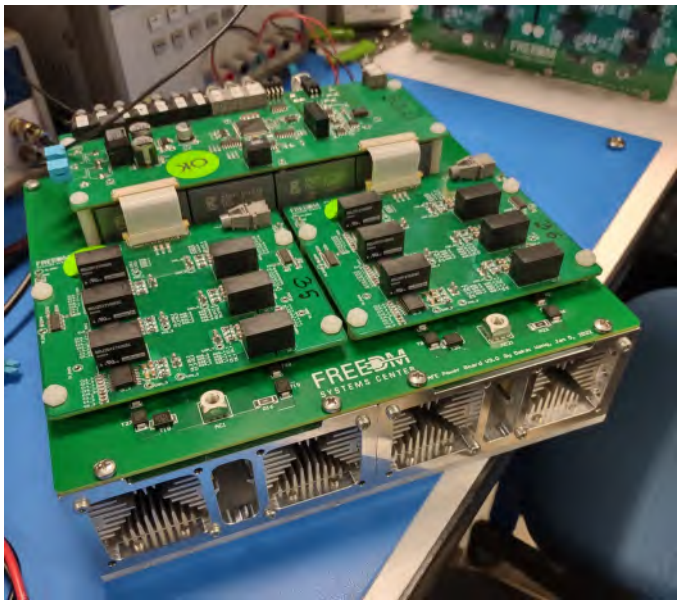


Figure 10: Fully Assembled AFE

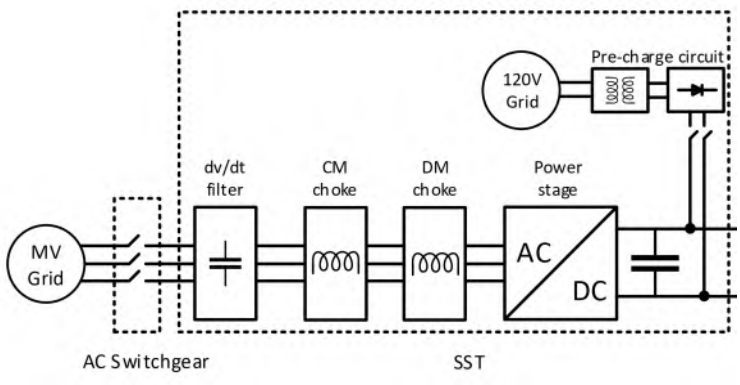


Figure 11: Filters used on the grid side of the SST

from 7-30kV for the 20 samples. The oil-filled solution proved to be unreliable with the inception voltage reducing over time and significantly after shipment to the deployment site. The isolation failure of the transformers was the reason why the field demonstration was halted, as described later in the report.

3.5 Filters

Three types of filters are used in the grid side of the SST as shown in Fig. 11. The differential mode (DM) choke is a set of three-phase inductors which reduces the grid current ripple due to high frequency switching of the AFEs. The DM choke is designed to keep the peak-to-peak current ripple under 5% of the rated current. After that, there is a common mode choke to minimize the common mode (CM) noise by providing high impedance for the common mode signals. This CM choke helps to reduce the conductive electromagnetic interference (EMI) of the SST which is being injected to the grid. The dv/dt filter is a three-phase Y-capacitor bank where the neutral is connected to ground. This filter reduces the inductive kick due to switching events and also provides a ground path for the common mode noise.

3.6 Sensors

The central controller of the SST receives feedback from the grid voltage sensors, grid current sensors, neutral point voltage sensor, LV bus voltage sensor, and load current sensor. All this data is transferred over optical fibers as bit-streams using Delta-Sigma encoding. The optical fiber provides the required electrical isolation between every sensor and the control board. The voltage and current sensors were designed with the Delta-Sigma modulator chip AMC1306E25. This chip transmits Manchester-encoded data using a single optic fiber cable per sensor [5]. The grid voltage sensor was developed using a series connection of high precision surface mount resistors to make a high impedance voltage divider.

3.7 Auxiliary power supply

To achieve galvanic isolation between the SST MV circuit and the grounded power source, a gate driver power supply (GDPS) was utilized, as depicted in Fig. 12 [6]. The proposed GDPS was designed with high voltage isolation, low coupling capacitance, and regulated output voltage in mind. Specifically, the input and output voltages of the power supply were set to 24 VDC, and the rated output power was 20 W. The transformer used in the GDPS featured partial discharge inception voltage of 20 kV RMS, extinction voltage of 18kV RMS, and had a coupling capacitance of 2.1 pF. Move information about the auxillary power supply design can be found in [6].

Figure 12: Auxiliary power supply

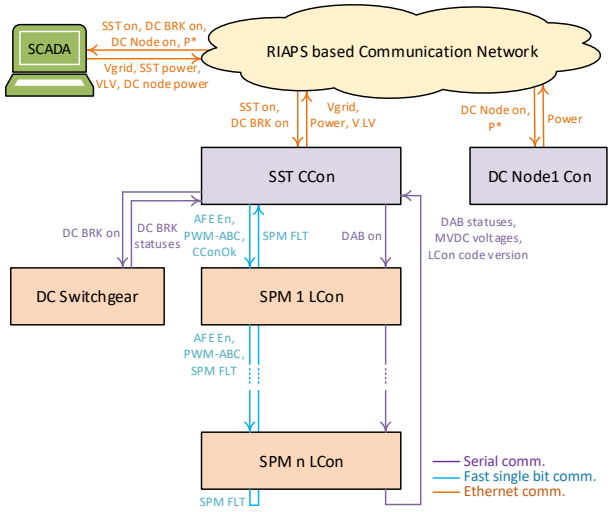


Figure 13: Communication and dataflow structure of the XFC station

3.8 Communication and Data Flow

As the XFC station contains several subsystems which need to function in a coordinated way, a robust communication and data flow structure is required between the subsystem controllers. Fig. 13 shows the communication structure of the system. The SST has local controllers (LCon) which control the DABs of the SPMs and a central controller (CCon) that controls the AFEs. All communication between the controllers is implemented using fiber optic channels eliminating the issue of isolation between the control boards.

The CCon is connected with the LCons through two types of communications, namely, fast single-bit link and slower serial communication link. Fast single-bit link is used for critical signals such as enable AFEs (AFE En), PWM gate signals for phase A, B and C (PWM-ABC), central controller OK (CConOk), and SPM fault (SPM FLT) as shown in Fig. 13. Instead of a star connection configuration among the CCon and LCons, a daisy chain topology was used which reduces the input and output channel requirements of the CCon and simplifies the wiring of the optic fibers. CCon sends AFE En and PWM-ABC signals that are repeated and passed through by the LCons while CConOk signal is ANDed with module fault inside LCon, sent to next LCon, and finally, looped back to CCon as the SPM FLT input.

The slower serial communication link between CCon and LCons is also implemented with the daisy chain method where CCon acts as the master node. CCon initiates the communication by sending commands

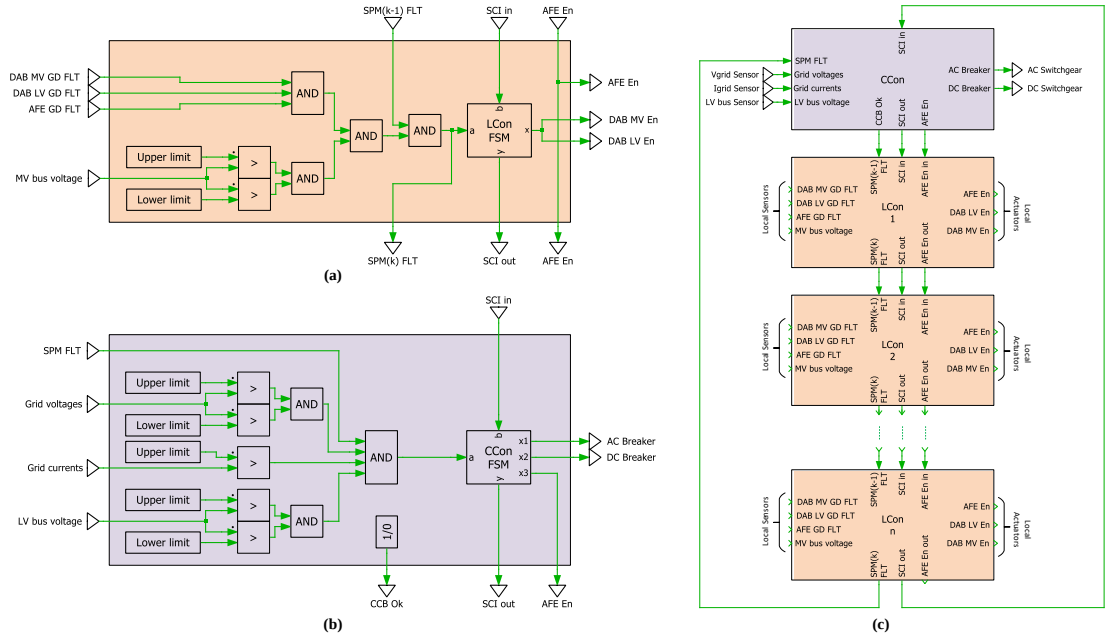


Figure 14: (a) Local protection logic, (b) Central protection logic, and (c) Overall protection scheme

and pulling data from LCons through this link. CCon sends start/stop command (DAB on) to the LCons and receives information regarding DAB operating states (DAB status), MV DC link voltages (MVDC voltage), and the version of the code being used in the LCons (LCon code ver) as shown in Fig. 13. There is another serial communication link between the SST CCon and the DC Switchgear controller. Through this link the breakers of the DC switchgear can be closed or opened individually (DC BRK on) and their status (DC BRK status) can be communicated to the CCon.

The CCon of the SST and the controllers of each DC node are connected to a RIAPS based communication network and a SCADA platform on a computer through Ethernet link. The operator can send start and stop commands to the SST (SST on), the DC Switchgear (DC BRK on), and the individual DC nodes (DC Node on) as well as the charging power references (P*) to the respective DC nodes. Critical system parameters like grid voltages (Vgrid), power being processed by the SST (SST power), charging power of DC nodes (DC Node power), and LV DC bus voltage (VLV) are sent and displayed on the SCADA GUI. This communication structure ensures smooth operation of the SST based XFC station while performing control and protection of the system.

3.9 SST System and component protection design

The SST has a decentralized protection feature for each SPM, while a central protection scheme has been implemented on the CCon. Fig. 14(a) shows the local protection inputs/sensors, logic, and responses/actuators of each SPM executed by the local controller. Here, all fault signals are active low where an '1'/high value represents a healthy state and a '0'/low value represents a faulty state. The combined fault signal of the SPM ($SPM_{(k)}$ FLT) is used in the finite state machine (FSM) based protection logic to shutdown the DAB by turning off the enables for H-bridges. This signal is also propagated to next SPM. The central protection scheme of the SST is shown in Fig. 14(b). The inputs for the centralized protection method comes from the daisy chained SPM fault signal, grid voltages, grid currents, SST neutral point voltage, and LV bus voltage sensors. The combined fault signal is used by the CCon FSM based protection logic

to operate the AC breakers, DC breakers, and AFEs of the SPMs. The DABs of SPMs can be turned on and off by sending a command through the slow SCI link. To shutdown the SST, first the switching of the AFEs switching is turned off. Next, the AC breakers and main DC breaker are opened to isolate the system. Finally, all the DABs are turned off by sending a command through the SCI. In addition, the DC switchgear also provides protection from over current or short circuit on any of the DC nodes.

Fig. 14(c) shows the coordination of the central and local protection methods, which forms the SST's overall protection mechanism. The protection set-points such as the upper and lower threshold limits are determined from detailed simulation study based on scenarios identified by failure mode and effect analysis (FMEA) [7]. This FMEA study also helped to develop safe shutdown sequence. For example, in case of a short circuit fault at one of the MV DC links, the grid currents become unbalanced and reaches the maximum allowable limit after $2.8ms$ in the worst case scenario. The delays of the sensors, controller, and actuators were assessed to check if the fault identification and the system shutdown can be done within that time. The details of the FMEA for protection design is beyond the scope of this paper and will be presented in a future paper.

3.10 Mechanical design and isolation

The SPMs were stacked inside of commercially available standard electrical cabinets. Two electric discharge paths exist in the SST system: The DAB transformer between the HV and LV sides of each module, and the HV side to the grounded cabinet. The DAB transformer design has a minimum clearance and creepage distance of 342 mm, which meets the isolation distance required for a 13.2 kV system per the IEC 61800-5 standard[8]. The SST and cabinet feature a minimum clearance and creepage distance of 106 mm and 124 mm, respectively in between also meeting the IEC 61800-5 standard. Garolite baseplates and a 12 mm clearance provide isolation of adjacent modules within the same cabinet which have a 2.2 kV potential difference in between.

To ensure long-term continuous operation of the charging system, partial discharge (PD) tests were performed on the SST using the phase-resolved partial discharge (PRPD) method at both the module and cabinet levels, as shown in Fig. 15. During the module level PD test, the AFE input terminals were connected to the high-voltage PD tester, while the LV DC outputs were shorted to ground and the MV DC link capacitors were also shorted to avoid stressing them beyond their voltage rating. This test evaluates the PD performance of the DAB transformer and isolated auxiliary power supply and detects any abnormal discharge due to dust contamination or loose electrical connections on the PRPD monitor [9]. After each module passed the PD test, the cabinet level PD test was performed to evaluate the converter to the cabinet PD. All six AFE inputs were shorted and connected to the PD tester, and all LVDC outputs were shorted and connected to ground, with the cabinet also grounded. All PD tests followed the IEC 60076-11 standard, which requires a maximum PD level of less than 10 pC for a PD free system. Satisfactory results meeting the 10 pC maximum requirement were obtained at both the module level, and then at the cabinet level [10].

3.11 Test Results

The laboratory test setup is shown in Fig. 16 where each phase cabinet consists of six SPMs. It also shows the CM and DM chokes, AC and DC breakers, and CCon board. The DC node is connected to the LV DC bus through the DC breaker with its output connected to a 0.8 Ω resistive load, which is not shown in the picture. The input of the system was connected to a MV grid feed.

The start-up of the system is shown in Fig. 17. When a start command is sent from SCADA through RIAPS

Figure 15: Cabinet level partial discharge test setup

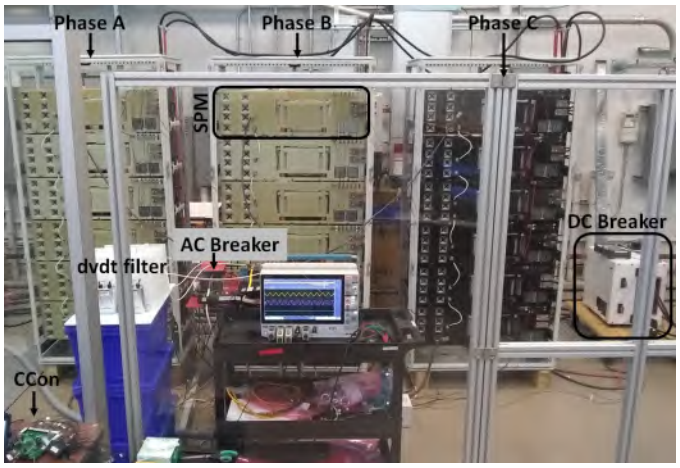


Figure 16: Laboratory hardware setup showing SST, dv/dt filter,
AC and DC breakers

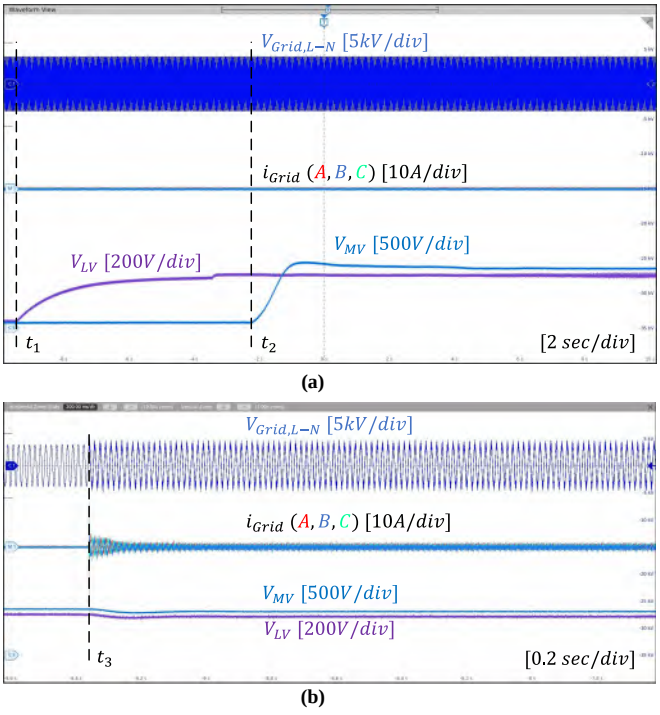
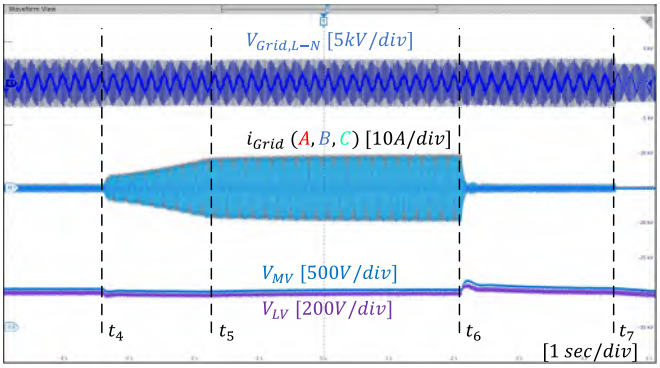
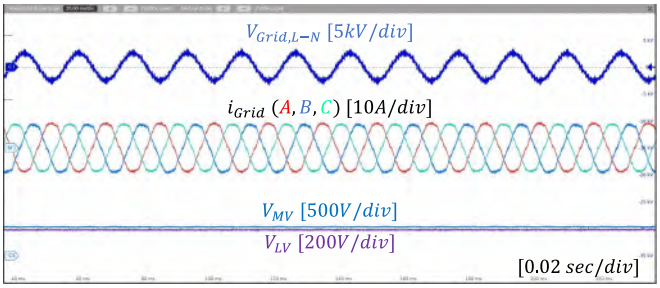


Figure 17: (a) LV DC bus charging and DAB soft start up to charge MV DC link and (b) start of grid connected operation of SST after starting the AFEs.



(a)



(b)

Figure 18: (a) DC node soft start up, constant power operation, and shutdown and (b) SST operation at 35 kW of load.

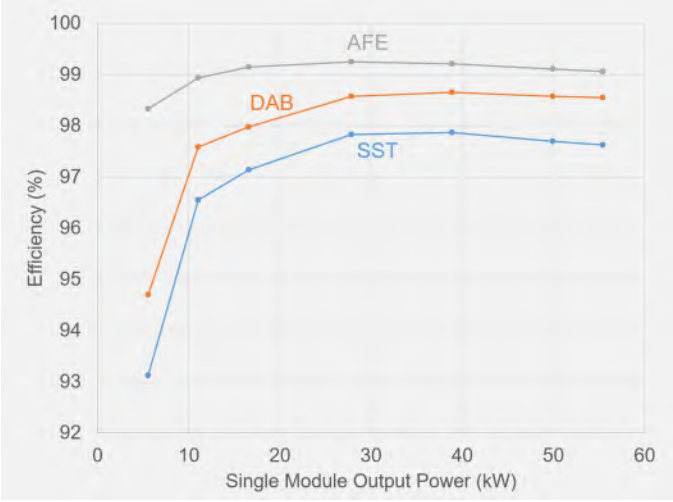


Figure 19: SST Efficiency

and grid voltage is within 5% of the nominal voltage at time, t_1, the LV DC bus is charged by the precharge circuit. The precharge circuit has a precharge resistor to limit the initial charging current of the LV DC bus capacitor which is later bypassed after the voltage reaches 80% of final value. Subsequently, the DABs of all eighteen SPMs starts one after another to charge the MV DC links to the nominal voltage starting at t_2. The staggered start-up of DABs reduces the power rating requirement of the precharge circuit. This process is shown in Fig. 17(a). Fig. 17(b) shows the closing of the AC breakers and the start-up of the AFEs to regulate the LV DC bus beginning at t_3. This set of experiments were done at 4.5kV L-L on the grid side, 870V on the MV DC links, and 290V on the LV DC bus.

Figure 18(a) shows the startup of the DC node at t_4 with a soft ramp up of power. Steady state is reached at t_5 when the power delivery level is at $35kW$ per the user demand. Figure 18(b) shows the grid currents at this condition. The DC breaker opens at t_6 emulating a loss of load. As a result, there is an 11% overshoot in the LV DC bus and it settles to the reference value within $0.25s$. Finally, the SST is shut down at t_7 by sending the stop command from SCADA.

Figure 19 shows the measured SST efficiency as a function of the power level. The efficiency was measured at a single module level. Since the system scales with the number of modules, the system efficiency also scales proportionally.

4 Protection System Design

The following sections provide an overview of the protection system contribution from NCSU's corporate partner (ABB) for this XFC project, whose team focused on the development of a ultra-fast protection for the DC distribution system including solid state circuit breakers of different ratings and assembled into a switchboard and ready to be deployed with the rest of the XFC system. This switchboard houses the solid state circuit breakers (SSCB) which interface the source SST connected to the MVAC grid, battery energy storage option, and the high current DC charging nodes that supply the EV's for extreme fast charging. This high-level overview provides details about the research and development of the overall protection system, including the SSCBs, the switchboard cabinet, and their associated hardware considerations. Finally, the results of the solid state circuit breakers testing as individual units and the testing of the coordination of the protection system are covered. In a later section, the packaging of the DC switchboard into a shipping container and deployment to the testing site with the rest of the XFC system is described in details.

4.1 Protection System Overview

A solid-state DC switchboard and the associated protection coordination schemes were developed to ensure selective and rapid isolation of any fault in the proposed XFC station operating as a DC microgrid. The DC switchboard features two types of DC SSCBs: two 1500A class DC SSCBs are used as main bidirectional circuit breakers, one connecting the power from the main power source/SST (CB2) and another connecting the battery energy storage system (CB1 in Fig. 20). Four 500A class SSCBs are unidirectional breakers that are used as branch circuit breakers to protect the EV charging ports against short circuit and grounding faults (CB3-CB6 in Fig. 20).

The six SSCBs were designed and verified through extensive simulation before being assembled and thoroughly tested. After verifying the individual tripping performance of each unit, protection coordination was verified between the assembled prototypes in two configurations: 1500A and 1500A CB, and 1500A and 500A CB. These two combinations of breakers, configured in several different test setup arrangements, allow comprehensive verification of breaker coordination. This is important, to validate that in the case of

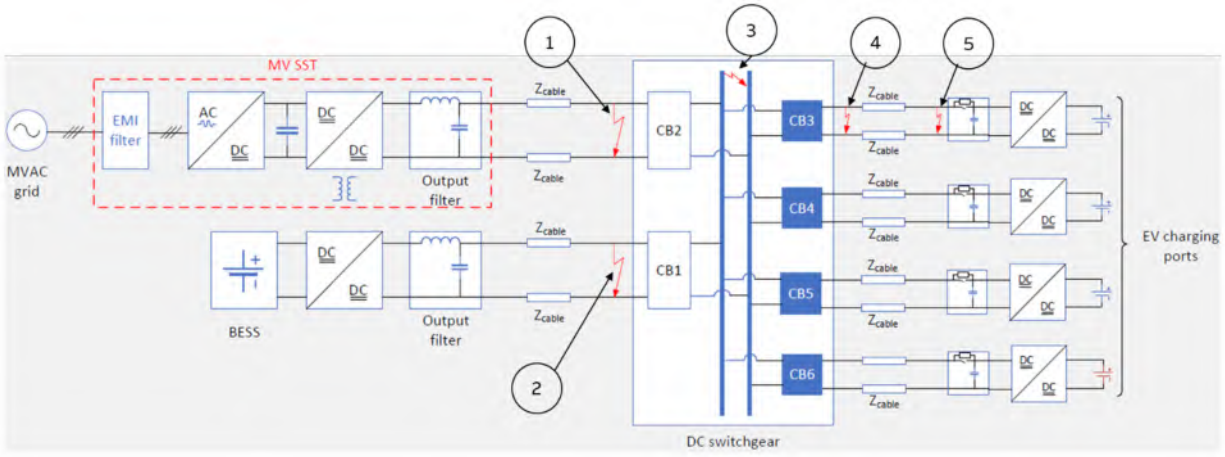


Figure 20: Five fault scenarios considered for circuit simulation and experimental validation.

a fault event, only the breaker in the fault branch closest to the fault is selectively tripped and the rest of the system can continue operation, ensuring a high system availability. The five fault scenarios of interest are shown in Fig. 20 and they were validated both through system simulation in Matlab Simulink Simscape Electric and in a testing lab environment at full scale. Five Key Fault Scenarios from Figure 20 are:

1. Fault at the output of the SST
2. Fault at the output of the BESS DC-DC converter
3. Fault at the DC bus (within the switchboard cabinet)
4. Fault on one of the charger branches, just after a 500A "Type 2"breaker (high di/dt fault)
5. Fault on one of the charger branches, near the input of the charger DC-DC converter (lower di/dt fault compared to 4)

The six breakers were eventually housed within a customized switchboard enclosure. Significant simulation and design considerations went into the layout of the cabinet so that the placement of the six SSCBs and simultaneous thermal management strategy all work towards achieving the many goals of the switchboard, for instance:

- Minimizing the overall volume and footprint of the cabinet (1.1m x 1.5m, can be further optimized)
- Minimizing copper usage (overdesigned for temperature, can be further reduced)
- Achieving high switchboard efficiency (99.42% measured at full current, up to 99.6
- Optimizing airflow while keeping the internal pressure low (negligible rise in assembled cabinet, 5Pa)
- Keeping operating temperatures well within acceptable limits of busbars, devices (max temp rise 45K)

The verification of the SSCBs and the switchboard involved thermal testing, short circuit testing, and coordination testing. The fault scenarios and various operating condition cases were tested in simulations before being verified with the assembled hardware. The system has passed all tested scenarios for all the shown fault locations under different system impedances and DC bus voltages, covered in more detail in the following sections. Tests were demonstrated to the extent that fault interruption was proven at nominal system operating conditions in less than 10µs; the theoretical capability of the SSCB's proper function extends well beyond the tested di/dt fault current interruption speeds as well as at higher current levels.

Figure 21: (Left) Corner view of the switchboard; the two larger line-side breakers on the bottom left. (Middle) Rear view, with doors opened. (Right) Load side cable connections shown at NYPA Pilot in Marcy, NY.

4.2 Breaker Design

As two types of SSCB were developed to address the 1500 A and the 500A nominal ratings, two types of cooling systems were developed, each optimized for one of the two circuit breaker classes. The cooling systems for the 1500 A class breaker is based on an advanced thermosyphon, a two-phase cooling method dissipates large amounts of heat making it well-suited for nominal currents between 1000 and 2000 A and enables high power density. Figure 22 shows the open prototype of the 1500 A solid state DC circuit breaker, including the thermosyphon cooling design. The cooling system performance has been experimentally validated on a full-scale prototype. The main benefits of the advanced thermosyphon design include:

1. High Power Density (-60% volume reduction, -50% weight reduction compared to air heatsink)
2. Simplicity of air-cooled solution (compared to liquid cooling)
3. Performance comparable to liquid cooling but with less auxiliaries and maintenance

The cooling elements were designed for following requirements:

1. Thermal loads up to 750 W per cooler
2. Design target $R_{th} = 0.067K/W$, with $\Delta T < 50K$, at 40C intake temperature
3. Heat flux up to $20W/cm^2$

The cooling system for the 500 A class breaker is based on forced-air heat sinks designed for double side cooling of the power semiconductors. This cooling system is robust and economical, and it fits well the requirements of the 500 A class SSCB. Advantages of forced air-cooling for 500 A include the simplicity and low cost of air-cooled solution and the ability to reduce the footprint for 500 A breaker (<50% volume compared to 1500A breaker). The cooling elements were designed for following requirements:

1. Air flow validation for 500 A and overload conditions
2. Thermal loads up to 250 W per heat sink
3. Design target $R_{th} = 0.2K/W$, with $\Delta T < 50K$, at 40C intake temperature

Figure 22: (Left) Partially assembled prototype of 1500 A SSCB CB1 and CB2 (inside view) where eight two-phase thermosyphon coolers are visible in a single SSCB unit. (Right) Partially assembled prototype of unidirectional 500 A SS DCCB CB3...6 (inside view). The forced air heatsinks are shrouded within red air ducts running the front-back length of the SSCB; fans mounted on front wall and vents in rear.

4. Heat flux up to $10W/cm^2$

Figure 22 shows an open frame 500 A solid state circuit breaker, including the forced-air heat sink cooling design. The cooling system performance has been experimentally validated on a full-scale prototype.

The team designed and manufactured:

1. The cooling system for the 1500 A class SSCB and the mechanical design of the internal bus bar connections, the custom 40kN mechanical clamp for the bidirectional stack, and the mechanical support structures.
2. The samples of power stack for the 500 A class SSCB based on the selected and validated cooling elements.
3. The mechanical support structures and bus bar connections for the galvanic isolation switch and the metal oxide varistors for the 500 A class SSCB.

In addition to advanced cooling method implementations, a mixed signal electronic circuit was designed, simulated, and manufactured to function as a ultra-fast detection circuit for high di/dt faults that requires minimal measurement and propagation delays and for protection coordination that operates in the 10-100 µs time frame. The final version of this PCB was used in all six constructed SSCB units with settings tuned to the specific breaker. The control circuit was designed for strong noise immunity and robust performance, capable of fault detection in less than 10 µs for up to 500A/µs. The mixed signal solution has the robustness of digital filters and logic and the speed of analogue circuits. The fast short circuit detection will enable protection coordination for systems with high power converters penetration, like EV charging infrastructures.

The bidirectionality of power flow within each breaker on the line side of the switchboard is realized by placing two reverse blocking IGCTs (RB-IGCT) in anti-parallel configurations. Both 1500A breakers use the described structure, meaning voltage will be blocked in both the positive and negative direction when the breaker is commanded open, and if closed will still allow current to flow through both poles in either direction by flipping the "ON"-state devices effectively realizing a four-quadrant switch. The trip threshold is $3x$ nominal ratings: $1500x3 = 4500A$ in the forward direction, and $500x3 = 1500A$ in the reverse direction,

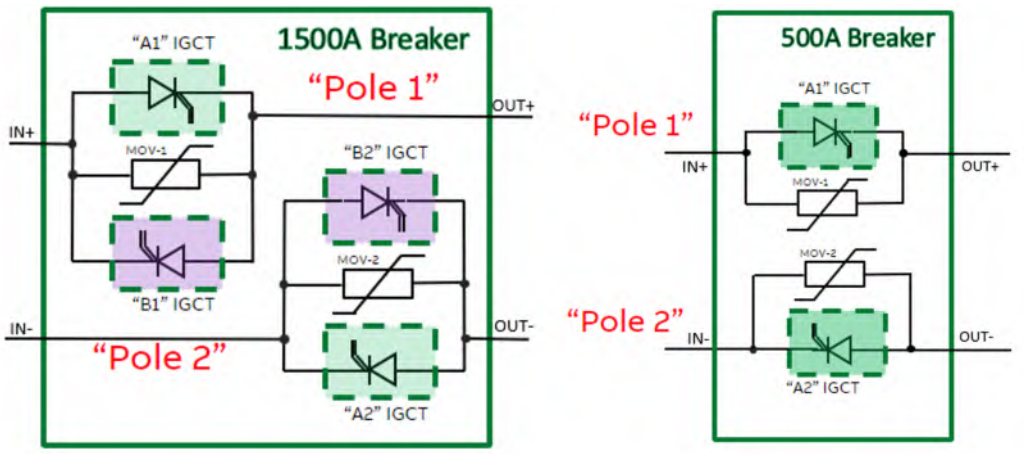


Figure 23: (Left) Highly simplified internal construction of 1500A 2-pole breaker, showing the antiparallel configuration of two IGCTs on each pole. (Right) Simplified model of unidirectional 500A breaker, with only one "forward conducting, reverse blocking" IGCT on each pole.

when power is regenerated toward the grid. The reason for two directional-dependent thresholds for the 1500A bidirectional breaker is to ensure coordination in case of a line-side fault.

The 500A class breakers are by contrast constructed as two quadrant switches, so each pole consists of only one device that can carry current only to or from the load in only the forward direction. This design is for today's typical extreme fast-charging installation scenario, where EV owners aim only to charge their cars and not back-feed energy to the grid as the priority is minimum time charging. This could be adjusted in the future for applications that required vehicle to grid interaction.

Each solid-state switch is in series with a mechanical breaker to provide galvanic isolation in the event of servicing or maintenance. Aside from the power device architecture of each kind of breaker, the key components of each assembled SSCB include MOVs for energy dissipation, thermal relief/management (heatsinks, fans, vents), a power supply, an isolated power supply board, a main control board, current sensors, and an HMI panel for flexibility of status reading, remote controllability, and programmability.

The team manufactured the cooling system for the 1500A class SSCB and the mechanical design of the internal bus bar connections, the custom mechanical clamp for the bidirectional stack, and the mechanical support structures. The team also designed and manufactured samples of the power stack for the 500A class SSCB based on the selected and validated cooling elements. The team designed the mechanical support structures and bus bar connections for the galvanic isolation switch and the metal oxide varistors for 500A class SSCB.

4.3 Breaker Design Validation and Testing

The fault current di/dt transient speeds were set by manipulating setup-controlled variables like DC capacitor bank charge and cable lengths, see Fig. 25 below. Tests could therefore safely be conducted starting with higher levels of system inductances ($L_{sys} > 400\mu H$) and low system voltages ($V_{Cap} < 250VDC$), before progressing to full voltage (up to $V_{Cap} = 1000$ VDC), full current, and faster fault transients ultra-low loop inductance ($L_{sys} < 4\mu H$). The test voltage was incrementally increased at each inductance to safely validate the trip curve and performance of the control electronics at faster transients.

The team completed the assembly and testing of the finalized designs of the individual breakers (shown earlier in Fig. 24) including improved assembly of the semiconductor stacks with dedicated, forced-air

Figure 24: Final version of the 500 A (CB3. . . 6) Class DC SSCBs and 1500 A class DC SSCBs (CB1 and CB2).

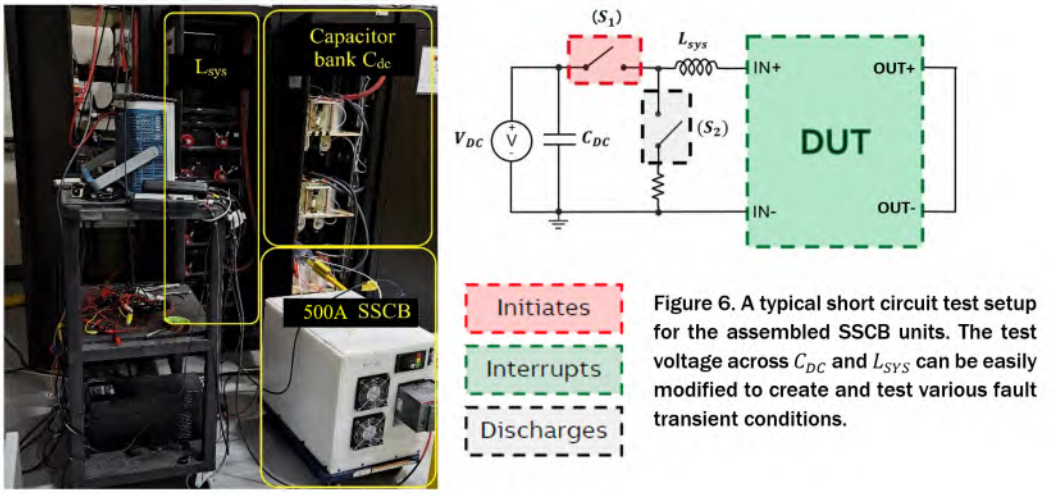


Figure 6. A typical short circuit test setup for the assembled SSCB units. The test voltage across C_{DC} and L_{SYS} can be easily modified to create and test various fault transient conditions.

Figure 25: A typical short circuit test setup for the assembled SSCB units. The test voltage across C_{DC} and L_{SYS} can be easily modified to create and test various fault transient conditions.

cooling, and fine-tuned electronics design incorporating extensive filtering for noise immunity and ultra-fast accurate sensing, and a protective control scheme with redundancies for current interruption. Key components in the stack assemblies have been delivered and certified by experimental tests for both electrical and thermal performance. All sub-assemblies within each breaker unit were tested for accurate performance, al-lowing the buttoning up of the six SSCB units before each was subjected to rigorous thermal and short circuit testing.

Thermal tests were done methodically, first identifying the potential trouble spots where maximum heat is expected to be generated, for instance at the center of the RB-IGCT wafer in the high current press-pack thermal stack, or at the cross sections of the copper busbar splice plates within the 1500 A class SSCBs. Measurements were taken pre-construction to baseline the expected device thermal performance, then again after a unit was enclosed in its walls and subject to nominal airflow/cooling, and finally again after being mounted within the DC switchboard enclosure and experiencing a worst case rise in ambient air temp. Below is a sample temp-rise test, where results give strong indication of effective thermal design. Full-current steady state is reached within two hours.

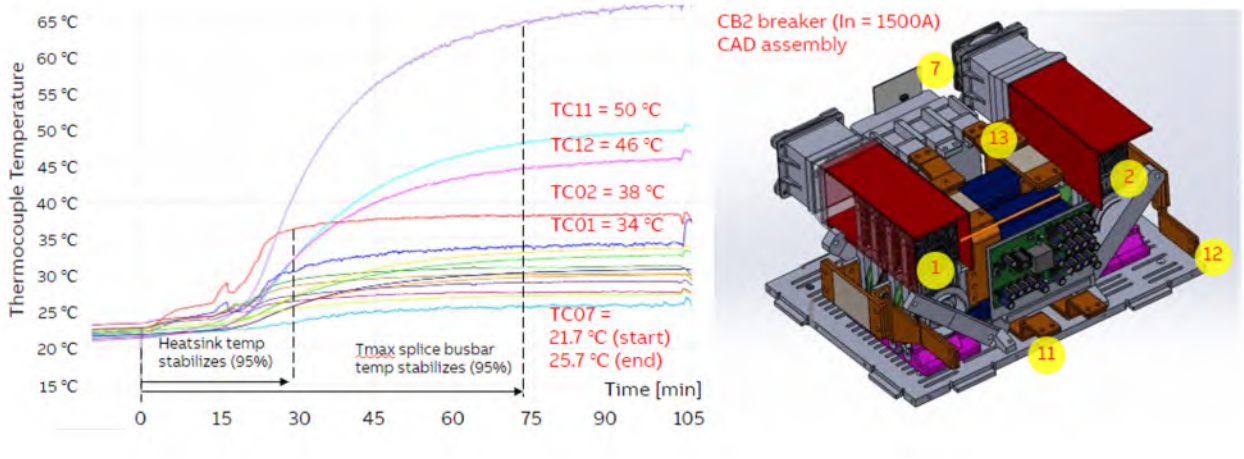


Figure 26: An example of a temperature-rise test on a 1500A SSCB, with key monitored suspect hot spots.

The switchboard cabinet, which hosts the six DC SSCBs, was assembled by the team in-house. All six breakers were connected after the final thermal and electrical performance verification of each individual breaker, marking the start of the final round of "final assembly" testing. The switchboard has its own forced ventilation for cooling and a compact bus structure for power distribution.

Short circuit tests were performed on each individual SSCB unit. Below in Fig. 27 are the results of the short circuit tests run at the final stage of individual SSCB testing.

Both plots show a strong correlation between the three data sets (calculation, simulation, experimental), indicating good precision and accuracy of analysis on the performance of the designed electronics. After verifying goodness of fit with each type of unit functioning as designed, the team was able to move onto the next stage of short circuit testing, demonstrating ultra-fast coordination, covered in the following section.

4.4 Protection Coordination Validation

The μs-fast tripping made possible with SSCBs also poses a key challenge concerning ultra-fast coordination. Ideal coordination in a fault scenario entail opening only the breaker closest to the fault so the maxi-mum number of nodes in the microgrid remain connected to power. For instance, a fault at the EV charger (location 4 or 5 from Fig. 20) should be interrupted by the closest 500A breaker. The upstream 1500A

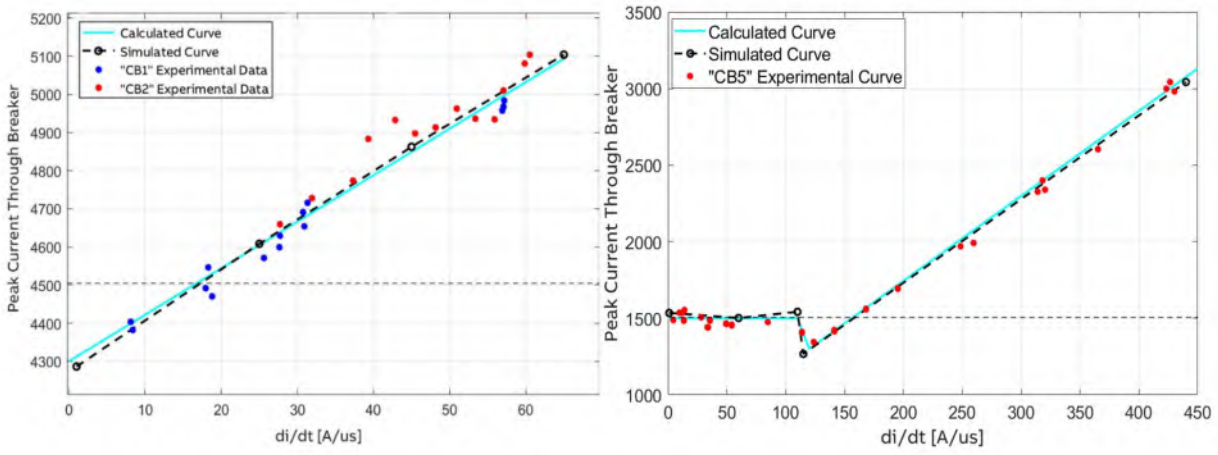


Figure 27: A summary of theoretical vs. practical results of the 1500A (left) and 500A (right) SSCB's individual short-circuit interruption capabilities.

breaker should act as backup protection in case of some maloperation of the load-side breaker and therefore must wait for some predefined delay before interrupting. It should otherwise remain closed during the initial transient and provide continued electrical service to the system, as simplified in Fig 28.

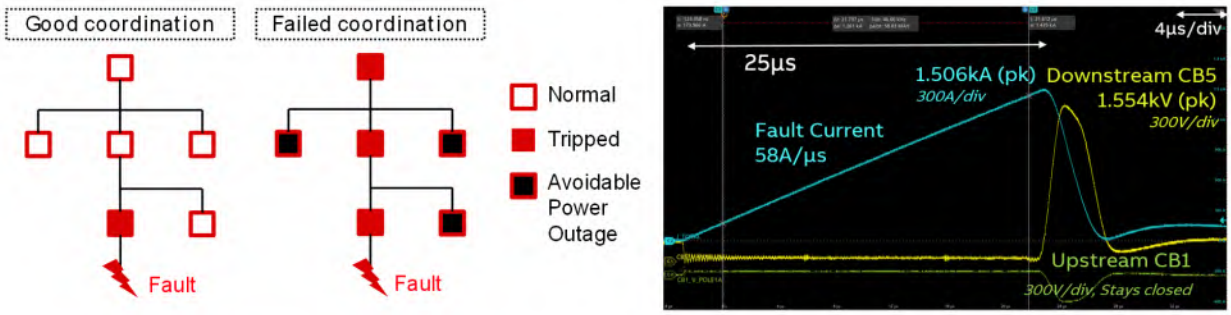


Figure 28: (Left) Aim of coordination protection. (Right) Oscillogram shows a successful test within 10s of µs.

Fault Location	SSCB Coordination		Trip Setting		Fault di/dt [A/µs]				
	Upstream	*Downstream*	*Upstream*	*Downstream*	250	125	100	60	10
Source (1,2)	1500A Breaker	1500A Breaker	4500A	-1500A	ok	ok	ok	ok	ok
Switchboard Internal (3)	1500A Breaker	500A Breaker	4500A	N/A	O.C	ok	ok	ok	ok
Load (4,5)	1500A Breaker	500A Breaker	4500A	1500A	ok	ok	ok	ok	ok

Figure 29: Coordination results expected from delay equations (1) and (2) below.

Extreme precision is required; too little delay may result in both upstream and downstream breakers opening, and too long delay can result in device failure and potentially catastrophic damage. Either case constitutes failed coordination, and a range of possible fault locations and fault transient speeds complicate the solution. In tackling the challenge of accurately setting the delay of the upstream breaker, the internal delays of the CB must be approximated with extreme accuracy for the possible failure modes, and then compensated for with electronics. Based on the inherent device characteristics of the IGCTs, the current sensors, and the developed signal conditioning circuits, equations that model the delays allow us to predict

coordination beyond 700Aμs between the two breaker types, and 125Aμs for scenarios where a 4500A trip threshold is set (specifically, location 3). Beyond this fault transient rate of rise, the actual system current interruption level approaches the 6kA current-interrupting rating of the IGCT and there is growing risk of overcurrent (O.C) damaging the device (Fig. 29).

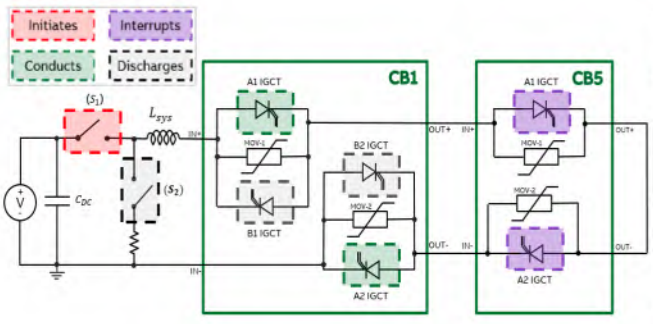
The delay of each CB, t_{delay}, can be roughly split into three main components: the sensing delay t_s, the analog trip detection circuitry delay t_d, and the gate driver delay t_{gd}.

$$t_{delay} = t_s + t_d + t_{gd} \tag{3}$$

The exact values for each component vary depending on the design, components, and fault conditions. Simulations with modified input parameters like voltage or total inductance can approximate unique delay values for a wide range of fault current transient speeds. After these delay values are approximated, it is possible to estimate the "maximum current" points along a trip curve of an isolated breaker (dependent on the fault current di/dt due to the nature of the IGCT device and the trip detection circuit used), shown as:

$$I_{trip} = I_{th} + (t_{delay} - t_{comp}) * \frac{di}{dt} \tag{4}$$

where I_{th} is some fixed set value threshold and t_{comp} is the compensation factor used to achieve a trip curve with desirable slope, offset, and linearity. Just as t_{delay} varies with the fault current di/dt and trip threshold I_{th}, so does t_{comp}. This is to ideally achieve a flat, instantaneous trip curve over a broad range of possible faults. The same compensation circuit is used in both breaker types. Bandwidth limitations of the designed filtering and delay compensation circuit predict only being able to achieve the flattening of the actual trip curve up to some maximum fault current transient speed. The trip curve's slope transition point is apparent only for the smaller 500A breaker, see the elbow point in the right-side plot of Fig 27. Furthermore, the efficacy of this compensation decreases as the maximum current that is sensed and interrupted increases. For the 1500A bidirectional breaker with a 4500A trip level, simulations for forward conduction predict an under-compensated design at any di/dt, where the peak current will continue to rise in direct proportion to the fault current transient; this is visible in the left-side plot of Fig. 27. Having already validated these delays in simulation and individual SSCB testing, the team confidently moved on to coordination tests and confirmed the tripping behavior.



Fault Location	di/dt [$A/\mu s$]	Downstream Breaker Trip?	Upstream Breaker Trip?	Pass?
1) SST	140	YES	NO	
2) BESS	40	YES	NO	
3) internal	3	YES	NO	
4) load	45	YES	NO	
4) load	150	YES	NO	
5) load	0.5	YES	NO	

Figure 30: (Left) Aim of coordination protection. (Right) Oscillogram shows a successful test within 10s of μs.

Successful coordination was demonstrated for each type of fault scenario, see table in Fig. ref11. A representative sample of test results is displayed, where proper operation of the DC breaker system is shown over a large range of fault transient speeds at each key location. The breaker combination for a

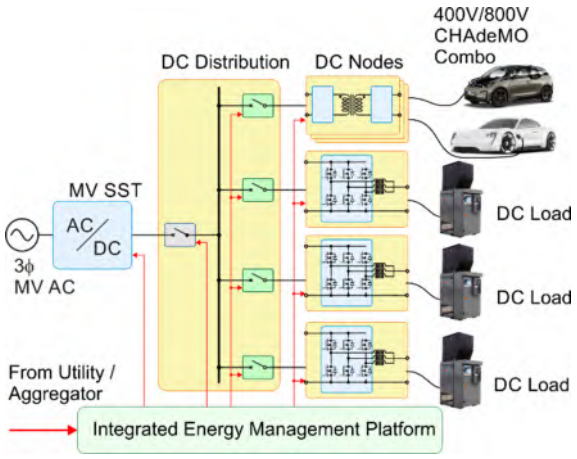


Figure 31: Planned System Demonstration

Figure 32: DC/DC converter

fault at location 3 (switchboard internal fault) is like that for locations 4/5 (load-side fault), the difference being at location 3 the 1500A breaker trips, interrupting the fault, while the 500A SSCB opens. The results confirm the efficacy of this DC protection solution.

5 System Integration

The system integration task consists of bringing together the NC State developed medium voltage SST; the DC distribution and protection system developed by ABB; the DC nodes; and the integrated energy management platform. The SST and the DC distribution systems were described in the previous sections. In this section we will describe the DC note and the integrated energy management platform design.

5.1 DC Node

In order to simulate the behaviour of an electric vehicle, the team used a resistive load interfaced to a DC/DC converter. The use of the DC/DC converter enables emulating a vehicle charging profile without the need for access to an eclectic vehicle with appropriately sized battery at the correct state of charge. This allows rapid testing of the performance of the SST and the breaker. The DC/DC converter is controlled by the integrated energy management platform.

The non-isolated DC/DC is shown in Fig. 32. The unit uses off-the-shelf Wolfspeed module (CRD300DA12E-XM3) in interleaved buck converter mode,where each half-bridge of the module makes up the power stage of a buck converter. By connecting the unit to 750V bus input and delivering power to the load bank, the unit can emulate the power demand of two 150kW charger head-ends. In the system there is a total of three such buck converters, allowing the SST to be loaded up to 900kW. The team validated the electrical and thermal performance of the unit, up to the rated power. In addition, the full power efficiency was found to be 99.5%

Figure 33: Integrated energy management platform graphical user interface.

5.2 Integrated energy management platform

The integrated energy management platform communicates with all components of the EV charging station, including the solid state breakers the SST, the DC nodes (i.e. the DC/DC converters). SST and the DC node controllers are connected to a private network based on Resilient Information Architecture Platform for the Smart Grid (RIAPS) framework [1]. The station operator can use a graphical user interface (GUI) based supervisory control and data acquisition (SCADA) platform to startup/shutdown the SST, start/stop DC node for EV charging, monitor the system parameters, and provide the subsystem components' status. The developed GUI for the platform is shown in Fig. 33. The GUI is developed in NodeRed and communicates with the RIAPS platform using the MQTT protocol. Each component of the system (i.e. SST. DC Breaker, and each DC node) has a local, dedicated RIAPS node (i.e. a BeagleBone single board computer). Each local BeagleBone talks to the component it is connected to in the native protocol (i.e. CAN, Modbus of GPIO HI/LOW signals), while the RIAPS nodes communicate among each other using the MQZero protocol implemented over a LAN network.

5.3 System integration within the shipping container

All components that make up the XFC station are packed up inside the shipping container. Figure 34 shows the system model with all components inside. On the left hand side is the ABB solid state DC circuit breaker. In the middle is the SST. The right hand side houses the MV filters (differential mode choke, common mode choke and the oil filled capacitors) and the MV switchgear. MVAC line enters the shipping container from the bottom, near the MV mechanical switchgear, while the LVDC line going to the DC nodes exits the container from the bottom and under the DC switchgear. One short and one long side of the shipping containers open to allow for air flow into the container. The ABB switchgear pulls air though the front panel facing the open shipping container door and exhausts the air out the back. The SST pulls air in from three sides of and pushes air out the top of the container through an opening in the roof of the shipping container.

Figure 34: System integration within the shipping container. On the left hand side is the ABB solid state DC circuit breaker. In the middle is the SST. The right hand side is the MV filters.

Figure 35: Preparatory work completed prior to the delivery of the shipping container at the NYPA Clark Energy Center site. Left: conduit placement; Middle: placement of Trenwa trenches and concrete for the placement of switchgear. Right: completed installation of the MV switchgear.

6 System Deployment

The system was to be deployed at the Clark Energy Center, in Marcy New York, a secure facility operated by the New York Power Authority (NYPA). This site was ideal for the system deployment because NYPA is a self permitting entity and all personnel at the site are trained on the relevant safety procedures for medium voltage equipment as a part of the their regular duties.

At the NYPA Site, trenching, conduit and cable for entrance and exit between the anticipated R&D shipping container and the 15 kV transformer, were completed. Bonding and grounding procedures all followed in accordance with NYPA requirements. The excavated 'spoils' from digging were evaluated for any contamination, and will be trucked off site for proper disposal. Figure 35 shows some of the preparatory work completed prior to the delivery of the shipping container.

Details of the site layout is shown in Fig. 36. The entire site is fed by a 13.2kV feed coming off an existing tap on a step down transformer feeding an existing building. The MV line is fed to a MV four-way breaker that is operated by NYPA Personnel. This breaker controls the MV line supply to the entire station. The line then feeds the shipping container though an access point at the bottom of the container. Another access

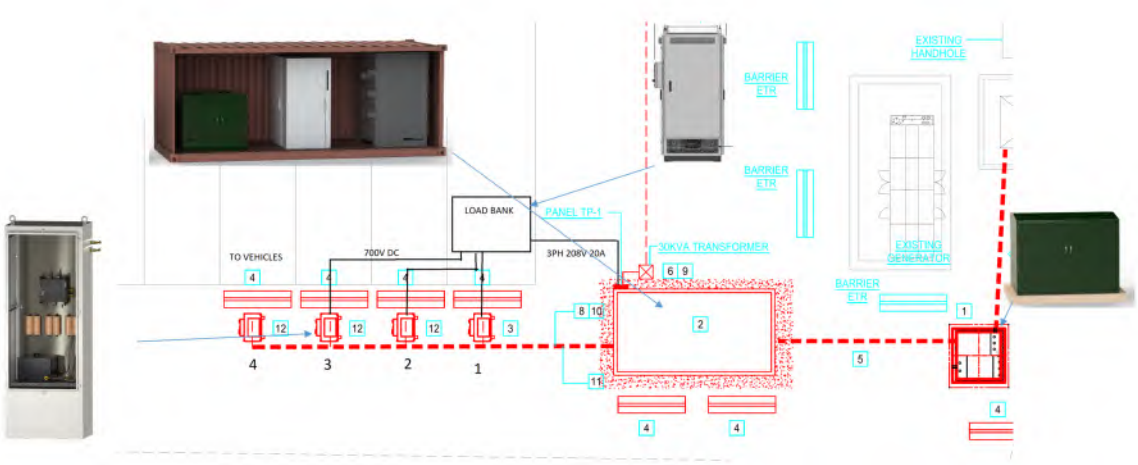


Figure 36: Proposed SST based XFC station architecture

point on the other end of the shipping container delivers the DC lines to the three DC nodes mounted on concrete slabs. A load bank is connected to the three DC/DC converters. Auxiliary 120V/208V power is supplied by a dedicated 3-kVA transformer.

After the system was tested at NC State, it was packaged into a shipping container and transported to the deployment site. Upon arrival, the system was successfully installed. Figure 37 shows the commissioning site during the commissioning process, and Figure 38 depicts the interior of the shipping container during various stages of this process. Due to the sensitivity of the oil-filled isolation transformer (or oil-field transformer), the modules comprising the solid-state transformer were removed for shipping to minimize the risk of damage. During commissioning, these modules had to be reinstalled into the enclosure in the field. This process was time-consuming and exposed the team to potential risks, including possible failures after reassembly.

The deployment commenced on July 10 and was halted on July 14. After the system installation and preliminary testing, the team discovered that several high-frequency transformers had been damaged during shipping. It was determined that proceeding with the system deployment using the existing transformers would be unsafe.

During the preliminary testing stage, an incident occurred where pre-charge capacitors shorted to the frame of the solid-state transformer enclosure. This incident led the team to conduct a root cause analysis to determine the reasons for the failure in the field. The root cause analysis attributed the incident to human error and a failure to adhere to testing procedures. However, during the root cause analysis, the team also identified several contributing factors that have led to the development of best practices that will be followed in all future deployments, thereby reducing the likelihood of future incidents. These best practices are summarized below:

- **Develop site specific test procedure prior to deployment:** The deployment team followed a test procedure tailored for their lab testing during the field deployment. For any subsequent testing,a site-specific test plan must be developed and submitted for feedback and approval. This test plan will cover on-site deployment procedures and emergency protocols. It will detail contingency plans for the deployment process in case of a (sub)system malfunction, specifying which repairs can be conducted in the field and which tests require shipping the (sub)system to a laboratory.
- **Design System for Seamless Deployment:** The team plans to redesign the SST system to

Figure 37: Field deployment of the SST hardware by the research team.

facilitate easier field deployment. First, modifications will be made to the shipping container to enable air intake with closed doors, using a metal mesh opening. This adjustment will allow testing with the doors closed as an additional safety precaution. Second, the power modules constituting the charger will be redesigned, eliminating oil-filled transformers in favor of dry-type transformers. Shipping the power modules within the enclosure, without concerns about oil spillage, will significantly reduce on-site labor and testing requirements. Third, an new enclosure will accommodate all MV chokes and protective devices. This configuration ensures dual layers of protection, where all MV equipment is within an enclosed container and the entire system is within a closed shipping container.

- **Personnel on Site:** By restructuring the extreme fast charger for assembled shipping, the deployment process will be expedited with a more compact team. The on-site team will consist of a researcher familiar with the system design, a professional engineer, and an independent electric contractor familiar with the equipment. All team members must have considerable experience operating the fast charger in the laboratory and will undergo any additional training recommended by NYPA before future deployments. Using a smaller team aims to minimize the likelihood of miscommunication among members.
- **Planning for Contingencies:** In the event of an emergency necessitating the departure of a team member, the deployment will be temporarily halted. A new test plan and procedure will then be submitted to NYPA for approval before resuming work. This report and procedure will detail the system's status, documenting any outstanding tests.

7 Summary

This project has tackled the challenge of designing compact MV XFC stations for EVs. Through the integration of SST technology directly into the MV distribution network, this framework not only streamlines system design but also enhances efficiency by eliminating the need for a traditional step-down transformer. The resulting benefits include reduced footprint, minimized losses, and the elimination of inrush currents during grid black-start scenarios. Furthermore, the incorporation of a shared DC bus enables seamless connection among multiple charging dispensers and storage/generation units, forming a DC microgrid for optimized power sharing with minimal conversion stages. Notably, the inclusion of intelligent SS DCCB ensures enhanced protection, rapidly isolating faulted circuits to maintain operational integrity. Through

Figure 38: Shipping container during various phases of the commissioning process. Left: Shipping container prior to the placement of XFC modules inside the Module rack. Right: Shipping container detail, with SST modules in place.

these advancements, this project lays the groundwork for a more resilient, efficient, and scalable infrastructure to propel the widespread adoption of electric transportation. Within the project scope the team developed and demonstrated the two key technologies proposed: the SST connecting to a 13.2kV feed and the SS DCCB. Both technologies were demonstrated in the laboratory environment, and were shipped and deployed at a field demonstration site in Marcy, NY. Due to the damage of the high frequency transformers during shipping, the system operation was not demonstrated in the field.

Future work includes the refurbishment of the system using oil-free high frequency transformers, followed by a re-deployment of the system in the field. This work will occur outside the scope of this project.

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