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A Planar Quantum Transistor Based on 2D-2D Tunneling in Double Quantum Well Heterostructures

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We report on our work on the double electron layer tunneling transistor (DELTT), based on the gate-control of two-dimensional -- two-dimensional (2D-2D) tunneling in a double quantum well heterostructure. While previous quantum transistors have typically required tiny laterally-defined features, by contrast the DELTT is entirely planar and can be reliably fabricated in large numbers. We use a novel epoxy-bond-and-stop-etch (EBASE) flip-chip process, whereby submicron gating on opposite sides of semiconductor epitaxial layers as thin as 0.24 microns can be achieved. Because both electron layers in the DELTT are 2D, the resonant tunneling features are unusually sharp, and can be easily modulated with one or more surface gates. We demonstrate DELTTs with peak-to-valley ratios in the source-drain I-V curve of order 20:1 below 1 K. Both the height and position of the resonant current peak can be controlled by gate voltage over a wide range. DELTTs with larger subband energy offsets (~21 meV) exhibit characteristics that are nearly as good at 77 K, in good agreement with our theoretical calculations. Using these devices, we also demonstrate bistable memories operating at 77

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K. Finally, we briefly discuss the prospects for room temperature operation, increases in gain, and high-speed.

INTRODUCTION

Electronic devices based on resonant tunneling in semiconductor heterostructures have seen considerable effort ever since Tsu and Esaki[1] proposed the double barrier resonant tunneling diode (DBRTD) in 1973. The device was shortly thereafter demonstrated by Chang, Esaki, and Tsu[2]. In the DBRTD, typically grown in the GaAs/$Al_xGa_{1-x}As$ material system, electrons in a three-dimensional (3D) emitter layer can pass into a 3D collector layer only by first resonantly tunneling through two-dimensional (2D) electron states which are confined in a quantum well (QW) between two narrow barriers. To first order, electrons can tunnel only when their energy and in-plane momentum are conserved[3]. As a voltage is applied between the emitter and collector, the energies of the 2D electrons in the QW are lowered until they align with those of the electrons in the emitter, and tunneling begins to occur. The tunneling stops when the voltage becomes too high for the conservation conditions to be met, causing the DBRTD to exhibit negative differential resistance (NDR). The inherent existence of NDR constitutes one of the highly desirable attributes of resonant tunneling devices, since it makes possible multifunctionality, enabling the same circuit functions to be achieved with fewer devices[4]. A second desirable attribute is the extremely high speed of resonant tunneling: to date DBRTDs are the fastest solid state electronic devices ever measured, having been operated at frequencies of 712 GHz[5,6], and exhibiting switching times of less than 2 ps[7]. The use of semiconductor materials with large conduction band offsets and small effective masses, as well as the use of strained layers, has allowed DBRTDs to show good performance at room temperature[8,9].

However, DBRTDs suffer from the lack of a third control terminal, necessary for electrical isolation between the input and output terminals. This severely limits their usefulness and range of applications. While hybrid devices formed by combining DBRTD structures with conventional transistors circumvent this difficulty, they do so by sacrificing much of the speed advantage of resonant tunneling[10,11]. By contrast, a DBRTD with a third terminal added so as to achieve a true quantum tunneling transistor would be ideal, if it could be made practical. Schemes to add a third terminal to the DBRTD have been of two types. The first type proposes to make electrical contact to the resonant tunneling layer[12,13], which has largely proven problematic[14]. The second type uses *lateral* gate control of the potential of the resonant tunneling layer in a narrow post-shaped DBRTD[15,16], or a DBRTD-like structure entirely laterally constructed in a two dimensional electron gas, where the *one-dimensional* resonant layer is formed by lateral quantum confinement[17,18]. However, such DBRTD-based devices are extremely sensitive to slight variations in lateral dimension, making them nearly impossible to reliably fabricate in the large numbers necessary for real-world applications. We note that this difficulty is shared by many other proposed quantum transistors based on mechanisms other than resonant tunneling, such as single electron transistors[19,20], Aharanov-Bohm type interferometers[21], and quantum cellular automata[22]. While there have been a couple of reports of vertical resonant tunneling transistors which did not require lateral confinement for their operation, these devices either showed surprisingly weak NDR even at low temperatures[23], or did not exhibit a resonant peak in the I-V curve whose voltage position could be controlled by the third terminal[24].

Here we report on a novel three terminal quantum device, the double electron layer tunneling transistor (DELTT), which does not require lateral depletion or lateral confinement but rather is entirely planar in configuration. (Preliminary reports of this work have previously appeared[25,26].) In contrast to the 3D-2D tunneling in a DBRTD, the DELTT's operation is based on 2D-2D tunneling between the two parallel 2D electron layers in a semiconductor double quantum well (DQW) heterostructure. The only critical dimensions reside in the growth direction, thus taking full advantage of the single atomic layer resolution of existing growth techniques such as molecular beam epitaxy (MBE) and/or metal-organic chemical vapor deposition (MOCVD). Because both electron layers of the DELTT are 2D, their energies --and hence the tunneling rate -- are easily controlled by applying a bias voltage to a surface gate, in stark contrast to the DBRTD. The DELTT shows excellent resonant NDR characteristics, with I-V peak-to-valley ratios of ~20:1 at 1.5 K. More importantly, both the height and position of the resonant tunneling I-V peak are controllable by gate voltage over a wide range. A single DELTT exhibits large regions of both negative and positive transconductance, readily enabling multifunctional applications. Different DELTT structures designed for higher temperature operation exhibit nearly as good characteristics at 77 K. Using these devices, we have demonstrated bistable static memory cells, both at 1.5 K and 77 K, which use half as many transistors as their conventional counterparts. We have also demonstrated DELTTs whose features are submicron in size, and hence should have low parasitic capacitances. Theoretical calculations of the I-V curves at different temperatures show fair agreement with the data. Finally, we also discuss proposed modifications of the DELTT so as to achieve high speed room temperature operation.

DEVICE STRUCTURE AND FABRICATION

Devices were processed from three different modulation-doped GaAs/$Al_{0.3}Ga_{0.7}As$ DQW heterostructures grown by molecular beam epitaxy. The GaAs QW widths ranged from 120 to 150 Å, and the $Al_{0.3}Ga_{0.7}As$ barriers between them had a thickness ranging from 100 to 125 Å. Details of the samples are provided in Table 1. While samples G1717 and EA255 had a small difference in electron density between the two QWs, sample G1881 had a rather large difference of 6.0 x 10^{11} cm^{-2}, corresponding to a difference in Fermi energy of ~21 meV. Electrical measurements were performed using both lock-in and DC techniques in a sorption-pumped ^3He system capable of temperatures from 0.3 K to 300 K. The electron densities in each QW were determined by Shubnikov-de Haas measurements.

A schematic of a completed DELTT structure is shown in Fig. 1. The source terminal makes electrical contact to the top QW only, while the drain terminal contacts the bottom QW only. These selective ohmic contacts to the individual QWs are formed by diffusing Au/Ge/Ni to *both* QWs, and then using a fixed DC bias on adjacent Ti/Au surface depletion gates in order to deplete electrons from the QW one does *not* wish to contact[27]. An additional Ti/Au surface gate, placed between the depletion gates, acts as a third terminal and controls the tunneling. Sample G1881 also had a back control gate, the same size as its top control gate and vertically aligned to it.

Because the tunneling cannot be controlled in the ungated regions between the control gate and the depletion gates, in order to achieve good device characteristics the gates must be spaced closely together, minimizing the tunneling leakage current in these

regions. Since the gating resolution of the backgate is given roughly by its distance from the electron layers, it is *crucial* that the backgates be in close proximity to the DQWs. We used our recently developed flip-chip processing scheme, the epoxy-bond-and-stop-etch (EBASE) technique, to place all backgates at a distance of 2.4 μm or less (see Table 1) from the bottom QW. Fig. 2 schematically shows the processing steps used in the EBASE technique, details of which have been given elsewhere[28]. While samples G1717 and G1881 had relatively large features patterned using optical lithography, sample EA255 had submicron features patterned with mutually aligned electron beam lithography on both sides of the epitaxial layers, to be described in more detail below.

OPERATING PRINCIPLE

In the DELTT, resonant tunneling can occur only when there exist states in both QWs with identical energy and in-plane momentum, since these quantities must be conserved in a 2D-2D tunneling event[29]. (In this simple exposition of the operating principle we use the single-electron picture, and ignore inelastic events and electron-electron scattering.) One can determine when this condition is met by sketching the allowed states of the DQW in energy-momentum space, i. e. the dispersion curve. Fig. 3(a) shows the dispersion of a DQW with a higher electron density in the top QW than in the bottom, at a top control gate voltage $V_{TC} = 0$, and a small applied source-drain bias V_{SD} [a] 0. Because both electron layers are 2D, their allowed states each form a paraboloid having states only on the surface, and none in the interior. While the chemical potentials $\mu_{1,2}$ of the two QWs coincide, their subband energies $E_{01,02}$ differ. Thus the paraboloids are offset in energy, no pairs of states of identical momentum and energy exist, and

tunneling does not occur. Tunneling can be switched on by (1) varying the densities of either 2D layer with surface gates, (2) changing the chemical potential difference between the QWs by applying a source-drain bias, or (3) both. Fig. 3(b) shows the dispersion for the first case, when $V_{SD} \cong 0$ and the density of the top QW is decreased via a negative V_{TC} until it equals that of the bottom QW. (To first order, V_{TC} has no effect on the bottom QW until the top QW is completely depleted, since electrons in the QW effectively screen the electric field.) The two paraboloids then coincide, allowing tunneling to occur. This situation corresponds to a peak in the small-signal source-drain conductance G_{SD} as a function of V_{TC}. Fig. 3(c) shows the dispersion for the second case, when $V_{TC} = 0$ and eV_{SD} is increased to equal the difference in Fermi energy E_{F1}-$E_{F2} \equiv \Delta E_F$. Now the two paraboloids again coincide; occupied states in the top QW are now paired with unoccupied states in the bottom QW at the same energy and in-plane momentum, and tunneling can occur. This situation corresponds to a peak in the source-drain current-voltage (I-V) curve. In general, the dispersion curves will coincide when

$$eV_{SD} - C_T V_{TC} \pi h^2/m^* = E_{F1}-E_{F2} = (n_1-n_2)\pi h^2/m^* \quad (1)$$

where C_T is the capacitance per unit area between the top control gate and the top QW, m^* is the electron effective mass, and n_1 and n_2 are the electron densities in the two QWs. In the above we have assumed that the in-plane resistances of the two QWs are negligible in comparison to the tunneling resistance.

At this point the advantages of the DELTT over transistors based on DBRTDs, in which the tunneling is 3D-2D, are readily apparent: (1) the greater restriction in momentum states leads to sharper tunneling resonances, and (2) the density of each 2D layer can be easily controlled by surface gates, allowing an entirely planar device

configuration. We note that while the physics of 2D-2D tunneling in DQWs was first explored in Ref. 29 and has been previously investigated by others[30,31], the use of such structures for electronic device applications, particularly their source-drain I-V curves, has received relatively little attention[32,33].

LOW TEMPERATURE ELECTRICAL CHARACTERISTICS

We now discuss the measured operating characteristics of DELTT G1717, a fairly large device with ΔE_F = 2.1 meV. (See Table 1.) Fig. 4(a) shows the small-signal source-drain conductance G_{SD} vs. top control gate voltage V_{TC} at 0.3 K, for $V_{SD} \cong 0$. A strong tunneling resonance appears, ~50 times larger than the background conductance. This happens at V_{TC} = -0.12 V, when the top QW has been partially depleted so as to have the same density as the bottom QW. The device thus exhibits a strong negative transconductance for V_{TC} > -0.12 V, which actually exceeds the positive transconductance occurring for V_{TC} < -0.12 V. [See Fig. 4(a) inset.] As will be shown below, this property is extremely useful for circuit applications[32]. Fig. 4(b) shows the source-drain I-V for several fixed values of V_{TC}, all at 0.3 K. A resonant tunneling peak occurs when the offset in chemical potential μ_1-μ_2 is equal to the difference in Fermi energies between the two QWs. (The V_{SD} required to achieve this condition is actually larger than $\Delta E_F/e$, due to a significant resistive voltage drop under the depletion gates.) At higher V_{SD} the current drops dramatically, resulting in a strong NDR. Peak-to-valley ratios approaching 20:1 are observed. More importantly, *the position of the resonance shifts strongly with* V_{TC}, clearly demonstrating the gate control of tunneling[34]. In contrast to DBRTDs, the resonance occurs only for one polarity of V_{SD}. Though not shown for this sample,

sufficiently negative V_{TC} moves the resonance to negative V_{SD}. No hysteresis in the I-V curves was observed, and these curves change little as the temperature is increased, until ~10 K. Finally, although the height of the resonance also changes with V_{TC}, the on-resonance value of the source-drain conductance $G_{SD} = I_{SD}/V_{SD}$ is nearly constant. This is shown in Fig. 5(a), where we have replotted the data of Fig. 4(b) as G_{SD}.

The sharp increase in negative current occurring at V_{SD} = -0.025 V is due to μ in the drain becoming sufficiently large that electrons can travel over the potential barrier imposed by the back depletion gate. This accounts for the increase in current being independent of V_{TC}. A more negative back depletion gate bias V_{BD} monotonically moves the current increase to a more negative V_{SD}, as shown in Fig. 5(b). The increase in current at V_{SD} = 0.04 V has a similar origin and behaves analogously with top depletion gate bias V_{TD}.

DEMONSTRATION OF A BISTABLE MEMORY

To show the multifunctionality of the DELTT, we demonstrated a bistable static memory cell[24], consisting of DELTT G1717 in series with a 1 kΩ load resistor, as shown in Fig. 6(a). Fig. 6(b) shows a sketch of the I-V curves of DELTT G1717 at three different V_{TC}, along with the resistor's load line. Because of the DELTT's NDR, at intermediate V_{TC} the resistor load line intersects the I-V curve at two stable points A and B, and one unstable point C. By sweeping the gate above an upper threshold or below a lower threshold, the solution to the circuit construction admits only one stable point, A' for high V_{TC} and B' for low V_{TC}. The circuit will then latch in that particular stable point, remaining there once V_{TC} is returned to an intermediate value. Thus at intermediate V_{TC}

the state of the circuit depends on its past history, causing it to behave as a bistable static memory cell. Fig. 6(c) shows an oscilloscope trace of the input and output voltages of this circuit at 1.5 K. A triangular wave is fed to the input, causing the output to switch to the low or high state whenever the write thresholds are reached, clearly demonstrating the memory effect. The on-off output voltage ratio is ~10:1, allowing simple biasing and good relative noise immunity. Because of the DELTT's NDR, this memory requires only one transistor and one load resistor, in contrast to the two transistors and two load resistors required in a conventional unipolar static memory cell.

HIGHER TEMPERATURE OPERATION

To first order the DELTT's operating temperature is limited by the leakage current appearing due to thermally-assisted tunneling between the two QWs in the ungated regions between the control and depletion gates. Roughly, this occurs when kT is comparable to ΔE_0, the energy difference between the two QW subbands. Thus for DELTT G1717, the G_{SD} vs. V_{TC} peak-to-background ratio degrades to 2:1 at ~40 K, when $kT \approx \Delta E_F = 2.1$ meV.

Because DELTT G1881 has a much larger ΔE_F of 21 meV, its operating temperature is much higher. Fig. 7(a) shows G1881's I-V curve for $V_{TC} = 0$ V and a back control gate voltage $V_{BC} = 1.2$ V. At 1.6 K the peak-to valley ratio is ~8:1. However, in contrast to DELTT G1717, the peak-to-valley ratio remains as high as 4:1 at 77 K. (Again, though not shown, the strength and position of the resonance depend strongly on V_{TC}.) Fig. 7(b) shows G_{SD} vs. V_{TC}, at $V_{BC} = 0$. The peak-to-background ratio is ~25:1 at 1.6 K, but only degrades to ~10:1 at 77 K. Indeed, we have observed ratios of ~2:1 at

temperatures as high as 170 K. With sufficient engineering of the growth structure, and a choice of material systems with larger conduction band offsets such as InGaAs/InAlAs, room temperature operation should be achievable. To show that useful circuit functions can be achieved at higher temperatures, we also demonstrated a bistable memory at 77 K using DELTT G1881, shown in Fig. 7(c). The circuit is the same as that shown in Fig. 6(a), except that it has a V_{DD}= 155 mV and a 4 kΩ load resistor.

THEORETICAL MODELING

To test our understanding of the data, we calculated the tunneling current as a function of the source-drain voltage V_{SD} for sample G1881. Here we take the limiting case where the in-plane resistances of the two QWs are negligible and the entire voltage drop occurs across the tunneling barrier, so that the chemical potentials of the top and bottom QWs are offset by eV_{SD}. We note that this limiting case solution can easily be extended to geometries in which the in-plane resistances are significant, by applying a differential transmission line model[35,36].

The tunneling rate is calculated to second order in the transfer integral J via a two-step perturbation theory[37]. Here $2J$ is the energy splitting between the lowest subbands of the two QWs when their densities are balanced. The calculation includes the back current, i. e. current due to thermally excited electrons moving in a direction opposite to the bias. The transition matrix calculation includes interactions with the screened potentials from impurities, acoustic and optical phonons, and other electrons, both before and after tunneling. For the case of our sample, where the barrier is undoped and so can be considered to contain an insignificant number of impurities, a detailed

knowledge of the impurity distribution is not needed. Rather, the effect of impurity interaction is entirely contained in the damping parameter Γ of the intermediate states. The transition to the intermediate state can be virtual or real (i.e., resonant). For the short range potentials appropriate to the case of our structure, the energy and momentum dependence of Γ can be neglected, allowing us to use Γ as the only adjustable parameter and greatly simplifying the calculation. The contribution from acoustic phonons includes the deformation potential and piezoelectric scattering, and remains very small compared with the LO-phonon contribution except at extremely low temperatures. The phonon parameters used here have been published previously[38,39]. We note that the contribution from long-wavelength phonons tends to be canceled through interference, since the phonons modulate the energies in both QWs in phase.

Fig. 8 shows the calculated total tunneling current I_{SD} as a function of V_{SD} for sample G1881 at both 0 K and 77 K. Here we have used the parameters Γ = 10 meV, J = 0.0014 meV, and a tunneling area (equal to the control gate area) of S = 0.001 cm^2. We have used the same Γ at both 0 K and 77 K, since Γ is not expected to vary significantly over this temperature range. The contributions from impurity-assisted tunneling alone are shown separately. While inelastic (non-impurity) contributions are very small at 0 K, they are seen to become significant at 77 K. The calculation shows qualitative agreement with the data of Fig. 7(a), although some important differences are present. First, in the data, the resonant peak in I_{SD} occurs at a significantly higher V_{SD} (~35 mV) than in the calculation (~23 mV). This can be attributed to there being a significant in-plane resistive voltage drop in the QWs, and is in qualitative agreement with calculations which include an external load resistor in series with the tunneling structure. Such a series

resistance tends to skew the I-V curve towards higher V_{SD}. Second, the turn-up in current after the NDR region occurs at rather low V_{SD} in the data, long before any current increase in the calculation. Again, this is attributed to the leakage of current over the top depletion gate at sufficiently high V_{SD}, as discussed earlier. Finally, we note that the choice of Γ = 10 meV provided reasonable agreement with the data; however, we expect that the actual tunneling Γ in the sample is somewhat narrower, and that the resonant current peak in the data is artificially broadened by the in-plane resistance of the QWs. Preliminary results on structures with a greater ΔE_F indicate that good performance at room temperature is achievable. Details will appear elsewhere[37].

SIZE AND SPEED CONSIDERATIONS

In any electronic device, two considerations come into play in determining its operating speed. The first is the intrinsic speed, determined by fundamental electron transport parameters such as, in conventional MOSFETs, the transit time across the gate, in turn determined by the electron saturation velocity. The second is the role of parasitics, which typically take the form of an RC time constant determined by parasitic capacitance between the gates and the semiconductor channel, and by the resistance of both the gate metal and the channel. In an actual device, the intrinsic speed can only be realized by reducing the parasitics sufficiently that they no longer constitute the limiting factor. This requires making both the channel and the gate very short (micron or submicron) and rather wide (of order 10 to 100 microns).

Because of the extraordinarily high oscillation frequencies (approaching THz) measured for DBRTDs, it is expected that the DELTT, which also operates via resonant

tunneling, will have a similarly high intrinsic operating speed. While a detailed equivalent circuit model has yet to be developed, the fact that the switching mechanism is tunneling across an extremely thin (~100 Å) barrier generally indicates high speed operation. In order to take advantage of these ultra-high intrinsic speeds in actual devices, however, it is necessary to be able to fabricate DELTTs with submicron gate lengths and contact-gate spacings, so as to sufficiently reduce the parasitic effects to the point where they no longer play a role.

Fortunately, the EBASE flip-chip processing scheme is sufficiently flexible and robust that such demanding geometries can be easily achieved. We have recently extended the EBASE technique so as to enable electron beam writing of patterns on both sides of the epitaxial layers, aligned to one another to an accuracy of a few 100 Å. Fig. 9(a) shows a scanning electron micrograph side view of a test structure produced with electron beam writing. A pair of gates on the back side of the structure --which becomes the exposed surface after the EBASE process-- is aligned to a pair of metallic gates on the front side, now buried beneath the epitaxial layers against the epoxy. Alignment of the patterns was achieved by using the same alignment mark for both writing steps, a micrograph side view of which is shown in Fig. 9(b). The alignment mark was placed in a recess etch, leaving only 0.25 microns of epitaxial material between it and the back surface. This is sufficiently thin that the electron beam can easily penetrate it, allowing the easy location of the alignment mark.

In Fig. 10 we show a scanning electron micrograph top view of DELTT EA255, produced by mutually aligned, dual side electron beam lithography in a manner similar to that just described. However, for EA255 a double stop-etch step was used, whereby the

first stop etch layer was removed in the second etch step. This reduced the total thickness of the epitaxial layers to only 0.235 microns, so that there was no need to recess the electron-beam alignment marks. As can be seen in Fig. 10, this is sufficiently thin that a good scanning electron micrograph image is obtained of all three gates, even though the top-side gates --which appear slightly darker in the figure-- are buried beneath the epitaxial layers. The width of the gates and the mesa-etched channel is 10 microns. The control gate length is 1.0 micron, while both depletion gates are 0.5 microns long and spaced 0.5 microns away from the control gate. (The ohmic contacts are far away, and lie outside of the margins of the figure.)

Fig. 11 shows I_{SD} vs. V_{SD} curves obtained from DELTT EA255 for several different top control gate voltages V_{TC}, at 0.3 K. The data is qualitatively similar to that obtained for G1717, with a strong NDR, peak-to-valley ratios of order 10:1, and a resonant current peak which is controllable by V_{TC} over a wide range. (In this case the range of V_{TC} values shown is sufficiently large that the resonant current peak moves from positive V_{SD} to negative V_{SD}.) The current is an order of magnitude lower than in G1717, owing to the much smaller area of the device. A small extra resonance is apparent at V_{SD} $\approx$ 7 mV, and is believed to be due to fringing fields from the depletion gates bringing about an unintentional tunneling condition over a very small area. Due to a hysterisis with respect to gate voltage in this sample, the QW densities existing when the data of Fig. 11 was taken are probably somewhat different from the equilibrium values quoted in Table 1. Nevertheless, overall the data establishes that working DELTTs with submicron feature sizes can be easily fabricated. While the ohmic contacts on this prototype device were too far away for it to be suitable for high speed operation (see Table 1), a similar

geometry with a wider channel and with ohmic contacts brought to within a micron or two of the depletion gates, currently in fabrication, is expected to have sufficiently low parasitics to yield a gate-channel RC time constant corresponding to frequencies of well above 100 GHz. We emphasize that, although this device has submicron gates, its electrical characteristics do not sensitively depend on the precise lateral dimensions of these small features.

ADDITIONAL CONSIDERATIONS

Although current trends in commercial microelectronics are towards a steadily decreasing operating voltage and operating current in order to reduce power consumption, the voltages and currents of the DELTTs described in this work are too low to be of practical use. This is primarily because electrical circuit noise could be large enough to cause unintentional switching. Fortunately, these problems are not insurmountable, and the approaches appropriate to their alleviation are clear. First, the same methods used to increase the current densities in DBRTDs can be used to increase the operating current of the DELTT. By using tunneling barriers of significantly smaller thickness, on the order of 30 - 50 Å rather than the present 100-125 Å, it is expected that the currents can be increased by a couple of orders of magnitude, into the mA range. The use of material systems with large conduction band offsets such as InGaAs/AlAs[8] and InAs/AlSb[9] has also been shown to significantly increase current densities in DBRTDs. Second, the requirement for room temperature operation of a large ΔE_F between the two QWs, will simultaneously also serve to increase the operating voltage: the use of InGaAs/AlAs and InAs/AlSb structures should enable Fermi energy differences of order

100 meV, significantly closer to what is considered practical. As for the gain of the DELTT, it can likely be significantly increased by bringing the control gates closer to the QWs. Finally, we note that a modified DELTT structure, incorporating a third "collector" layer of electrons at a much lower potential than the other two layers, could allow the operating voltage to be increased significantly. In this three-layer DELTT the 2D-2D tunneling between the first two layers would still be controlled via a gate voltage. However, after tunneling into the second layer, electrons would continue through a second tunneling barrier into the third collector layer, undergoing a large voltage drop in the process. This would also serve to significantly increase the gain. Such three layer structures are currently under investigation[40].

Finally, we note that while the EBASE process is very flexible and reliable, other fabrication methods may be more appropriate for industrial scale fabrication. A variation on the EBASE method which uses depletion etches of the correct depth rather than depletion gates would simplify the device connection, as well as removing unwanted paths to ground which could hinder high speed operation. Fabrication methods which utilize ion-implanted backgates[31] rather than a flip-chip technique, while inconvenient for laboratory scale experiments, may prove advantageous for mass production.

SUMMARY AND CONCLUSION

In summary, we have demonstrated a novel quantum tunneling transistor, the DELTT, based on the gate-control of 2D-2D tunneling. Because the structure is entirely planar, the DELTT can be reliably fabricated in large numbers. At 1.5 K we demonstrate peak-to-background ratios of ~50:1 in source-drain conductance vs. gate voltage, and

peak-to-valley ratios of ~20:1 in source-drain current vs. source-drain voltage. Highly density-imbalanced structures exhibit operating characteristics nearly as good at 77 K, and prospects for room temperature operation with different material systems appear good. Using a single DELTT and a load resistor, we demonstrate bistable memories at 1.6 and 77 K. Theoretical calculations of the I-V curves exhibit good agreement with the data. Finally, DELTTs with mutually aligned electron-beam written submicron gates on both the front and back sides have been demonstrated, indicating that devices with low parasitics can be fabricated. Elsewhere we have given a preliminary report on the use of the DELTT to construct digital logic gates[26].

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Sampl	w_{QW} Å	t_b Å	n_t 10^{11} cm^{-2}	n_b 10^{11} cm^{-2}	DE_F meV	d_{epi} mm	d_t mm	d_b mm	w_{chan} mm	L_{cont} mm	L_{depl} mm	$L_{cont\text{-}depl}$ mm	$N_{ohm\text{-}depl}$ squares
G1717	150	125	2.0	1.4	2.1	2.40	0.13	2.20	500	40	10.0	5.0	0.10
G1881	120	125	8.0	2.0	21.3	0.64	0.12	0.50	500	200	10.0	5.0	0.10
EA255	120	100	5.6	6.6	3.5	0.235	0.09	0.12	10	1.0	0.5	0.5	3.05

TABLE 1. Sample parameters for DELTT devices G1717, G1881 and EA255. Given are QW widths (w_{QW}), tunnel barrier thickness (t_b), built-in electron densities for the top and bottom QWs (n_t and n_b) and the resulting difference in Fermi energy ($DE_F = |E_{F1} - E_{F2}|$), when no biases are applied. Also listed are the total epitaxial layer thickness (d_{epi}) after the EBASE process, distances from the bottom surface to the bottom QW (d_b) and from the top surface to the top QW (d_t), device channel width (w_{chan}), and the length of the control gate(s) (L_{cont}) and depletion gates (L_{depl}). The lateral distance between the control and depletion gates ($L_{cont\text{-}depl}$), and the number of squares between the ohmic contacts and depletion gates ($N_{ohm\text{-}depl}$) are also tabulated.

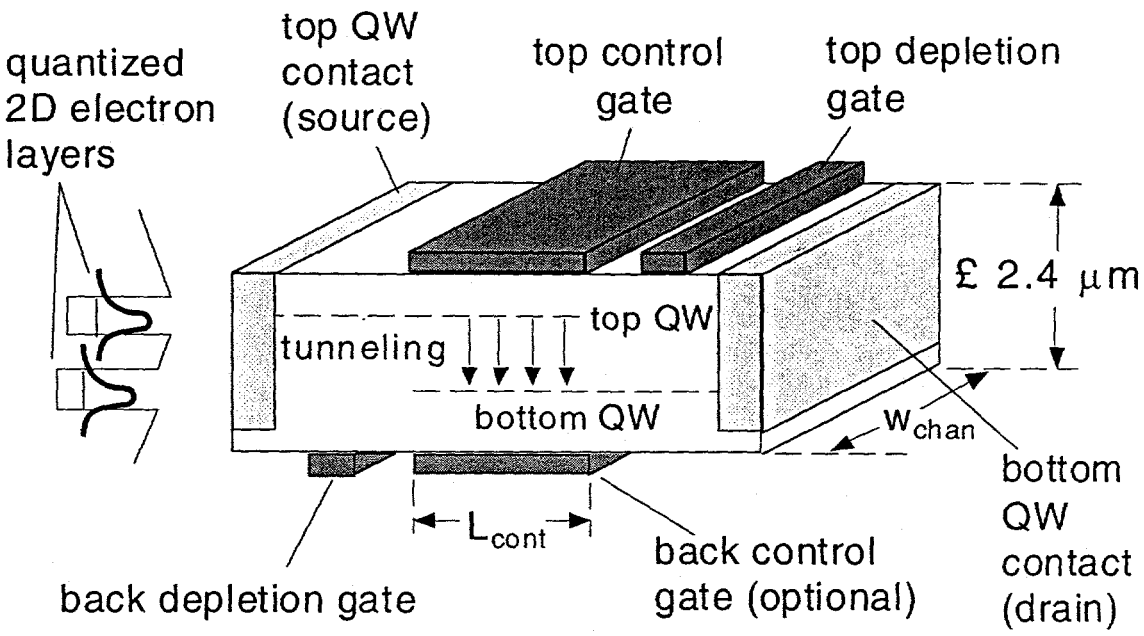

FIG. 1. Schematic of the double electron layer tunneling transistor (DELTT), not to scale. The source makes electrical contact to the top QW only, while the drain contacts the bottom QW only. The total thickness of the epitaxial layers ranges from 0.235 microns for sample EA255 to 2.4 microns for sample G1717. w_{chan} is the width of the channel, and L_{cont} is the length of the control gate(s). A sketch of the DQW energy band diagram is shown at left.

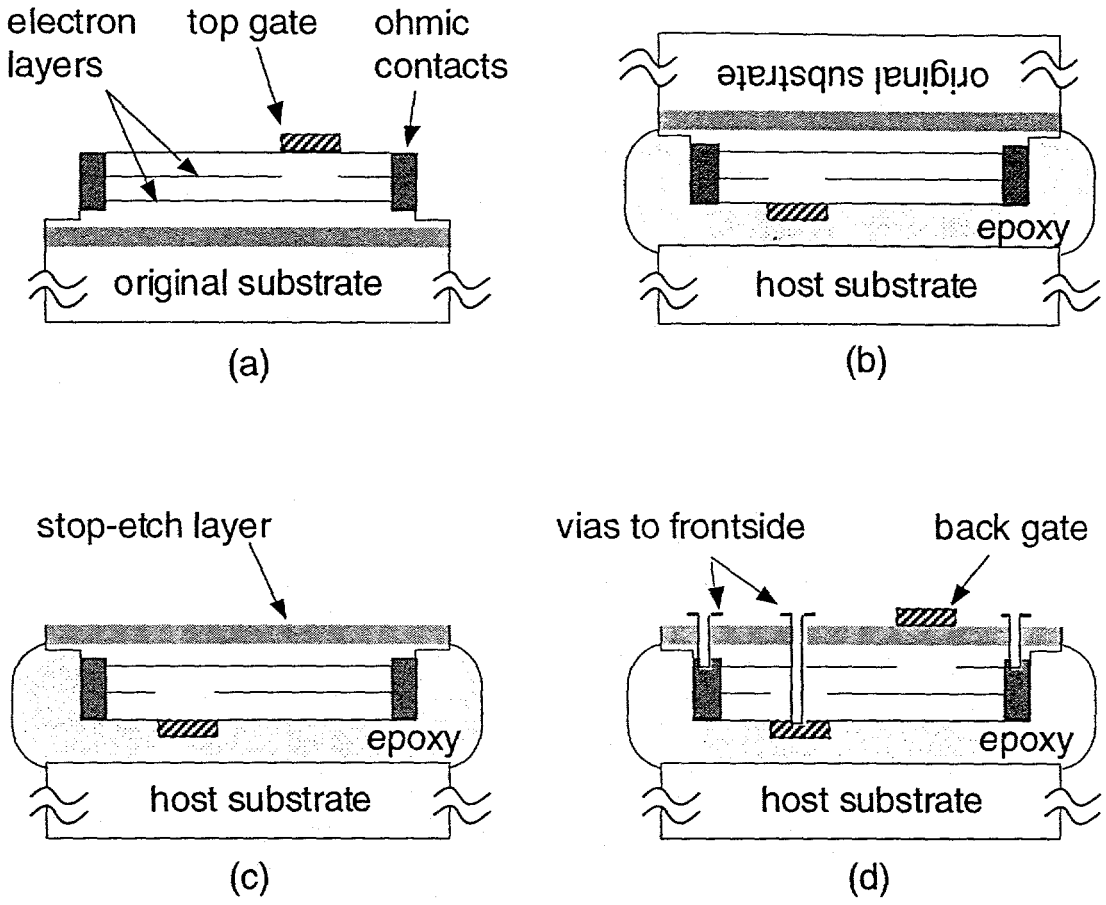

FIG. 2. Sketch of the different steps involved in the epoxy-bond-and-stop-etch (EBASE) technique. (a) After growth of the DQW structure including a stop-etch layer, the front-side processing is performed, including mesa etching and deposition of ohmic contacts, and top-side gates. (b) The sample is then epoxied top-side down onto a GaAs host substrate. (c) The original substrate is then removed, first by lapping until ~20 microns remain, and then by a high selectivity chemical etch which stops on the stop-etch layer. (d) The back-side processing is then performed, including deposition of back-side gates and etching of vias to the front-side contact pads. At no time in the EBASE process is it necessary to handle an unsupported thinned sample, and all bonding wires are attached to a single side of the sample.

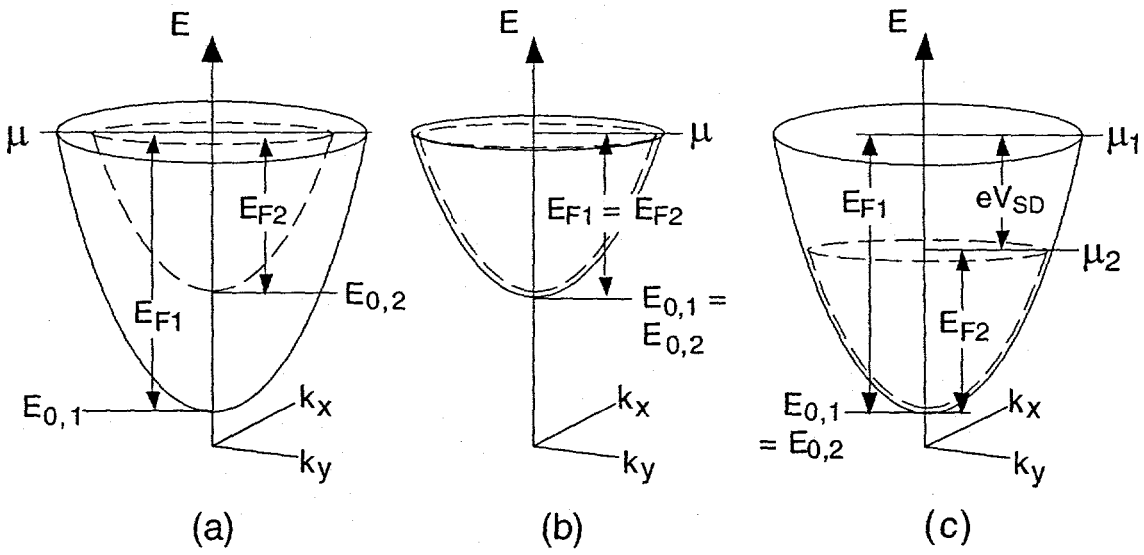

FIG. 3. Sketches of the allowed electron states of a DQW heterostructure in energy vs. in-plane momentum space, i. e. the dispersion curve. The two paraboloids have states only on the surface and none in the interior. (a) shows the case for a density-imbalanced DQW, with $V_{SD} = V_{TC} = 0$. Because no pairs of states of identical energy and momentum exist, tunneling cannot occur. In (b) V_{SD} remains at zero, but V_{TC} has been made sufficiently negative for the two paraboloids to coincide, allowing tunneling to occur. In (c) $V_{TC} = 0$, but V_{SD} has been increased so as to make the paraboloids coincide, again allowing tunneling current to flow.

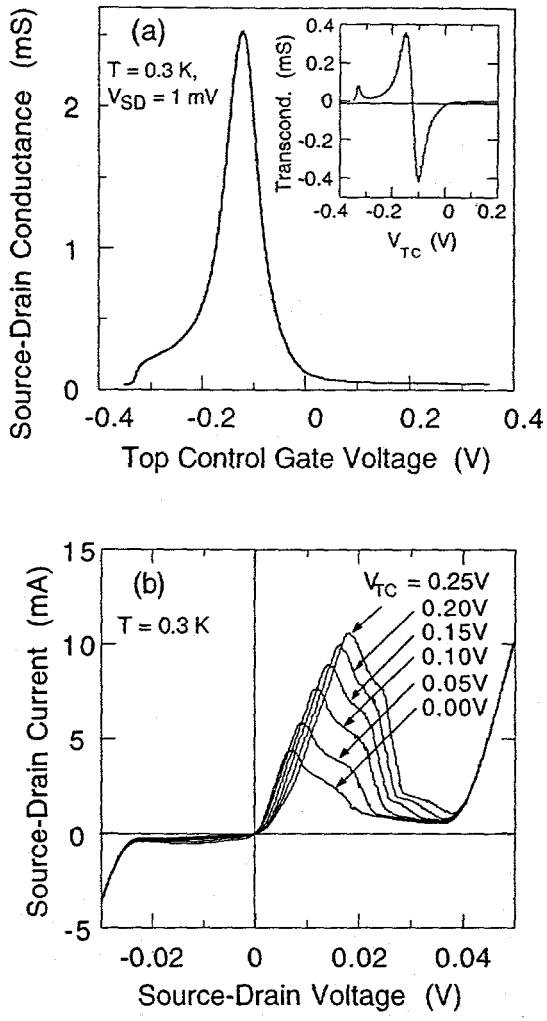

FIG. 4. Electrical characteristics of DELTT G1717 at 0.3 K. (a) G_{SD} vs. V_{TC} for V_{SD} = 1 mV; top depletion gate voltage V_{TD} = -0.35 V; and back depletion gate voltage V_{BD} = -4.5 V. Inset shows the small-signal transconductance, obtained by taking a derivative of the data in (a). (b) Source-drain current I_{SD} vs. source-drain voltage V_{SD} for several values of V_{TC}. Both the height and position of the resonant current peak can be controlled by V_{TC}. To prevent electrons from leaking over the depletion-gate barriers, the depletion gates were biased to V_{TD} = -0.52 V and V_{BD} = -6.5 V.

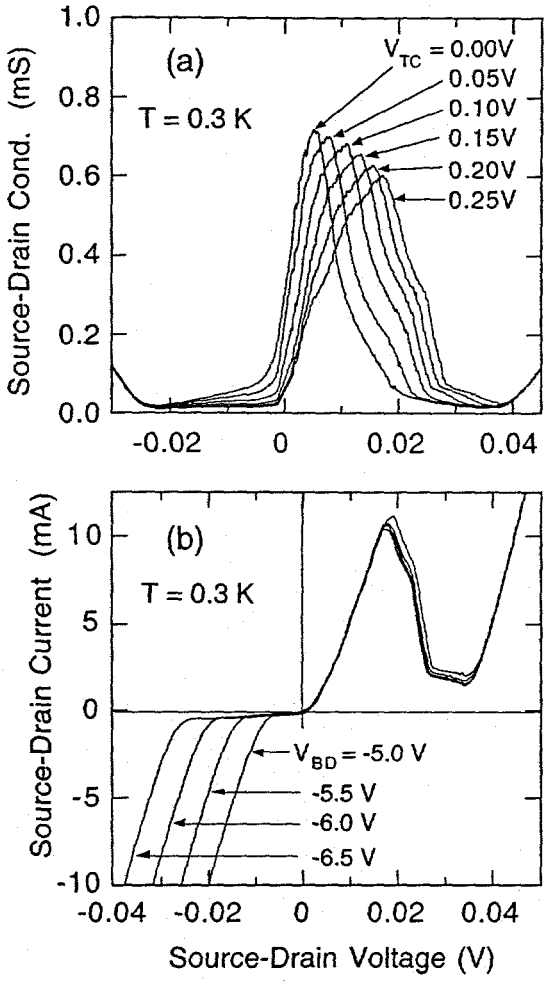

FIG. 5. Additional electrical characteristics of DELTT G1717. In (a) is shown the data of Fig. 4(a), only plotted as source-drain conductance $G_{SD} = I_{SD}/V_{SD}$ as a function of V_{SD}. The size of the conductance peak stays relatively constant with V_{TC}. (b) shows I_{SD} vs. V_{SD} for V_{TC} = 0.25 V and V_{TD} = -0.52 V, at several different back depletion gate voltages V_{BD}. The position of the sharp increase in negative current is seen to depend linearly on V_{BD}, indicating that the increase is due to electrons passing over the backgate-induced potential barrier when V_{SD} is sufficiently high.

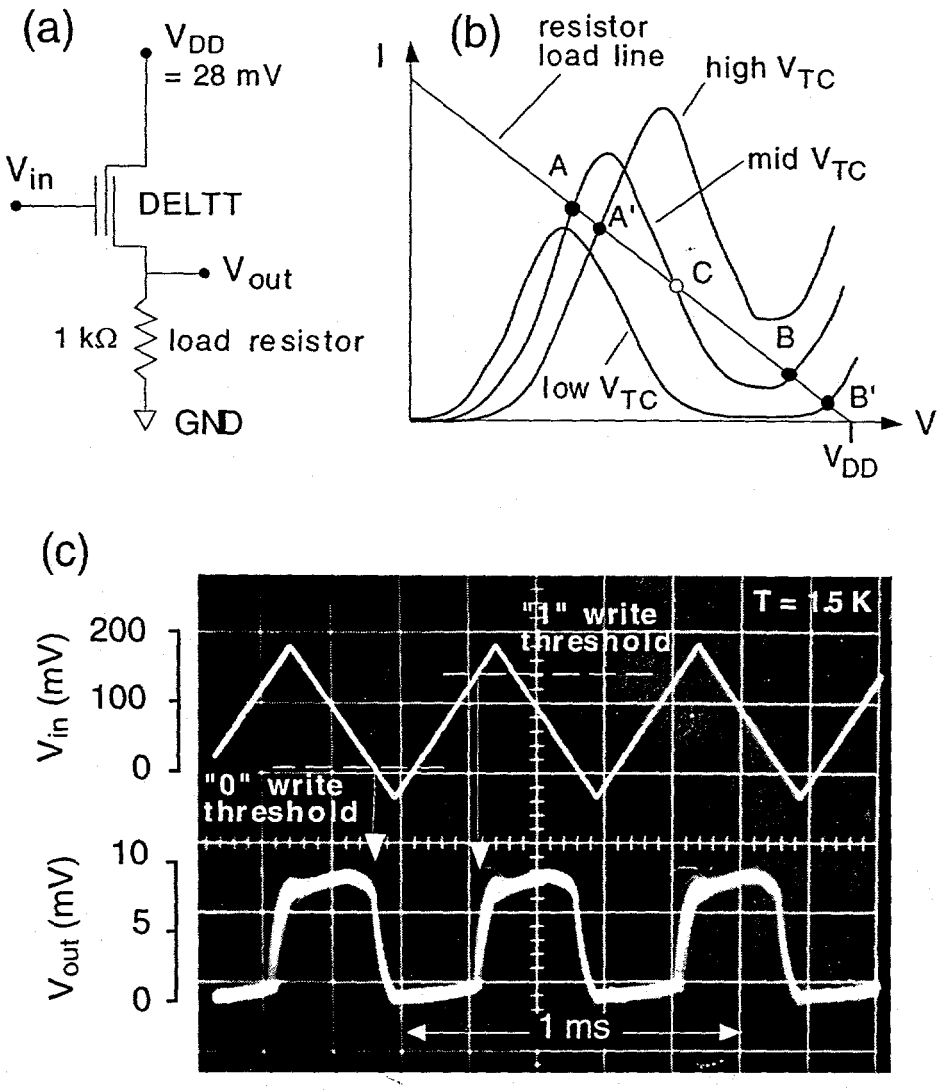

FIG. 6. (a) Bistable memory circuit using a single transistor, DELTT G1717. (b) Sketch of DELTT G1717's I-V curves at three characteristic values of V_{TC}, and the resistor load line. For intermediate values of V_{TC}, the circuit has two stable operating points A and B. When the gate voltage is raised above an upper threshold or below a lower threshold, the circuit has only one stable operating point, A′ or B′. (c) Oscilloscope data taken at 1.5 K, demonstrating that the circuit behaves as a memory. Whenever the input voltage crosses one of the thresholds, the output switches its state. Here V_{TD} = -0.52 V and V_{BD} = -6.5 V.

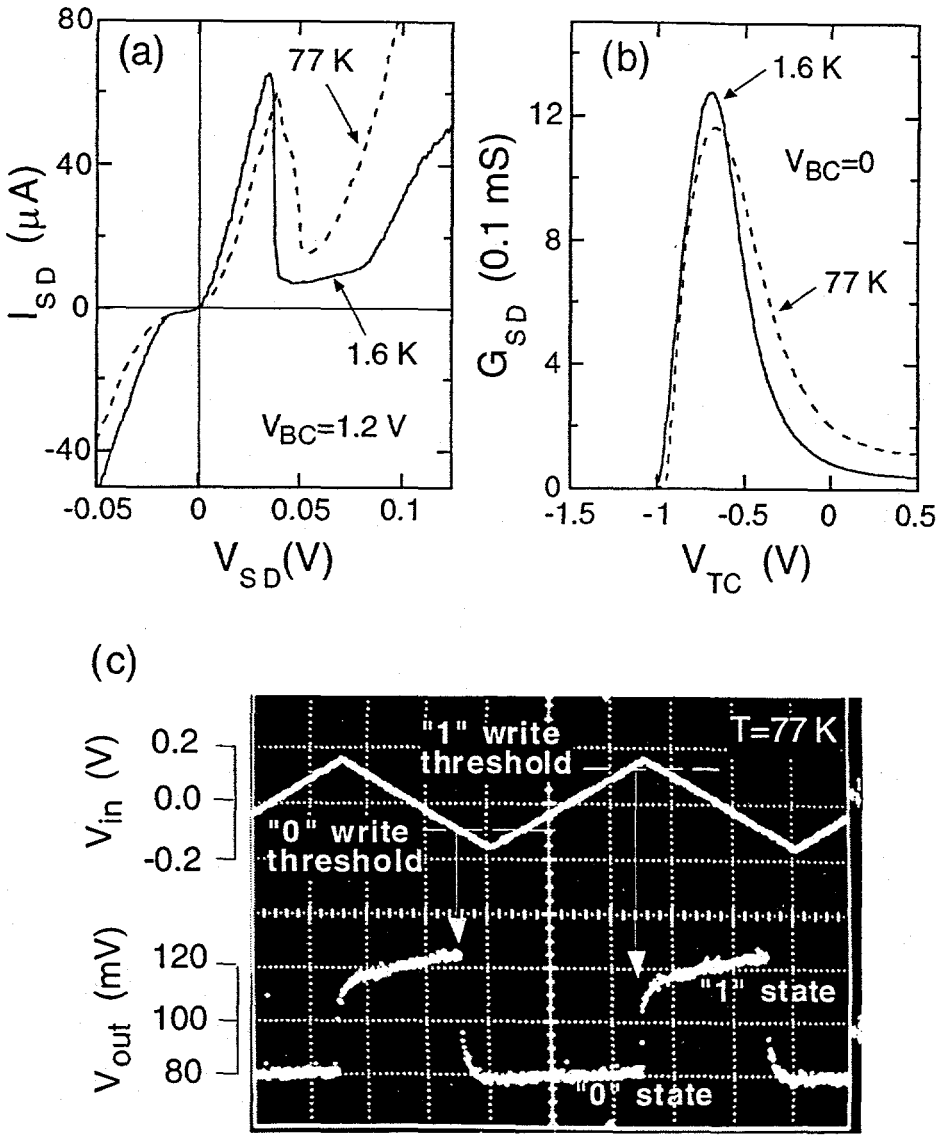

FIG. 7. Electrical characteristics of DELTT G1881, which had a large density imbalance (ΔE_F = 21 meV) for higher temperature operation. (a) shows the I-V curve, and (b) shows the small signal G_{SD} vs. V_{TC}, both at 1.6 K and 77 K. The characteristics change little between 1.6 and 77 K. (c) Demonstration of bistable memory circuit similar to that of Fig. 6(a), but using DELTT G1881 and operating at 77 K. For this circuit V_{DD} = 155 mV and the load resistor was 4 kΩ. For (a), (b) and (c) V_{TD} = -1.3 V and V_{BD} = -2.7 V.

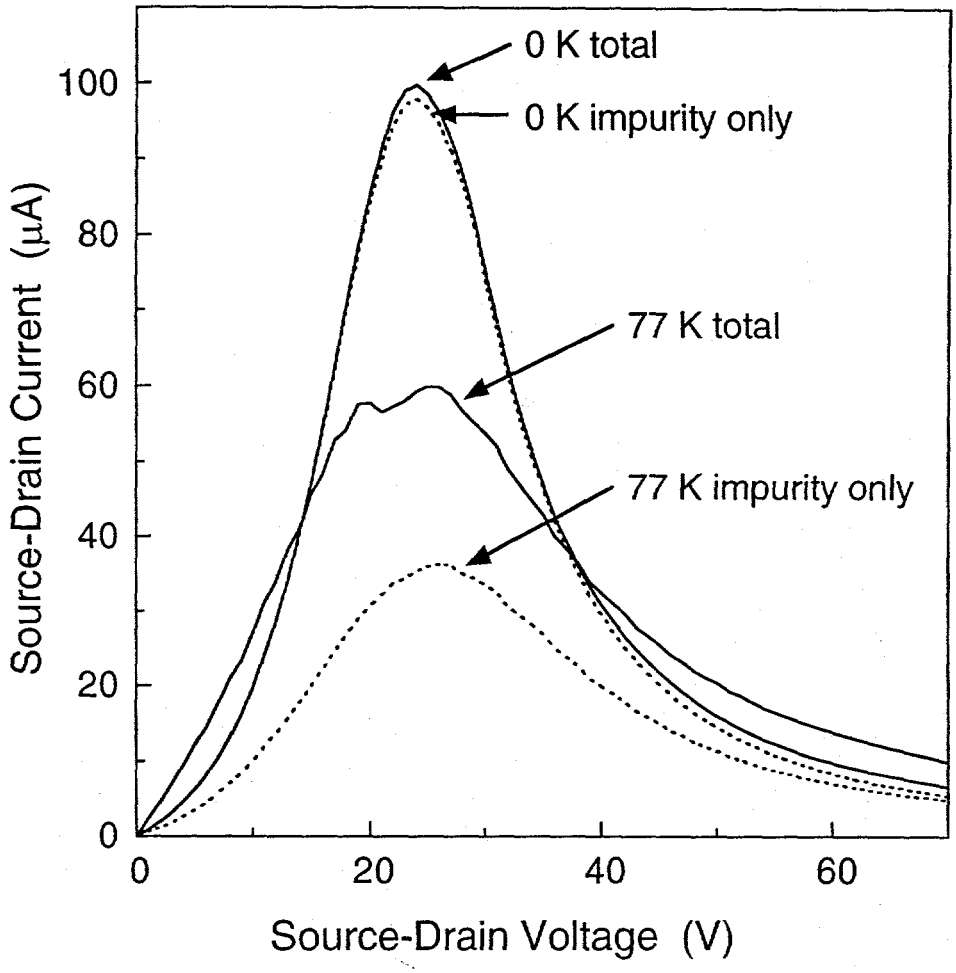

FIG. 8. Theoretical calculations of the I-V curves of DELTT G1881, using a two-step perturbation theory, for both 0 and 77 K. The dashed lines are the contributions from impurity scattering only, while the solid lines also include contributions from scattering with acoustic and optical phonons, and electron-electron scattering. The damping parameter Γ is 10 meV.

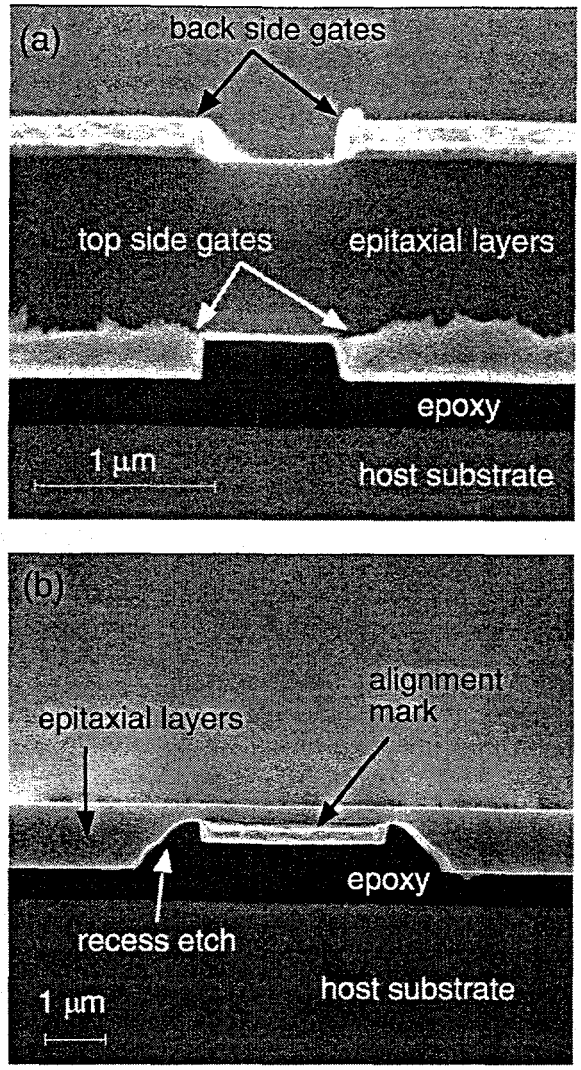

FIG. 9. Scanning electron micrograph side views of an epoxy-bond-and-stop-etch (EBASE) test structure. (a) A pair of electron-beam written Ti/Au split gates on the backside of the epitaxial layers, aligned to another pair of split gates on the front side. Because the EBASE process is a flip-chip technique, the original top surface ends up buried beneath the epitaxial layers, against the epoxy. The irregularities in the top gate metal are due to cleaving. (b) The Ti/Au alignment mark used to write the structure in (a), which was originally placed in a recess etch on the front surface. After flipping of the structure, the epitaxial material remaining after the stop-etch is sufficiently thin that the electron beam can easily penetrate it from the back side, allowing the same alignment mark to be used for the writing of the backside gate patterns.

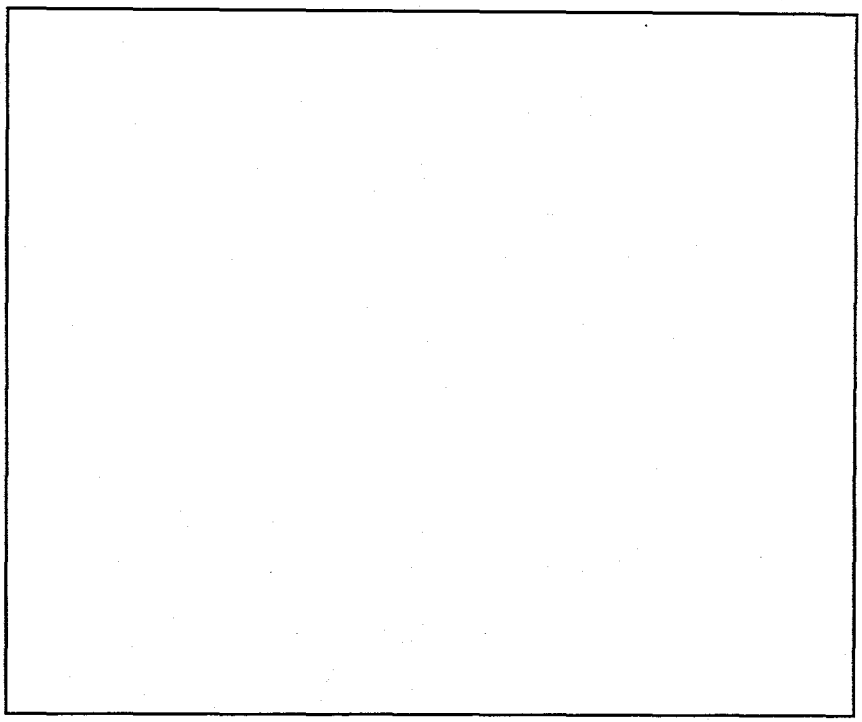

FIG. 10. Scanning electron micrograph top view of DELTT EA255. Because the thickness of the epitaxial layers is only 0.235 microns, the electron beam can easily penetrate them, making the mesa and top side gates clearly visible even though they lie on the other side. Because the back depletion gate lies on the exposed surface of the structure, it is slightly brighter than the two top gates.

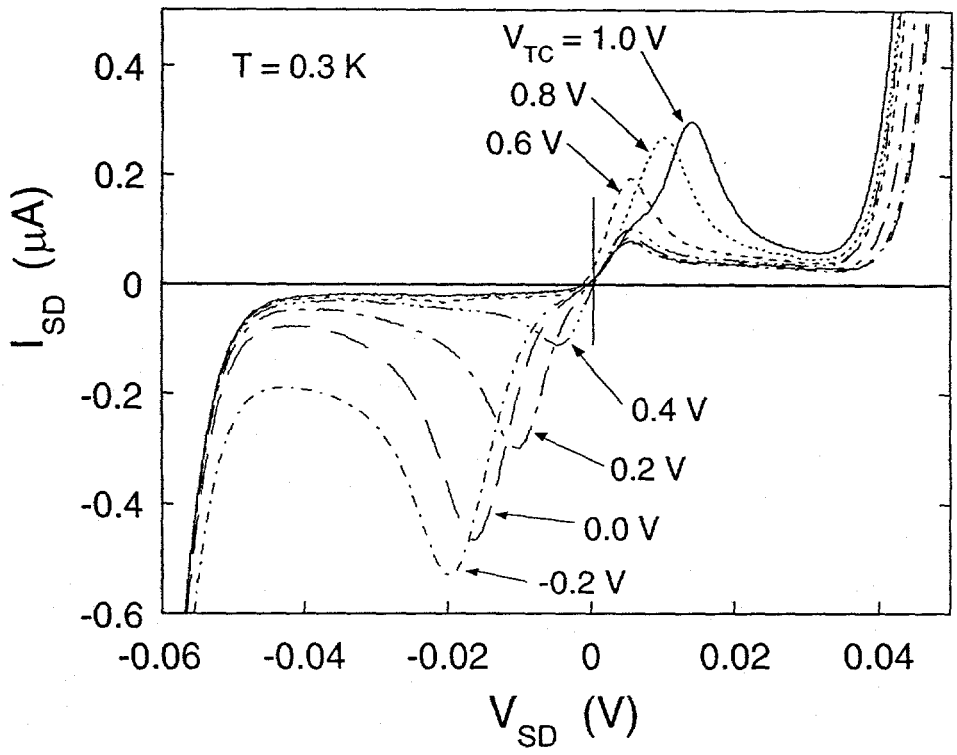

FIG. 11. Electrical characteristics of DELTT EA255, the device shown in Fig. 10, at 0.3 K. Shown are the source-drain currents I_{SD} as a function of source-drain bias V_{SD} at several top control gate voltages V_{TC}. The position and height of the resonant current peak is clearly controlled by V_{TC}, demonstrating that the DELTT can be produced in submicron geometries with low parasitics, and is clearly a scalable device.