Zero Voltage Switching AC-DC Converter Based on Zero State Modulation (ZSM)

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Abstract— In this paper, a half-bridge building block that can achieve soft switching across the complete operating range while operating under fixed frequency is proposed. In addition, dead-beat model predictive controls to control the same are also proposed. The proposed converter, referred to as zero-state modulated (ZSM) converter, uses a zero state, enabled by a small auxiliary switch, to achieve soft-switching. The approach allows lower switching loss, controlled dv/dt, small filter inductor, fixed frequency operation allowing interleaving to reduce filter capacitor. A single half-bridge building block can used to realize a ZVS DC-DC converter or multiple of these building blocks can be used to achieve soft switching 1-phase or 3-phase AC-DC converters.

Keywords—Zero voltage switching, soft switching, dc/dc converter, ac/dc converter, predictive controls, dead-beat controls.

I. Introduction

The non-isolated DC-AC converter is a requirement in several applications such as PV, storage, and electric drives etc. In addition, a 1-phase AC-DC converter is one of the main building blocks in cascaded H-bridge based MV converters. Since the DC-AC converter is such a critical component, it is desirable to optimize it in terms size, cost, and performance. With Si IGBTs, such AC-DC converters are normally operated in the range of 5-20 kHz. The advent of SiC MOSFETs have enabled operation at > 20 kHz. However, the upper bound on switching frequency is still dictated by the switching loss and the dv/dt induced noise. The switching loss can be reduced through soft switching approaches, either zero-voltage switching (ZVS) or zero-current-switching (ZCS). However, ZVS is required to address dv/dt related issues.

In literature, there are two basic approaches to implement ZVS AC-DC converter. The first approach relies on additional auxiliary resonant circuits on the DC side, Fig 1(a) [1]. The resonant stage increases the blocking voltage of the main switches to 1.1 pu (per unit). The converter is bidirectional, but the power factor is restricted to +/- π/3. A modified switching scheme to increase the control region to +/- π/2 is proposed in [3] but it will increase the switching frequency F_s of the main switches. The second approach relies on zero voltage transition (ZVT) by controlling the filter inductor current to oscillate between opposite polarities such that the main switches are turned-on when the current is flowing in the corresponding anti-parallel free-wheeling diode (FWD) [2], Fig 1(b). The second method does not need any auxiliary circuits but uses a variable frequency-based method called triangular current modulation (TCM) technique, shown in Fig 1(b), to achieve ZVS. The switching frequency can vary from 1x to 15x. A modified scheme is presented where the variation in F_s can be limited to 3x [4]. With TCM, the current, ripple increases to 200 % compared to 5-10% in traditional converter, resulting in a smaller inductor. However, it means an increase in the size of the filter capacitor. Interleaving is used to limit the capacitor size but achieving interleaving with variable frequency is complex to implement [5].

In this paper, a half-bridge building block that can achieve ZVS across the complete operating range while operating under fixed frequency is proposed. Multiple of these half-bridge building blocks are proposed to realize novel ZVS AC-DC. The schematic, operating principle, control algorithm based on dead-beat model predictive controls are explained and C-HIL results verifying the converter operation is presented. A comparison with standard approaches is also presented. Experimental results using a 1.0 kV converter are also presented to demonstrate the proposed converter.

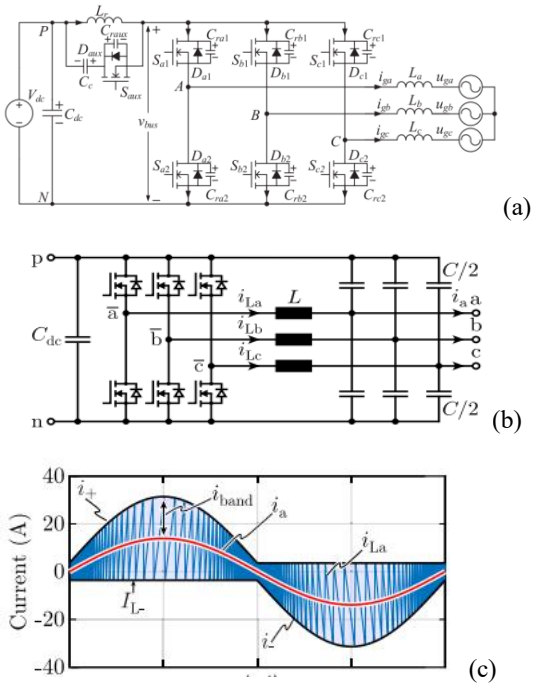

Fig 1: (a) ZVS AC-DC Converter with DC side auxiliary [1]. (b) ZVT AC-DC converter with Triangular Current Modulation (TCM) [2]. (c) Triangular Current Modulation (TCM) [2].

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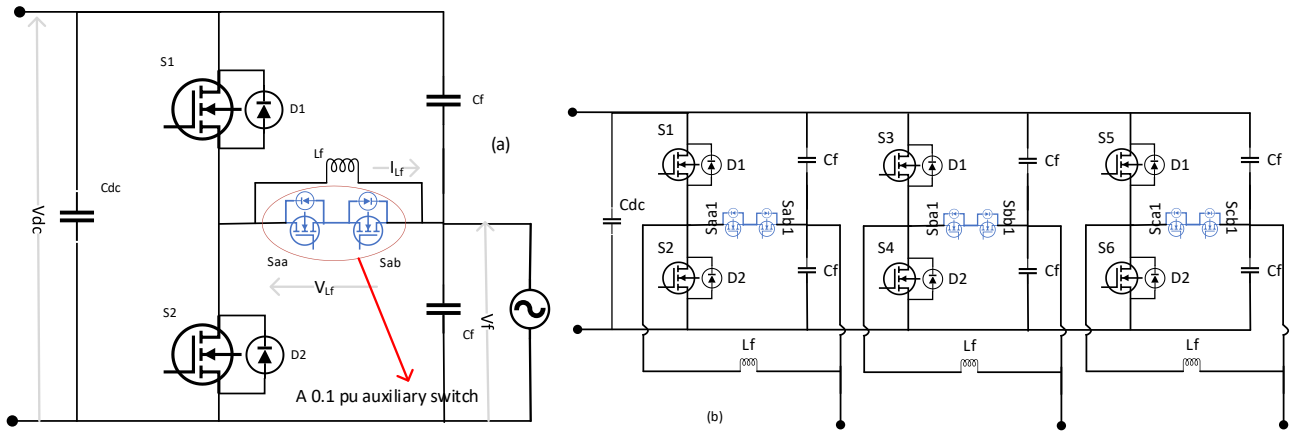

Fig 2: Schematic of proposed zero state modulation (ZSM) AC-DC Converter. (a) Basic building block – a half bridge (b) AC-DC Converter in 3-phase 3-wire configuration.

II. Proposed Converter Topology and Operation

A. Topology

The proposed zero state modulation (ZSM) AC-DC converter configuration is shown in Fig 2. A half-bridge with an auxiliary switch, a filter inductor, and filter capacitors forms the basic building block of the proposed approach as shown in Fig 2 (a). The auxiliary switch is an AC switch connected across the filter inductor and could be achieved by connecting two switches in common emitter or common collector configuration. The AC switch must block 1.0 pu (per unit) voltage but it must only handle <0.1 pu of the line current. The basic building block is standalone even form control point of view as explained later. This approach allows extension of this principle to achieve multiple configurations, such as a 3-phase 3-wire version, shown in Fig 2(b), 1-phase DC/AC inverter, 3-ph 4-wire inverter.

B. Operation

The operating principle will be explained for a single half-bridge, as a 1-phase or a 3-phase converter will just be combination of multiple of these half-bridge blocks and each of these bridges operate independently. The operation of the proposed topology is like a TCM [2] converter except with the addition of zero state. Typically in a half-bridge converter, a voltage of $V_{dc}+V_f$ or - V_f is applied across the filter inductor L_f. However, with the additional auxiliary switch it is possible to apply 0 V across the filter inductor, which hereby will be referred to as "zero state". The zero state will allow the converter to operate with fixed F_s which in turn will allow interleaving. In addition, the bias current maintained in the filter inductor during the zero state will ensure ZVS turn-on of the main switches as will be explained here.

The operation is illustrated using the half bridge shown in Fig 2**Error! Reference source not found.** (a), with power being delivered from V_{dc} to V_f. The conceptual waveforms are shown in Fig 3. Let the initial current in the inductor be a small negative bias current, I_{Lf_zs}, such as -0.1 pu. At this instant, all the main switches are turned off and the inductor current is flowing through the auxiliary switch *Saa* and FWD of *Sab*. At start of *t1*, the aux switch is turned off and the current transitions to the

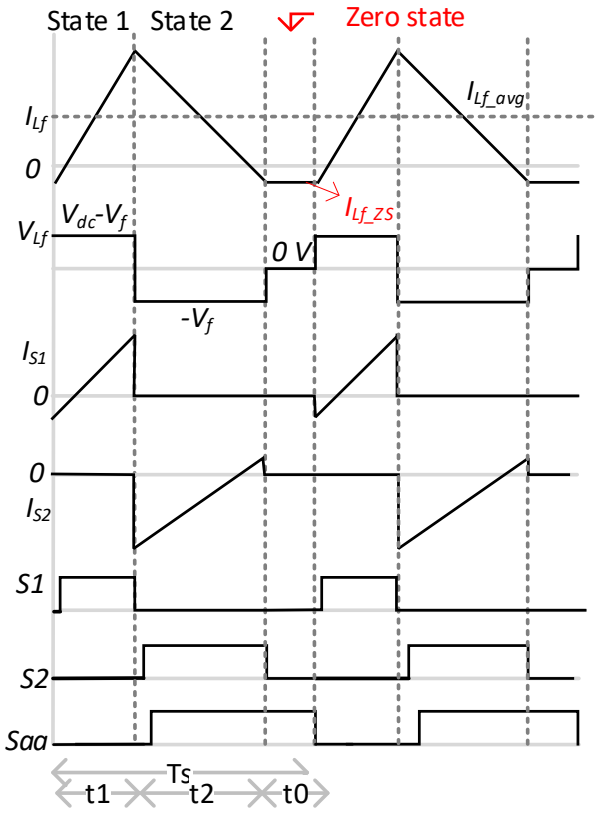

Fig 3: Conceptual switching waveforms of proposed ZSM converter in half-bridge configuration operating in boost mode.

FWD of *S1*. The aux switch will have quasi-ZVS turn-off. Since the current is flowing through the corresponding FWD at this point, *S1* will have ZVS turn-on. *S1* is on to apply a voltage of $(V_{dc}-V_f)$ for a time *t1*, where *Vdc* is the DC link voltage and V_f is the filter capacitor voltage. The inductor current will turn positive and transfer to *S1* from its FWD. At the end of *t1*, the current will reach I_{pk}. *S1* is now turned off with quasi ZVS. The current will transition to FWD of *S2*. *S2* can now be turned on

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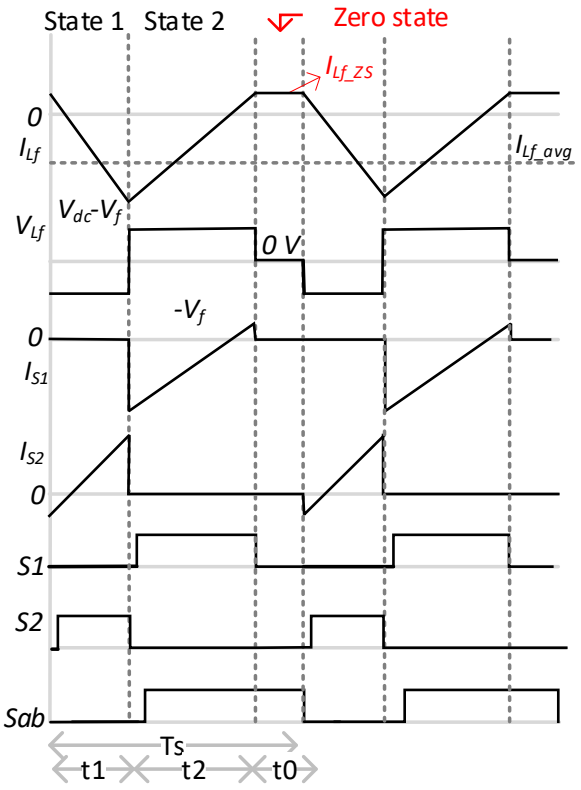


Fig 4: Conceptual switching waveforms of proposed ZSM converter in half-bridge configuration operating in buck mode.

with ZVS. In addition, the aux switch *Saa* is turned on after a short delay. Since the FWD across the *Saa* is forward biased, *Saa* will be turned on with both ZVS and ZCS. These switches *S2*, and *Saa* will be on till the current reaches zero-state current I_{Lf_zs}. At this instant, the switch *S2 is* turned off with quasi-ZVS. The current will transition to *Saa* and will be in that state, *t0,* for the remainder of that switching cycle. In the selected operating mode, I_{Lf_zs} is ensuring ZVS turn-on of *S1,* which is not possible in traditional continuous conduction mode (CCM) and discontinuous conduction mode (DCM) of operations.

The operating waveforms for reverse power flow (power flowing from V_{dc} to V_f or buck mode) is shown in Fig 4. Compared to forward power flow, the polarity of the average inductor current changes to negative and the polarity of the zero-state current I_{Lf_zs} changes to positive. In this case, I_{Lf_zs} is enabling ZVS turn -on of *S2*.

In a 1-phase converter, two half bridges will be operated in a similar way but with current references of opposite polarity. It is shown above that the operating principle applies for both positive and negative power flow. Hence it can be assumed, that the ZVS can be achieved over the four-quadrants in a 1-phase converter. Similarly, the operating principle can be extended to 3-phase 3-wire or 4-wire systems.

As explained above, all the switches including the auxiliary switch achieve soft switching. The dv/dt can be controlled by adding a small capacitor across the auxiliary switch (*Saa* & *Sab*).

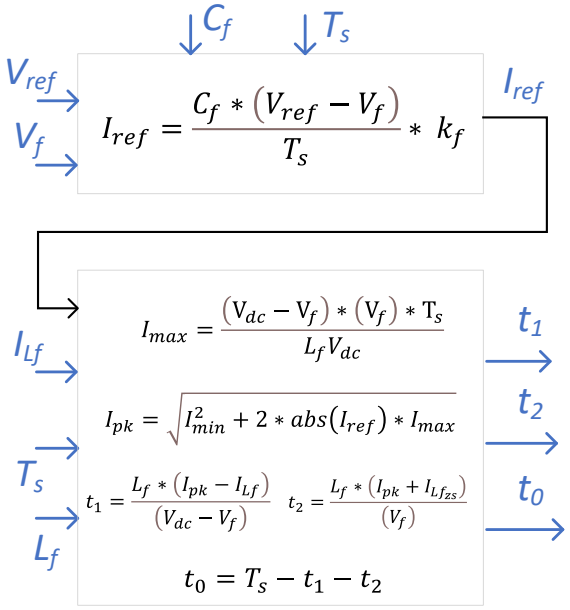


Fig 5: Dead-Beat Model Predictive Control (DB-MPC) schematic of the proposed converter.

The inductor will operate with 200 % peak-to-peak ripple compared to the mean current in the inductor. In a traditional converter the ripple is typically 10-20%. Operating with high current ripple allows to reduce the filter inductor value by 10-20 x compared to traditional converter. The filter inductor however must handle twice the peak current of the traditional converter. Hence the reduction in inductor size, which depends on LI^2, will be 3-5 x. Increased current ripple implies increased filter capacitor size. However, the proposed approach allows the converter to operate with fixed frequency, which will enable use of interleaving technique to reduce the filter capacitor size. The fixed frequency approach will also simplify EMI filter design.

III. Dead Beat Model Predictive Controls

In the proposed operating mode of the converter, the inductor current has a huge ripple and in addition, within each switching cycle the inductor current must be controlled to reach I_{Lf_zs} at the end of the two active states. Hence, Dead-Beat Model Predictive Control (DB-MPC) technique is selected to generate cycle-by-cycle control of inductor current I_{Lf}. In DB-MPC, the converter model is used to generate duty cycles for all the switches. The converter model for the current control loop is just the filter inductor. For desired average current I_{ref} and the measured inductor current I_{Lf}, the timings for each state are derived using (1-2).

$$t_1 = \frac{L_f * (I_{pk} - I_{Lf})}{(V_{dc} - V_f)}, \quad t_2 = \frac{L_f * (I_{pk} + abs(I_{Lf\_zs}))}{(V_f)}, \quad t_0 = T_s - t_1 - t_2 \tag{1}$$

where $I_{pk} = \sqrt{I_{Lf\_zs}^2 + 2 * abs(I_{ref}) * I_{max}}$,

$I_{max} = \frac{(V_{dc} - V_f) * (V_f) * T_s}{L_f V_{dc}}$, V_{dc} is the DC bus voltage, V_f is the filter capacitor voltage, I_{Lf_zs} is the desired current during the zero state and T_s is the switching time period.

If I_{ref} is negative,

$$t_1 = \frac{L_f * (I_{pk} + I_{Lf})}{(V_f)}, \quad (2)$$

$$t_2 = \frac{L_f * (I_{pk} + abs(I_{Lf\_zs}))}{(V_{dc} - V_f)}$$

In case filter capacitor voltage control is desired, the model will now include the filter capacitor. The voltage control loop will generate the current reference for the current loop.

$$I_{ref} = \frac{C_f * (V_{ref} - V_f)}{T_s} * k_f \quad (3)$$

where V_{ref} is the filter capacitor desired voltage, and C_f is the filter capacitor value. K_f is the factor ($0<K_f<1$) determining how quickly filter capacitor is reached. It is typically chosen to be around 0.3 to reach the desired value in 4-5 cycles. The DB-MPC scheme including the voltage and current loop is shown in Fig 5. The scheme is implemented once every switching cycle.

IV. Converter Design

The converter design involves selection of filter inductor, filter capacitor and zero-state current.

A. Filter Inductor Design, L_f

The objective of the filter inductor selection in to ensure desired current is delivered even during the worst-case condition where the difference between DC bus voltage and filter capacitor voltage is minimum. Accordingly, the filter inductor selection depends on the values of minimum DC bus voltage V_{dc_min}, peak filter capacitor votlage V_{f_pk}, switching frequency F_s and desired maximum average current in the inductor $I_{avg,max}$.

$$L_f = \frac{(V_{dc\_min} - V_{f\_pk}) * (V_{f\_pk})}{I_{max} V_{dc\_min} F_s}, \quad (4)$$

where $I_{max} = 2 * (I_{avg,max} - I_{Lf\_zs})$ is the maximum current in the inductor.

B. Zero state current, I_{Lf_zs}

The objective of the selection of zero state current is to ensure ZVS turn on the main switch while accounting for the dead time, t_d. The first condition to ensure ZVS is that the energy stored in the inductor has to be larger than the energy required to charge the equivalent device output capacitance.

$$L_f I_{LF\_ZS}^2 > C_{equiv} V_{dc}^2, \quad (5)$$

where C_{equiv} is the sum of device capacitances of top and bottom devices *S1* and *S2* and any external capacitance added to control dv/dt.

The second condition for selecting I_{Lf_zs} is related to the dead time. Considering the worst case di/dt of the inductor current $di/dt_{max} = max\left(\frac{(V_f)max}{L_f}, \frac{(V_{dc} - V_f)max}{L_f}\right)$ the time available for the turn on the main switch is $\frac{abs(I_{Lf\_zs})}{di/dt_{max}}$. The dead time must be less than the time available as given by the following equation.

$$abs(I_{Lf\_zs}) > t_d * di/dt_{max}, \quad (6)$$

$$where\ di/dt_{max} = \frac{(V_{dc} - V_f)_{max}}{L_f}$$

C. Filter capacitor, C_f

The filter capacitor selection is to limit the voltage ripple to be less than the allowed voltage ripple, V_{pp_max} and is given by the following equation.

$$C_f > \left(\frac{I_{max} - I_{max\_avg}}{2}\right) * \frac{T_s}{2} * \frac{1}{V_{pp\_max}} \quad (7)$$

V. Controller Hardware-in-Loop (C-HIL) Results

A 1-phase converter shown in Fig 6 is implemented in C-HIL using Typhoon™ with the following parameters: L_f =55 uH, C_f = 40 uF, I_{Lf_zs} = 20 A and *Fs* = 10 kHz. The DC bus is maintained at 2000 V and the grid votlage is set at 1200 V rms. The converter operational results are shown in Fig 8. Initially the grid is just delivered reactive power to the filter capacitors. The converter when activated to deliver active power. The current reference for the converter is in phase with the grid votlage. The grid current is lagging the voltage because of the reactive power to be delivered to the filter capacitor from the grid. As shown in the figure, the converter can deliver sinusoidal currents. The current reference is later changed by 180 deg to absorb active power. The immediate change in inductor current can be observed. The < 2 cycle response is due to the DB-MPC controls employed. In the zoomed-in waveforms for the I_{Lf}, the large current ripple and the small bias current of 20 A can be

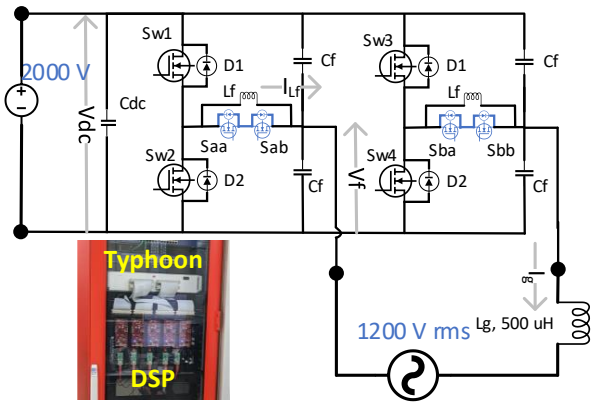


Fig 6: Schematic of 1-ph converter used implemented in C-HIL using Typhoon.

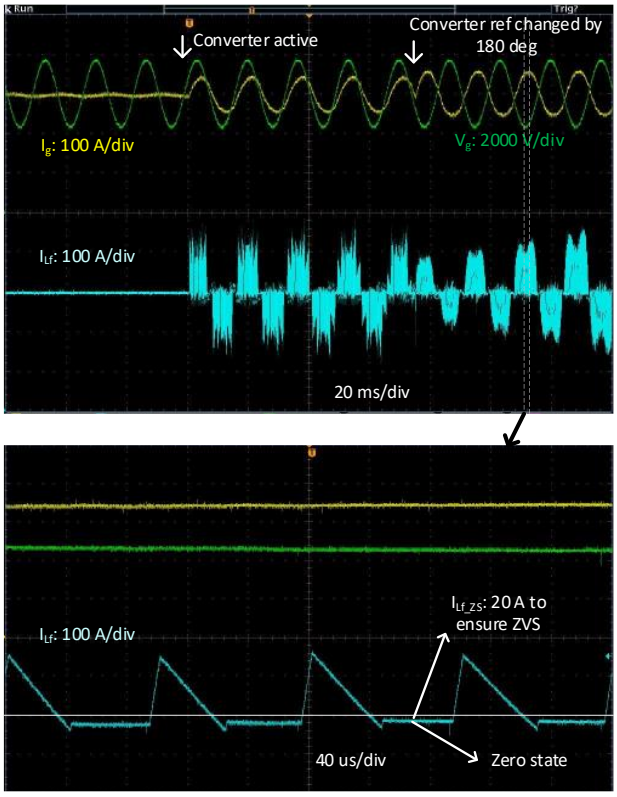


Fig 8: Results of 1-ph ZSM AC-DC converter at 2000 V DC, 50 kW. Bottom is zoomed-in waveform.

observed. The bias current ensures ZVS of all switches as explained in Section II.

VI. Experimental Setup

As shown in Fig 7a, a 2 kV DC half-bridge converter operating in boost mode will be used to demonstrate the proposed operating scheme. The main switch is 3300 V, 450 A, Si IGBT from Infineon. The auxiliary switch is made up of two 3600 V 50 A Si IXYS MOSFETs connected in common emitter fashion. The auxiliary switch is 30 x smaller in size and cost compared to the main switch as shown in Fig 7b. The boost converter is designed to deliver 240 kW. The filter inductor is chosen to be 1 mH, 450 A to deliver 200 A average current while operating at 1200 V on the low voltage side and 1800 V on the boost side, and with switching frequency of 1 kHz (as per Eq. 4). The filter capacitors on either side are chosen to be 720 uF to maintain peak-to-peak ripple at <5%. The experimental test setup as shown in Fig 7a consists of a 2 kV DC source and a resistor load. The image of the test setutp is shown in Fig 7d.

The results of the proposed ZSM converter at 1 kV and 20 kW are shown in Fig 9. The inductor current is shown in plot 1, voltage across swtich S2 is shown in plot 2, voltage across switch S1 is shown in plot 3, voltage across the inductor and the auxilairy switch is shown in plot 4 and output voltage across the load is shown in plot 5. The objective of the converter controls is to maitain 1040 V on the boost side. Intially the capacitors on either terminal are pre-charged to 800 V. At t1, the converter starts operating and charges the output capacitor to 1040 V. At

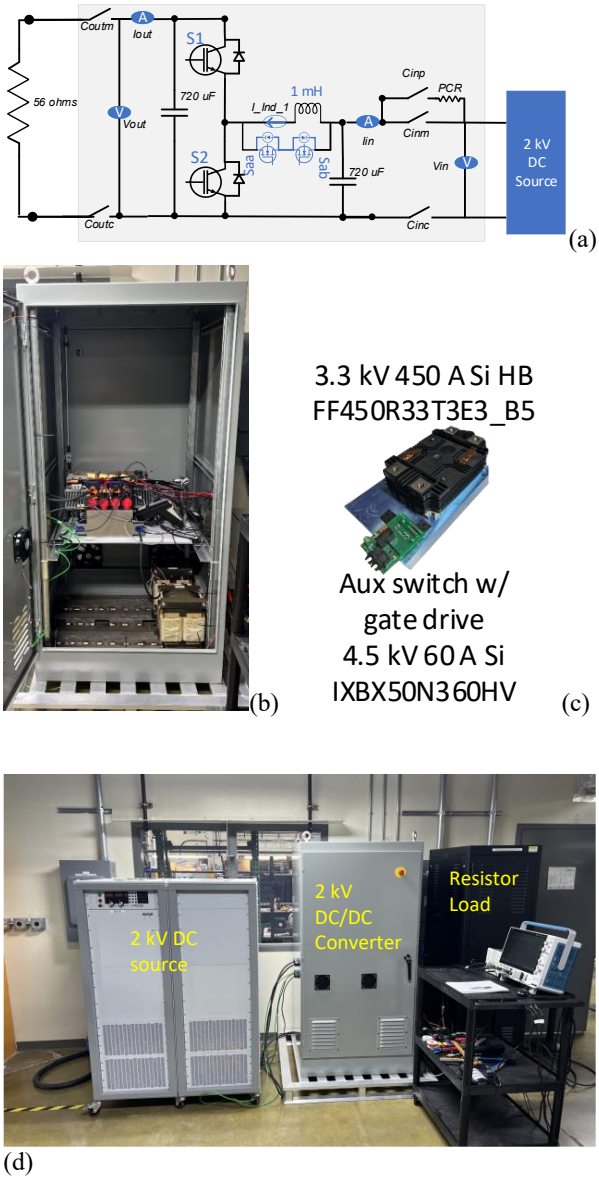
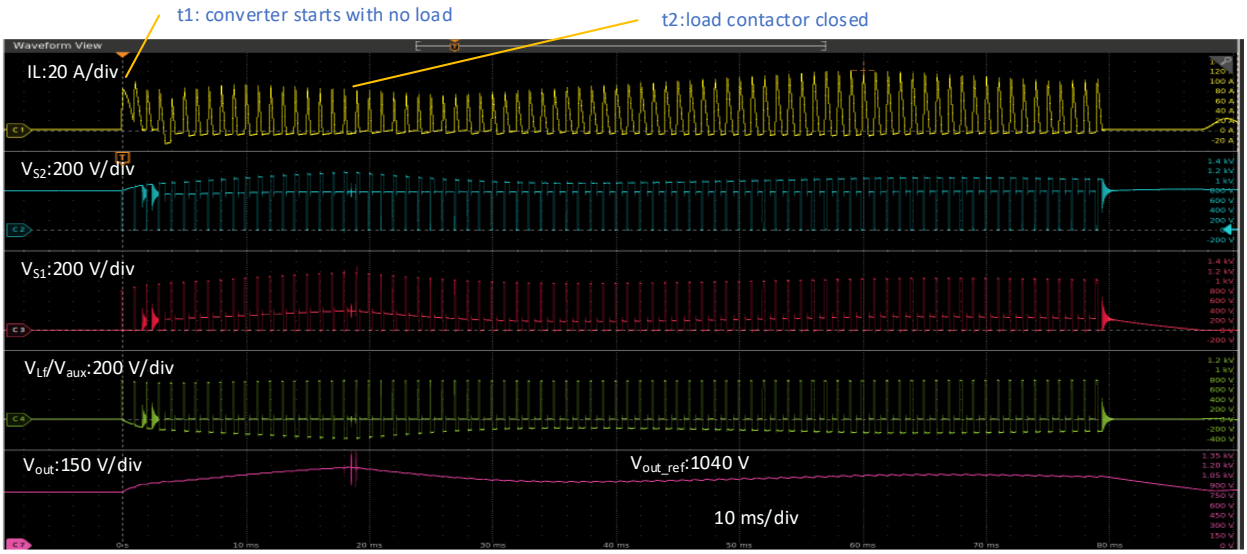


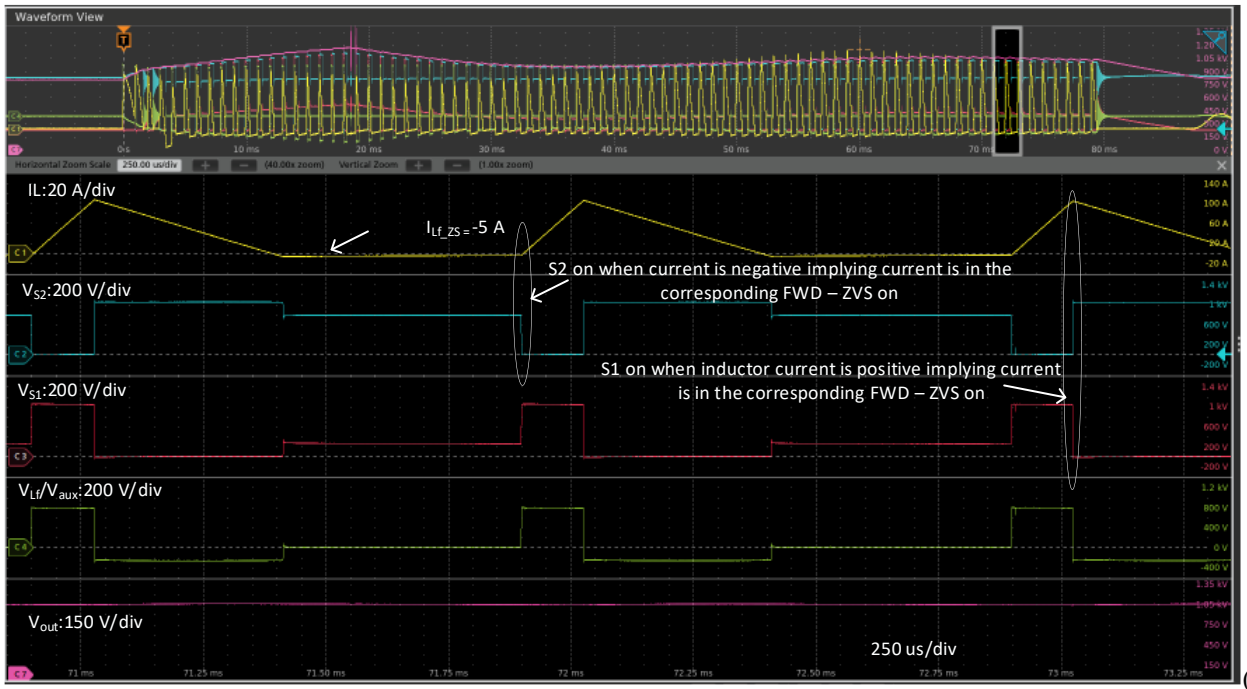
Fig 7: (a)Schematic of the test setup for a 2 kV half-bridge converter based on proposed configuration. (b) Image of the 2 kV half-bridge converter. (c) 3300 V 450 A Si switch and auxiliary switch built using two 3.6 kV 50 A Si MOSFETs (d) image of the complete test setup.

this instant, there is no load. At t2, load is connected and C_{out} starts discharging. A drop in V_{out} at this isntant can be observed. The converter acts to bring the C_{out} voltage to 1040 V within 40 ms. The large ripple in the inductor current and constant negative current of -5 A durign the zero state can be observed. The results show the ability of the proposed DB-MPC technique to achive cycle-by-cycle current control to reach zero-state current of -5A even under varying active states.

The zoomed in waveforms are shown in Fig 9(b). To understand ZVS operation, consider the inductor current in Fig 7a. When the inductor current is postive and $S2$ & $Saux$ (Saa and Sab) are off, it will flow through the FWD of $S1$. That implies that $S1$ can have ZVS turn-on if it is switched when



(a)



(b)

Fig 9: (a) Experimental results of proposed ZSM half-bridge converter operating in boost mode at 1 kV and 20 A (20 kW). (b) Zoomed-in waveforms

inducotr current is positive. When the inductor current is negative and $S1$ and $Saux$ (Saa and Sab) are off, it will flow through the FWD of $S1$. That implies that $S1$ can have ZVS turn-on if it is switched when inductor current is negative. In Fig 9, it can be seen that $S1$ is turned on when the inductor current is positive and $S2$ is being turned on when the inductor current is negative, which implies ZVS turn-on of $S1$ and $S2$ is achieved. Please note that the auxilairy switch is actually turned right along with $S1$. At this isntant, the inductor current is flowing in the FWD of $S1$ and hence the auxilairy switch achieves both ZCS and ZVS.

$S2$ has ZVS turn-on only because, a small negative current is maintined in the inductor durign the zero state, which is the basic idea of the propsoed toplogy. The zero state also enables operatign the converter with fixed frequency while maintaining negative current required to achieve ZVS turn-on. In the experimental results, the inductor current can be seen to be reaching -5A durign the zero state, indicated by $V_{Lf} = V_{aux} = 0V$. The current durign this period is circulating between the inductor and the auxilairy switch.

The experimental results prove the ability to achieve ZVS turn-on of all main switches with the help of a small auxiliary switch.

VII. dv/dt CONTROL

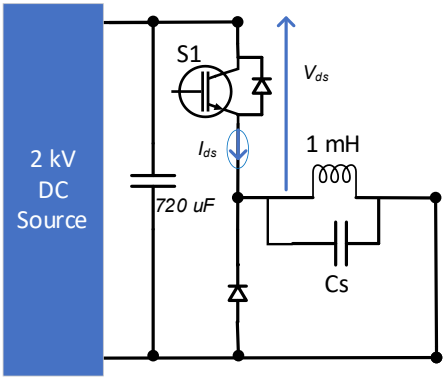


Fig 10: Schematic of test circuit to verify the impact of C_s in reducing

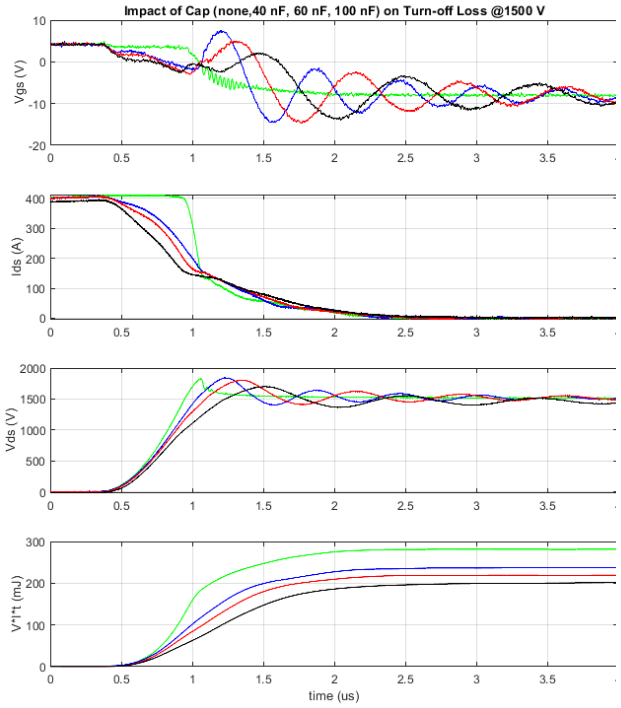


Fig 11: Switching results of Infineon 3.3 kV 450 A Si device showing the impact of additional capacitor across to device in reducing the turn-off loss and dv/dt. Green: no capacitor, Blue: 40 nF, Red: 60 nF, Black: 100 nF.

As mentioned in Section II, it is possible to add a capacitor across the filter inductor and thereby the auxiliary switch and achieve dv/dt control. To demonstrate the same, double-pulse test was conducted on the same 3.3 kV 450 A Si device using the circuit shown in Fig 10. A capacitor C_s is connected across the inductor. C_s effectively increases the device output capacitance. Initially, switch $S1$ is turned on and the current starts increasing in the inductor. During this period the votlage across C_s is equal to V_{dc}. When $S1$ is turned off, the inductor current discharges C_s and only when C_s is fully discharged, the inductor current transitions to the diode. The value of the inductor current and the value of C_s will determine the dv/dt. The reduction in dv/dt through addition of C_s will also reduce turn-off loss.

Please note that addition of C_s will increase turn-on loss of $S1$. To avoid that, $S1$ needs to be turned-on under ZVS condition, which is possible with the proposed auxiliary switch.

The impact of C_s on turn-off loss and dv/dt is shown in Fig 11. The first plot is the gate-emitter voltage, the second plot is the device current, the third plot is the device voltage, and the fourth plot is the integral of device voltage and current indicating the switching loss. The tests are conducted at 1500 V and 400 A with four different values of C_s: none, 40 nF, 60 nF, 100 nF. As shown in the figure, the turn-off loss reduces from 290 mJ with no capacitor to 200 mJ with 100 nF, about 40 % reduction. The reduction in dv/dt can also be observed.

The reduction in switching loss with increased C_s has diminishing returns. This is because of the minority carriers in the IGBT as observed in the long tail current in the device current plot. The reduction is switching loss with C_s is expected to be much higher with SiC MOSFET as it does not have the tail-current issues.

VIII. EFFICIENCY ANSLSYIS

Consider the same half bridge converter shown in Fig 7. To calculate losses for the base case, assume the converter is operated in CCM with V_f = 1200 V and V_{dc} = 1800 V and 200 A. The filter inductor is chosen so that the current ripple is < 10%. From the data sheet of 3.3 kV, 450 A, Infineon device [6] , it is deduced that the turn-on loss at 1800 V, 200 A, 125 degC will be 350 mJ, the turn off loss will be 300 mJ and the reverse recover loss will be 350 mJ. Therefore, the total switching loss will be 1000 W at 1 kHz Fs. The Vce and Vf drop is around 2.2 V, resulting in conduction loss of 440 W. The total loss of the conventional half bridge operating in CCM will be 1440 W.

Assuming the converter is operating in DCM with filter inductor of 1 mH. The inductor will have a maximum peak current of 400 A. The switching loss will just be the turn off loss of the main switches. At 1800 V and 400 A, the turn off loss from the data sheet is 550 W. The forward characteristics of diode and IGBT can be represented by a constant voltage drop of 1.2 V and a resistance of 4 mΩ at 125 degC. The inductor current has an average component of 200 A and an RMS component of 230 A. Accordingly the conduction loss is calculated to 454 W. The total loss of the proposed converter will be 1004 W.

Assuming the converter is operating in the proposed ZSM mode. The operation is simar to the DCM except the provision to add an additional capacitor across the inductor. The additional capacitor as suggested earlier can reduce the turn-off loss. The device was characterized to evaluate the impact of the proposed capacitor. As shown in Fig 7, the turn off loss at 1500 V and 400 A can be reduced from 290 mJ with no capacitor to 200 mJ with 100 nF. The reduction is about 40 %. Assuming I_{Lf_zs} = 20 A and minimum of 5% time is spent in the zero state, the inductor peak current will increase to 440 A. The turn off loss at 1800 V, 445 A, with the assumption of 40 % reduction due to the capacitor, will be 367 W. The conduction loss will increase by 5% to 480 W. The conduction loss in the auxiliary switch will

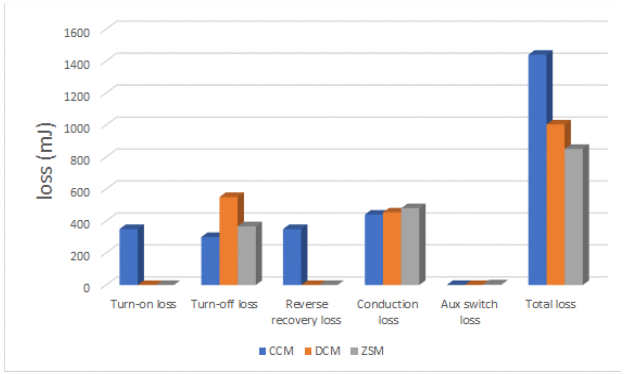


Fig 12: Loss calculation for a half-bridge (Infineon switch) operated in boost mode delivering 200 A from 1200 V to 1800 V. CCM: Continuous conduction mode, DCM: Discontinuous conduction mode, ZSM: Proposed zero-state switching mode.

be because of a 4 V drop including the switch and the diode for 5% of the switching cycle, resulting in a loss of 20*4*0.05 = 4 W. The total loss in the proposed converter will be 851 W.

The comparison between CCM, DCM and proposed ZSM modes are shown in Fig 12. Moving from CCM to DCM reduces the total loss by 30 % and then moving to the proposed ZSM mode will result in further 15 % reduction. In summary, the proposed method results in loss reduction of 40% compared to the conventional converter operation.

IX. Comparison with other approaches

A comparison of the proposed ZSM approach is compared with the traditional approaches and is shown in Table 1. The proposed approach needs two 1.0 pu auxiliary switches per filter inductor but the current rating is very small (0.1 pu). In terms of semiconductor VA rating, this will increase the VA from 4.0 pu to 4.4 pu in case of 1-ph converter and 6.0 pu to 6.6 pu in case of three-phase converter. However, in terms of advantages, it delivers ZVS across all switches, controlled dv/dt and fixed frequency approach allowing interleaving capability and simple EMI filter design.

X. Conclusion

A novel half-bridge building block with a zero-state, enabled by a small auxiliary switch (0.1 pu), is presented. The topology and the operating principle of the proposed zero-state modulated converter is presented. Control scheme based on Dead-beat model-predictive-control technique is presented to enable cycle-by-cycle control of the inductor current. The converter operation and control scheme to achieve ZVS are verified through experimental results at 1 kV, 20 kW. It is shown that the addition of zero-state allows the converter to achieve ZVS across all switches and across all operating conditions and while operating with fixed switching frequency. It is shown that the proposed approach needs a 3-5 x smaller filter inductor compared to the conventional converter. The ability to control dv/dt and further reduce turn-off loss is also demonstrated. Multiple of the proposed half-bridge building blocks can be used to achieve 1/3-phase 3/4 wire ZVS AC-DC converters. Accordingly, operation of 1-phase AC-DC converter consisting of two of the half bridge building blocks is verified using C-HIL. An efficiency analysis was conducted, and it was shown that with the proposed approach a 40 % reduction in loss can be achieved compared to a standard half-bridge converter. The proposed approach is compared with other ZVS AC-DC converters showing the advantages in loss and size reduction.

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Table 1: Comparison of ZVS AC-DC configurations

	Main Sw voltage	current stress	Irms	Auxiliary circuits	Filter ind	Filter cap	Modulation	Control region	Main Sw Fsw
DC Res ZVS [1]	1.1 pu	1.1 pu	1x	1 switch, 1.1 pu voltage, 0.1 pu current	1x	1x	SVM	+/- π/3	1x
DC Res ZVS [3]	1.1 pu	1.1 pu	1x	1 switch, 1.1 pu voltage, 0.1 pu current	1x	1x	SVM	+/- π/2	2x
ZVT [2]	1.0	2.2 pu	1.15x	No	0.2 x	20x	TCM	+/- π/2	Variable 1-15 x
ZVT [4]	1.0	2.2 pu	1.15x	No	0.2x	20x	S-TCM	+/- π/2	Variable 1-3.5 x
Proposed topology	1.0	2.2 pu	1.1 x	2 switches, 2.0 pu voltage, 0.1 pu current	0.2x	1x with interleaving	ZSM	+/- π/2	1x