Journal of Applied Physics

RESEARCH ARTICLE | MARCH 04 2024

Nonvolatile memory cells from hafnium zirconium oxide ferroelectric tunnel junctions using Nb and NbN electrodes

Jessica Haglund-Peterson ; Benjamin L. Aronson ; Samantha T. Jaszewski ; Scott Habermehl ; Giovanni Esteves ; John F. Conley, Jr. ; Jon F. Ihlefeld ; M. David Henry

J. Appl. Phys. 135, 094104 (2024)
https://doi.org/10.1063/5.0191757

02 April 2024 12:34:25

AIP Publishing

Applied Physics Letters
Special Topic:
Advances in Quantum Metrology
Submit Today

Journal of Applied Physics | ARTICLE | pubs.aip.org/aip/jap

Nonvolatile memory cells from hafnium zirconium oxide ferroelectric tunnel junctions using Nb and NbN electrodes

Cite as: J. Appl. Phys. **135**, 094104 (2024); doi: 10.1063/5.0191757
Submitted: 15 December 2023 · Accepted: 17 February 2024 ·
Published Online: 4 March 2024

Jessica Haglund-Peterson,[1,2] Benjamin L. Aronson,[3] Samantha T. Jaszewski,[1,3] Scott Habermehl,[1] Giovanni Esteves,[1] John F. Conley, Jr.,[2] Jon F. Ihlefeld,[3,4] and M. David Henry[1,a)]

AFFILIATIONS

[1]MESA Fabrication Facility, Sandia National Laboratories, Albuquerque, New Mexico 87185, USA
[2]Department of Electrical Engineering and Computer Science, Oregon State University, Corvallis, Oregon 97331, USA
[3]Department of Materials Science and Engineering, University of Virginia, Charlottesville, Virginia 22904, USA
[4]Charles L. Brown Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, Virginia 22904, USA

[a)]**Author to whom correspondence should be addressed:** mdhenry@sandia.gov

ABSTRACT

Ferroelectric tunnel junctions (FTJs) utilizing hafnium zirconium oxide (HZO) have attracted interest as non-volatile memory for microelectronics due to ease of integration into back-end-of-line (BEOL) complementary metal oxide semiconductor fabrication. This work examines asymmetric electrode NbN/HZO/Nb devices with 7 nm thick HZO as FTJs in a memory structure, with an output resistance that can be controlled by read and write voltages. The individual FTJs are measured to have a tunneling electroresistance of 10 during the read state without significant filament conduction formation and reasonable ferroelectric performance. Endurance and remanent polarizations of up to 10^5 cycles and 20 μC/cm^2, respectively, are measured and are shown to be dependent on the cycling voltage. Electrical measurements demonstrate how magnitude of the write pulse can modulate the high state resistance and the read pulse influences both resistance values as well as separation of resistance states. Then, by using two opposite switching FTJ devices in series, a programmable nonvolatile resistor divider is demonstrated. Measurements of these two FTJ unit memory cells show wide applicability to a BEOL microfabrication process for a re-readable, rewritable, and nonvolatile memory cell.

02 April 2024 12:34:25

© 2024 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution-NonCommercial-NoDerivs 4.0 International (CC BY-NC-ND) license (http://creativecommons.org/licenses/by-nc-nd/4.0/). https://doi.org/10.1063/5.0191757

INTRODUCTION

Ferroelectricity in hafnium oxide was first reported in 2011, and since then, it has continued to attract interest due to compatibility of this thin film material in complementary metal oxide semiconductor (CMOS) manufacturing and ease of integration in the back-end-of-line (BEOL) fabrication.[1] Additionally, ferroelectricity in atomic layer deposited (ALD) doped/substituted hafnia (HfO_2) and hafnium zirconium oxide (HZO) is associated with ferroelectric properties that are advantageous for devices, including coercive fields (E_c) close to 1 MV/cm (which for films ≤10 nm in thickness is compatible with existing CMOS voltage rails), remanent polarization (P_r) values between 10 and 35 μC/cm, and robust ferroelectric behavior at thicknesses below 5 nm.[2–5] As deposited, ALD (Hf,Zr)O_2 laminates are amorphous and require annealing to establish the orthorhombic crystal structure (space group $Pca2_1$) required for ferroelectricity.[6–8] HZO is typically annealed via rapid thermal annealing (RTA) for crystallization, and the resulting devices often need to be field cycled to exhibit a strong ferroelectric response through a process called wake-up.[9] The wake-up process involves electric field cycling above the coercive field; as the number of cycles increases, ferroelectric domains that are aligned with the field and phase transformations occur from other metastable, non-ferroelectric phases to the ferroelectric phase.[1,6,10–13] After the initial cycling, the ferroelectric properties remain stable for many cycles, but eventually, fatigue begins to occur and P_r decreases until the device undergoes a dielectric breakdown.

There are several memory architectures that seek to take advantage of the ferroelectric properties. These include ferroelectric

© Author(s) 2024

random-access memory (FeRAM), ferroelectric field effect transistors (FeFETs), and ferroelectric tunnel junctions (FTJs). FeRAM is structured like traditional static RAM (SRAM), but the capacitor is replaced with a ferroelectric dielectric. This allows for nonvolatility, but the read cycle is typically destructive such that memory must be rewritten, adding to circuit complexity and design overhead.[14,15] FeFETs place the ferroelectric as the gate dielectric and the read cycles are not destructive. The change in polarization shifts the conductivity of the channel and can be read without destroying the saved information. This allows for fast cycles and nonvolatile memory (NVM). The downside of FeFETs is that they require larger gate voltages and thicker gate dielectrics, as well as instability due to adventitious linear dielectric interlayers that are present between the ferroelectric and the semiconductor.[16] Furthermore, instantiation of FeFETs requires integration with front-end-of-line (FEOL) processes, which can be very expensive to modify. The FTJ is a third class of memory technology that utilizes the metal-ferroelectric-metal (MFM) structure, but the ferroelectric thickness is typically only 1–8 nm, several nm thinner than the FeRAM, due to the tunneling electroresistance (TER) requiring a thinner dielectric.[17–26] FTJs are observed to have large changes in current when the ferroelectric switches states. This is understood to occur because as the polarity changes, the barrier heights between the two electrode interfaces' change. This shifting in the barrier height, in turn, modulates the current by changing conduction between tunneling and thermal emission mechanisms.[12,27–29] Hence, the FTJ demonstrates a voltage-controlled modulation in the device's resistance with the benefit of scaling with the device area, providing a range of resistances needed in a circuit design. The decreased dielectric thickness for FTJ based devices also decreases the voltage necessary for switching polarization states, as well as changes in conduction. As a single circuit element, these devices are intriguing for integration into microelectronics as a NVM with switching resistances controlled by voltage levels used in most CMOS technologies.

A recent work by Liu *et al.* has demonstrated techniques using field programmable ferroelectric diodes which, when arranged such that two diodes are connected in parallel but with opposite switching behaviors, enable ternary content addressable memory (TCAM) cells to be configured with high, low, and "do not care" states.[30] These devices offer device and integration advantages due to the lack of a transistor but complicate the design owing to high coercive fields for switching the diodes. Alternatively, ferroelectric hafnium oxide based crosspoint arrays using two FTJs in series with the same switching behavior may serve as a searchable quick access memory. In Lim *et al.*, a TaO_x barrier was placed at opposite interfaces to shift the hysteresis by holding charge at the interface and creating rectifying circuits.[31] Similarly, the idea of complementary resistive switches has been demonstrated with other ferroelectric perovskites, such as $BaTiO_3$, and conductive film stacks such as $La_{2/3}Sr_{1/3}MnO_3$ or silicon electrodes.[24,32–34] However, there has not been a study of the impact of different read and write voltages on the measured output of two FTJs in series with opposite switching dynamics. Here, we use opposite switching dynamics to describe the observation that a positive pulse applied to the top electrode to switch a FTJ to a high conduction state, referred to in this work as a low resistance state (LRS), could also switch a second FTJ to a low conduction state, referred to in this work as a high resistance state (HRS), if applied to the bottom electrode. In this work, we characterize FTJs with NbN and Nb asymmetric electrodes and extend the complementary resistive switching dynamics method to a proposed NVM rewritable device structure consisting of two oppositely oriented FTJs in series. In this architecture, when one Nb/HZO/NbN FTJ device is pulsed with a positive write voltage and switches to the high conduction state, the second NbN/HZO/Nb FTJ device in series switches to a low conduction state. Application of a subsequent read voltage pulse across both FTJs then demonstrates a voltage divider. The separation of write and read pulses permits a multi-time read device with significant separation of voltages. Nb-based electrodes are specifically interesting as they are useful superconductors at low temperatures where ferroelectric properties in HZO also exist, although superconducting properties are not investigated here.[35]

EXPERIMENTAL PROCESS

The bottom electrode used a Ti/NbN stack that was sputtered deposited on a 150 mm diameter Si ⟨100⟩ wafer using a multi-chamber sputter deposition tool. Prior to the deposition of the bottom electrode stack, a sputter etch was done on the Si wafer to pre-clean the surface. Then, Ti films were DC magnetron sputtered using Ar gas and a substrate temperature of 350 °C. Subsequently, NbN films were reactively sputtered, without a vacuum break, from a Nb target using a combination of N_2/Ar gas and a substrate temperature of 350 °C. The Ti/NbN stack resulted in a strong NbN {111} texture, and thickness was extracted from x-ray reflectivity to be 94 and 115 nm for Ti and NbN, respectively.

Following this deposition, the sample was placed in an Oxford FlexAL II plasma-enhanced ALD system, and growth was conducted using previously published conditions.[36] Tetrakisethylmethylamine (TEMA)Hf, TEMA-Zr, and oxygen plasma were used as precursors. Three cycles of TEMA-Hf and oxygen plasma were alternated with two cycles of TEMA-Zr and oxygen plasma to form a supercycle. To get the desired 7 nm thickness, 11 supercycles were used. Owing to larger growth rates for ZrO_2 than HfO_2, the final composition is approximately $Hf_{0.5}Zr_{0.5}O_2$.

Following HZO deposition, 20 nm of Nb was sputtered deposited as a full-coverage layer on top of HZO. Following Nb deposition, Ti and Pt electrodes were evaporated, utilizing a Temescal e-beam evaporator, and lifted off using a photolithography defined pattern for the top electrodes with a variety of capacitor diameters ranging from 3 to 300 μm. Following deposition, the samples were rapid thermal annealed at 580 °C for 90 s in an argon-purged 1 Torr atmosphere. A plasma dry etch was used to remove the top Nb and HZO outside of these capacitors. This resulted in isolated device stacks of HZO and Nb. The bottom electrode remained continuous. Further photolithography and plasma dry etching patterned the bottom electrode. The device structure can be seen in a schematic in Fig. 1(a).

Following device fabrication, samples were characterized using current-voltage (IV) measurements with a Keithley 4200A instrument utilizing a four-probe resistance measurement configuration such that there was a sense and a force probe on both the top and bottom electrodes to minimize artifacts resulting from contact resistance; we note that given the large resistances of the measured

02 April 2024 12:34:25

© Author(s) 2024

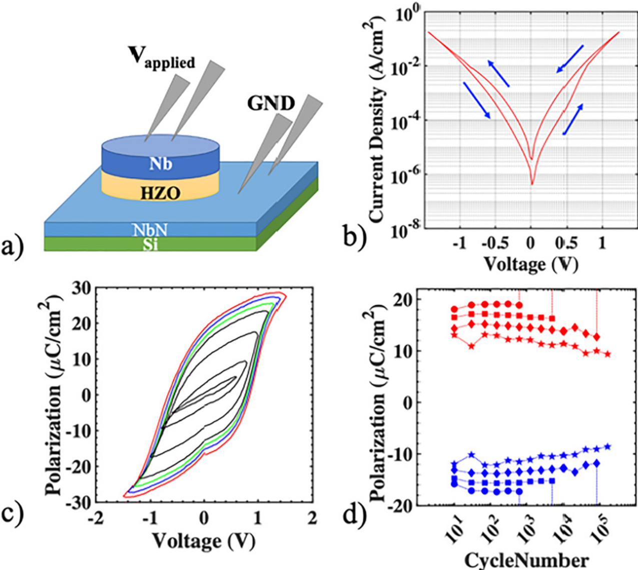


FIG. 1. (a) Structure of a single FTJ device with Nb as the top electrode and NbN as the bottom electrode, (b) IV sweep from −1.5 to 1.3 V switching from the low resistance state (LRS) to the high resistance state (HRS), (c) nested polarization loop for the 7 nm thick HZO, and (d) endurance measurements of the FTJ device using 10 Hz, 10 μs pulses at ±1.2 V (star), 1.3 V (diamond), 1.4 V (square), and 1.5 V (circle) to cycle and PE loop to extract remanent polarization.

FTJs, a four-probe measurement is not required. The measurements were taken by positioning the probes on the Nb top electrode and the surrounding NbN bottom electrode. Voltage was swept from −1.5 to 1.3 V with the Keithley 4200A SCS Parameter Analyzer in "Quiet" mode (a measurement setting optimizing for low noise at the expense of speed by taking the average of multiple measurements at every point as described in the instruments' user manual) with a representative IV curve shown in Fig. 1(b). The IV curves were used to distinguish the write voltage necessary to set the state of the device and select the read voltage for the highest TER.

Polarization-electric field (PE) loops were taken using a Radiant Technologies Multiferroic II instrument. Symmetric triangular voltage sweeps up to 1.5 V at 0.1 ms sweep rates were used, with an example shown in Fig. 1(c). Remanent polarizations (P_r) were approximately 16 to 20 μC/cm^2; however, there were conductive current artifacts in the polarization response, as to be expected for a tunnel device. Coercive voltages were 0.83 and −0.61 V when poled at 1.5 V for MFMs. Endurance cycling was performed with 1.2–1.5 V, 10 Hz, 10 μs pulses to extract up to a 10^5 cycle lifetime, Fig. 1(d).

The data displayed in Fig. 1 suggest that HZO, with a coercive field of 1.05 MV/cm and 2P_r of 36 μC/cm^2, is of quality consistent with previous reports.[6,10] Previous reports demonstrate that both frequency and pulse duration can have significant impacts on endurance;[37–40] however, a greater than 100 factor increase in endurance was also observed by reducing the cycling voltage from 1.5 to 1.2 V, with a concomitant reduction in remanent polarization.

Although the ferroelectricity of HZO can be demonstrated with a clear remanence of polarization, the FTJ device is interesting from a resistance differential perspective and, as such, establishment of the resistance states required investigation. Resistance hysteresis loops can be useful in determining when switching occurs, the on:off resistance ratio, and the presence of multistate resistances. To examine multistate functionality, an initial write pulse of −1.5 V was then followed by a series of pulses from 0 to 1.3 V, back to −1.5 V, and then from −1.5 to 0 V. In between each of the write voltages, a 0.2 V read voltage was used to extract the resistance state of the FTJ with the results in Fig. 2(a). All pulse widths used were 50 ms. As the device switches from the HRS to the LRS and back, the resistance shows some intermediate states when the new state is not completely set for a range of approximately 0.5 V, but between 1.0 and 1.3 V, the LRS becomes stable. As the device switches from the LRS to the HRS, the intermediate state is maintained for approximately 1 V, where at −1.5 V, the HRS begins to saturate. The analog functionality of these devices is demonstrated by the ability to set the LRS by pulsing a positive write voltage above 1 V, and an array of HRS by pulsing a negative write voltage from −1 to −1.5 V. This aspect could be used to vary the output states and demonstrates a neuromorphic-like behavior. This has been observed in FTJs previously and is thought to be useful for mimicking synapses in electronics.[41–43] The resistance measurements were extracted from the pulsed hysteresis loops for devices of different areas and show a linear relationship between area and resistance, Fig. 2(b). This relationship was proportional to the 1/area, which demonstrates the presence of TER, as compared to filament formation in HZO. The on:off ratio was approximately 10 for all devices.

With the observation shown in Fig. 2 potentially enabling multiple high resistance states and Fig. 1(d) suggesting that driving the ferroelectric at higher voltages reduces the endurance of the FTJ, the devices were pulsed with a four-step voltage pulse, Fig. 3(a). The first was a positive write voltage of 50 ms duration pulse, followed by a 0.2 V, 50 ms duration read pulse. This was followed by a negative write pulse and a 0.2 V read pulse. Resistance was measured

02 April 2024 12:34:25

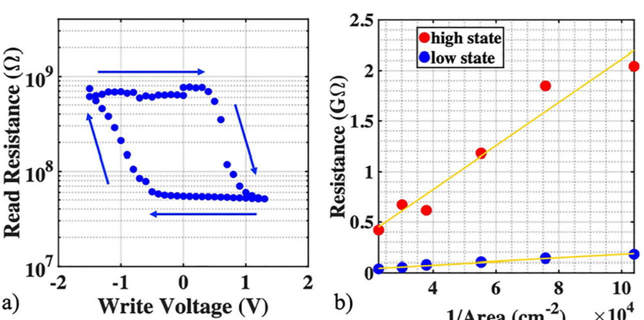


FIG. 2. (a) Pulsed hysteresis curve for a 32 μm diameter device where the write voltages, initially setting at −1.5 V and progressing to 1.3 V, were followed by a 0.2 V read pulse. (b) The high resistance state (HRS) and the low resistance state (LRS) of the devices scaled linear with the inverse area.

© Author(s) 2024

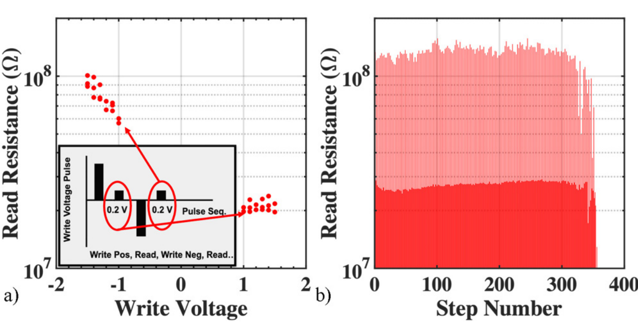


FIG. 3. (a) Read resistance switching of the FTJ device with write voltages from 1.0 to 1.5 V with read voltages of 0.2 V, spaced by 0.1 V for each write pulse for a 30 μm radius device. (b) Endurance cycling of the device between 1.0 V and −1.5 V.

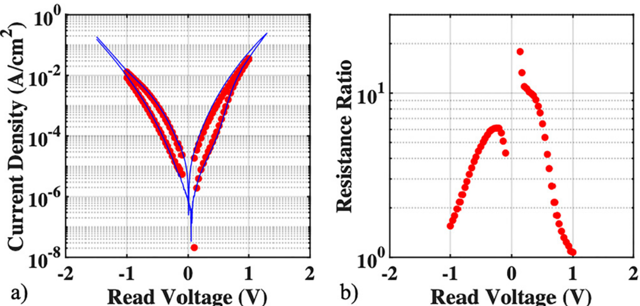


FIG. 4. (a) A 100 μm device that had both an I–V sweep and a set of read pulses applied after the device was set in either the HRS or LRS. (b) Extracted resistance ratio between states for the read pulses; a maximum resistance ratio of better than 10× is measured.

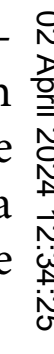
for each of the four pulses. The positive and negative write voltage pulses were kept symmetric in amplitude and were stepped from 1.0 to 1.5 V in 100 mV increments for a 30 μm radius device. The LRS for all write voltages remained at approximately 20 MΩ. However, as shown in Fig. 3(a), as the magnitude of the negative write voltage pulse increased from −1.0 to −1.5 V, the HRS increased from 50 to 100 MΩ. This observation is consistent with the increase in polarization in each PE loop as the cycling voltage increased from 1.1 to 1.5 V as shown in Figs. 1(c) and 1(d); effectively, the ferroelectric barrier height increased, which decreased the tunneling current. From this measurement, it was determined that a +1.0 and −1.5 V would enable a reasonable resistance differential. To measure the endurance with this asymmetric pulsing, another pristine 30 μm radius device was cycled with the negative write voltage pulse at −1.5 V and the positive write voltage pulse at 1.0 V with a 5 ms pulse width and 100 ms off time. Figure 3(b) shows the results with a read voltage of 0.2 V where a 28 MΩ LRS and a 157 MΩ HRS were observed. It is notable that wake-up across the device occurs very rapidly, in less than 20 cycles, as seen in the LRS stabilization.

From the IV measurements of Fig. 1(b), the difference in current density between the HRS and the LRS is seen to fluctuate, suggesting that an optimization of the read pulse might enable the maximization of TER. To determine the optimal read voltage, a device was set in the LRS or HRS by a −1.5 or 1.3 V write pulse, respectively. This was followed by a series of read voltages for each state, where the current was then measured at the read voltage, as shown by red dots in Fig. 4(a). To ensure that pulse measurements were consistent with the previous sweeps, a subsequent IV sweep was applied and overlaid (blue) with the pulse measurements. For each read voltage tested, the HRS and LRS states were compared to extract the TER, shown in Fig. 4(b), where it can be seen that a read voltage below +0.2 V permits a TER greater than 10.

From the pulsed endurance data of Fig. 1(d), an FTJ capable of only 1000 cycles at 1.5 V for only a 9× modulation in resistance would be a challenge for circuit-based applications. As noted, however, a lower voltage applied across the FTJ permits an extended device lifetime. Hence, how many read cycles were attainable becomes a pertinent question. A pristine 40 μm radius device was cycled with a 0.2 V, 10 Hz, 10 μs pulse with a 1.5 V hysteresis pulse used to extract remanent polarization. The remanent polarization from the 0.2 V read cycle was overlaid with the endurance write pulse and shown in Fig. 5. A single FTJ was able to endure more than 10^7 read cycles, noting that the experiment was ended before the device failed, for more than 10^3 write cycles.

Memory cell structure

Using the previously discussed device structure, a thought experiment can conclude that if the top and bottom electrodes were switched, the FTJ should switch resistance states in the opposite manner. As an example, with Nb as the top electrode, a high voltage pulse drives the FTJ to a LRS. If, however, NbN were the top electrode, a high voltage pulse should drive the device to a HRS. With that insight, a memory cell architecture can be



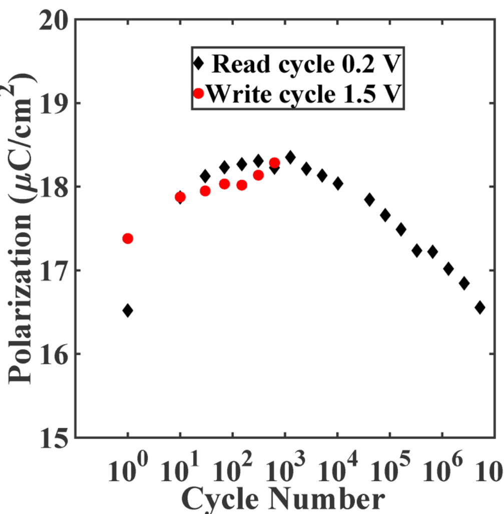


FIG. 5. Endurance cycling for a 40 μm FTJ device using 10 Hz, 10 μs pulses at ±0.2 V (diamond) and 1.5 V (circle) to cycle and 1.5 V PE loop to extract remanent polarization.

© Author(s) 2024

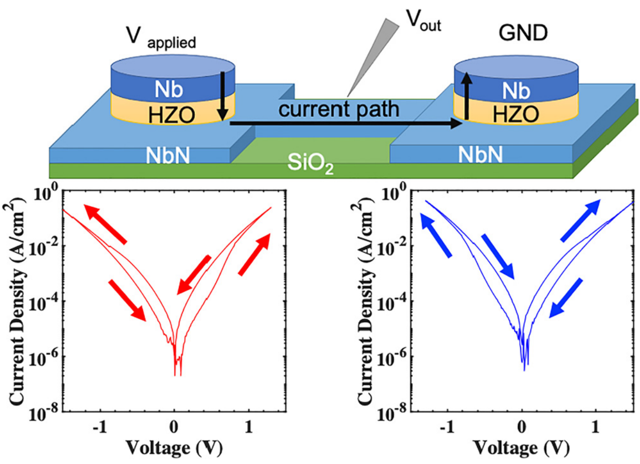


FIG. 6. Operation of two FTJ devices in series for the memory module. When a positive write pulse, 3.1 V, is applied across both devices, the left device goes to a LRS and the right device goes to a HRS. Subsequent read pulses then will have a high V_{out} state. When a negative write voltage is applied, −3.1 V, the left device goes to a HRS and the right device goes to a LRS. Subsequent read pulses will then have a low V_{out} state.

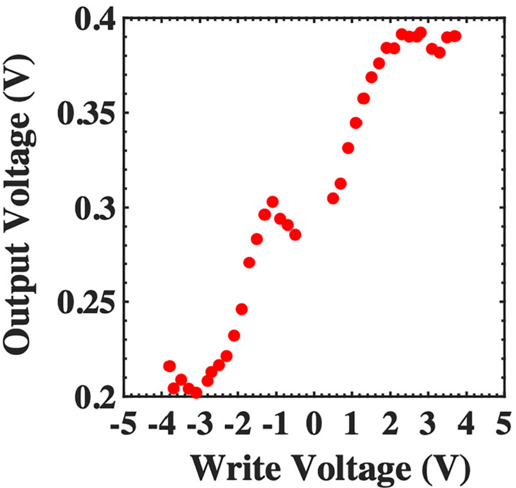


FIG. 7. Determination of the needed write voltage was performed on a pair of 30 μm FTJs placed in series. The devices were set by pulsing a write voltage and then using a 0.6 V read voltage and measuring the output. From this, a write pulse of ±3.1 V was concluded to be sufficient.

constructed using two FTJs connected in series such that current will travel from the top of the first device to the shared bottom electrode and then back through the top electrode. The output voltage can be taken across the shared bottom electrode. This is shown schematically in Fig. 6.

In Fig. 6, the IV curve taken by applying a voltage pulse between the left and right device top electrodes and the shared bottom electrode shows the opposing behavior of the respective devices. When a large positive (negative) voltage pulse, a "write voltage," is applied across the two devices, the left FTJ will switch to the LRS (HRS) while the right FTJ device will switch to the HRS (LRS), respectively. Subsequent read pulses can then measure the state of the devices without switching states. Each of these back-to-back FTJ elements, in principle, should function individually as previously described. If the applied voltage is placed on the top of the left device and 0 V or ground on the top of the right device, then a HRS and a LRS device pair act as a resistive voltage divider, enabling an output from the shared BE to register two distinct output voltage states. However, the pulsed hysteresis loop in Fig. 2(a) adds complication over that of a normal resistive voltage divider. The magnitude of the write state influencing the size of the resistive barrier was shown. However, the complication of two devices in series also implies that the current through both must be the same when the left device is in the HRS and the right device is in the LRS and vice versa. If the devices, for example, had the same area and the current density through both devices was approximately 10^{-4} A/cm^2, then the LRS device would have a 0.2 V drop and the HRS would have a 0.4 V drop. Hence, understanding the write voltage's impact requires further study.

To determine the write voltage necessary to set both devices, a series of voltage pulses with increasing magnitude and alternating sign was applied with a read voltage of 0.6 V, as shown in Fig. 7. The results suggest that 3.1 V provides a sufficient field to switch each device reversibly from each state and place it close to a maxima for a 0.6 V read pulse. In this measurement, each element of the FTJ device pair was awoken individually beforehand and the final pulse was positive. Therefore, a negative voltage was used to reset the device pair.

After determining an appropriate write voltage for 0.6 V read pulses, the device states were then set with a voltage pulse, either 3.1 or −3.1 V, and a sweep of low voltages was performed to determine the read voltage that provides the largest difference between states, Fig. 8. The read voltage sweep also demonstrates the convergence of resistance at higher voltages; however, the difference between the high and low states persists until 2 V. This observation is consistent with the IV curves in Fig. 6, where it is noted that the current in the LRS and the HRS are approximately the same but still distinguishable between each other.

In this dual FTJ device architecture, the devices behave as a variable resistor divider, whose state can be set with the write voltage. Depending on the input voltage applied, a wide variety of output voltage ratios can be achieved for two separable logic states. A chief benefit to this structure is that the state can be set and remain after power is turned off, resulting in a non-volatile memory element that can output a consistent voltage after being written. This shows that the positive applied write voltage causes a higher magnitude of output voltage during the read pulse, whereas a negative applied voltage will reduce the output voltage during the read pulse. Although output voltage states benefited from a 10× hysteresis in the current for the LRS and the HRS, it is noted that it was not a 10× modulation in output voltage states; in fact, it was a logarithmic reduction since the output was chosen to be a voltage rather than a current. However, the 10× modulation could be increased back if the circuit readout utilized a current rather

02 April 2024 12:34:25

© Author(s) 2024

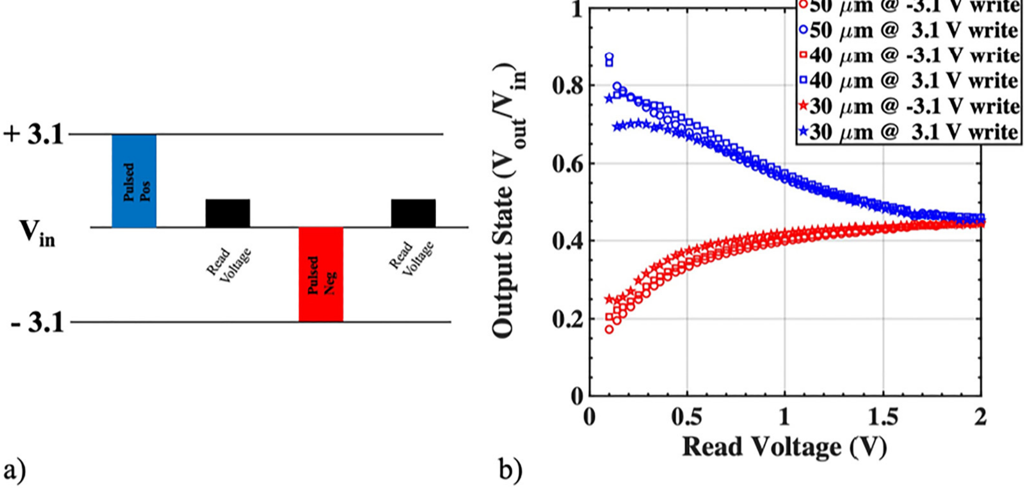


FIG. 8. (a) Pulse sequence for setting the logic 1 and logic 0 states. The positive 3.1 V write pulse, blue, sets FTJs such that the first device is in the LRS and the second device is in the HRS when a read pulse is applied. The negative 3.1 V write pulse, red, sets the first FTJ into the HRS and the second FTJ in the LRS. (b) The output logic state as measured from the common node then shows a delineation between "1" and "0" logic states as a function of the read pulse voltage for a 30 (star), 40 (square), and 50 μm (circle) radius device pair.

than a voltage. This demonstrates the use of FTJs as a voltage-controlled variable resistance divider that could be utilized in memory cell circuits such as SRAM, inverter logic, or even to set a CMOS field effect transistor gate.

CONCLUSION

This work demonstrated the utilization of Nb/HZO/NbN FTJ devices with TER on:off ratios of greater than 10. Characterization of the HZO film showed remanent polarizations up to 20 μC/cm^2 with endurance beyond 10^5 cycles. When utilized with asymmetric electrodes, devices were area scalable with current densities and switching voltages typical of CMOS technologies. The FTJ devices were also shown to have multiple high resistance states for the negative write pulses, which is useful for memory applications and synaptic-mimicking electronics. By reversing the electrodes and linking two devices in series, a non-volatile memory structure composed of two FTJs was constructed and shown to have control and variation of the output read voltage. This demonstrated that the devices could function as programmable resistor dividers that can be set by a write pulse and then used at the lower read pulse voltages. This device pair architecture has high applicability for integration in a re-readable, rewritable non-volatile memory in CMOS technologies.

ACKNOWLEDGMENTS

This material is based on work supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences Energy Frontier Research Centers Program under Award No. DE-SC0021118. S.T.J. acknowledges support from a U.S. National Science Foundation Graduate Research Fellowship under Award No. DGE-1842490. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International Inc., for the U.S. Department of Energy's National Nuclear Security Administration under Contract No. DE-NA0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

02 April 2024 12:34:25

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jessica Haglund-Peterson: Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal). **Benjamin L. Aronson:** Investigation (equal); Resources (equal); Writing – review & editing (equal). **Samantha T. Jaszewski:** Conceptualization (equal); Formal analysis (equal); Resources (equal); Writing – review & editing (equal). **Scott Habermehl:** Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Giovanni Esteves:** Formal analysis (equal); Investigation (equal); Resources (equal); Writing – review & editing (equal). **John F. Conley:** Formal analysis (equal); Supervision (equal); Writing – review & editing (equal). **Jon F. Ihlefeld:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Resources (equal); Writing – review & editing (equal). **M. David Henry:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition

© Author(s) 2024

(equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]T. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Appl. Phys. Lett. **99**(10), 102903 (2011).

[2]U. Schroeder, M. Materano, T. Mittmann, P. D. Lomenzo, T. Mikolajick, and A. Toriumi, Jpn. J. Appl. Phys. **58**(SL), SL0801 (2019).

[3]U. Schroeder, M. H. Park, T. Mikolajick, and C. S. Hwang, Nat. Rev. Mater. **7**(8), 653–669 (2022).

[4]M. Cervo Sulzbach, H. Tan, S. Estandia, J. Gazquez, F. Sanchez, I. Fina, and J. Fontcuberta, ACS Appl. Electron. Mater. **3**(8), 3657–3666 (2021).

[5]B. Prasad, V. Thakare, A. Kalitsov, Z. Zhang, B. Terris, and R. Ramesh, Adv. Electron. Mater. **7**(6), 2001074 (2021).

[6]S. S. Fields, S. W. Smith, P. J. Ryan, S. T. Jaszewski, I. A. Brummel, A. Salanova, G. Esteves, S. L. Wolfley, M. D. Henry, P. S. Davids, and J. Ihlefeld, ACS Appl. Mater. Interfaces **12**(23), 26577–26585 (2020).

[7]J. F. Ihlefeld, S. T. Jaszewski, and S. S. Fields, Appl. Phys. Lett. **121**(24), 240502 (2022).

[8]D. Zhou, J. Xu, Q. Li, Y. Guan, F. Cao, X. Dong, J. Müller, T. Schenk, and U. Schröder, Appl. Phys. Lett. **103**(19), 192904 (2013).

[9]H. A. Hsain, Y. Lee, G. Parsons, and J. L. Jones, Appl. Phys. Lett. **116**(19), 192901 (2020).

[10]E. D. Grimley, T. Schenk, X. Sang, M. Pešić, U. Schroeder, T. Mikolajick, and J. M. LeBeau, Adv. Electron. Mater. **2**(9), 1600173 (2016).

[11]T. Shimizu, Y. Tashiro, T. Mimura, T. Kiguchi, T. Shiraishi, T. J. Konnno, O. Sakata, and H. Funakubo, Phys. Status Solidi RRL **15**(5), 2000589 (2021).

[12]U. Schroeder, C. S. Hwang, and H. Funakubo, *Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices* (Woodhead Publishing, 2019).

[13]M. Lederer, C. Mart, T. Kämpfe, D. Lehninger, K. Seidel, M. Czernohorsky, W. Weinreich, B. Volkmann, and L. Eng, Appl. Phys. Lett. **123**(2), 022903 (2023).

[14]T. Schenk and S. Mueller, paper presented at the 2021 IEEE International Symposium on Applications of Ferroelectrics (ISAF), Sydney, Australia, 2021, pp. 1–11.

[15]Q. Wu, Y. Cao, Q. Luo, H. Jiang, Z. Han, Y. Han, C. Dou, H. Lv, Q. Liu, and J. Yang, IEEE J. Solid State Circuits **59**(1), 208–218 (2023).

[16]K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, IEEE Trans. Electron Devices **65**(6), 2461–2469 (2018).

[17]S. S. Cheema, N. Shanker, C. H. Hsu, A. Datar, J. Bae, D. Kwon, and S. Salahuddin, Adv. Electron. Mater. **8**(6), 2100499 (2022).

[18]J. Y. Park, D. H. Choe, D. H. Lee, G. T. Yu, K. Yang, S. H. Kim, G. H. Park, S. G. Nam, H. J. Lee, and S. Jo, Adv. Mater. **35**(43), 2204904 (2023).

[19]S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, and M. Saitoh, paper presented at the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, 2016, pp. 1–2.

[20]F. Ambriz-Vargas, G. Kolhatkar, R. Thomas, R. Nouar, A. Sarkissian, C. Gomez-Yáñez, M. Gauthier, and A. Ruediger, Appl. Phys. Lett. **110**(9), 093106 (2017).

[21]Y. Goh and S. Jeon, Nanotechnology **29**(33), 335201 (2018).

[22]A. Shekhawat, G. Walters, N. Yang, J. Guo, T. Nishida, and S. Moghaddam, Nanotechnology **31**(39), 39LT01 (2020).

[23]Y. Wei, S. Matzen, T. Maroutian, G. Agnus, M. Salverda, P. Nukala, Q. Chen, J. Ye, P. Lecoeur, and B. Noheda, Phys. Rev. Appl. **12**(3), 031001 (2019).

[24]M. C. Sulzbach, S. Estandía, X. Long, J. Lyu, N. Dix, J. Gàzquez, M. F. Chisholm, F. Sánchez, I. Fina, and J. Fontcuberta, Adv. Electron. Mater. **6**(1), 1900852 (2020).

[25]M. C. Sulzbach, S. Estandía, J. Gàzquez, F. Sánchez, I. Fina, and J. Fontcuberta, Adv. Funct. Mater. **30**(32), 2002638 (2020).

[26]J. Yoon, S. Hong, Y. W. Song, J.-H. Ahn, and S.-E. Ahn, Appl. Phys. Lett. **115**(15), 153502 (2019).

[27]M. Tarkov, F. Tikhonenko, V. Popov, V. Antonov, A. Miakonkikh, and K. Rudenko, Nanomaterials **12**(24), 4488 (2022).

[28]M. Y. Zhuravlev, R. F. Sabirianov, S. Jaswal, and E. Y. Tsymbal, Phys. Rev. Lett. **94**(24), 246802 (2005).

[29]M. Liehr, J. Hazra, K. Beckmann, V. Mukundan, I. Alexandrou, T. Yeow, J. Race, K. Tapily, S. Consiglio, and S. K. Kurinec, J. Vac. Sci. Technol. B **41**(1), 012805 (2023).

[30]X. Liu, J. Ting, Y. He, M. M. A. Fiagbenu, J. Zheng, D. Wang, J. Frost, P. Musavigharavi, G. Esteves, K. Kisslinger, S. B. Anantharaman, E. A. Stach, R. H. Olsson III, and D. Jariwala, Nano Lett. **22**(18), 7690–7698 (2022).

[31]S. Lim, Y. Goh, Y. K. Lee, D. H. Ko, J. Hwang, Y. Jeong, H. Shin, S. Jeon, and S.-O. Jung, IEEE J. Solid State Circuits **58**(7), 1860–1870 (2023).

[32]M. Qian, I. Fina, F. Sánchez, and J. Fontcuberta, Small **15**(11), 1805042 (2019).

[33]Z. Xi, C. Zheng, and Z. Wen, ACS Appl. Mater. Interfaces **10**(6), 6024–6030 (2018).

[34]M. Abuwasib, H. Lu, T. Li, P. Buragohain, H. Lee, C.-B. Eom, A. Gruverman, and U. Singisetti, Appl. Phys. Lett. **108**(15), 152904 (2016).

[35]M. D. Henry, S. Smith, R. Lewis, and J. Ihlefeld, Appl. Phys. Lett. **114**(9), 092903 (2019).

[36]S. S. Fields, D. H. Olson, S. T. Jaszewski, C. M. Fancher, S. W. Smith, D. A. Dickie, G. Esteves, M. D. Henry, P. S. Davids, and P. E. Hopkins, Appl. Phys. Lett. **118**(10), 102901 (2021).

[37]K. Shajil Nair, M. Holzer, C. Dubourdieu, and V. Deshpande, ACS Appl. Electron. Mater. **5**(3), 1478–1488 (2023).

[38]B. Manchon, G. Segantini, N. Baboux, P. Rojo Romeo, R. Barhoumi, I. C. Infante, F. Alibart, D. Drouin, B. Vilquin, and D. Deleruyelle, Phys. Status Solidi RRL **16**, 2100585 (2022).

[39]S. Starschich, S. Menzel, and U. Böttger, Appl. Phys. Lett. **108**(3), 032903 (2016).

[40]M. K. Lenox, S. T. Jaszewski, S. S. Fields, N. Shukla, and J. F. Ihlefeld, Phys. Status Solidi A **221**, 2300566 (2024).

[41]H. Yamada, V. Garcia, S. Fusil, S. Boyn, M. Marinova, A. Gloter, S. Xavier, J. Grollier, E. Jacquet, and C. Carrétéro, ACS Nano **7**(6), 5385–5390 (2013).

[42]Z. Xi, J. Ruan, C. Li, C. Zheng, Z. Wen, J. Dai, A. Li, and D. Wu, Nat. Commun. **8**(1), 15217 (2017).

[43]A. Sünbül, T. Ali, K. Mertens, R. Revello, D. Lehninger, F. Müller, M. Lederer, K. Kühnel, M. Rudolph, and S. Oehler, IEEE Trans. Electron Devices **69**(2), 808–815 (2021).

02 April 2024 12:34:25

© Author(s) 2024