Sonrisa Research, Inc.

Final Technical Report

A New Class of SiC Power MOSFETs with Record-Low Resistance

DE-AR0001009

Award:	DE-AR0001009
Sponsoring Agency:	USDOE, Advanced Research Projects Agency-Energy (ARPA-E)
Lead Recipient:	Sonrisa Research, Inc., Santa Fe, NM
Project Team Members:	Purdue University, West Lafayette, IN
Project Title:	A New Class of SiC Power MOSFETs with Record-Low Resistance
Program Director:	Dr. Isik C. Kizilyalli
Principal Investigator:	Prof. James A. Cooper
Contract Administrator:	ARPA-E, USDOE, AR-1, 1000 Independence Av., SW, Washington DC 20585
Date of Report:	10/14/2023
Reporting Period:	06/17/2019 – 06/16/2023 (includes 1 yr. NCE)

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number [DE-AR0001009]. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

☒ This Report contains no Protected Data.

Table of Contents

Table of Figures/Tables

Public Executive Summary

Silicon carbide (SiC) power transistors are used in the main traction inverter of electric vehicles (EVs). Tesla began installing SiC power MOSFETs in 2017, and has now produced 4.8 million EVs containing over 169 million SiC power MOSFETs. Looking ahead, the worldwide EV market is projected to exceed 50 million vehicles per year by 2030 (Reuters, Oct. 25, 2022). This will create a demand for over two billion SiC power MOSFETs per year. Our program aims to double the efficiency of today's commercial power MOSFETs. This will cut the number of MOSFETs per EV in half, reducing cost, simplifying assembly, decreasing weight, and increasing vehicle reliability through reduced parts count.

Our approach is to apply innovative design and advanced processing to increase the density of current-controlling channels in SiC power MOSFET. We have developed two new MOSFET devices, each of which increases the channel density by a factor of six over today's best commercial MOSFETs. This required implementing new fabrication processes, creating new device designs, and integrating the processing steps and device designs into a manufacturable technology. In this project we have developed two innovative devices: (i) a novel three-dimensional structure, the "tri-gate MOSFET," and (ii) a deeply-scaled, fully self-aligned trench MOSFET, the "IMOSFET". Both products were experimentally demonstrated during this project and meet the program goals of increased efficiency relative to the current state-of-the art commercial products.

In the process we have generated significant IP, with two US patents issued and three applications pending. We have also published three journal articles and given reports on this technology at seven international conferences.

The success of this program has led to significant follow-on funding from industry. In May 2023 Purdue University signed a five-year R&D contract with GlobalFoundries to transfer our novel technology to commercial production. With headquarters in Malta, NY, Global Foundries is one of the largest pure-play silicon foundries in the world, with annual revenue of $8.1B. Their SiC foundry will be built around the next-generation 200-mm diameter SiC wafers, which will double the number of die per wafer and reduce per-die production cost.

Acknowledgements

This work was supported by grant (DE-AR0001009) from the Advanced Research Projects Agency - Energy (ARPA-E) and managed by Dr. Isik C. Kizilyalli. Prof. Steven Bayne of Texas Tech University performed short-circuit withstand measurements on our thin oxide MOSFETs, and Prof. Christina DiMarino at Virginia Tech University conducted switching loss measurements. Dr. Kaushik Ramadoss of Purdue University assisted with helpful technical advice.

Accomplishments and Objectives

This grant enabled Sonrisa Research, Inc. and Purdue University to achieve feasibility demonstration of two novel SiC trench power MOSFETs intended for the medium-voltage (400–1200 V) market. Figures 1–3 show the novel tri-gate MOSFET and Figs. 4–6 show the fully self-aligned IMOSFET. Both structures exhibit reduced on-resistance in the blocking voltage regime used in electric vehicles. Successful completion of this project and demonstrations such as shown below led to significant follow-on funding from GlobalFoundries to transition this technology into commercial production.

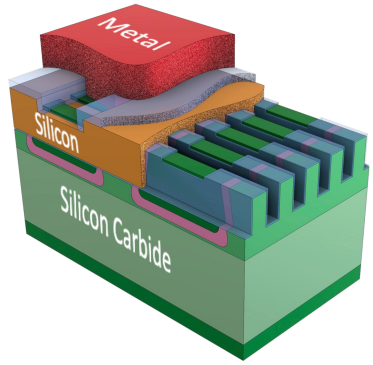

Fig. 1 The tri-gate MOSFET has a FinFET geometry

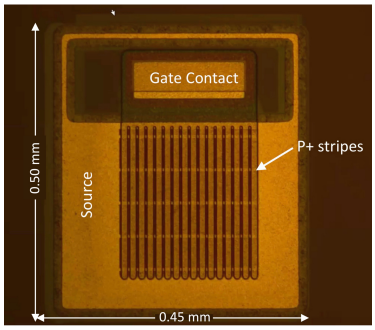

Fig. 2 A fabricated tri-gate MOSFET

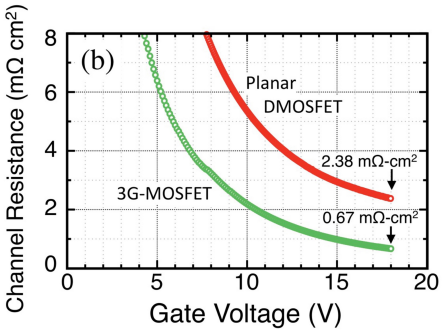

Fig. 3 The tri-gate channel resistance is 3.5x lower than a comparable DMOSFET

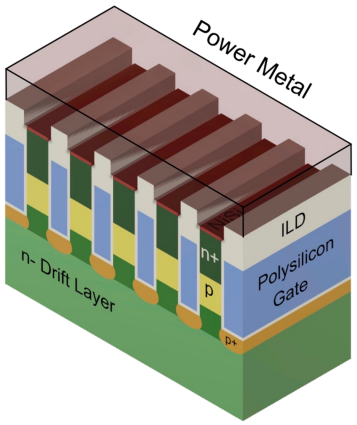

Fig. 4 The deeply-scaled, fully self-aligned IMOSFET

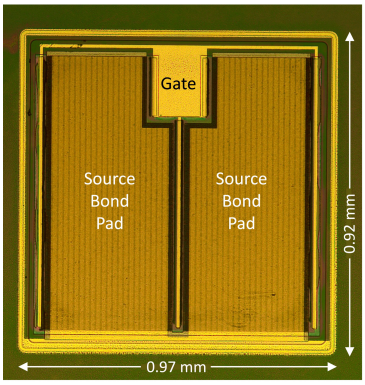

Fig. 5 A fabricated IMOSFET

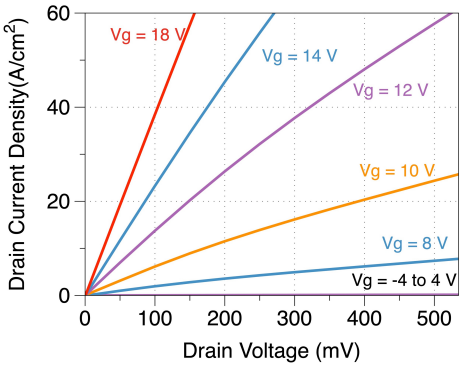

Fig. 6 On-state I-V curves of a 650-V IMOSFET with $R_{ON,SP}$ of 1.57 mΩ-cm²

This program had a number of technical milestones and objectives. Table 1 summarizes the tasks, milestones, metrics, deliverables, and results.

Table 1: Key Milestones and Deliverables

Tasks	Milestones and Deliverables
Task 1: Refine Tasks and Milestones	Q1: Refine tasks and milestones for the work plan Tasks and milestones were refined and approved by the PD.
Task 2: Tri-Gate MOSFETs 2.1 Initial tri-gate MOSFETs with 2 µm trenches 2.2 Manufacturable tri-gate MOSFETs with 2 µm trenches 2.3 Initial tri-gate MOSFETs with 1 µm trenches 2.4 Manufacturable tri-gate MOSFETs with 1 µm trenches	Q3: First 3G-MOSFETs with 2 µm deep trenches completed and tested. These devices will have self-aligned short channels, but will not have thin gate oxides or waffle substrates. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 3.5 mΩ cm^2 ($R_{ch,sp}$ < 2.0 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 3.2 mΩ cm^2 ($R_{ch,sp}$ < 2.0 mΩ cm^2). The first 3G-MOSFETs with 2 µm deep trenches were fabricated and characterized. These devices suffered from source-drain shorts caused by the loss of small features on the polysilicon implant mask after the p-base implant and before the n+ source implant. This will be prevented on later process lots by a redesign of the base implant mask to eliminate this feature. Q5: First 3G-MOSFETs with 1 µm deep trenches completed and tested. These devices will have self-aligned short channels, but will not have thin gate oxides or waffle substrates. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 4.1 mΩ cm^2 ($R_{ch,sp}$ < 2.6 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 3.8 mΩ cm^2 ($R_{ch,sp}$ < 2.6 mΩ cm^2). The first 3G-MOSFETs with 1 µm deep trenches were fabricated and characterized. These devices were functional but the yield was low due to small post features on the base implant mask that popped off when the mask was expanded by oxidation. The performance of 650-V rated devices was excellent, with $R_{on,sp}$ = 2.2 mΩ-cm^2 at a blocking voltage of 706 V. Q9: Manufacturable 3G-MOSFETs with 2 µm deep trenches completed and tested. These devices will have self-aligned short channels and thin gate oxides, but will not have waffle substrates. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 2.0 mΩ cm^2 ($R_{ch,sp}$ < 0.5 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 1.7 mΩ cm^2 ($R_{ch,sp}$ < 0.5 mΩ cm^2). Numerical simulations indicated that the performance of devices with 2-µm deep trenches was only slightly higher than devices with 1-µm deep trenches. Devices with 2-µm deep trenches require higher-energy implants and thicker implant masks, complicating manufacturing and adding cost. Accordingly, with the concurrence of the PD we discontinued work on devices with 2-µm deep trenches and focused on devices with 1-µm trenches. Q10: Manufacturable 3G-MOSFETs with 1 µm deep trenches completed and tested. These devices will have self-aligned short channels and thin gate oxides, but will not have waffle substrates. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 2.9 mΩ cm^2 ($R_{ch,sp}$ < 1.4 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 2.6 mΩ cm^2 ($R_{ch,sp}$ < 1.4 mΩ cm^2). Because of time and staff limitations, we did not complete 3G-MOSFETs with thin gate oxides.
Task 3: Tri-Gate MOSFETs with Waffle Substrates	Q6: First 3G-MOSFETs with 2 µm deep trenches and waffle substrates completed and tested. These devices will have self-aligned short channels, but will not have thin gate oxides. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 2.6 mΩ cm^2 ($R_{ch,sp}$ < 2.0 mΩ

3.1 Initial tri-gate MOSFETs with 2 µm trenches and waffle substrates 3.2 Manufacturable tri-gate MOSFETs with 2 µm trenches and waffle substrates 3.3 Initial tri-gate MOSFETs with 1 µm trenches and waffle substrates 3.4 Manufacturable tri-gate MOSFETs with 1 µm trenches and waffle substrates	cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 2.3 mΩ cm^2 ($R_{ch,sp}$ < 2.0 mΩ cm^2). As stated above, fabrication of devices with 2-µm deep trenches was discontinued because of the limited performance advantage over 1-µm deep trenches. Q8: First 3G-MOSFETs with 1 µm deep trenches and waffle substrates completed and tested. These devices will have self-aligned short channels, but will not have thin gate oxides. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 3.2 mΩ cm^2 ($R_{ch,sp}$ < 2.6 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 2.9 mΩ cm^2 ($R_{ch,sp}$ < 2.6 mΩ cm^2). To simulate the effect of a waffle substrate, the substrate of our functional 3-MOSFET sample was thinned. However, this this produced almost no reduction in $R_{ON,SP}$. This was because our MOSFET dimensions were comparable to the thickness of the substrate and current spreading in the substrate was already reducing the resistance. Accordingly, the PD advised us to discontinue adding waffle substrates on our small test devices. Q12: Optimized 3G-MOSFETs with 2 µm deep trenches and waffle substrates completed and tested. These devices will have self-aligned short channels and thin gate oxides. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 1.1 mΩ cm^2 ($R_{ch,sp}$ < 0.5 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 0.8 mΩ cm^2 ($R_{ch,sp}$ < 0.5 mΩ cm^2). As stated earlier, fabrication of devices with 2-µm deep trenches was discontinued because of the limited performance advantage over 1-µm deep trenches. Q12: Optimized Gen-2 3G-MOSFETs with 1 µm deep trenches and waffle substrates completed and tested. These devices will have self-aligned short channels and thin gate oxides. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 2.0 mΩ cm^2 ($R_{ch,sp}$ < 1.4 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 1.7 mΩ cm^2 ($R_{ch,sp}$ < 1.4 mΩ cm^2). As discussed above, thinning the substrate or applying a waffle substrate on test devices whose dimensions are smaller than the substrate thickness does not reduce the on-resistance because it is already reduced by current spreading. A waffle substrate will only be effective for devices that are large compared to the substrate thickness.
Task 4: Oxide-Shielded IMOSFETs 4.1 Initial oxide-shielded IMOSFETs fabricated and characterized 4.2 Manufacturable oxide-shielded IMOSFETs fabricated and characterized 4.3 Initial oxide-shielded IMOSFETs	Q6: First oxide-shielded IMOSFETs completed and tested. These devices will not have thin gate oxides or waffle substrates. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 3.4 mΩ cm^2 ($R_{ch,sp}$ < 1.9 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 3.1 mΩ cm^2 ($R_{ch,sp}$ < 1.9 mΩ cm^2). The first oxide-shielded IMOSFETs were completed and characterized. The specific on-resistance of 650-V rated IMOSFETs was 1.57 mΩ-cm^2 with a blocking voltage of ~570 V. The IMOSFETs did not reach avalanche breakdown due to an anomalous leakage above 500 V, but pin diodes with the same edge terminations exhibited a blocking voltage of 890 V. Q9: First oxide-shielded IMOSFETs with waffle substrates completed and tested. These devices will not have thin gate oxides. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 2.5 mΩ cm^2 ($R_{ch,sp}$ < 1.9 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 2.2 mΩ cm^2 ($R_{ch,sp}$ < 1.9 mΩ cm^2).

with waffle substrates fabricated and characterized 4.4 Manufacturable oxide-shielded IMOSFETs with waffle substrates fabricated and characterized	As discussed above, these test devices were so small that current spreading in the 350-µm thick substrate had already reduced the substrate resistance, and no additional improvement would be expected by adding a waffle substrate. Q11: Optimized oxide-shielded IMOSFETs completed and tested. These devices will have thin gate oxides, but will not have waffle substrates. Devices will be identified with rated blocking voltage = 900 V and Ron,sp < 2.1 mΩ cm2 (Rch,sp < 0.6 mΩ cm2). Other devices will be identified with rated blocking voltage = 650 V and Ron,sp < 1.8 mΩ cm2 (Rch,sp < 0.6 mΩ cm2). Based on learnings from the initial IMOSFET process, a modified process that is compatible with standard industry practice was developed. This required process changes to produce a planar surface for all litho steps, and switching from metal hard masks to oxide or polysilicon hard masks. These new unit processes were developed and demonstrated, but optimized IMOSFETs were not completed due to lack of time. Additionally, planar DMOSFETs with thin gate oxides were characterized for on-resistance, short-circuit withstand time, and switching energy. Q12: Optimized oxide-shielded IMOSFETs with waffle substrates and thin gate oxides completed and tested. Devices will be identified with rated blocking voltage = 900 V and $R_{on,sp}$ < 1.2 mΩ cm^2 ($R_{ch,sp}$ < 0.6 mΩ cm^2). Other devices will be identified with rated blocking voltage = 650 V and $R_{on,sp}$ < 0.9 mΩ cm^2 ($R_{ch,sp}$ < 0.6 mΩ cm^2). As discussed above, these test devices were so small that current spreading in the 350-µm thick substrate had already reduced the substrate resistance, and no additional improvement would be expected by adding a waffle substrate.
Task 5: Tech Transfer 5.1 IP Strategy and initial impact sheet drafted 5.2 Initial T2M studies 5.3 Techno-economic analysis 5.4 Interactions with commercial partners	Q1: IP activity including invention disclosures, patent applications, and full patent publications will be reported on a quarterly basis. Patent applications stemming from work performed in this project will be entered into the Federal iEdison system. Submission of draft Impact Sheet that describes the desired impact the project team would like to have by the end of the project. Present plans for IP generation during the project to T2M Advisor & Program Director for approval. Six patent applications were filed with the USPTO, three of which have now issued as patents. Other key elements of this technology are protected by nine US patents that were filed prior to the start of this program. Q4: Identify possible commercialization partners and possible foundry partners. Deliver report highlighting the outcome of the activity and the planned approach for the remainder of the project and M5.3 to T2M Advisor and PD. Several SiC power device manufacturers and foundries were contacted, including Wolfspeed, MicroChip, Littelfuse, Coherent (II-VI), Qorvo (United SiC), GlobalFoundries and XFAB Texas. Letters of support were received from Wolfspeed, Coherent, and XFAB. Q8: Conduct techno-economic analysis based on results from M2.1, M2.3, M3.1 and M4.1. Quantify value proposition and assess potential market impact. Deliver report highlighting the outcome to T2M Advisor and PD. Our market analysis identified EV electric drive trains as the fastest-growing application for medium-voltage power MOSFETs, including our tri-gate MOSFET and our IMOSFET. Tesla has installed 48 650-V SiC DMOSFETs in the main traction inverter of each EV since 2017, and the projected worldwide market for EVs is expected to reach 50 million vehicles per year by 2030 (Reuters, Oct. 25, 2022). With six times the channel density as today's best commercial SiC

	MOSFETs, the IMOSFET and tri-gate MOSFET developed under this program are well positioned to compete in this market. Q11: Publish SPICE models and preliminary data sheets based on results from M2.1-M2.4, M3.1, M3.3 and M4.1-M4.3. Identify commercialization partners and/or foundries to implement a manufacturable process and develop a line of commercial products. Describe transfer plan to suitable commercial partner and details of the engagement including timing to T2M Advisor and PD. Submission of updated Impact Sheet. We have attracted interest from several SiC device manufacturers, and in May 2023 we signed a five-year, $2,626,061 development contract with GlobalFoundries to transition this technology into commercial production. We are currently fabricating Gen-2 versions of the tri-gate MOSFET, the IMOSFET, and a scaled planar DMOSFET, all of which make use of technology developed under this program.

Project Activities

This project was tasked with (i) developing process technology for advanced SiC power MOSFETs in the medium-voltage (400 – 1200 V) regime, (ii) integrating the unit processes into a full flow process, (iii) fabricating and characterizing both tri-gate (FinFET) MOSFETs and deeply-scaled, fully self-aligned trench MOSFETs (IMOSFETs), and (iv) developing contacts with industry with the goal of transferring this technology into commercial production. The new processing modules include high-energy (MeV) ion implantations that require thicker masks, and narrow (0.5 µm) SiC trenches with vertical sidewalls, minimal sidewall roughness, and negligible sidewall roughness. All these objectives were achieved. Working prototypes of both the tri-gate MOSFET and the IMOSFET were demonstrated, with performance that approximated or exceeded our program goals. As a result of our success, we were able to attract follow-on funding in the form of a five-year development contract with GlobalFoundries.

The two main modifications to the SOW were (i) to discontinue work on 2-µm deep trenches for the tri-gate MOSFET because of the minimal advantage over 1-µm deep trenches, and (ii) to suspend work on including waffle substrates because the device dimensions were comparable to the substrate thickness, and substrate resistance had already been reduced by current spreading.

Project Outputs

A. Journal Articles

[1] R. Ramamurthy, N. Islam, M. Sampath, D. T. Morisette, and J. A. Cooper, "The tri-gate MOSFET: a new vertical power transistor in 4H-SiC," *IEEE Electron Device Letters*, **42**, 90 (2021).

[2] J. A. Cooper, M. Sampath, D. T. Morisette, C. Anderson, M. Westphal, J. Ransom, C. Stellman, and S. Bayne, "Gate-charge scaling for increased short-circuit withstand time in silicon carbide power MOSFETs," *IEEE Transactions on Electron Devices*, **68**, 4577 (2021).

[3] B. D. Rummel, J. A. Cooper, D. T. Morisette, L. Yates, C. Glaser, A. T. Binder, K. Ramadoss, R. J. Kaplar, "Sources of measurement error and methods to improve accuracy in quasi-static capacitance-voltage measurements of interface state density in wide bandgap semiconductors," *Journal of Applied Physics*, **134**, 125302 (2023).

B. Conference Presentations

[1] J. A. Cooper, "Progress is impossible without change: innovation as a driver of SiC technological evolution," [PLENARY] *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

[2] J. A. Cooper, D. T. Morisette, and M. Sampath, "Increased short-circuit withstand time and reduced DIBL by constant-gate-charge scaling in SiC power MOSFETs," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019)*, Kyoto, Japan, September 29 - October 4, 2019.

[3] M. Sampath, A. Salemi, D. T. Morisette, and J. A. Cooper, "The IMOSFET: a deeply-scaled, fully-self-aligned trench MOSFET," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2019),* Kyoto, Japan, September 29 - October 4, 2019.

[4] M. Sampath, D. T. Morisette, and J. A. Cooper, "Constant-gate-charge scaling for increased short-circuit withstand time in SiC power devices," *International Reliability Physics Symposium (Virtual IRPS 2020)* April 28 – May 30, 2020.

[5] M. Sampath, D. T. Morisette, and J. A. Cooper, "The IMOSFET: A deeply-scaled, fully-self-aligned trench MOSFET in 4H-SiC," *International Conference on Silicon Carbide and Related Materials (ICSCRM-2022),* Davos, Switzerland, September 11-22, 2022.

[6] B. Ngu, M. D. Gaffar, C. DiMarino, J. A. Cooper, M. Sampath, and D. T. Morisette, "Characterization of constant-gate-charge scaled MOSFETs to improve silicon carbide MOSFET Robustness," *PCIM Europe*, Nuremberg, Germany, May 9-11, 2023.

[7] J. A. Cooper, D. T. Morisette, and B. D. Rummel, "Evaluation and Optimization of the MOS Interface in SiC Power DMOSFETs," **[INVITED],** *International Conference on Silicon Carbide and Related Materials (ICSCRM-2023)*, Sorrento, Italy, September 17–27, 2023.

C. Status Reports

(N/A)

D. Media Reports

[1] Feature article on tri-gate MOSFETs in *Semiconductor Today*, December 10, 2020.

E. Invention Disclosures

See patent applications [3, 4, and 5] below

F. Patent Applications/Issued Patents

[1] J. A. Cooper, "MOS-Based Power Semiconductor Device Having Increased Current Carrying Area and Method of Fabricating Same," U.S. Patent #10,403,270, September 3, 2019.

[2] J. A. Cooper, "MOS-Based Power Semiconductor Device Having Increased Current Carrying Area and Method of Fabricating Same," U.S. Patent #11,145,721, October 12, 2021.

[3] J. A. Cooper, D. T. Morisette, and M. Sampath, "Method for Increasing Short-Circuit Robustness in SiC Power MOSFETs," Application #16,438,055, filed June 11, 2019, patent pending.

[4] J. A. Cooper and D. T. Morisette, "Power Devices with Improved On-Resistance," Application PRF-68146-04 PRF-69941-01, filed July 30, 2022, patent pending.

[5] J. A. Cooper, "Level-Shifting Circuit for Gate-Charge-Scaled Thin Oxide SiC MOS-Based Power Devices," Application PRF-70361-01, filed August 3, 2023, patent pending.

G. Licensed Technologies

(N/A)

H. Networks/Collaborations Fostered

(N/A)

I. Websites Featuring Project Work Results

(N/A)

J. Other Products (e.g. Databases, Physical Collections, Audio/Video, Software, Models, Educational Aids or Curricula, Equipment or Instruments)

(N/A)

K. Awards, Prizes, and Recognition

(N/A)

Follow-On Funding

Table 2: Follow-On Funding Received

Source	Funds Committed or Received
GlobalFoundries, Malta, NY	$2,626,091 committed / $725,000 received