Isolated Single-stage Three-phase AC/DC Converter using Bidirectional Switches

Ramandeep Narwal[†], Isaac Wong[x], Subhashish Bhattacharya[‡], B. Jayant Baliga[§] and Douglas C. Hopkins[*]

FREEDM Systems Center, Department of Electrical and Computer Engineering

North Carolina State University

Raleigh, NC 27695, USA

Email: [†]rnarwal@ncsu.edu, [x]twong3@ncsu.edu, [‡]sbhatta4@ncsu.edu, [§]bjbaliga@ncsu.edu, [*]dchopkins@ncsu.edu

Abstract—The advent of the SiC Bidirectional FET (BiDFET), a monolithic 1.2 kV bidirectional switch, has rendered the single-stage three-phase AC/DC converter topology a promising approach for implementing AC/DC converters. This topology, which integrates a full-bridge converter with a single-phase to three-phase matrix converter via a high-frequency transformer, is particularly suitable for applications requiring galvanic isolation, buck-boost functionality, and bidirectional power flow. The single-stage design eliminates the need for bulky and unreliable electrolytic capacitors, and utilizes a single magnetic component for power transfer. In the matrix converter, bidirectional switches, which were traditionally implemented using combinations of multiple semiconductor devices such as MOSFETs, IGBTs, and diodes, can now be realized using the single-chip solution, BiDFET. This advancement leads to a lower switch count, compact converter implementation, with lower inductance commutation cells, thereby enhancing the overall efficiency and compactness of the system. The paper presents a unified model of the converter, considering all control parameters, including the duty cycles and phase shift of transformer voltages. Detailed expressions for power transfer, transformer currents, and currents at AC and DC ports are provided. Additionally, the paper outlines the conditions necessary for soft-switching of all switches and the commutation schemes required for the practical implementation of the matrix converter modulation scheme. A hardware prototype of a 10 kW, 480 $V_{RMS, LL}$/ 800 V AC/DC system has been developed, and experimental results are presented to demonstrate its performance.

Index Terms—Bidirectional switches, SiC bidirectional FET, BiDFET, four-quadrant switches, isolated AC/DC converter, matrix converter, dual active bridge (DAB), modeling, modulation, commutation, soft switching, zero voltage switching (ZVS).

Fig. 1. Isolated three-phase AC/DC converter: (a) Two-stage implementation using dual-active bridge (DAB) cascaded with voltage-source converter through a bulky electrolytic capacitor, and (b) Single-stage implementation using full-bridge converter directly interfaced with monolithic SiC BiDirectional FET (BiDFET) based single-phase to three-phase matrix converter through a high-frequency transformer and inductor.

I. INTRODUCTION

The three-phase AC/DC converters play a vital role in high-power applications, including photovoltaic inverters, data centers, telecommunications, electric vehicle battery chargers, DC microgrids and wind energy conversion systems. A salient requirement in many of these applications is galvanic isolation, which mitigates ground loop issues, facilitates voltage scaling, ensures fault tolerance, and accommodates application-specific grounding configurations. Moreover, the dynamic DC voltage profiles inherent in interfaces with batteries and solar arrays underscore the necessity for converter systems that possess both buck and boost capabilities.

Conventionally, these isolation and buck-boost features are realized using a two-stage conversion topology. This involves a voltage source converter followed by a DC-DC converter (series resonant converter or dual active bridge converter) for galvanic isolation. An alternative approach is the single-stage conversion topology, which consists of a full-bridge on the DC-side and a single-phase to three-phase matrix converter on the AC-side, interconnected via a high-frequency transformer. This design not only provides galvanic isolation and buck-boost functionalities in one stage but also obviates the need for an intermediate DC bus formed by bulky and unreliable electrolytic capacitors. Additionally, this topology supports bidirectional power flow, a critical feature for applications such as EV charging stations with Vehicle-to-Grid (V2G) functionality, grid-connected energy storage systems (ESS), and hybrid energy systems.

The isolated single-stage single-phase AC/DC converter topology, a derivative of the dual active bridge converter [1], was first reported in [2], with its three-phase AC/DC converter counterpart subsequently introduced in [3]. The power flow within this converter is modulated by manipulating the duty cycles and phase shift of the transformer voltages. A plethora of literature exists where certain control parameters are adjusted while others are held constant, resulting in converter models that are specifically tailored to these varying parameters. For instance, the approaches in [3] and [4] employ phase-shift control, whereas [5] maintains a phase-shift of 90% and varies the matrix converter's modulation index. The study in [6] presents a coordinated control of both the phase-shift and modulation index, but keeps the full-bridge output duty cycle fixed at 50%. Conversely, in [7], the matrix converter side transformer voltage duty cycle is kept constant, while
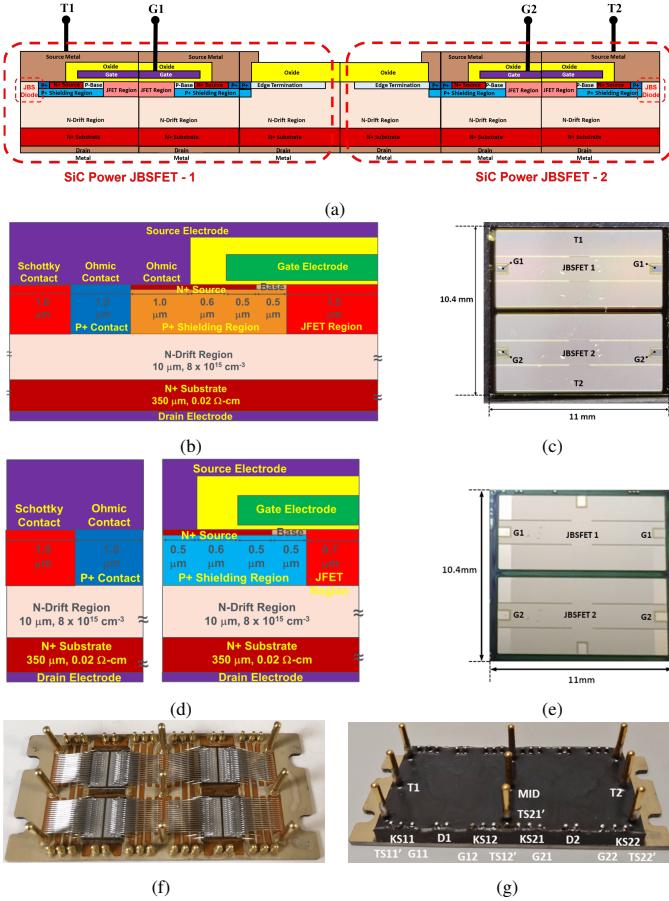
Fig. 2. (a) The 4H-SiC 1.2 kV BiDirectional FET (BiDFET) device structure; (b), (c) Gen-1 BiDFET device JBSFET cross-section and chip image; (d) (e) Gen-2 BiDFET device JBS diode and MOSFET cross-sections and chip image; and (f), (g) Custom designed BiDFET half-bridge module with and without the encapsulation.

phase-shift and full-bridge output duty cycle are varied. [8] introduces a modulation strategy for rectifier-mode operation, incorporating all control parameters. However, it does not provide expressions for power flow and harmonic content in the AC and DC port currents. Furthermore, the RMS value of the transformer current is derived using Fourier series expansion, with its accuracy contingent upon the number of harmonics considered.

In this paper, a generic model of the converter is presented which considers all the converter control parameters and provides expressions for power transfer, transformer currents (RMS and peak), three-phase AC currents (RMS, fundamental, harmonics), and DC current (RMS, DC, harmonics). This model can be employed to establish an optimization problem for converter design, as well as to derive small-signal and large-signal models of the converter, although these aspects are not explored within the scope of this paper. Also, in contrast to prior research that employed bidirectional switches realized from combinations of MOSFETs, IGBTs, and diodes, this paper introduces the use of a single-chip, monolithic bidirectional switch: the SiC Bidirectional FET (BiDFET). The SiC BiDFET is a monolithic bidirectional device comprised of two constituent 1.2 kV 4H-SiC JBS (Junction Barrier Schottky)-

diode-embedded-power MOSFETs (JBSFETs) connected in a common-drain configuration [9], [10]. The monolithic design of the BiDFET enables a reduction in device count, minimizes switch volume, and lowers commutation cell inductance, while simplifying packaging. These attributes collectively contribute to a more efficient and compact converter implementation.

The BiDFET device was fabricated at the six-inch commercial foundry, X-FAB, using the NCSU PRECiSE$^{\text{TM}}$ process [11]. The fabricated BiDFET die has a chip area of approximately 1.1 cm^2, with each internal JBSFET occupying an active area of 0.45 cm^2. The device design incorporates two gate-pads for each JBSFET. The first-generation (Gen-1) BiDFET die demonstrated an on-state resistance of 46 mΩ, while the second-generation (Gen-2) BiDFET achieved a reduced on-resistance of 23 mΩ using the same chip area, by spatially separating the JBS diodes from the MOSFET cells and positioning them at the chip's four corners [9]. The optimized design and performance of the single-phase AC/DC DAB converter, utilizing discrete packages of Gen-1 BiDFET devices, are detailed in [12], [13]. Additionally, a custom half-bridge module designed to house up to two BiDFET dies per switch location is demonstrated in [14].

The paper's structure is as follows: Section II delves into the converter operation, elucidating expressions for power transfer, transformer currents, AC port currents, and DC port current. It also delineates the conditions essential for achieving soft-switching in each commutation cell and ensuring sinusoidal AC currents at the three-phase AC port. Section III provides a brief overview of the hardware prototype. Section IV presents the hardware results demonstrating the converter's performance under varying load conditions. The hardware prototype is designed for flexibility, accommodating phase-legs built using both back-to-back (B2B) MOSFETs and BiDFET modules. The hardware prototype, when equipped with B2B MOSFETs is tested upto 800 V DC input and 480 V$_{\text{RMS}}$, 10 kW AC output. On the other hand, the version equipped with the Gen-1 BiDFET-based half-bridge module (single device per switch location) is tested up to 400 V DC input and 240 V$_{\text{RMS}}$, 2.5 kW AC output.

II. CONVERTER OPERATION AND STEADY-STATE MODEL

The isolated single-stage AC/DC converter consists of a full-bridge converter on the DC port and a single-phase to three-phase matrix converter on the three-phase AC port, interconnected through a single-phase high-frequency transformer and inductor. An external inductor can be employed, or alternatively, a transformer with the requisite leakage inductance can be utilized. The full-bridge converter generates a quasi-square wave AC voltage, v_{tdc}, while the matrix converter produces a half-wave symmetric AC staircase waveform, v_{tac}. The staircase waveform is achieved using two of the three line-to-line voltages, v_{ab}, v_{bc}, and v_{ca}, and a zero voltage created by shorting the transformer through matrix converter switches corresponding to the same phase. This zero voltage can be created by switches corresponding to the phase common to v_1 and v_2, as this helps reduce the number of switchings
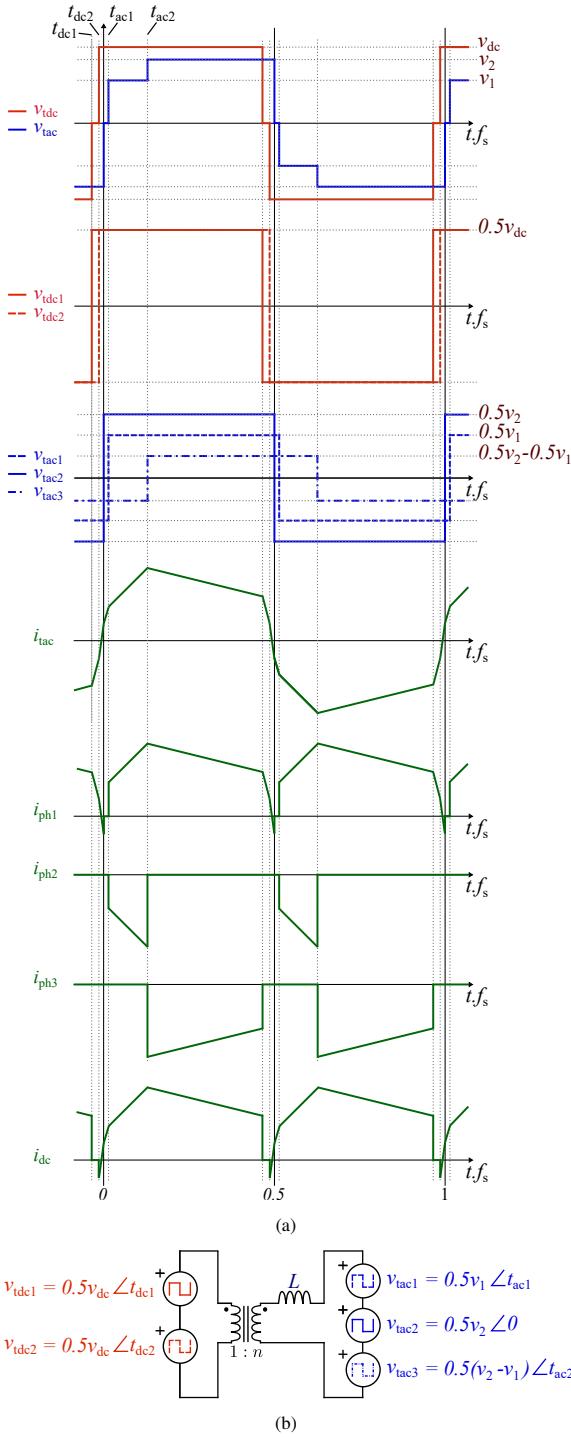
Fig. 3. Isolated single-stage AC/DC converter (a) Transformer voltages (v_{tdc}, v_{tac}) and their decomposed square-wave voltages ($v_{\text{tdc}} = v_{\text{tdc1}} + v_{\text{tdc2}}$ and $v_{\text{tac}} = v_{\text{tac1}} + v_{\text{tac2}} + v_{\text{tac3}}$), AC-side transformer current (i_{tac}), AC port currents (i_{ph1}, i_{ph2}, and i_{ph3}), and DC port current (i_{dc}) [Figure is not to scale]. (b) Equivalent model.

per switching cycle. The power transfer between the converter terminals can be controlled using the duty cycles of v_{tdc}, v_1 and v_2, as well as phase-shift between v_{tdc} and v_{tac}.

The transformer voltages, v_{tdc} and v_{tac}, can be expressed as the sums of AC square-wave voltages [15], [8], as illustrated in Fig. 3a.

$$v_{\text{tdc}} = v_{\text{tdc1}} + v_{\text{tdc2}}$$
$$v_{\text{tac}} = v_{\text{tac1}} + v_{\text{tac2}} + v_{\text{tac3}} \tag{1}$$

where

$$v_{\text{tdc1}} = 0.5 \cdot v_{\text{dc}} \angle t_{\text{dc1}}$$
$$v_{\text{tdc2}} = 0.5 \cdot v_{\text{dc}} \angle t_{\text{dc2}}$$
$$v_{\text{tac1}} = 0.5 \cdot v_1 \angle t_{\text{ac1}} \tag{2}$$
$$v_{\text{tac2}} = 0.5 \cdot v_2 \angle 0$$
$$v_{\text{tac3}} = 0.5 \cdot (v_2 - v_1) \angle t_{\text{ac2}}$$

The phase-shift times t_{ac1}, t_{ac2}, t_{dc1} and t_{dc2}, normalized with respect to switching cycle period and defined relative to v_{tac2}, encapsulate all the control parameters of the converter. By employing the principles of simple phase-shift modulation of a single-phase dual-active bridge (DAB) [1], in conjunction with superposition principles, a unified model of the converter is derived. This model facilitates a comprehensive understanding of the converter's operation across all control parameters.

A. Power transfer over a switching period

Given the high switching frequency of the converter compared to the grid frequency, the average power over the converter's switching period approximates the instantaneous power, P, processed by the converter. Power transferred between two square-wave voltages having amplitudes v_a and v_b, separated by an inductor, L, and a 1:N turns-ratio transformer, and having a phase-shift time normalized with respect to switching cycle period, t_ϕ is given by

$$P = \frac{N \cdot v_{\text{a}} \cdot v_{\text{b}}}{f_{\text{s}} \cdot L} \cdot t_\phi \cdot (1 - 2|t_\phi|) \tag{3}$$

By applying the superposition principle, the power transferred from the DC-side to the AC-side can be calculated as the summation of the power transferred from each of the DC-side square-wave voltages (v_{tdc1} and v_{tdc2}) to each of the AC-side square-wave voltages (v_{tac1}, v_{tac2}, and v_{tac3}).

$$
\begin{aligned}
P =& P_{\text{dc1-ac1}} + P_{\text{dc1-ac2}} + P_{\text{dc1-ac3}} + P_{\text{dc2-ac1}} + P_{\text{dc2-ac2}} + P_{\text{dc2-ac3}} \\
=& \frac{N \cdot v_{\text{dc}}}{4 f_{\text{s}} \cdot L} [v_1 t_{\phi_{11}} (1 - 2|t_{\phi_{11}}|) + v_2 t_{\phi_{12}} (1 - 2|t_{\phi_{12}}|) + \\
& (v_2 - v_1) t_{\phi_{13}} (1 - 2|t_{\phi_{13}}|) + v_1 t_{\phi_{21}} (1 - 2|t_{\phi_{21}}|) + \\
& v_2 t_{\phi_{22}} (1 - 2|t_{\phi_{22}}|) + (v_2 - v_1) t_{\phi_{23}} (1 - 2|t_{\phi_{23}}|)]
\end{aligned}
\tag{4}
$$

The differences in phase-shift times between square wave voltages are normalized to a range of -0.5 to 0.5 to ensure the validity of the power transfer equation.

$$
\begin{aligned}
t_{\phi_{11}} &= (0.5 - t_{\text{dc1}} + t_{\text{ac1}})\%1 - 0.5 \\
t_{\phi_{12}} &= -t_{\text{dc1}} \\
t_{\phi_{13}} &= (0.5 - t_{\text{dc1}} + t_{\text{ac2}})\%1 - 0.5 \\
t_{\phi_{21}} &= (0.5 - t_{\text{dc2}} + t_{\text{ac1}})\%1 - 0.5 \\
t_{\phi_{22}} &= -t_{\text{dc2}} \\
t_{\phi_{23}} &= (0.5 - t_{\text{dc2}} + t_{\text{ac2}})\%1 - 0.5
\end{aligned}
\tag{5}
$$

Using the modulo operation with 1 (denoted as %1) ensures that any number is wrapped within the interval [0, 1). If the number is negative, it is brought into the [0, 1) interval in a cyclic manner, ensuring periodicity. If the number is ≥ 1, it is reduced to lie within the [0, 1) range.

B. Transformer currents

By applying the superposition principle in an alternative manner, the transformer currents, i_{tac} and i_{tdc}, can be calculated as the cumulative sum of triangular-shaped AC currents contributed by each independent square-wave AC voltage appearing across the inductor, L.

$$
\begin{aligned}
i_{\text{tac}} = \frac{i_{\text{tdc}}}{N} &= i_{\text{dc1}} + i_{\text{dc2}} + i_{\text{ac1}} + i_{\text{ac2}} + i_{\text{ac3}} \\
&= \frac{1}{8f_s L}[Nv_{\text{dc}}(1 - 4|0.5 - (t - t_{\text{dc1}})\%1|) \\
&\quad + Nv_{\text{dc}}(1 - 4|0.5 - (t - t_{\text{dc2}})\%1|) \\
&\quad - v_1(1 - 4|0.5 - (t - t_{\text{ac1}})\%1|) \\
&\quad - v_2(1 - 4|0.5 - t\%1|) \\
&\quad - (v_2 - v_1)(1 - 4|0.5 - (t - t_{\text{ac2}})\%1|)]
\end{aligned}
\tag{6}
$$

Under ideal conditions, the transformer currents exhibit a half-wave symmetric, piecewise linear waveform. Consequently, their RMS and peak values can be determined using an algorithm similar to one reported in [16]. The steps of this algorithm are as follows:

- Identify the switching instants corresponding to the same transformer current switching half-cycle.

$$
\begin{aligned}
t_{\text{swac1}} &= t_{\text{ac1}} \\
t_{\text{swac2}} &= t_{\text{ac2}} \\
t_{\text{swac3}} &= 0.5 \\
t_{\text{swdc1}} &= \begin{cases} t_{\text{dc1}} & \text{if } t_{\text{dc1}} > 0 \\ 0.5 + t_{\text{dc1}} & \text{if } t_{\text{dc1}} \leq 0 \end{cases} \\
t_{\text{swdc2}} &= \begin{cases} t_{\text{dc2}} & \text{if } t_{\text{dc2}} \geq 0 \\ 0.5 + t_{\text{dc2}} & \text{if } t_{\text{dc2}} < 0 \end{cases}
\end{aligned}
\tag{7}
$$

- Arrange the switching instants in ascending order to ensure continuity of the piece-wise linear function.

$$
\{t_1, t_2, t_3, t_4, t_5\} \in \{t_{\text{swac1}}, t_{\text{swac2}}, t_{\text{swac3}}, t_{\text{swdc1}}, t_{\text{swdc2}}\}
\tag{8}
$$

- Determine the transformer current, i_{tac}, at each switching instant.

$$
\{I_1, I_2, I_3, I_4, I_5\} = i_{\text{tac}} \text{ at } \{t_1, t_2, t_3, t_4, t_5\}
\tag{9}
$$

- Compute the transformer current RMS value over the switching cycle by summing the squares of weighted and normalized RMS values of the individual subintervals, and taking the square root.

$$
i_{\text{tac,RMS}} = \sqrt{\sum_{k=1}^{k=5} \frac{2}{3}(t_{k+1} - t_k)(I_k^2 + I_k I_{k+1} + I_{k+1}^2)}
\tag{10}
$$

$$
\forall\, k \in \{1, 2, 3, 4, 5\}; \; I_6 = -I_1; \; t_6 = t_1 + 0.5
$$

- Compute the transformer current peak, which is also the peak of the current flowing through the semiconductor devices.

$$
i_{\text{tac,peak}} = \frac{i_{\text{tdc,peak}}}{N} = \max(|I_1|, |I_2|, |I_3|, |I_4|, |I_5|)
\tag{11}
$$

C. Three-phase AC port currents

The instantaneous values of the phase currents' fundamental AC line frequency components can be approximated using their mean value over a switching cycle. The transformer current, i_{tac}, flows into each phase during specific time intervals, which are determined by the switching instants, as depicted in Fig. 3a. Therefore, the fundamental components of phase currents can be calculated by integrating the transformer current over these distinct intervals. The algorithm for determining the fundamental, RMS, and harmonic content of phase currents comprises the following steps:

- Identify the time interval during which transformer current, i_{tac} flows into each phase.
- Compute the phase current average value over the switching cycle by summing the integrals across the individual subintervals and dividing the result by normalized half-switching-cycle period (= 0.5).

$$
\begin{aligned}
\bar{i}_{\text{ph1}} &= \sum_{k|t_k=t_{\text{swac1}}}^{k|t_k=t_{\text{swac3}}-1} (t_{k+1} - t_k)(I_k + I_{k+1}) \\
\bar{i}_{\text{ph2}} &= \sum_{k|t_k=t_{\text{swac1}}}^{k|t_k=t_{\text{swac2}}-1} -(t_{k+1} - t_k)(I_k + I_{k+1}) \\
\bar{i}_{\text{ph3}} &= \sum_{k|t_k=t_{\text{swac2}}}^{k|t_k=t_{\text{swac3}}-1} -(t_{k+1} - t_k)(I_k + I_{k+1})
\end{aligned}
\tag{12}
$$

The current i_{ph1} corresponds to the phase that stays active throughout the switching positive half-cycle, while i_{ph2} and i_{ph3} denote the currents corresponding to the returning phases in v_1 and v_2, respectively.

- Compute the phase current RMS value over the switching cycle by summing the squares of weighted and normalized RMS values of the individual subintervals within the interval of interest, and taking the square root.

$$
\begin{aligned}
i_{\text{ph1,RMS}} &= \sqrt{\sum_{k|t_k=t_{\text{swac1}}}^{k|t_k=t_{\text{swac3}}-1} \frac{2}{3}(t_{k+1} - t_k)(I_k^2 + I_k I_{k+1} + I_{k+1}^2)} \\
i_{\text{ph2,RMS}} &= \sqrt{\sum_{k|t_k=t_{\text{swac1}}}^{k|t_k=t_{\text{swac2}}-1} \frac{2}{3}(t_{k+1} - t_k)(I_k^2 + I_k I_{k+1} + I_{k+1}^2)} \\
i_{\text{ph3,RMS}} &= \sqrt{\sum_{k|t_k=t_{\text{swac2}}}^{k|t_k=t_{\text{swac3}}-1} \frac{2}{3}(t_{k+1} - t_k)(I_k^2 + I_k I_{k+1} + I_{k+1}^2)}
\end{aligned}
\tag{13}
$$

- Compute the RMS value of harmonic content in each phase current.

$$i_{\text{ph1,h,RMS}} = \sqrt{i_{\text{ph1,RMS}}^2 - \bar{i}_{\text{ph1}}^2}$$
$$i_{\text{ph2,h,RMS}} = \sqrt{i_{\text{ph2,RMS}}^2 - \bar{i}_{\text{ph2}}^2} \tag{14}$$
$$i_{\text{ph3,h,RMS}} = \sqrt{i_{\text{ph3,RMS}}^2 - \bar{i}_{\text{ph3}}^2}$$

D. DC port current

The DC component value of the DC port current is simply determined using the power equation.

$$\bar{i}_{\text{dc}} = \frac{P}{V_{\text{dc}}} \tag{15}$$

The RMS value of the DC port current is calculated in a manner analogous to the AC port currents. This involves identifying the time intervals during which the transformer current, i_{tdc}, flows into the DC port, and then integrating this current over these intervals.

$$i_{\text{dc,RMS}} =$$
$$\begin{cases} N\sqrt{\sum_{k|t_k=t_{\text{swdc2}}}^{k|t_k=t_{\text{swdc1}}-1} R} & \text{if } t_{\text{dc1}} \cdot t_{\text{dc2}} \leq 0 \\[2ex] N\sqrt{\sum_{k=0}^{k|t_k=t_{\text{swdc1}}-1} R + \sum_{k|t_k=t_{\text{swdc2}}}^{k=4} R} & \text{if } t_{\text{dc1}} \cdot t_{\text{dc2}} > 0 \end{cases}$$
$$\forall \ k \in \{1, 2, 3, 4, 5\}; \ I_0 = -I_5; \ t_0 = 0;$$
$$R = \frac{2}{3}(t_{k+1} - t_k)(I_k^2 + I_k I_{k+1} + I_{k+1}^2) \tag{16}$$

The RMS value of harmonic content in DC port current can be calculated as

$$i_{\text{dc,h,RMS}} = \sqrt{i_{\text{dc,RMS}}^2 - \bar{i}_{\text{dc}}^2} \tag{17}$$

E. Sinusoidal AC currents constraint

Using the instantaneous power theory [17], the instantaneous reactive power, Q, at three-phase AC port is given by

$$Q = \frac{1}{\sqrt{3}}[v_{\text{ab}}i_c + v_{\text{bc}}i_a + v_{\text{ca}}i_b] \tag{18}$$

Under ideal operation, when all line-to-line voltages and phase currents are balanced and exhibit a sinusoidal nature, the following conditions apply:

$$i_a + i_b + i_c = 0$$
$$v_{\text{ab}} + v_{\text{bc}} + v_{\text{ca}} = 0 \tag{19}$$

Therefore, expression for Q can be simplified to

$$Q = \frac{1}{\sqrt{3}}[v_{\text{ab}}(i_b + 2i_c) - v_{\text{ac}}(i_c + 2i_b)] \tag{20}$$

For instance, when the condition $v_a > v_b > v_c$ holds, and if v_{ab}, v_{ac} are chosen as v_1, v_2 respectively, then i_{ph2} and i_{ph3} correspond to i_b and i_c respectively. It leads to a generalized expression for Q.

$$Q = \frac{1}{\sqrt{3}}[v_1(\bar{i}_{\text{ph2}} + 2\bar{i}_{\text{ph3}}) - v_2(\bar{i}_{\text{ph3}} + 2\bar{i}_{\text{ph2}})] \tag{21}$$

This condition should be verified while calculating the phase-shift times to ensure the generation of sinusoidal AC currents at the three-phase AC port.

F. Commutation schemes and Soft-switching constraints

DC-side H-bridge consists of two one-pole, two-throw current-bidirectional commutation cells, S_{ap} and S_{an} form the first, and S_{Bp} and S_{Bn} form the second. A simple dead-time-based two-step commutation scheme can be utilized to prevent a short-circuit across the DC voltage source during the commutation process, independent of i_{tdc} polarity. On the other hand, AC-side matrix converter consists of two one-pole, three-throw bidirectional commutation cells, Q_{ap}, Q_{bp} and Q_{cp} form the upper commutation cell, and Q_{an}, Q_{bn} and Q_{cn} form the lower commutation cell. To prevent short-circuit across the AC terminals and open-circuit of the power transfer inductor and transformer leakage inductance, the bidirectional commutation cells require a multi-step commutation scheme, the choice of which depends on whether i_{tac} polarity, v_{tac} voltage-edge polarity, or both polarities are known [18].

At the points $t \cdot f_s = 0$ and t_{ac1} during the positive half-switching-cycle (as well as the corresponding times in the negative half-switching-cycle), v_{tac} undergoes transitions to or from a zero voltage. Hence, voltage-edge polarity is known, and consequently voltage polarity-based four-step commutation is employed at these switching instants. Conversely, at $t \cdot f_s = t_{\text{ac2}}$, v_1 might be greater than or lesser than v_2, depending on the selection of line-to-line voltages, AC power factor, the point of operation on AC line-cycle, and the voltage ripple at the switching node. Therefore, current polarity-based four-step commutation is chosen for this switching instant.

Switching the commutation cells results in either rising or falling voltage edges in transformer voltages, v_{tdc} and v_{tac}. Achieving zero-voltage-switching (ZVS) in a commutation cell requires the current to flow into the pole and commutate from the phase with a lower voltage to the phase with a
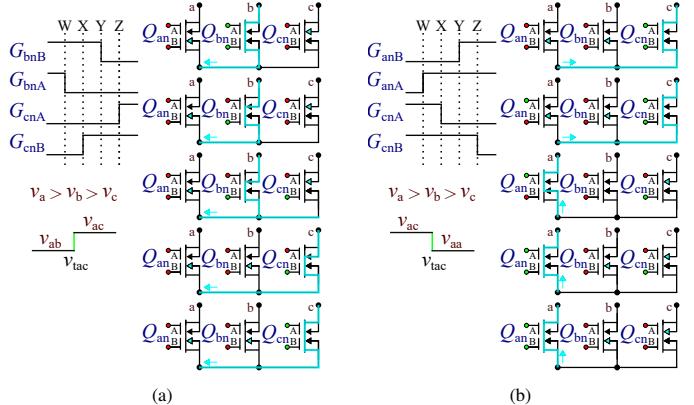
Fig. 4. (a) Matrix converter's lower commutation cell depicting current transition from phase b to phase c. Here, Q_{ap} is active with positive i_{tac} current. The event aligns with the $t \cdot f_s = t_{\text{ac2}}$ switching instant, utilizing the current polarity-based commutation scheme. (b) In the same cell, the current commutates from phase c to phase a with Q_{ap} active and negative i_{tac} current. This transition is synchronized with the $t \cdot f_s = 0.5$ switching instant, adopting a voltage polarity-based commutation scheme. The blue line denotes current flow path, and the blue body-diodes indicate reverse-biased diodes.

higher voltage, or vice versa [18]. Therefore, to satisfy the soft-switching condition, the transformer current should be negative at rising edges of v_{tdc} and falling edges of v_{tac}, and positive at falling edges of v_{tdc} and rising edges of v_{tac}. Due to the half-wave symmetry of transformer ac voltages and currents, soft-switching conditions need to be evaluated only in half of the switching cycle. Specifically, v_{tdc} experiences rising edges at $t \cdot f_s = t_{dc1}$ and t_{dc2}, while v_{tac} incurs rising edges at $t \cdot f_s = 0$, and t_{ac2}. v_{tac} can experience rising or falling edge at t_{ac1}, depending on the relative magnitudes of v_1 and v_2. By calculating the transformer current at these switching instants using (6), the soft-switching conditions can be evaluated independently for each commutation cell. The zero-voltage-switching conditions are defined as

$$
\begin{aligned}
&i_{tdc}(t_{dc1}), \ i_{tdc}(t_{dc2}) < -I_{zvs,min}; \\
&i_{tac}(t_{ac1}), \ i_{tac}(t_{ac2}) > I_{zvs,min}; \\
&i_{tac}(t_{ac1}) = \begin{cases} > I_{zvs,min} & \text{if } v_2 > v_1 \\ < -I_{zvs,min} & \text{if } v_2 < v_1 \end{cases}
\end{aligned} \tag{22}
$$

$I_{zvs,min}$ is the minimum current necessary to fully discharge the switch output capacitance within a specified commutation time. Zero-current-switching (ZCS) will occur in the commutation cells when the transformer currents reach zero at corresponding switching instants.

III. HARDWARE DESIGN

A hardware prototype of the single-stage isolated AC/DC converter (Fig. 5a) is developed for the system parameters listed in Table I. This prototype supports phase-legs with both back-to-back (B2B) TO-247 package MOSFETs and BiDFET half-bridge modules. Phase-leg PCBs with B2B MOSFETs are interchangeable with those featuring BiDFET half-bridge modules. For this paper, the half-bridge module having single Gen-1 BiDFET die per switch location is utilized. The full-bridge converter is realized by employing two of the three phase-legs housed within a printed circuit board assembly (PCBA) that is same as the matrix converter. The high frequency AC link comprises a 27 µH inductor and a transformer

TABLE I. System parameters.

Parameter	Variable	Value
Nominal power	$P_{o,rated}$	10 kW
Nominal AC voltage	v_{xy}	480 $V_{RMS, LL}$
Nominal DC voltage	V_{dc}	800 V
DC filter capacitor	C_{dc}	150 µF
AC line frequency	f_L	60 Hz
Power transfer inductor	L	27.6 µH
Transformer turns ratio	$1:N$	18:14
Filter capacitors	C_f	2 µF
Filter inductors	L_f	10 µH
Filter damping resistors	R_f	6 Ω
DC-side Switches	S	C3M0016120K
AC-side Switches	Q	C3M0016120K/ BiDFET
Switching frequency	f_s	50 kHz
Switches gate resistance	R_G	10 Ω
Switches gate voltage	V_{GS}	15/ -4 V
Overlap and dead time	t_o, t_d	300 ns

(a)

(b)   (c)

(d)
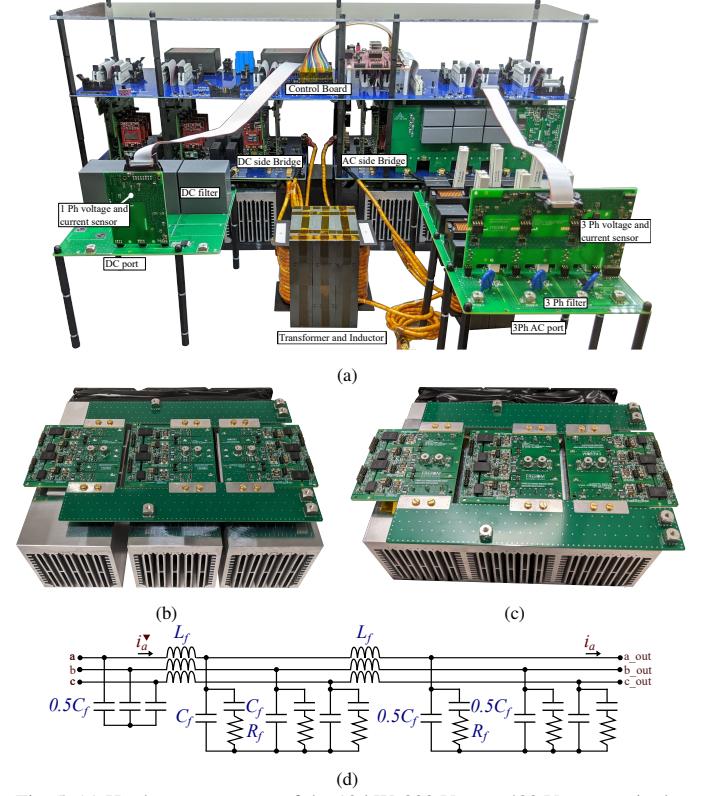
Fig. 5. (a) Hardware prototype of the 10 kW, 800 V_{DC} to 480 $V_{RMS, LL}$ single-stage isolated three-phase AC/DC converter, (b) Back-to-back MOSFETs based matrix converter power stage, (c) BiDFET half-bridge module based matrix converter power stage, and (b) Three-phase AC filter schematic.

with 18:14 turns ratio and 12.1 µH AC-side referred leakage inductance. Further details on transformer and inductor design optimization and implementation are provided in [19]. The three-phase AC filter schematic is depicted in Fig. 5d. This paper's scope is limited to testing the converter's performance in inverter mode across varying three-phase Y-connected resistive loads at the AC terminals.

IV. EXPERIMENTAL RESULTS

The hardware prototype was tested using a DC power supply on its DC-side and a Y-connected resistive load on the AC-side. The control parameters (t_{dc1}, t_{dc2}, t_{ac1}, and t_{ac2}) were calculated to optimize the transformer RMS current, and subsequently stored in a look-up table to operate the converter in an open-loop configuration. The experimental results for the converter, featuring the B2B MOSFETs-based matrix converter, at 800 V DC input and 480 $V_{RMS, LL}$, 10 kW AC output, are detailed in Fig. 6. Fig. 6a shows the transformer voltages (v_{tdc} and v_{tac}), transformer currents (i_{tdc} and i_{tac}), three-phase AC line-to-line voltages(v_{ab}, v_{bc}, and v_{ca}), and phase current (i_a), both before and after filtering. Using the Hioki Power Analyzer PW6001, the converter's efficiency was gauged at 98.1%, and AC currents THD at 3.5% (Fig. 6e).

Fig. 6f charts the converter efficiency and AC currents THD against load variation of 2 to 10 kW. Within this operational power range, the converter's efficiency rises from 94.6% at 2 kW to 98.1% at 10 kW due to the greater
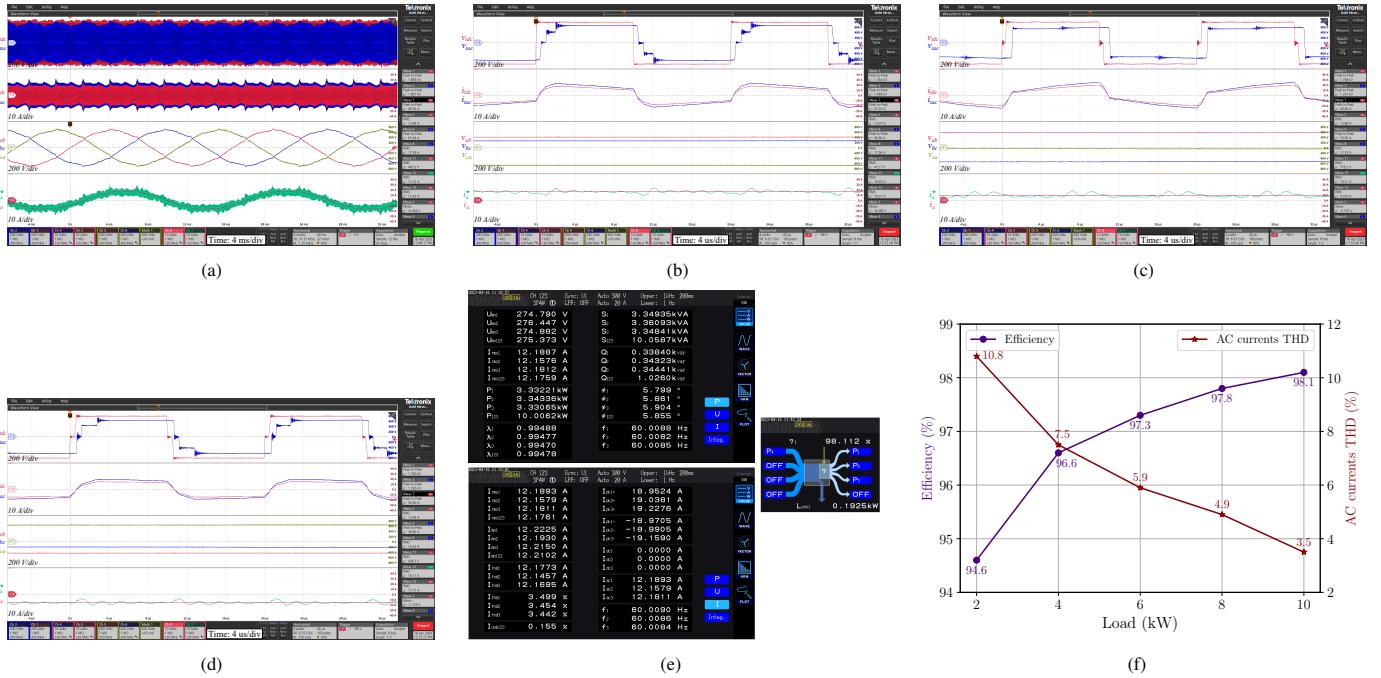
Fig. 6. Experimental results for isolated AC/DC system implemented using B2B MOSFET devices based matrix converter, at 480 V$_{\text{RMS, LL}}$, 10 kW output, and 800 V DC input. (a) Operating waveforms waveforms, (b), (c), (d) Zoomed-in switching waveforms, (e) converter efficiency and AC currents THD measured using Hioki Power Analyzer PW6001, and (f) efficiency and AC currents THD variation with load.

influence of switching losses over conduction losses at low power operation. At a power level where conduction losses start dominating switching losses, the converter efficiency will start declining. The stated efficiency omits losses from the gate driver, control board, and cooling fan, as these are contingent on the implementation specifics. The DC-side full-bridge also uses back-to-back MOSFETs, leading to equivalent switching losses same as a single MOSFET but doubled conduction losses. An alternative full-bridge converter design utilizing a single MOSFET will enhance converter efficiency.

Conversely, AC currents THD reduces from 10.8% at 2 kW to 3.5% at 10 kW operation. This decrease is primarily attributed to the three-phase filter, which draws a capacitive current based on consistent AC voltages, regardless of load variations. As a result, converter's AC currents become increasingly capacitive as the load decreases, while the control parameters were derived under the assumption of zero-reactive power, that is, $Q = 0$ in (21). Additionally, THD is affected by the commutation process's impact on switch duty cycles. By setting appropriate value for Q and including compensation for errors caused by commutation process, during the calculation of the control parameters, the AC currents THD can be improved throughout the range of operation. To verify soft-switching at 10 kW operation, zoomed-in waveforms over a switching cycle at various points on the line cycle are depicted in Fig. 7(b-d). All the soft-switching constraints, as defined in (22), are satisfied.

Furthermore, testing was conducted on the BiDFET half-bridge module-based matrix converter, retaining the original DC-side full-bridge with back-to-back MOSFETs. Experimen-

tal results at 400 V DC input and 240 V$_{\text{RMS, LL}}$, 2.5 kW AC output are depicted in Fig. 7. The converter achieved an efficiency of 97.7% and an AC currents THD of 3.9%. These results demonstrate that the BiDFET devices can withstand the demands of continuous converter operation and are poised to become a reliable cornerstone in power converter designs.

V. CONCLUSION

The emergence of monolithic 1.2 kV SiC Bidirectional FET (BiDFET) has positioned the single-stage three-phase AC/DC converter topology as an attractive choice for applications that demand galvanic isolation, buck-boost functionality, and bidirectional power flow. This topology inherently eliminates the need for bulky and unreliable electrolytic capacitors, and when implemented using BiDFET, has the potential to realize compact, reliable, and efficient isolated AC/DC converters.

The paper provides a unified model of the single-stage AC/DC converter, detailing power transfer, transformer currents, and both DC and AC port currents in terms of control parameters, t_{dc1}, t_{dc2}, t_{ac1}, and t_{ac2}. It introduces algorithms for determining the RMS value, fundamental component, and harmonic components of both DC and AC port currents, leveraging the expressions derived for transformer currents. These harmonic currents facilitate the design of filters for the AC and DC ports. Additionally, the paper elucidates the conditions required for soft-switching of every commutation cell in the converter, and discusses the selection of commutation schemes based on the matrix converter's switching instants. The same converter model is applicable to the rectifier mode of operation, and can be employed to establish an optimization
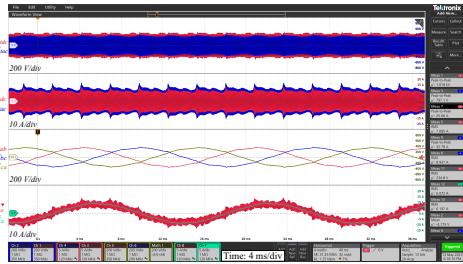
(a)

(b)

Fig. 7. Experimental results for isolated AC/DC system implemented using Gen-1 BiDFET half-bridge modules-based matrix converter at 240 $V_{RMS, LL}$, 2.5 kW output, and 400 V DC input. (a) Line-frequency waveforms, and (b) converter efficiency and AC currents THD measured using Hioki Power Analyzer PW6001.

problem for converter design, as well as to derive small-signal and large-signal models of the converter.

Finally, experimental results from a 10 kW hardware prototype, compatible with both B2B MOSFETs and BiDFET modules, are presented at a switching frequency of 50 kHz. The control parameters were calculated to optimize the transformer currents' RMS value. The B2B MOSFETs-based converter achieved an efficiency of 98.1% and AC currents THD of 3.5% at 800 V DC to 480 $V_{RMS, LL}$, 10 kW operation. On the other hand, the BiDFET module-based converter achieved an efficiency of 97.7% and AC currents THD of 3.9% at 400 V DC to 240 $V_{RMS, LL}$, 2.5 kW operation. These experimental results further validate the design and packaging of the monolithic SiC BiDFET device, demonstrating its suitability for continuous operation within power converters.

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