Switching Characteristics of a 1.2 kV, 50 mΩ SiC Monolithic Bidirectional Field Effect Transistor (BiDFET) with Integrated JBS Diodes

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***Abstract*—The switching performance of large area (1cm x 1cm) monolithic 1.2 kV 50 mΩ 4H-SiC bidirectional field effect transistor (BiDFET) with integrated JBS diodes is reported for the first time. The devices were fabricated in a 6-inch commercial foundry and then packaged in a custom-designed four-terminal module. The switching performance of the BiDFET has been observed to be 1.4x better than that of its internal JBSFETs. Dynamic characterization was performed at 800 V with different gate resistances, current levels and case temperatures. An increase in switching losses was observed for the BiDFET with increasing gate resistance and current level as observed for SiC power MOSFETs. The BiDFET showed a 9% reduction in total switching loss from 25 °C to 150 °C with a current of 10 A.**

Keywords—Silicon Carbide, Monolithic, Bidirectional, Four-Quadrant, Integrated, JBS Diode

I. Introduction

Bidirectional power switches are used in matrix or cycloconverters and multistage inverter circuits to facilitate high-frequency AC-to-AC conversion [1]. These topologies enable power conversion without intermediate storage elements like DC-link capacitors, thus reducing the system volume and enabling higher operating temperatures, increased power density, and improved output waveform quality [2].

The unavailability of commercial high-performance bidirectional switches has hindered the widespread deployment of these topologies [1]. Bidirectional switches have employed various combinations of discrete power transistors and diodes, at the cost of switching and conduction loss and a large device count [3]. The Silicon Carbide (SiC) **BiD**irectional **F**ield **E**ffect **T**ransistor (BiDFET) [3] was developed as a 1.2 kV monolithic four-quadrant switch with integrated JBS diodes designed to achieve a low forward voltage drop and fast switching performance with a single package footprint. The BiDFET is designed with two JBS-integrated MOSFET (JBSFET) devices grown with a common drain connection. The cross section of the BiDFET cell is shown in Fig. 1. 1.2 kV SiC JBSFETs have been fabricated previously with an active area of 0.045 cm² to achieve an on-resistance of 230 mΩ [4]. The BiDFET employs a similar cell structure for the internal JBSFETs, but with a 10x larger active area, resulting in an overall on-resistance of 50 mΩ.

This paper reports the dynamic characterization of the 1.2 kV SiC BiDFET through clamped inductive load switching experiments to demonstrate its performance under different operating conditions.

II. Fabrication and Packaging

A. Fabrication

The BiDFET was fabricated at a 6-inch commercial foundry, X-FAB, TX, using the NCSU PRESiCE™ process [5], with 10 µm thick, 8 x 10^{15} cm^{-3} doped epitaxial layers grown on N^+ substrates. The internal JBSFETs in the device were each provided with two gate pads and multiple gate runners to minimize the gate signal propagation delay. The top-side image of the fabricated BiDFET is shown in Fig. 2(a).

B. Packaging

The BiDFET was encapsulated in a custom 4-terminal, 12-pin module made with flex PCBs. The power terminals T1 and T2 were provided with dual pins to allow parallel current paths. The gate terminals G1 and G2 were each provided with two pins placed near the gate pads and a dedicated kelvin pin to complete the gate loop. The module was encapsulated with epoxy resin. The internal wire-bonding and an image of the encapsulated module are shown in Fig. 2(b). The cross-section of the encapsulated module showing the constituent layers is shown in Fig. 2(c).

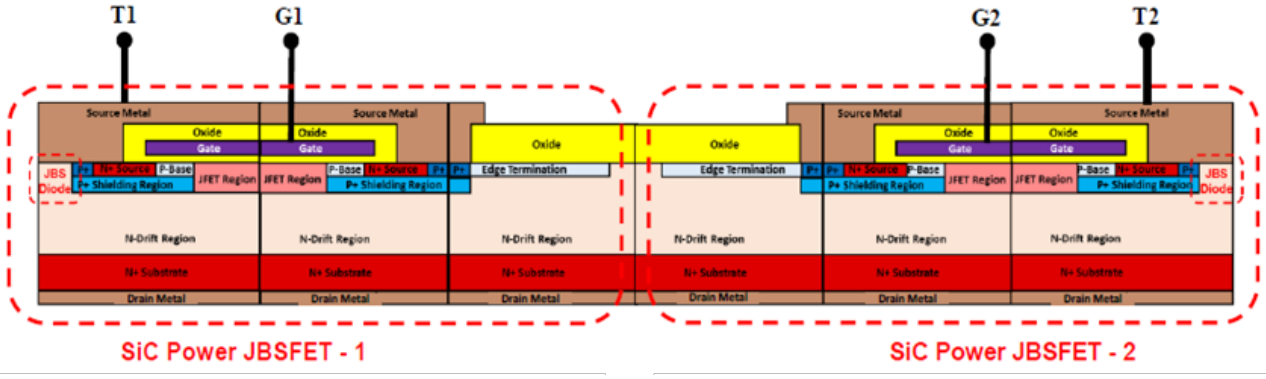

Fig. 1. Cross section of the monolithic 1.2 kV 4H-SiC BiDFET structure.

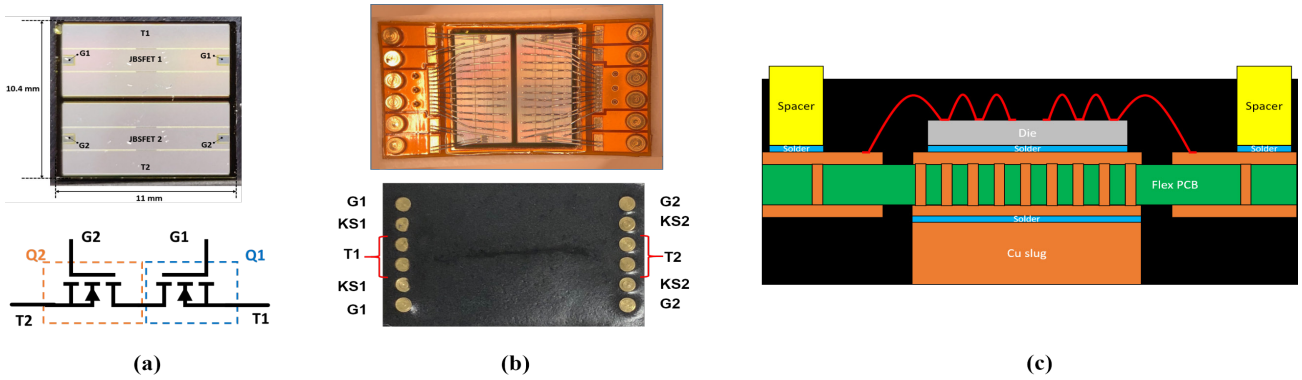

Fig. 2. (a) Image of a fabricated 1.2 kV SiC BiDFET device (top) and a schematic of its internal structure (bottom); (b) Top-View Image of the Flex PCB showing the internal wire-bonding (top) and the encapsulated module (bottom); and (c) Schematic of the encapsulated module showing its constituent layers.

III. Test Methodology

Static Characterization was conducted using a Keysight B1505A Curve Tracer. Measured parameters included on-resistance, transconductance and breakdown voltage.

Dynamic Characterization was conducted on a clamped inductive load switching circuit with a 150 µH solenoid inductor. The clamped inductive load switching setups used in this paper are shown in Fig. 3 and Fig. 4. The schematic in Fig. 3 shows a totem-pole with a SiC JBS diode D_1 in the high-side position and the device-under-test (DUT) as the switch in the low side position. An inductor is connected from the pole to the positive DC bus rail. The DUT is turned on using two successive -5/+20 V gate pulses. The first pulse is used to build up the desired current in the inductor and turn the DUT off. The second pulse is used to turn the DUT on at the desired current, which circulates between the inductor and JBS diode D_1 in the interval between the two pulses. This setup helps to evaluate the switching performance of a single transistor. The schematic in Fig. 4 shows a totem-pole with BiDFETs in both high-side and low side positions. The low-side BiDFET is used as the DUT, while the high-side BiDFET allows investigation of the BiDFET's body diode behavior. This configuration is similar to a half-bridge phase-leg, and the switching loss data obtained from this setup can be used to inform converter designs using the SiC BiDFET device.

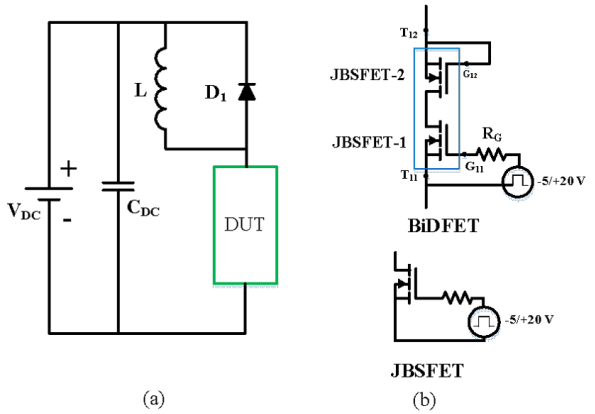

Fig. 3. (a) Schematic of the clamped inductive load switching test used to compare the switching performance of (b) the BiDFET and a single internal JBSFET.

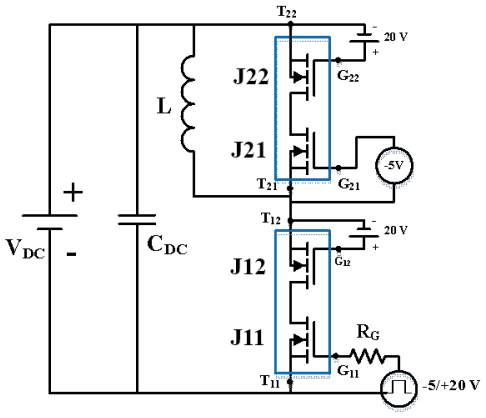

Fig. 4. Schematic of the clamped inductive load switching test used to evaluate the switching performance of the BiDFET in the phase leg configuration.

Experiments were conducted on BiDFET switches at different DC bus voltages, switching currents, gate resistances and case temperatures to infer various aspects of the BiDFET's dynamic performance. Experiment 1 compared the behavior of the BiDFET to that of its internal JBSFET at 400 V and 10 A. The internal JBSFET-1 was accessed by drawing out the common drain terminal through the Cu slug (see Fig. 2(c)) with a thick copper pin. Experiment 2 compared the switching performance of a BiDFET with G_{12} turned off to that when bias is applied to G_{12}. Experiment 3 measured the BiDFET switching losses across different current levels. Experiment 4 measured the BiDFET switching losses with increasing gate resistance. The impact of case temperature on the BiDFET switching losses was quantified in experiment 5.

IV. Experimental Results

A. Static Characteristics

The measured on-state characteristics of the BiDFET device for the first and third quadrant are shown in Fig. 5. The BiDFET had an on-resistance of 46 mΩ for a current of 10 A, at a gate bias of 20 V across G_1-T_1 and G_2-T_2 terminals. A DC bias of 20 V was maintained across G2-T2 for first quadrant measurements and across G1-T1 for third quadrant measurements. Turning–on the channels of both of the internal JBSFETs achieves a low forward voltage drop of about 0.5 V at 10 A in the first and third quadrants.

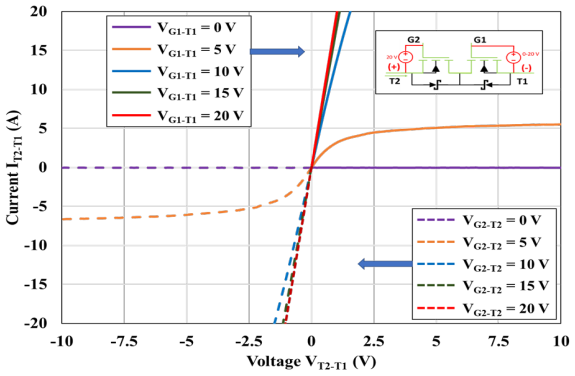

Fig. 5. Measured on-state characteristics for the 1.2 kV SiC BiDFET in the first and third quadrants.

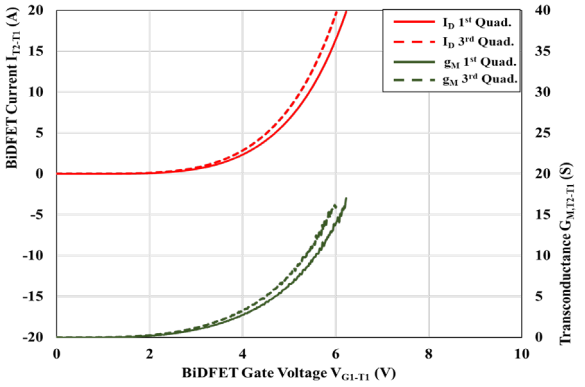

Fig. 6. Measured transfer characteristics for the 1.2 kV SiC BiDFET in the first and third quadrants.

The measured transfer characteristics for the BiDFET in the first and third quadrants, for a DC bias of 20 V across T_2-T_1 are shown in Fig. 6. For a current of 10 A, the BiDFET has a transconductance of about 9 S in both the first and third quadrants. The breakdown voltage of the BiDFET was greater than 1400 V in both the first and the third quadrants [6]. These results demonstrate that the BiDFET device exhibits symmetric characteristics in the first and third quadrants as desired for a bidirectional switch.

B. Dynamic Characterization

Five clamped inductive load switching experiments were conducted to observe the switching behavior of the BiDFET under different conditions. In each experiment, turn-on and

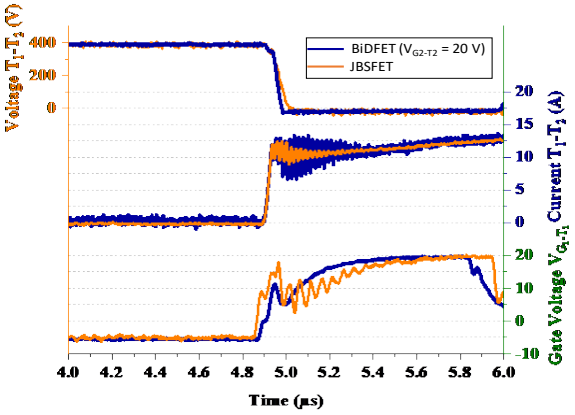

Fig. 7. Measured turn-on switching transition for the 1.2 kV SiC BiDFET and its internal JBSFET. V_{DC} = 400 V, I_D = 10 A and R_G = 10 Ω.

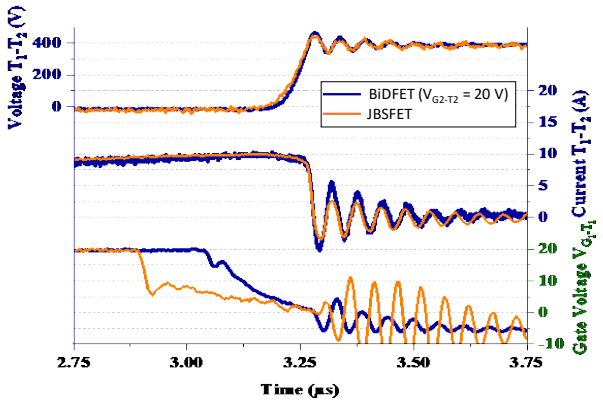

Fig. 8. Measured turn-off switching transition for the 1.2 kV SiC BiDFET and its internal JBSFET. V_{DC} = 400 V, I_D = 10 A and R_G = 10 Ω.

turn-off switching losses were calculated by integrating the voltage-current product across the duration of the transition.

Experiment 1: The setup shown in Fig. 3(a) was used with V_{DC} = 400 V, gate resistance R_G = 10 Ω, and the Wolfspeed 1.2 kV SiC JBS Diode C4D05120A as D_1. Switching tests were conducted at different current levels for the BiDFET with G_2-T_2 turned on (Case 1-1) and for one of its internal JBSFETs (Case 1-2) as DUTs. The measured turn-on and turn-off switching waveforms for experiment 1 are shown in Figs. 7 and 8. For a current of 10 A, the BiDFET had a turn-on loss E_{ON} of 149 µJ and a turn-off loss E_{OFF} of 109 µJ, resulting in a total switching loss $E_{SW,T}$ of 258 µJ. The internal JBSFET had an E_{ON} of 214 µJ and an E_{OFF} of 146 µJ, resulting in an $E_{SW,T}$ of 360 µJ. The measured switching loss values for

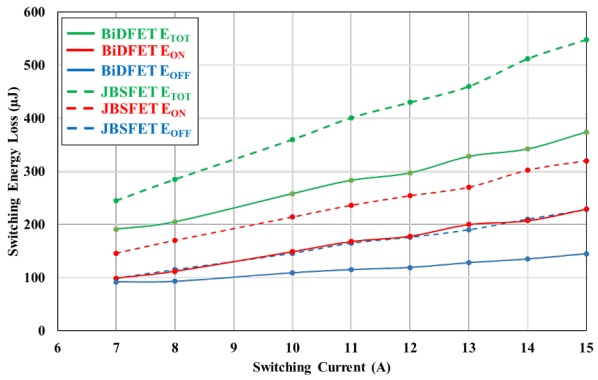

Fig. 9. Measured switching loss data at different currents for the 1.2 kV SiC BiDFET and its internal JBSFET. V_{DC} = 400 V.

TABLE I. SWITCHING TEST DATA FOR EXPERIMENT 1

I_{ON} (A)	(1-1) 1.2 kV BiDFET			(1-2) 1.2 kV JBSFET			$E_{SW,T}$ Norm. (2)/(1)
	E_{ON} (µJ)	E_{OFF} (µJ)	(1) $E_{SW,T}$ (µJ)	E_{ON} (µJ)	E_{OFF} (µJ)	(2) $E_{SW,T}$ (µJ)	
7	99	92	191	149	99	245	1.28
8	112	93	205	170	115	285	1.39
10	149	109	258	214	146	360	1.39
11	168	115	283	236	165	401	1.42
12	178	119	297	254	176	430	1.45
13	200	128	328	270	190	460	1.40
14	207	135	342	302	210	512	1.50
15	229	145	374	320	228	548	1.47

the two cases are plotted in Fig. 9 and are listed in Table I. These results show that the BiDFET device has lower switching losses compared to its internal JBSFET by a factor of 1.4x.

Experiment 2: The setup shown in Fig. 3(a) was used with the BiDFET as the DUT. Switching tests were conducted at V_{DC} = 800 V and a gate resistance of R_G = 1Ω with different currents. No bias was applied to terminal G_2 for Case 2-1 so that current flow occurred through the JBS diode in its JBSFET-1. A gate bias of 20 V was applied to G2 for Case 2-2 so that the current flowed through the channel of the JBSFET-1. The measured turn-on and turn-off switching waveforms for the BiDFET under Cases 2-1 and 2-2 for currents of 10 A and 20 A are shown in Figs. 10 and 11, respectively. The waveforms for Cases 2-1 and 2-2 for both

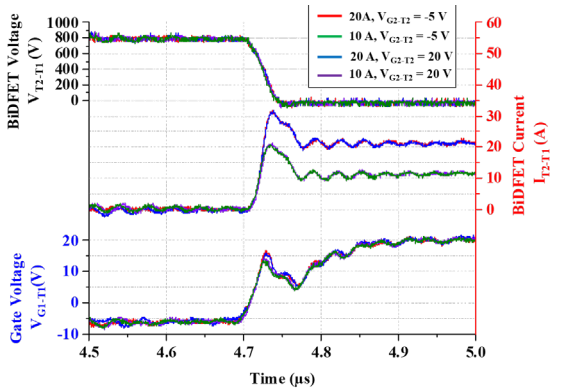

Fig. 10. Measured waveforms for the turn-on switching transient for the BiDFET Cases 2-1 and 2-2 at 10 A and 20 A. V_{DC} = 800 V, R_G = 1Ω

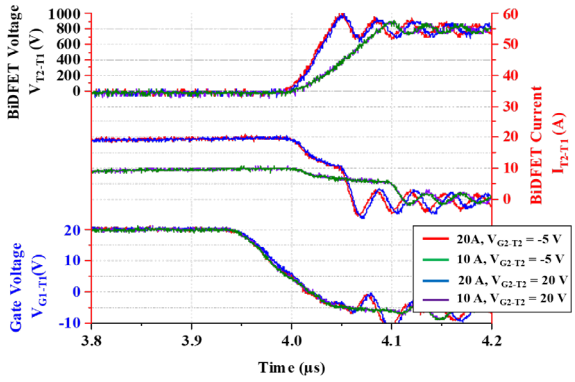

Fig. 11. Measured waveforms for the turn-on switching transient for the BiDFET Cases 2-1 and 2-2 at 10 A and 20 A. V_{DC} = 800 V, R_G = 1Ω

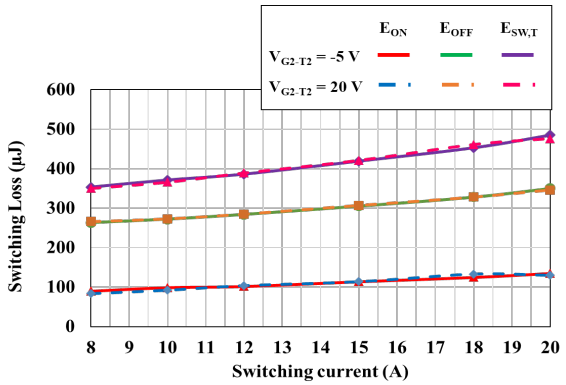

Fig. 12. Measured turn-on, turn-off and total switching losses for the BiDFET Cases 2-1 and 2-2. V_{DC} = 800 V, R_G = 1Ω.

10 A and 20 A overlap each other. For a current of 10 A, Case 2-1 had an E_{ON} of 99 µJ and an E_{OFF} of 272 µJ, resulting in an $E_{SW,T}$ of 371 µJ. Case 2-2 had an E_{ON} of 93 µJ, an E_{OFF} of 273 µJ and an $E_{SW,T}$ of 366 µJ. Similarly, at 20 A, Case 2-1 had an E_{ON} of 135 µJ, E_{OFF} of 350 µJ and an $E_{SW,T}$ of 485 µJ, while Case 2-2 had an E_{ON} of 130 µJ, E_{OFF} of 346 µJ and an $E_{SW,T}$ of 476 µJ. These results show that the switching performance of the BiDFET is not affected by the path taken by the current through its internal JBSFETs. The measured turn-on, turn-off and total switching losses for Cases 2-1 and 2-2 across different switching currents are plotted in Fig. 12. The measured values are summarized in Table II.

TABLE II. COMPARISON OF BIDFET SWITCHING DATA WITH G_2 ON AND WITH G_2 OFF

I_{ON} (A)	(2-1) V_{G2-T2} = -5 V			(1-2) V_{G2-T2} = 20 V			% Diff. (2) – (1)
	E_{ON} (µJ)	E_{OFF} (µJ)	(1) $E_{SW,T}$ (µJ)	E_{ON} (µJ)	E_{OFF} (µJ)	(2) $E_{SW,T}$ (µJ)	
8	90	263	353	84	266	350	-0.03
10	99	272	371	92.7	273	366	-0.05
12	102	284	386	104	25	389	0.03
15	114	305	419	114	307	421	0.02
18	125	328	453	133	328	461	0.08
20	135	350	485	130	346	476	-0.09

Experiment 3: The setup shown in Fig. 4 was used to measure the switching performance of the BiDFET in the phase-leg configuration. Switching tests were conducted at V_{DC} = 800 V and a gate resistance R_G = 10 Ω with different current levels. The measured switching waveforms for experiment 3 are shown in Fig. 13. The measured turn-on, turn-off and total

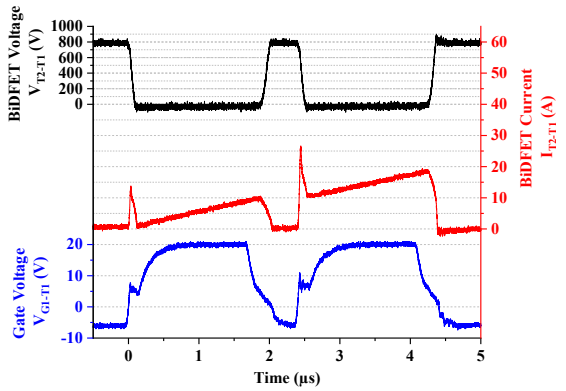

Fig. 13. Measured switching waveforms for experiment 3 with the phase-leg configuration shown in Fig. 4. V_{DC} = 800 V, I_D = 10 A, R_G = 10 Ω.

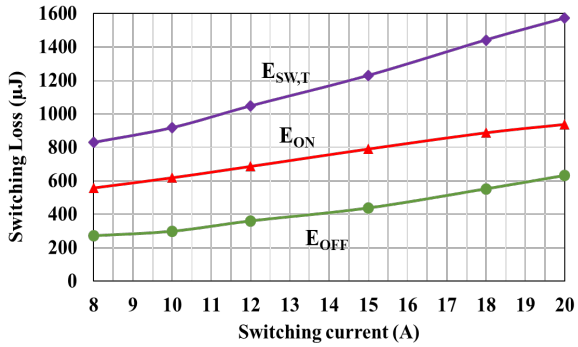

Fig. 14. Measured turn-on, turn-off and total switching losses for the BiDFET at different currents with V_{DS} = 800 V, R_G = 10 Ω.

TABLE III: SWITCHING TEST DATA FOR EXPERIMENT 3

Loss Parameters	Switching Currents $I_{T3\text{-}T1}$ (A)					
	8	*10*	*12*	*15*	*18*	*20*
E_{ON} (µJ)	559	620	688	792	889	939
E_{OFF} (µJ)	271	298	360	438	553	633
$E_{SW,T}$ (µJ)	830	918	1048	1230	1442	1572
$E_{SW,T}$ (Norm.)	0.9	1.0	1.14	1.34	1.57	1.71

switching loss at different currents are plotted in Fig. 14, and the values are summarized in Table III. These results show that the BiDFET exhibits an increase in total switching energy loss of 1.71x when the current increases from 10 A to 20 A.

Experiment 4: The setup shown in Fig. 4 was used to measure the switching performance of the BiDFET in the phase leg configuration. Switching tests were conducted at V_{DC} = 800 V and 10 A with different gate resistances. The measured turn-on and turn-off transitions for the BiDFET with gate resistances of 2Ω, 5Ω, 10Ω and 20Ω are shown in Figs. 15 and

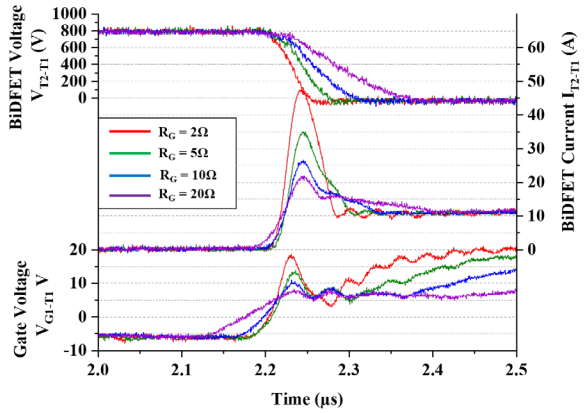

Fig. 15. Measured waveforms for the turn-on transition for the BiDFET with different gate resistances in Experiment 4. V_{DC} = 800 V, I_D = 10A.

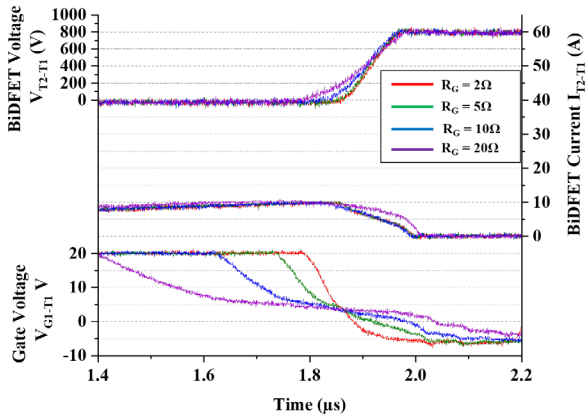

Fig. 16. Measured waveforms for the turn-off transient for the BiDFET with different gate resistances in Experiment 4. V_{DC} = 800 V, I_D = 10A.

TABLE IV: SWITCHING TEST DATA FOR EXPERIMENT 4

Switching Loss Parameters	Gate Resistance R_G (Ω)			
	2	*5*	*10*	*20*
E_{ON} (µJ)	313	456	620	964
E_{OFF} (µJ)	252	259	298	566
$E_{SW,T}$ (µJ)	565	715	918	1530
$E_{SW,T}$ (Norm.)	0.62	0.78	1.00	1.67

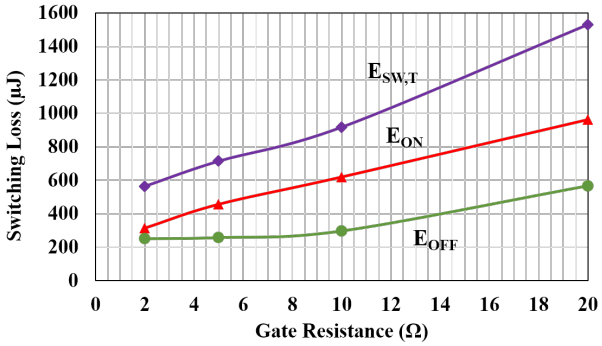

Fig. 17. Measured turn-on, turn-off and total switching losses for the BiDFET with different gate resistances in Experiment 4. V_{DS} = 800 V, I_D = 10 Ω.

16. The measured turn-on, turn-off and total switching loss values for Experiment 4 with the different resistances are plotted in Fig. 17 and summarized in Table IV. These results show that the total switching loss increases by a factor of 1.67x when the gate resistance doubles from 10 Ω to 20 Ω.

Experiment 5: The setup shown in Fig. 4 was used to measure the BiDFET switching performance in the phase-leg configuration with different case temperatures. Switching tests were conducted with V_{DC} = 800 V, I_D = 10 A and R_G = 10 Ω. The measured waveforms for the turn-on and turn-off transitions for the BiDFET are shown in Fig. 18 and 19. The measured switching losses for the BiDFET across different case temperatures are plotted in Fig. 20 and are listed in Table

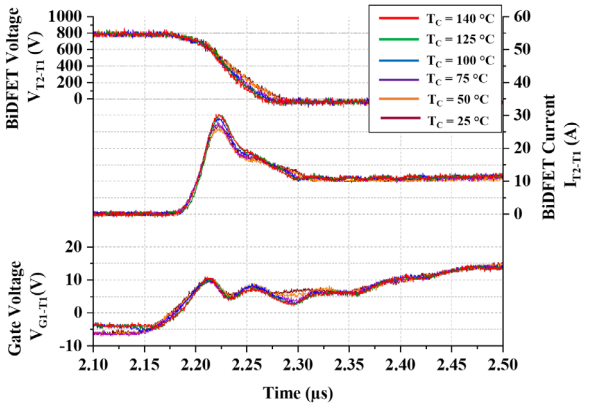

Fig. 18. Measured waveforms for the turn-on transition for the BiDFET with different case temperatures in Experiment 5. V_{DC} = 800 V, I_D = 10A, R_G = 10 Ω.

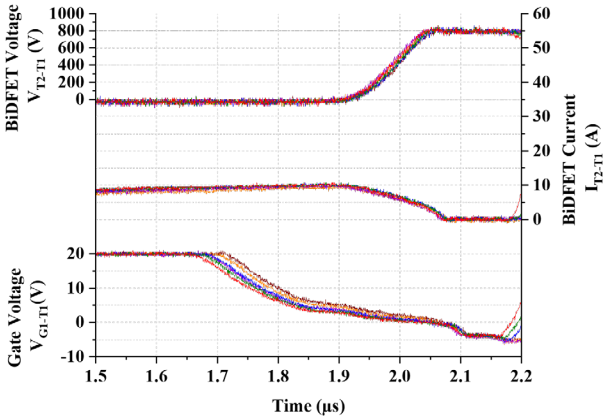

Fig. 19. Measured waveforms for the turn-off transition for the BiDFET with different case temperatures in Experiment 5. V_{DC} = 800 V, I_D = 10A, R_G = 10 Ω.

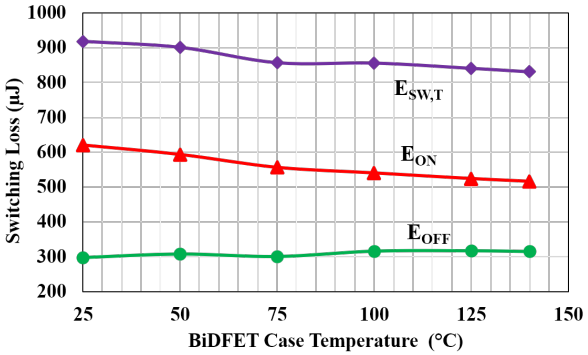

Fig. 20. Measured turn-on, turn-off and total switching losses for the BiDFET across different case temperatures. V_{DS} = 800 V, I_D = 10 Ω and R_G = 10 Ω.

V. These results show that as the case temperature of the BiDFET is increased from 25 °C to 140 °C, its total switching loss reduces to 0.83x – from 918 µJ to 831 µJ.

TABLE V: SWITCHING TEST DATA FOR EXPERIMENT 5

Loss Parameters	Case Temperatures (°C)					
	25	*50*	*75*	*100*	*125*	*140*
E_{ON} (µJ)	620	593	556	540	524	516
E_{OFF} (µJ)	298	308	301	316	317	315
$E_{SW,T}$ (µJ)	918	901	857	856	841	831
$E_{SW,T}$ (Norm.)	1	0.96	0.90	0.87	0.85	0.83

V. DISCUSSION

A. *Experiment 1: BiDFET vs internal JBSFET*

The device capacitances of the DUT influence its switching performance. The capacitances of the JBSFETs within the BiDFET are shown in Fig. 21(a). The relevant combination for determining the BiDFET output capacitance is shown in Fig. 21(b). The output capacitance of the BiDFET in its on-state is about half that of either of its internal devices [6] because the individual output capacitances of the JBSFETs combine in series. Consequently, the BiDFET achieves a better switching performance compared to a single internal JBSFET.

B. *Experiment 2: BiDFET Switching with G_2 On vs. G_2 Off*

The 1.2 kV SiC BiDFET is a bidirectional switch comprising of two internal JBSFET devices connected back-

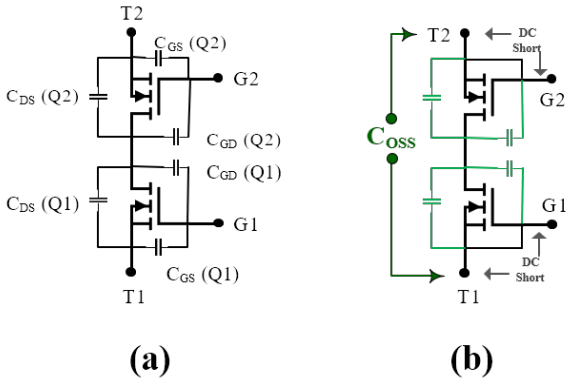

Fig. 21. (a) Device Capacitances internal to the BiDFET, and (b) the relevant combination for the BiDFET output capacitance.

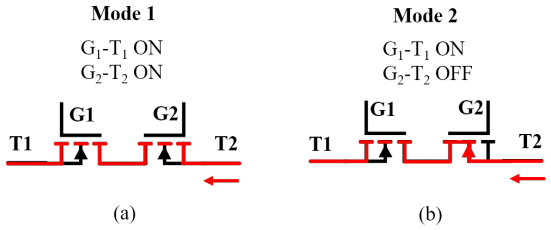

Fig. 22. BiDFET Schematic showing the current flow through its internal JBSFETs with (a) G_2-T_2 on, and (b) G_2-T_2 off.

to-back in a common-drain configuration. The BiDFET can be operated in two modes – 1) driving G_1-T_1 with G_2-T_2 On, and 2) driving G_1-T_1 with G_2-T_2 Off, as shown in Fig. 22.

The internal transistors in the BiDFET are equipped with JBS body diodes, which do not contribute large reverse recovery currents unlike the P-N body diodes in SiC MOSFETs. Furthermore, since the JBS body diode and the MOSFET share the drift region, the output capacitance appearing across the drain source terminals of the internal JBSFET-2 is approximately the same in both mode 1 and mode 2. Consequently, the observed switching behavior for the BiDFET with G_2-T_2 on is close to that with G_2-T_2 off.

C. *Experiments 3 and 4: Turn-on Current Overshoot*

The BiDFET exhibited a large spike during turn-on transitions, as seen at t = 0 and 2.4 µs in Fig. 10. The presence of the spike at t=0 despite the absence of current flow, and the similarity of the magnitudes of the spikes at 0 A and 10 A observed in Fig. 10 indicate that this could be a result of the output capacitance of the high-side BiDFET undergoing a large voltage transition during turn-off. The measured values of the current overshoot at turn-on, calculated as $I_{OVERSHOOT} = I_{ON,PEAK} - I_{ON}$, for the first and second pulses, along with the dV/dt value of the corresponding voltage transition are listed in Table V for the cases considered in Experiment 3 (V_{DS} = 800 V, various switching currents and R_G = 10 Ω). The capacitance producing the spike, calculated as the quotient $I_{OVERSHOOT}/(dV/dt)$.is also listed in Table VI. The capacitance and overshoot currents are plotted in Fig. 23. The capacitance producing the current spikes for the first pulse is around 1.5 nF. Since the high-side BiDFET is on up to the beginning of the gate pulse, its output capacitance typically large, consequently causing the current spike.

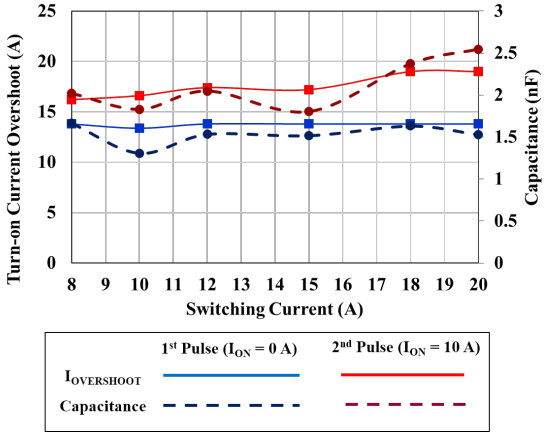

Fig. 23. Plot of turn-on current overshoot and the capacitance causing it at the beginning of the first and second pulses in Experiment 3.

TABLE VI: PEAK CURRENT OVERSHOOT ANALYSIS DATA FOR EXPERIMENT 3

Parameters	Switching Currents $I_{T3\text{-}T1}$ (A)					
	8	***10***	***12***	***15***	***18***	***20***
First Pulse (I_{ON} = 0 A)						
(1) $I_{OVERSHOOT}$ (A)	13.8	13.4	13.8	13.8	13.8	13.8
(2) dV/dt (kV/µs)	8.3	10.2	9.0	9.1	8.5	9.0
C = (1)/(2), nF	1.7	1.3	1.5	1.4	1.4	1.7
Second Pulse (I_{ON} = 10 A)						
(3) $I_{OVERSHOOT}$ (A)	16.2	16.6	17.4	17.2	19	19
(4) dV/dt (kV/µs)	8.0	9.1	8.5	9.5	8.0	7.5
C = (3)/(4), nF	2.0	1.8	2.0	1.8	2.4	2.5

D. Experiment 5: High-Temperature Switching Tests

The results in Table IV and Fig. 17 indicate that the turn-on loss E_{ON} of the low-side BiDFET decreases with increasing case temperature. This behavior is seen when a JBS diode is used as a freewheeling element across the inductor, such as the set-up shown in Fig. 3(a) [7]. The high-side device in Experiment 5, the BiDFET is operated with G_2-T_2 turned on, and G_1-T_1 turned off, essentially creating a JBS diode antiparallel to the inductor. The forward voltage of SiC JBS diodes increases with increasing temperatures [7], which increases its voltage drop, reducing its junction capacitance. The reduction in the junction capacitance results in a smaller current overshoot and a faster voltage transient during the turn-on transition for the low-side BiDFET, consequently reducing its switching loss.

VI. CONCLUSIONS

The 1.2 kV 4H-SiC Bi-Directional Field Effect Transistor (BiDFET) has been developed as a monolithic four-quadrant switch with integrated JBS diodes for use in AC-AC conversion applications. The devices exhibit symmetric on-state characteristics, transfer curves, and blocking voltages in the forward (1st quadrant) and reverse (3rd quadrant) directions. The BiDFET has an on-resistance of 46 mΩ which results in a low forward voltage drop of about 0.5 V at 10 A and 1.0 V at 20 A. Dynamic characterization of the BiDFET was performed under different operating conditions, including different DC bus voltages, various switching currents, multiple gate resistances and across a wide range of case temperatures. The results extracted through five clamped inductive load switching experiments indicated the following features:

- At a DC bus voltage of 400 V, The BiDFET has a better switching performance than its internal JBSFETs operating individually.
- Operating the BiDFET in mode 1 (G_1-T_1 On, G_2-T_2 On) or mode 2 (G_1-T_1 On, G_2-T_2 Off) produce similar switching losses.
- When operating in the phase-leg configuration, a current spike is observed at the turn-on transition of the low-side BiDFET due to the output capacitance of the high-side BiDFET.
- In the phase-leg configuration, the BiDFETs exhibit a decrease in turn-on switching loss values with increasing case temperature due to a reduction in device capacitance.

The BiDFETs can be used to develop AC-AC converter topologies with a small device footprint and high operating frequencies, leading to systems with high power density and compact form factor.

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