Optimized Highly Efficient SSCB Using Organic Substrate Packaging for Electric Vehicle Applications

Utkarsh Mehrotra, Bahji Ballard, Tzu-Hsuan Cheng, B. Jayant Baliga, Subhashish Bhattacharya, Douglas C. Hopkins
Electrical and Computer Engineering
North Carolina State University
Raleigh, North Carolina USA
E-mail: umehrot@ncsu.edu, dchopkins@ncsu.edu

***Abstract* - Solid State Circuit Breakers (SSCBs) are an attractive protection solution for their arcless current interruption and fast actuation speeds over mechanical breakers. This paper proposes a Bidirectional SSCB (BSSCB) with a thermally defined and digitally controlled current time profile for fault protection in EV and other low-voltage DC systems. The paper proposes an organic packaging approach utilizing flex circuitry to develop a reliable, cost-effective power module for BSSCBs. The paper studies transient heat transfer in the power modules using finite element analysis (FEA). An RC themal ladder network is extracted to define a fusing curve. To demonstrate and verify the design, a 1kV/50 A SiC MOSFET BSSCB prototype is fabricated and tested, having a power density of 60 W/cm^3 and 4x reduction in form factor over presently researched breakers. Also, given are results for 750 V/150 A operation showing interruption in 2.4 µs.**

Keywords— Solid-State switch, circuit breaker, dc distribution network, short circuit protection, bidirectional, electric vehicle, organic power packaging, digitally controlled fuse curve, common-drain topology, RC ladder networks

I. INTRODUCTION

DC distribution systems are on the rise in many applications including data centers, commercial buildings and electric vehicles (EVs) [1]. EV propulsion is showing substantial advancements due to Wide Band Gap (WBG) power semiconductors. Recent literature indicates voltages up to 800V for electric propulsion [2][3]. These high voltages combined with low system impedance [4] result in inherently high short circuit currents at high di/dt placing harsh design constraints on the protection systems.

Compared to AC breakers, which utilize the natural zero crossing in sinusoidal current, DC breakers are designed to always break full fault current and accompaning arc. Mechanical breakers are also rated with limited operations due to issues such as contactor bounce and wear [5].

Solid State Circuit Breakers (SSCBs) compared to mechanical breakers use a power semiconductor device to interrupt current with the absence of an arc. The SSCBs have faster actuation, longer life, and flexibility in programmability to fit multiple systems applications as needed in smart grid integration. The SSCB can be designed for soft start to limit inrush current, current limiting to manage system stress, and coordination with the battery management systems to dynamically manage master-slave schemes with mechanical and hybrid circuit breakers to reduce costs.

However, compared to mechanical breakers, the SSCB semiconductor devices have continuous on-state loss, which affects system efficiency. To minimize loss WBG technology, e.g. Silicon Carbide based devices, offers lower on-resistance for a given chip area at high voltage compared to Si and provides >200^{0}C capability [6]. These advantages along with faster switching possibilities make it suitable for breaker applications.

In [7], a 400 V/12.5 A SiC breaker is presented, with novelty in overvoltage minimization using gate control with a response of 0.5 ms. A 600 V/50 A breaker based on SiC JFETs is also reported in [8] and [9] in a common source topology with a response of 10 µs, but higher conduction loss limiting efficiency to 95%. A 1kV DC SSCB based on Si RB-IGCT technology is described in [10] has limitations due to thermal problems preventing scalability. Recently, a 1 kV/125 A bidirectional dc circuit breaker for Aerospace DC networks with a 2.5µs response and 98.4% efficiency at rated current was reported using SiC JFETs in [11], but the breaker uses TO-247 packaged devices limiting overcurrent to 2x nominal. Common to these cited breakers is performance limitations due to thermal limitations.

This paper defines a trip curve based on the thermal operating points of the power module and uses a mathematical model to predict the junction temperature in real time utilized in the controller. A model to predict junction temperature is key to ensure the SSCB is fail-safe and reliable [12].

A simplified model of an EV power system is shown in Fig. 1 [12], where V_S is nominal battery voltage, R_{INT} is internal battery pack resistance and R_L denotes the system load.

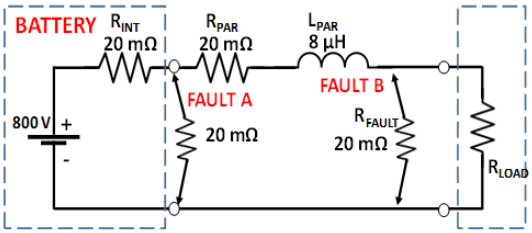

Fig 1: Typical EV power system

When FAULT A occurs and R_L is large, the continuous fault current reaches 20 kA with a near infinite di/dt. For FAULT B, the continuous current is only 13 kA with an initial di/dt at 100 A/µs (The time constant is 134 µs). Thus, depending on the position of the fault the current can ramp to tens of kiloamps

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within times limited only by internal cable inductance. Thus, the circuit breaker should:

1. protect the system in case of a gross overcurrent from the supply, short circuit on the output or an overload [13],
2. reliably interrupt fault current in microsecond response time, de-energize the line and completely isolate the system preventing cascading failures,
3. minimize power loss in bidirectional current flow, and
4. never fail.

II. System Design

Circuit breakers like electric fuses protect cabling and sources and are characterized by a trip curve or I^2t curve. The curve is a graphical representation of the operational behavior and plots a relationship of the maximum time duration a device can conduct at different current levels [14] before clearing the fault. Assuming constant fuse resistance, the time integral of I^2Rt ($\int(I^2Rt)dt$) calculates the thermal energy absorbed by the fuse actuation. For the SSCB, the curve represents the maximum thermal absorption boundary of the semiconductors, which are constrained by their Safe Operating Area (SOA). A typical circuit breaker trip curve is shown in Fig. 2. Unlike mechanical breakers, the curve has tight tolerances and can be reprogrammed to operate anywhere below the curve.

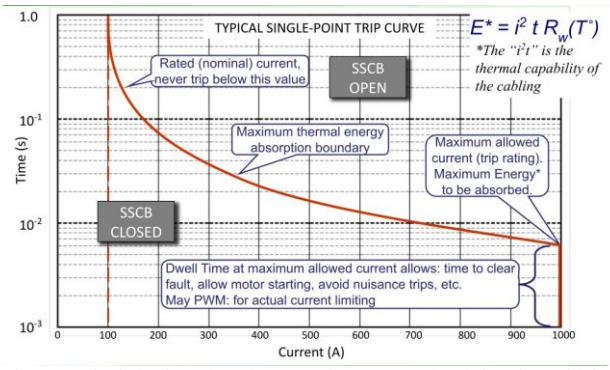


Fig 2: Typical single-point trip curve for a 100A circuit breaker which can operated to 10X rated current

A. Module Design

For an SSCB the semiconductor module should be designed with low thermal resistance, high thermal and mechanical reliability, small form factor, low-cost, and have high transient thermal absorption capability. To achieve the above organic laminate substrates, versus metal clad ceramics (e.g. DBC), and compatible packaging approaches are explored. Flex circuitry was selected, and material properties are listed in Table I.

Table I: Material properties of polyimide and Al_2O_3 substrate

	Flex (Polyimide)	Al_2O_3	Units
Thermal Conductivity	0.16	24	W/mK
T_g	300	-	^{0}C
Modulus	2.5	340	GPa
CTE	14-17	4.5-7	ppm/^{0}C
Dielectric Strength	5/120 µm	20/mm	kV

The low modulus of polyimide greatly reduces the transfer of mechanical stress onto the power die for higher reliability. In addition, an organic packaging approach reduces the module cost by 40% compared to traditional AlN. To compensate for the low thermal conductivity of polyimide, thermal via's are added to provide a direct heat conduction path. The custom developed SSCB power module utilizes 100 µm thick substrate, shown in Fig. 3. Two CREE SiC MOSFETs CPM2-1200-0025B are co-placed on a center copper pad as shown in Fig 3 (b) and wire bonded to interconnect with the power/driving terminals as shown in Fig 3(c). Then a Cu heat spreader is placed at the bottom of the package to enhance heat spreading and provide transient thermal absorption. Finally, the module is molded with a high thermally conductive epoxy from RISHO to improve thermal performance and provide a mechanical housing further reducing cost and weight. Its attractive properties include breakdown dielectric strength of 15 kV/mm and thermal conductivity of 1.9 W/mK. The final encapsulated power module is shown in Fig 3(d). The over all power module measures 24.5 mm*14.5 mm* 2 mm and has 12 terminals, which can be flipped and soldered onto the PCB for simpler power stage integration.

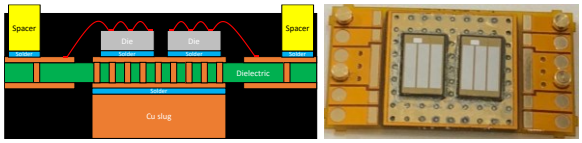
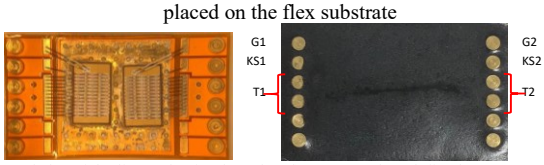


Fig 3:(a) Packaging layer stack for the fabricated module (b) CREE die placed on the flex substrate



(c) module with die and wire bonds (d) encapsulated final power module

Multiphysics tools are utilized to predict the thermal performance and extract the stray electrical parasitics from the power module. COMSOL results show that the $R_{thj\text{-}c}$ = 0.655 ^{0}C/W and Ansys Q3D results show that the power path stray resistance and inductance is 3.54 mΩ and 10.2 nH respectively.

The step-by-step power module fabrication along with package characterization results can be found in [15,16] along with exploration into a new highly thermally conductive Epoxy Resin Composite Dielectric (ERCD), which can further improve the performance of the switch and the SSCB.

B. Electrical Design

A simplified model to show the position of the breaker in an EV power system is shown in Fig. 4.

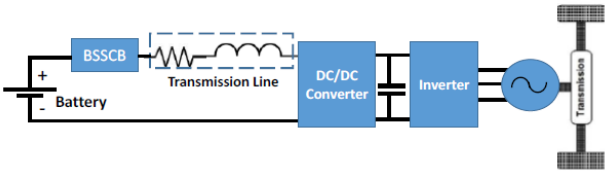


Fig 4: Block diagram of an EV power system

The block diagram shows the position of the BSSCB and should support bidirectional protection for both charging and discharging of EV battery pack. A SiC MOSFET is selected as the power devices for the BSSCB and are placed in a back to back common drain connection as shown in Fig. 5.

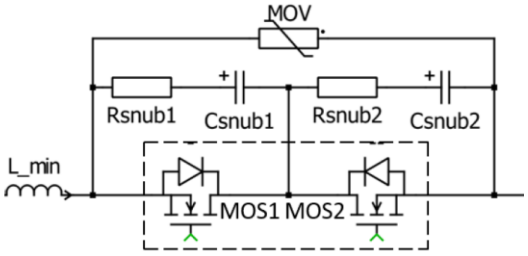


Fig 5: Power stage schematic of the SSCB

The common drain topology enables simple and compact power module designs and provides a plausible way of tapping into the center point (device drain) to connect snubbers. The common drain connection also enables through hole thermal via's for direct thermal conduction to ambient, which supports higher thermal energy absorption and a wider trip curve. A possible disadvantage is that the "electrically hot" heat sink isolation problem is transferred to the next level of packaging. A novel monolithic device called the **B**i-**D**irectional **F**ield **E**ffect **T**ransistor (BiDFET) integrates two JBSFETs [17] and may further enhance the thermal and electrical performance.

The BSCCB is composed of functional 'Layers'. When the device (i.e. semiconductor module) layer receives an actuation signal from a sense & control layer to interrupt the peak allowed fault current, the module opens and commutates current to the snubber layer. The snubber shapes the di/dt to limit overshoot voltage from the cable inductance (Fig. 1). As the snubber capacitor fills, the current commutates to the MOV clamping the overshoot voltage seen by the module, Fig 5.

As discussed, FAULT A as shown in Fig 1 would produce an infinite di/di. Hence, to guarantee the BSSCB can detect and respond to the "fastest fault," a current limiting inductance, L_{min} is added into the BSSCB as shown in Fig. 5, which also limits the peak current. The L_{min} dictates the timing requirement of current sensing mechanics, the computation time of the microcontroller and the gate drive actuation circuitry. The faster the controller acts the lower the L_{min} value needed.

Table II: Overall system specification of the EV BSSCB

Specification	***Design***
Rated Voltage and Current	1 kV/50 A with 3 X trip (150A)
Power	50 kW with 150 kW peak
Efficiency	99.7 % @ rated current @25^{0}C
Line Inductance	6 µH
Power Density	60 W/cm^2
Minimum Inductance	0.5 µH
Device Selection	**CPM2-1200-0025B**
Rated V_{ds} & I_d	1200 V/71 A
$R_{DS(ON)}$	25 mΩ @ 25^{0}C
Snubber Design	
Snubber Capacitance	850 nF
Snubber Resistance	4.8 Ω
MOV	**MOV-14D751K**
Clamping Voltage	1200 V
Nominal Voltage	850 V

To calculate component values for the example application discussed in this paper, a 7.6 m (25 ft) Cu cable is assumed with inductance of 6µH. Design guidelines in [18]-[20] are used to complete the snubber and MOVs sizing calculations, respectively. The resulting system specification of the EV BSCCB is given in Table II. The snubbers and MOV are sized to de-energize the system and clamp the voltage to 1200 V protecting the semiconductor devices.

C. Controller Design

A PSoC® 5LP: CY8C58LP was selected as the microcontroller and the scheme shown in Fig 6 was software coded for digital control in TI Code Composer Studio (CCS). The scheme has two modes of operation for fast and slow tracking. Fast tracking detects a threshold value for trip, whereas slow uses the thermal model described in Section III. A temperature sensor provides ambient temperature calibration.

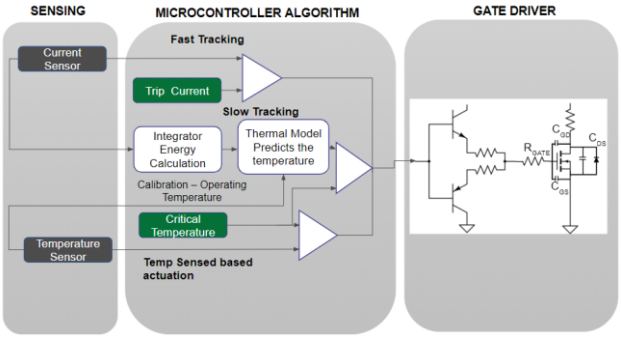


Fig 6: Controller overview of the BSSCB

The fault detection system detects a fault level by sensing voltage across a high bandwidth (~20 MHz) resistive sensor and signals the microprocessor to select and activate a protection scheme, finally triggering the gate drive circuits. A unique low-cost, low overshoot resistive sensor was developed for this application as described in [21].

III. THERMAL DESIGN AND DEFINING SSCB TRIP CURVE

Traditionally the short circuit capability of a solid-state device is calculated in terms of the specific heat and device volume. However, the combination of high thermal conductivity of SiC and wafer thinning the power module substrates can now play a more significant role in thermal absorption during short circuit [22].

Two thermal network topologies using electrical analogies are commonly used to represent the thermal impedance along the heat-flow path in a power module, namely Cauer and Foster method. Both use Rs and Cs to represent a time response of temperature. In the Cauer network, a resistor-capacitor (RC) T-network represents the thermal characteristics based on the physical material layers along a 1D heat flow path, and each node represents the temperature at a physical location in the module. Whereas the Foster model has no physical detail and

depicts the time constant present in the total network making it easier to represent mathematically [23].

In this section, an RC Cauer model is developed for a custom power module design and then converted into an RC Foster model to develop a mathematical model to be utilized in the control scheme of the breaker shown in Fig 6. The RC Foster model helps model the rate of rise of temperature along with calculating the maximum junction temperature for any timed current pulse.

For a Cauer model, the value of each resistance and capacitance is related to the geometry and material properties of each layer per the following equations:

$$R_{th} = \frac{d}{\lambda A} \quad (1)$$

$$C_{th} = c\rho dA \quad (2)$$

Where, λ (W/mK) is thermal conductivity of the material, ρ (kg/m^3) is material density, Cp (J/kg K) is specific heat, A (mm^2) is cross-sectional area to heat flow, and d (mm) is the thickness of the layer. A limitation of this model is that it assumes 1D heat flow, which does not account for thermal spreading. This can be compensated for by adjusting area, 'A' based on a spreading angle, e.g. 45^0. More accurate determination of spreading angle is discussed in [24]. The final capacitance and resistance values are presented in Table III.

Table III: Material Properties of the module layers to calculate RC Cauer model

	λ W/m K	ρ kg/m^3	c J/kg . K	d mm	A mm^2	R_{th}	C_{th}
Chip	380	3200	1200	0.18	28.02	0.016	0.019
Solder	50	9000	150	0.03	29.92	0.020	0.001
Cu	398	8700	385	0.04	30.60	0.003	0.004
Substrate	30	4452	526	0.12	42.36	0.094	0.012
Cu	398	8700	385	0.04	31.97	0.003	0.004
Solder	50	9000	150	0.05	32.43	0.031	0.002
Cu spreader	398	8700	385	0.9	33.02	0.068	0.031

The RC Cauer model is then converted to the Foster model by using the Joy and Schlig method described in [25] and the MATLAB curve fitting toolbox. Table IV shows the RC values to form the Foster and Cauer RC ladder networks.

Table IV: Foster and Cauer RC models

	Cauer Cap	Cauer Res	Foster Cap	Foster Res
Chip	0.0193	0.0169	0.4500	0.0474
Solder	0.0012	0.0200	0.2255	0.0222
Top Cu	0.0041	0.0032	0.1275	0.0210
Substrate (Flex)	0.0119	0.0944	0.1427	0.0676
Bottom Cu	0.0043	0.0031	0.2550	0.0046
Solder	0.0021	0.0308	0.2132	0.0340
Cu spreader	0.0308	0.0685	0.1518	0.0400

Using the Foster RC ladder model, the time dependent impedance is represented mathematically as the sum of exponential terms:

$$Z(t) = \sum_{i=1}^{K} R_{thi}\left(1 - e^{-\frac{t}{R_{thi}C_{thi}}}\right) \quad (3)$$

where K is the number of stages in the ladder. The junction temperature, T_j, for the module is:

$$T_j(t) = P(T_j) * \sum_{i=1}^{7} R_{thi}\left(1 - e^{-\frac{t}{R_{thi}C_{thi}}}\right) + T_{case} \quad (4)$$

where T_{case} is the case temperature of the module and $P(T_j)$ is the power dissipation of the device (joule heating) during the turn-on process and can be represented as:

$$P(T_j) = I_{DS}^2 R_{on}(T_j) \quad (5)$$

where R_{on} (T_j) is the MOSFET on-resistance as a function of temperature; the relationship can be obtained from device datasheets. Equations (3)-(5) are used in conjunction with the integration of the power dissipation to approximate junction temperature in real time by the controller.

Both the models were then compared through simulations in PLECS. Results are shown in Fig. 7. The Foster RC model predicts the junction temperature variations under differing overcurrent conditions within PLECS. The rate of rise of temperature at different current levels from 1x to 3x of rated current in 0.4x current intervals is shown in Fig 8.

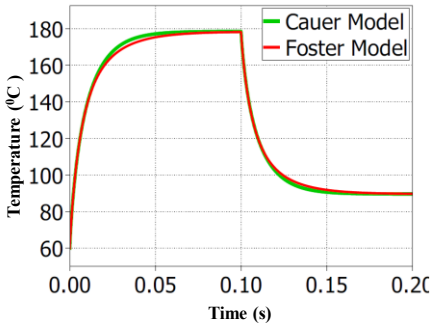


Fig 7: PLECS simulations to verify the accuracy of the foster model

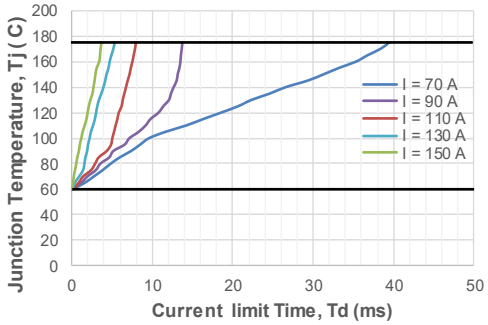


Fig 8: Junction temperature of the device at different current level using the RC foster network

Time taken for the device to heat to 175^{0}C from 60^{0}C ambient is shown in Table V.

Table V: Time to reach T_j=175^{0}C from T_a=60^{0}C for differing currents

Current	Time taken to reach 175^{0}C at junction
70 (1.4x)	39.5 ms
90 (1.8x)	13.8 ms
110 (2.2x)	7.96 ms
130 (2.6x)	5.28 ms
150 (3x)	3.73 ms

Hence, for the same initial conditions, the larger the fault current, the faster the T_j increases. From the datapoints in Table V, the I-t trip profile of the BSSCB is shown by the black line in Fig 11.

A. Multiphysics Model Validation

To verify the computational accuracy of the RC ladder network, an FEA was employed. A 3D model was created and imported into COMSOL with material properties from Table I and shown in Fig. 9.

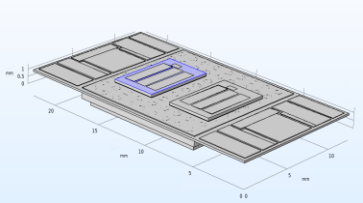


Fig 9: 3D rendering of the BSSCB in COMSOL

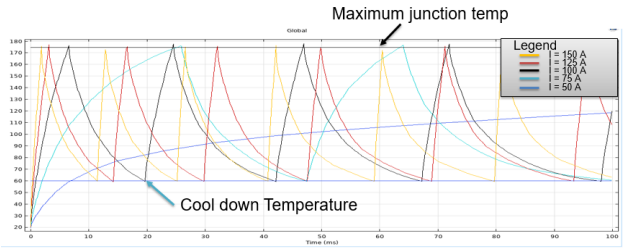


Fig 10: COMSOL results

A heat source equivalent to $I^2R_{DS(ON)}$ is applied to the top of the die for 50A to 150A in 20A steps. A heat transfer coefficient, h, of 50W/m^{2}K with T_a=60^{0}C is applied to the bottom of the Cu spreader replicating forced air convection. The results are shown in Fig 10. The times to reach T_j=175^{0}C and cool to ambient (60^{0}C) for the different currents were used to plot the I^2t curve in Fig 11.

The figure shows that the RC model is within a 10% the FEA COMSOL results and supports use of a 45^0 average spreading angle approximation to mathematically model transient heat transfer. This margin of error can be justified as the RC ladder approach does not model the exact spatial and temporal pattern of input power. The model can be further extended to include the RC network of a designated heat sink. The approach also effectively predicts any device temperature for an ultra-thin package as described in this paper.

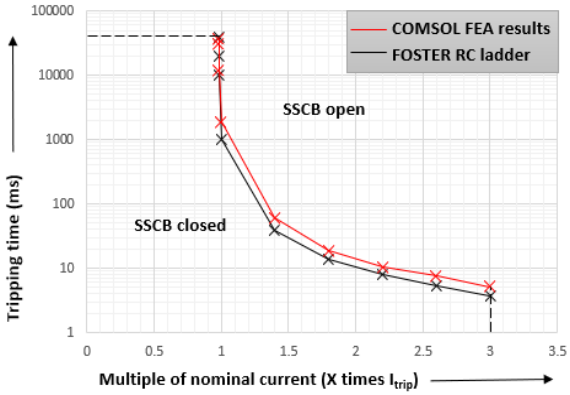


Fig 11: Trip Curve of the SSCB

IV. Experimental Testing

To demonstrate fast interruption performance, the device was tested at 750V/150A. The test circuit is shown in Fig 12(a). The BSSCB current was slowly ramped to go beyond 150A mimicking a fault. The result is shown in Fig 12(b).

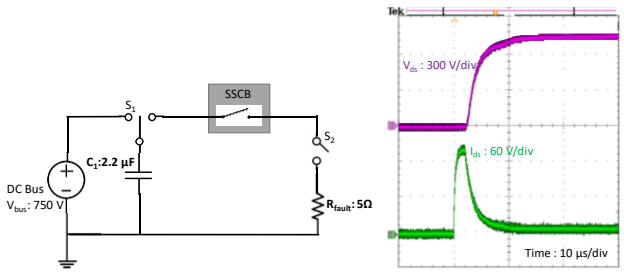


Fig 12 (a) : Test circuit (b) Empirical validation of fast interruption.

It was observed that it takes 0.8µs for the current sensor to respond to the input, 1.4 µs to signal the gate drive and 0.2 µs delay in the driving circuitry and switch opening. Overall the entire system takes 2.4 µs to respond.

Conclusion

The paper presents an 800V/50 A breaker for Electric Vehicle applications. An electrical topology for bidirectional protection using back to back devices in a common drain topology is discussed showing performance benefits. A cost-effective polyimide based module optimized for low thermal and electrical resistance was developed and validated with COMSOL and Q3D simulations. Transient thermal heat transfer was studied for the organic package to design the fusing curve of the breaker. An RC ladder model was developed to approximate FEA results, and used to predict the junction temperature of the semiconductors without a thermal sensor. A

two stage control scheme was discussed ensuring that the device is always operated in safe operating area. The package was fabricated and tested at a 750V and 150 A continuous current to demonstrate the fast overcurrent interruption. Experimental results demonstrated an interruption time of 2.4 µs which is a 1000X improvement over mechanical legacy breakers. This is the fastest solid state circuit breaker reported thus far in the literature.

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