

1.2 kV, 10 A, 4H-SiC Bi-Directional Field Effect Transistor (BiDFET) with Low On-State Voltage Drop

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Abstract. Bidirectional power switches are used in matrix- or cyclo-converters and in multistage inverter circuits to facilitate high-frequency AC-to-AC conversion. A new 1.2 kV bidirectional MOSFET (BiDFET) with low on-resistance is achieved using two discrete SiC power MOSFET bare die chips, packaged within a four-terminal custom-designed module. Static and dynamic characterization has been carried out to inspect the on-state and switching behaviour of the switch. The BiDFET is shown to have a low forward voltage drop of 0.6 V at a current of 10 A, which is more than 2.5x smaller than previous Si IGBT and SiC MOSFET based bidirectional switch implementations.

Introduction

Bidirectional power switches are used in matrix or cycloconverters and multistage inverter circuits to facilitate high-frequency AC-to-AC conversion [1]. These topologies enable power conversion without intermediate energy storage elements like DC-link capacitors, thus reducing the system volume and enabling higher operating temperatures, increased power density, and improved output waveform quality [2].

The performance of a matrix- or cyclo-converter is determined by the choice of switch implementation. A lack of commercial high-performance switches has hindered the development of these topologies [1]. Prior implementations of bidirectional switches have employed various combinations of discrete power transistors and diodes, as shown in Fig. 1. The switch in Fig. 1(a) employs 4 power diodes in a bridge configuration enclosing an asymmetric-blocking IGBT [1]. This implementation has a forward voltage equal to the sum of the forward voltage drop of the IGBT and that of two diodes. The IGBT also contributes to switching losses and limits the maximum operating frequency of the converter. The switch in Fig. 1(b) uses two asymmetric Si IGBTs – each with a freewheeling diode – series-connected at the emitter [2]. This implementation has a forward voltage drop equal to the sum of the forward voltage drop of the IGBT and that of one freewheeling diode. The asymmetric IGBT contributes to switching losses and limits the maximum operating frequency. The switch in Fig. 1(c) employs back-to-back reverse blocking symmetric Si IGBTs [3]. This implementation has a lower forward voltage drop than Figs 1(a) and (b), but has higher switching losses due to the symmetric IGBT structure [4]. The trade-off curves in Fig. 5 of [3] show that for an on-state voltage from 2.2 V, the turn-off switching energy loss is 3 mJ/cm² for a unidirectional NPT structure versus 14 mJ/cm² for the RB structure, an increase by a factor of nearly 5-times. Fig. 1(d) shows a four-device implementation using two series, source-connected silicon carbide (SiC) power MOSFETs – each with a freewheeling SiC Junction-Barrier Schottky (JBS) diode [5]. Fig. 1(e) shows a six-device implementation using two back-to-back SiC power MOSFETs with series and antiparallel SiC JBS diodes [6]. The use of SiC devices reduces the forward voltage drop and the switching losses for these implementations. The bi-directional switch in Fig. 1(e) was implemented using two antiparallel SiC Reverse-Blocking MOSFETs [7]. The 3.3kV reverse-blocking MOSFET implementation in [7] has many manufacturing challenges: a 350 μ m thick substrate was removed leaving behind a 40 μ m drift layer, which is difficult to perform. This process will be much more difficult for 1.2 kV devices with only 10 μ m thick drift layers. The edge termination region for the

RB 3.3 kV SiC MOSFETs was achieved on the bottom side with precise alignment with the top-side device structure. Such double-sided photolithographic alignment is not available in most manufacturing facilities because of their complexity. Furthermore, the Schottky contact on the back-side used to achieve reverse blocking capability has a high leakage current as observed in Fig. 7 of [7]. In addition, the Schottky contact in the RB-MOSFET based switch adds a knee voltage of at least 1 V in the on-state making its total on-state voltage drop at least 1.5 V.

A novel Bi-Directional Field Effect Transistor (BiDFET) was proposed as a monolithic switch built using 4H-SiC power JBSFETs to achieve a low forward voltage drop, fast switching device in a single package footprint [6]. Experimental implementation of a 1.2 kV monolithic device was demonstrated with an on-resistance of 500 m Ω [8]. This paper demonstrates a two-chip implementation for the BiDFET using series, drain-connected SiC power MOSFETs, shown in Fig. 1(f), within a single custom 4-terminal package. This switch option has been implemented using commercially available 1.2 kV SiC power MOSFET chips with on-resistance of 25-34 m Ω . The paper discusses the on-state characterization and dynamic behavior of this BiDFET, followed by presenting a trade-off between on-state voltage drop and switching loss for the different options mentioned above.

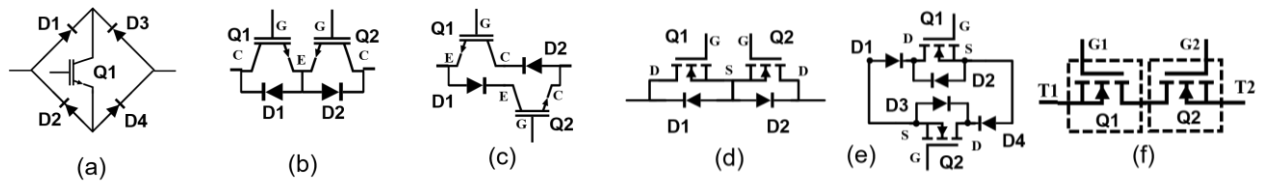


Fig. 1. Bi-directional switch implementations (a) Diode bridge with asymmetric blocking IGBT, (b) Series emitter-connected asymmetric blocking IGBTs with freewheeling diodes, (c) Back-to-back reverse blocking IGBTs, (d) Series source-connected SiC power MOSFETs, (e) Back-to-back SiC power MOSFETs with series reverse blocking diodes, (f) four-terminal SiC BiDFET demonstrated in this paper.

Devices and Experiments

The SiC BiDFET was implemented using commercially available Wolfspeed 1.2 kV SiC power MOSFET (CPM2-1200-0025B) bare die [9]. Two devices were co-located in a custom designed four-terminal package. Fig. 2 shows the cross section and the layer stack used in the BiDFET package with pertinent dimensions. Fig. 3 shows (a) the wire-bonding scheme, (b) the encapsulated view of the module, and (c) a device schematic. The devices are mounted on a flex-PCB (green layer in Fig. 2) to minimize bulk with spacers to create surface-mount terminals. A copper slug connected to bottom pad allows heat sink attachment to remove power dissipated in the chips.

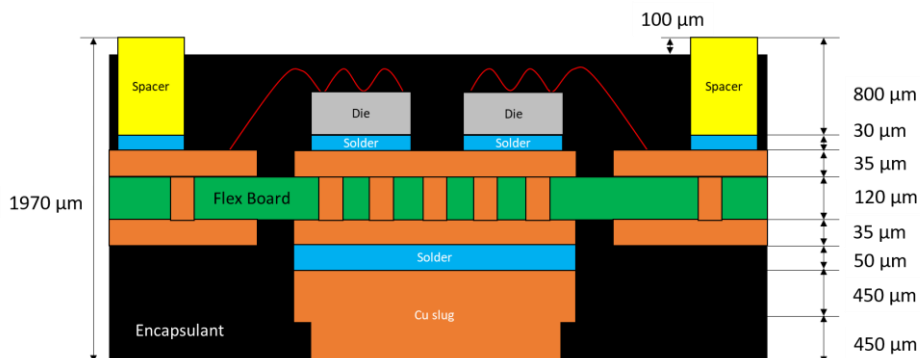


Fig. 2. Packaging layer stack for the fabricated BiDFET module.

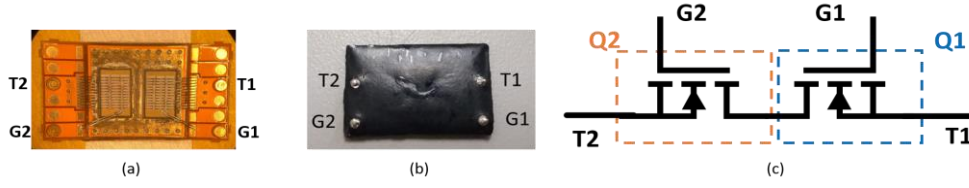


Fig. 3. Discrete 4-terminal BiDFET module: (a) un-encapsulated module showing MOSFET die and wire bonds, (b) encapsulated package; and (c) device schematic.

Experimental Results

Static characterization was conducted using a Keysight B1505A Curve Tracer. The measured parameters include on-resistance, forward voltage drop, threshold voltage, blocking voltage, transconductance, and capacitances.

Static Characteristics: Symmetrical blocking capability is a fundamental property of any bidirectional blocking device. The measured blocking characteristics for the BiDFET are shown in Fig. 4. The device has equal blocking voltage capability in the first and third quadrant as desired. The breakdown voltage was measured at the industry standard leakage current of 100 μA . The breakdown voltage of the 1.2 kV rated SiC BiDFET was observed to exceed 1700 V in the first (blue curve) and third (orange curve) quadrants. The use of commercial bare die of the same design ensures symmetrical blocking performance.

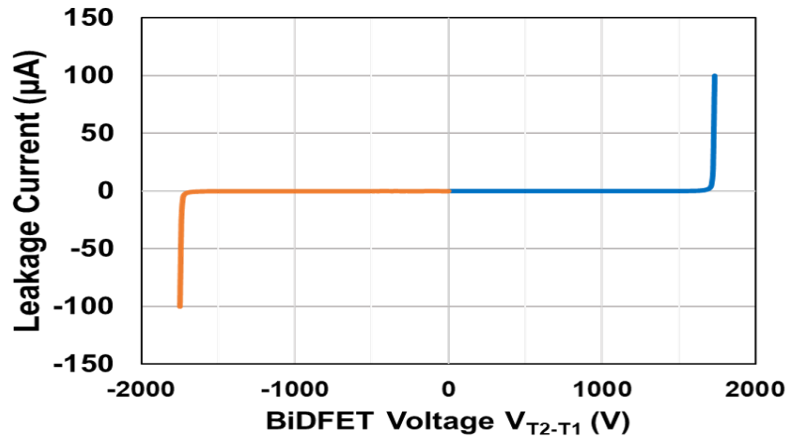


Fig. 4. Measured forward (blue curve) and reverse (orange curve) blocking characteristics.

On state-current flow in the BiDFET can be achieved in two modes in the first and third quadrants, based up on the gate control voltages applied to each internal MOSFET. Mode 1 involves controlling Q1 by applying a gate-voltage across G1-T1, while G2-T2 is shorted, in the first quadrant, and controlling Q2 by applying a gate-voltage across G2-T2, while G1-T1 is shorted, in the third quadrant. This maintains current flow through the channel of Q1 and the body diode of Q2 in the forward direction and through the channel of Q2 and the body diode of Q1 in the reverse direction. Mode 2 involves controlling Q1 by applying a gate-voltage across G1-T1, while maintaining a constant +20 V bias across G2-T2 in the first quadrant, and controlling Q2 by applying a gate-voltage across G2-T2, while maintaining a constant +20 V bias across G1-T1 in the third quadrant.

The measured output characteristics for the SiC BiDFET operated in Mode 1 are shown in Fig. 5. The internal current flow path is highlighted in red in the schematic adjacent to the graph. Current flow through the body diode of Q2 in the first quadrant and through the body diode of Q1 in the third quadrant produces in a knee voltage of about 2 V in both directions.

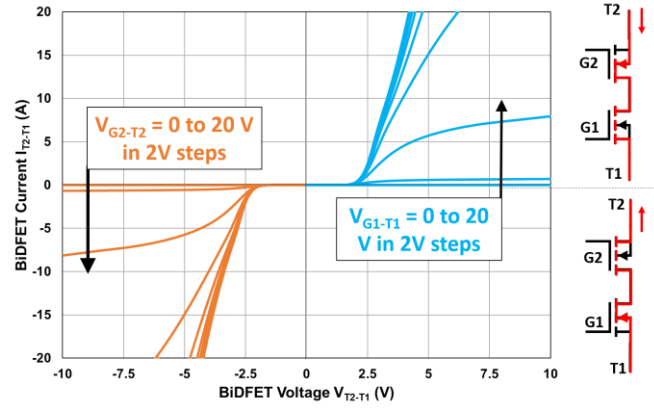


Fig. 5. Measured output characteristics for the BiDFET module operating in Mode 1 – with zero gate bias across G2-T2 in the first quadrant and zero gate bias across G1-T1 in the third quadrant.

The measured output characteristics for the SiC BiDFET operated in Mode 2 are shown in Fig. 6. The internal current flow path is highlighted in the schematic adjacent to the graph. The application of +20 V bias across G2-T2 in the first quadrant and across G1-T1 in the third quadrant forces current flow through the channel of both MOSFETs, eliminating the knee voltage. The on-resistance of the BiDFET, measured at a current of 10 A for a gate bias of 20 V, is found to be 59.4 mΩ in both the first quadrant and the third quadrant. Under these operating conditions, the forward voltage of the BiDFET is ~0.6 V.

The measured threshold voltage of the BiDFET is seen to be 2.2 V in the forward and 2.24 V in the reverse direction. The measured transfer curves for the BiDFET in the first and third quadrant are plotted in Fig. 7 on the left-hand side. The device transconductance, measured as the derivative of the transfer curve, is plotted on the right hand side in Fig. 7. It is seen that the device transconductance for a current of 10 A is about 9.3 S in the first quadrant and 9.1 S in the third quadrant. As expected, the use of two similar MOSFET die within the BiDFET ensures symmetric transfer characteristics and equal transconductance in both first and third quadrants.

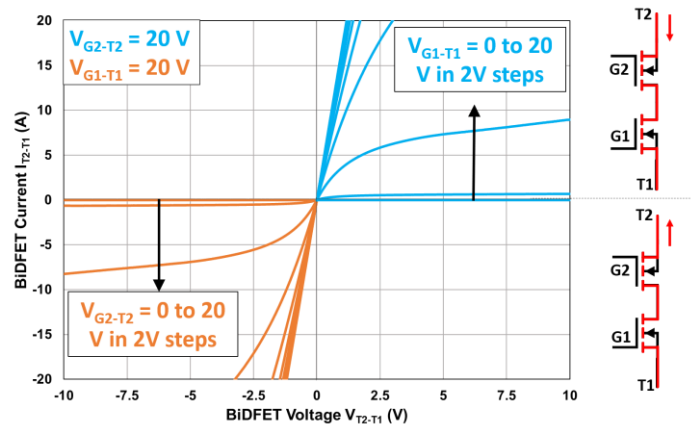


Fig. 6. Measured output characteristics for the BiDFET module operating in Mode 2 - with a +20 V gate bias across G2-T2 in the first quadrant and across G1-T1 in the third quadrant

The measured capacitance curves for the BiDFET are shown in Fig. 8. The capacitance tests were conducted as per standard test configurations using the Keysight B1505A Curve tracer. It is seen that the BiDFET capacitances are nearly identical in the first and third quadrants, as expected. The use of two similar MOSFET die within the BiDFET ensures symmetric capacitance characteristics in both first and third quadrants.

The static characterization data is summarized in Table I, along with datasheet values of the parameters for a single internal SiC power MOSFET chip. The values are compared in the discussion section. The values for measured device capacitance are discussed in the next section.

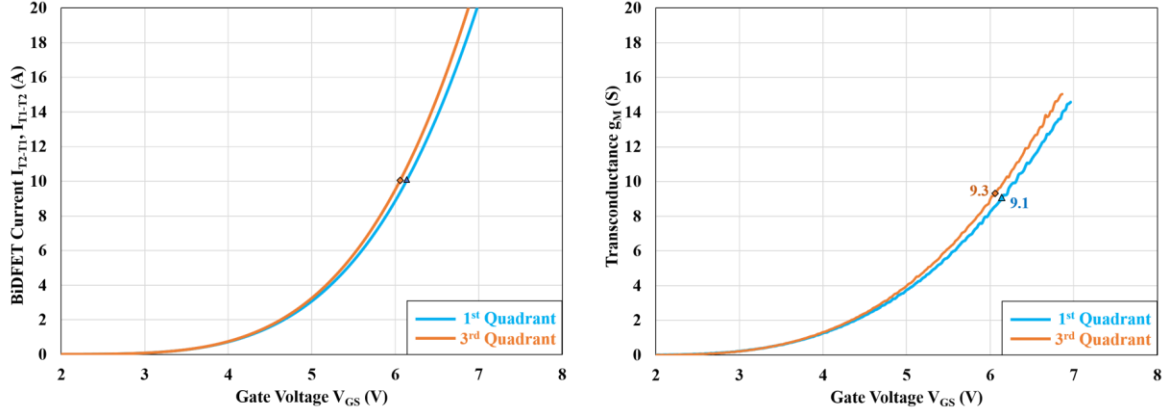


Fig. 7. Measured transfer characteristics and transconductance curves for the BiDFET in the first and third quadrants. A DC bias of 20V was provided across T2-T1 in the first quadrant and across T1-T2 in the third quadrant.

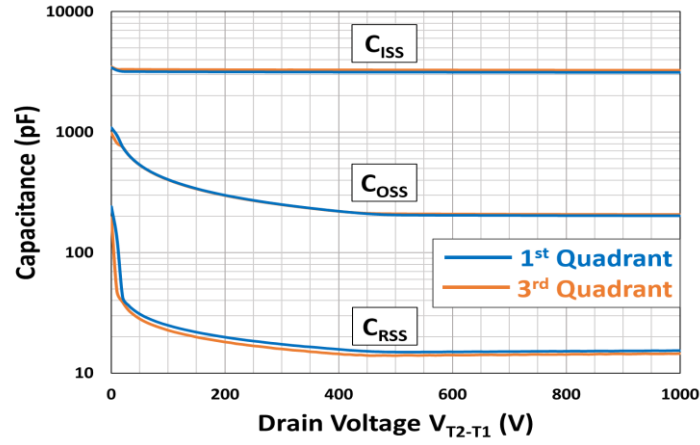


Fig. 8. Measured device capacitances for the 1.2 kV SiC BiDFET in the first and third quadrants.

TABLE I: BIDIRECTIONAL STATIC CHARACTERIZATION DATA FOR THE 1.2 kV SiC BiDFET

Parameter, Units (Conditions)	Forward Measurement (1 st Quadrant)	Reverse Measurement (3 rd Quadrant)	CREE CPM2-1200-0025B
$R_{DS,ON}$, m Ω , ($I_{T2-T1} = \pm 10A$, $V_{G1-T1} = V_{G2-T2} = 20V$)	59.4	59.4	25-34
Blocking Voltage, BV _{T2-T1} , V, ($I_{T2-T1} = 100\mu A$)	1731	1750	>1200
Threshold Voltage V_{TH} , V, ($V_{T2-T1} = \pm 0.1V$, $I_{T2-T1} = \pm 1 mA$)	2.2	2.24	2-4
Transconductance, g_m , ($V_{T2-T1} = \pm 20V$, $I_{T2-T1} = 10A$)	9.3	9.1	NA*

*Parameter tested under different test conditions

Preliminary Dynamic Characteristics: Switching tests were conducted to estimate the dynamic performance of the 1.2 kV SiC BiDFET, using a clamped inductive load switching setup assembled with the CREE KIT8020-CRD MOSFET Evaluation Kit, for a DC bus voltage of 800 V, switching current of 10 A, and a -5/+20 V gate drive with a gate resistance of 2.5 Ohm. A 350 μH solenoid inductor was used as the load. The schematic for the switching test circuit is shown in Fig. 9. The switching waveforms are shown in Fig. 10. The waveforms exhibit ringing due to parasitic inductances arising from the leads connecting the module to the board. The switching energies were

calculated by integrating the product of the current and voltage across the switching transient. The BiDFET has a turn-off switching loss of 1.12 mJ and a turn-on switching loss of 251 μ J, resulting in a total switching loss of 1370 μ J.

Additional switching tests were conducted with different gate resistances up to 35 Ω , keeping other parameters the same as for the gate resistance of 2.5 Ω . The plot of switching loss variation with gate resistance is shown in Fig. 11. The switching losses increase with R_G as expected. As discussed previously, some bidirectional switch implementations have used asymmetric IGBTs. The switching energy losses for a typical asymmetric commercial IGBT 1.2kV IXYS IXGH20N120A3 [10], scaled down from its datasheet values for gate resistances of 10 to 35 Ω , are also plotted in Fig. 11 for comparison. The total switching loss of the BiDFET is around 2.8x smaller than that for the IGBT, demonstrating its superior switching performance compared to IGBT based bidirectional switch implementations.

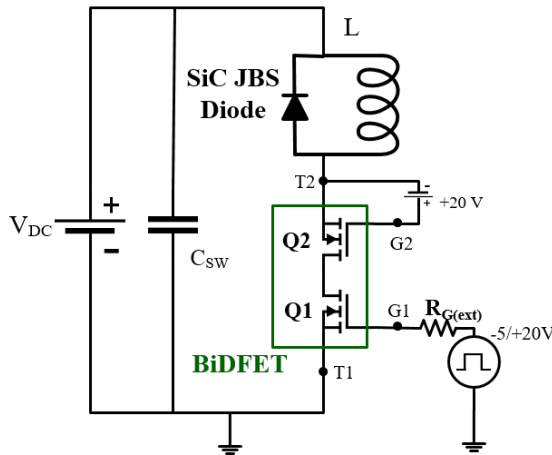


Fig. 9. Schematic for the Clamped Inductive Load Switching Circuit.

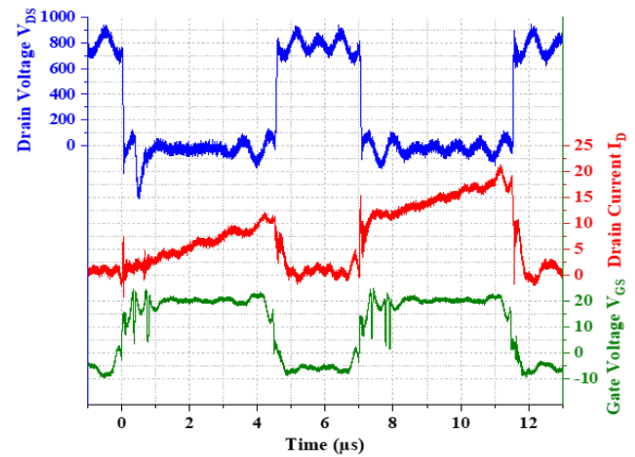


Fig. 10. Waveforms for the BiDFET switching tests with $V_{DS} = 800V$, $I_D = 10A$ and $R_G = 2.5 \Omega$.

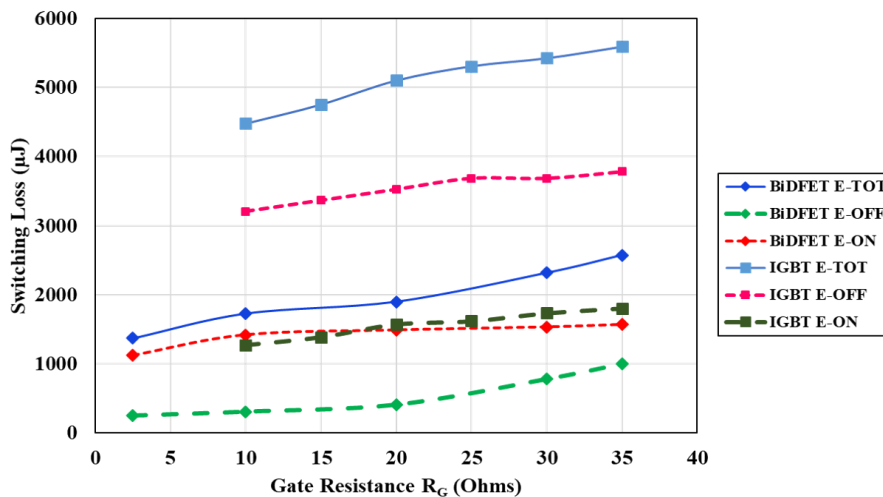


Fig. 11. Turn-off Switching Energy Loss Variation with Gate Resistance

Discussion

On-Voltage. The 1.2 kV SiC BiDFET module can be operated in two modes, as described in the previous section. Mode-2, i.e., applying a gate drive to one gate while maintaining a +20 V bias across the other gate, ensures current conduction through the channel of both internal transistors, hence achieving a low on-state resistance (R_{ON}) of 59.4 m Ω .

For the BiDFET module demonstrated above, an on-voltage drop of 0.6 V was observed at a current of 10 A. In contrast, other implementations using Si IGBTs and SiC MOSFETs, as shown in Fig. 1, exhibit a higher V_{ON} at a similar current level. A comparison of on-voltage drop and internal device count for different bidirectional switch implementations is provided in Table II. This comparison assumes a forward voltage of 1 V for the Si diodes, 1.5 V for the Asymmetric Si IGBT, 2.0 V for the Symmetric Si IGBT, and 0.25 V for the SiC power MOSFETs [8]. It is seen that Si IGBT-based implementations have a V_{ON} of at least 2 V, whereas the SiC MOSFET based implementations prior to this work achieve a minimum V_{ON} of 1.25 V. Thus, the BiDFET switch demonstrated in this paper achieves a *2.1x reduction* in on-state voltage drop compared to previous SiC bidirectional implementations while achieving a *4-6x reduction* in number of packages.

TABLE II - COMPARISON OF BIDIRECTIONAL POWER SWITCH IMPLEMENTATIONS

Bidirectional Switch Option		Device Count per switch	On-State Voltage Drop, V_{ON} (V)
1)	Diode-bridge with asymmetric IGBT [1]	5	3.5
2)	Series emitter-connected asymmetric IGBTs with flyback diodes	4	2.5
3)	Back-to-back reverse blocking IGBTs	2	2.0
4)	Series source-connected SiC power MOSFETs	4	1.25
5)	Back-to-back SiC powers MOSFETs with series reverse blocking diodes	6	1.25
6)	Four-terminal SiC BiDFET (this work)	1	0.6

Static Characteristics. The BiDFET consists of two devices connected at the drain and co-packaged in a four-terminal module. To minimize the forward voltage across the switch during normal operation, each BiDFET is operated by applying a gate drive to one internal transistor, while maintaining a +20 V gate bias across the other. Under this operating condition, it can be expected that the on-resistance of the switch is sum of the on-resistance of the individual internal transistors. The datasheet of the C2M0025120D bare-die shows the on-resistance of a single SiC MOSFET to lie between 25 and 34 m Ω as given in Table I. The BiDFET on-resistance of 59.4 m Ω is within twice this value in both forward and reverse directions as expected.

Capacitance Tests. The capacitance of the BiDFET is a combination of the device capacitances of the internal transistors. The input, output, and reverse transfer capacitances for the two internal MOSFETs are shown in Fig. 12(a). The measurement methods to evaluate the input, output, and reverse transfer capacitance for the BiDFET as a single switch, are shown in Figs. 12 (b), (c) and (d). The BiDFET exhibits similar capacitance profiles for the first and third quadrant. Hence, the capacitance analysis will be discussed only for the first quadrant, i.e, with a short across G2-T2 for all three capacitance tests. Capacitance behavior in the third quadrant can be expected to be identical.

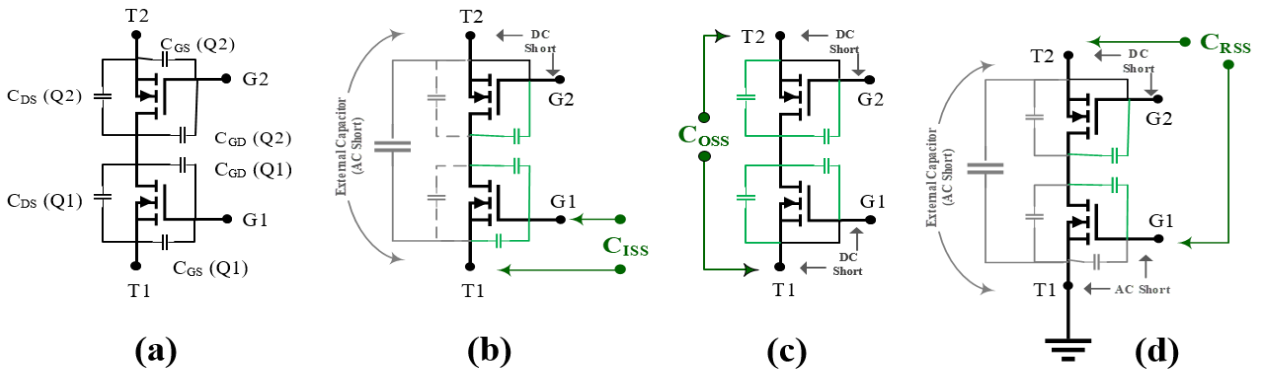


Fig. 12. Device capacitances in the BiDFET showing (a) Internal device capacitances (b) BiDFET input capacitance (c) BiDFET output capacitance, and (d) BiDFET reverse transfer capacitance

The input capacitance is measured by applying a 25 mV, 100 kHz AC signal, across the G1-T1 terminals. In the standard test procedure, the large external capacitor connected across T2-T1 effectively shorts the drain-source capacitances during this test. Following the schematic in Fig. 12(b), the input capacitance for the BiDFET can be expressed as

$$C_{ISS}(\text{BiDFET}) = C_{GS}(Q1) + \frac{C_{GD}(Q1) \times C_{GD}(Q2)}{C_{GD}(Q1) + C_{GD}(Q2)}. \quad (1a)$$

For a high DC bias of 1000 V across T2-T1, Q1 is reverse biased while Q2 is forward biased. The value for $C_{GD}(Q2)$ is consequently very large. Datasheet plots for device capacitance of the internal SiC MOSFET [9] shows a C_{GD} of 1000 pF for low (< 1 V) drain voltages. Substituting these values for the terms in (1a), C_{ISS} (BiDFET, 1 kV) can be computed as

$$C_{ISS}(\text{BiDFET}, 1 \text{ kV}) = 2773 \text{ pF} + \frac{15 \text{ pF} \times 1000 \text{ pF}}{15 \text{ pF} + 1000 \text{ pF}} = 2788 \text{ pF} \approx C_{ISS}(Q1, 1 \text{ kV}). \quad (1b)$$

For a low DC bias of 5V across T2-T1, Q1 is lightly reverse biased, while Q2 is forward biased. In this case, the values for $C_{GD}(Q1)$ and $C_{GD}(Q2)$ are both large. Substituting the datasheet values for the terms in (1a), C_{ISS} (BiDFET, 5V) can be computed as

$$C_{ISS}(\text{BiDFET}, 5 \text{ V}) = 3500 \text{ pF} + \frac{900 \text{ pF} \times 1000 \text{ pF}}{900 \text{ pF} + 1000 \text{ pF}} = 3973 \text{ pF} \approx C_{ISS}(Q1, 5 \text{ V}). \quad (1c)$$

The measured values for $C_{ISS}(\text{BiDFET})$, shown in Table III, are comparable to these numbers, as expected.

Output capacitance is measured by applying a 25 mV, 100 kHz AC signal, across the T2-T1 terminals, with an external short across G1-T1 and G2-T2. Following the schematic in Fig. 12(c), the output capacitance for the BiDFET can be expressed as

$$C_{OSS}(\text{BiDFET}) = \frac{C_{DS}(Q1) \times C_{DS}(Q2)}{C_{DS}(Q1) + C_{DS}(Q2)} + \frac{C_{GD}(Q1) \times C_{GD}(Q2)}{C_{GD}(Q1) + C_{GD}(Q2)}. \quad (2a)$$

For a high DC bias of 1000V across T2-T1, Q1 is reverse biased while Q2 is forward biased. The values for $C_{DS}(Q2)$ and $C_{GD}(Q2)$ are consequently very large. Substituting datasheet values for the terms in (2a), C_{OSS} (BiDFET, 1000 V) can be computed as

$$C_{OSS}(\text{BiDFET}, 1 \text{ kV}) = \frac{200 \text{ pF} \times 2000 \text{ pF}}{200 \text{ pF} + 2000 \text{ pF}} + \frac{15 \text{ pF} \times 1000 \text{ pF}}{15 \text{ pF} + 1000 \text{ pF}} = 198 \text{ pF} \approx C_{OSS}(Q1, 1 \text{ kV}). \quad (2b)$$

For a low DC bias of 5V across T2-T1, Q1 is lightly reverse biased while Q2 is forward biased. In this case, the values for all the capacitances are large. Substituting the datasheet values for the terms in (2a), C_{OSS} (BiDFET, 5V) can be computed as

$$C_{OSS}(\text{BiDFET}, 5 \text{ V}) = \frac{2000 \text{ pF} \times 2000 \text{ pF}}{2000 \text{ pF} + 2000 \text{ pF}} + \frac{500 \text{ pF} \times 1000 \text{ pF}}{500 \text{ pF} + 1000 \text{ pF}} = 1333 \text{ pF} \approx 0.5 \times C_{OSS}(Q1, 5 \text{ V}). \quad (2c)$$

The measured values for C_{OSS} (BiDFET), shown in Table III, are consistent with these numbers.

Reverse transfer capacitance is measured by applying a 25 mV, 100 kHz AC signal across the G1-T2 terminals. The T1 terminal is grounded, effectively resulting in an AC short across the G1-T1 and T2-T1 terminals. Following the schematic in Fig. 12(d), the reverse transfer capacitance for the BiDFET can be expressed as

$$C_{RSS}(\text{BiDFET}) = \frac{C_{GD}(Q1) \times C_{GD}(Q2)}{C_{GD}(Q1) + C_{GD}(Q2)}. \quad (3a)$$

For a high DC bias of 1000 V across T2-T1, Q1 is reverse biased while Q2 is forward biased. The value for $C_{GD}(Q2)$ is consequently very large. Substituting datasheet values for the terms in (3a), C_{RSS} (BiDFET, 1 kV) can be computed as

$$C_{RSS}(\text{BiDFET}, 1 \text{ kV}) = \frac{15\text{pF} \times 1000\text{pF}}{15\text{pF} + 1000\text{pF}} = 15 \text{ pF} \approx C_{RSS}(Q1, 1 \text{ kV}). \quad (3b)$$

For a low DC bias of 5V across T2-T1, Q1 is lightly reverse biased while Q2 is forward biased. In this case, the values for $C_{GD}(Q1)$ and $C_{GD}(Q2)$ are both large. Substituting datasheet values for the terms in (3a), C_{RSS} (BiDFET, 5 V) can be computed as

$$C_{RSS}(\text{BiDFET}, 5 \text{ V}) = \frac{500\text{pF} \times 1000\text{pF}}{500\text{pF} + 1000\text{pF}} = 333 \text{ pF} \approx \frac{1}{2} C_{RSS}(Q1, 5 \text{ V}). \quad (3c)$$

The calculated reverse transfer capacitance of the BiDFET is almost half that of one internal SiC MOSFET. From the values shown in Table III, the measured reverse transfer capacitance of the BiDFET at lower drain bias voltages is $\sim 4\times$ smaller than the datasheet numbers for one internal SiC MOSFET. This is beneficial in the high-frequency applications because it reduces the drain voltage turn-on and turn-off transit times, reducing switching loss.

TABLE III - MEASURED AND CALCULATED DEVICE CAPACITANCE

Parameter, Units (Condition)	BiDFET (1 st Quadrant)	BiDFET (3 rd Quadrant)	Calculated BiDFET Capacitance	CREE C2M0025120D (Datasheet)
Input Capacitance, C_{ISS} , pF ($V_{T2-T1} = 1000 \text{ V}$)	3138	3255	2788	2788
Input Capacitance, C_{ISS} , pF ($V_{T2-T1} = 5 \text{ V}$)	3341	3410	3973	3500
Output Capacitance, C_{OSS} , pF ($V_{T2-T1} = 1000 \text{ V}$)	202	208	198	220
Output Capacitance, C_{OSS} , pF ($V_{T2-T1} = 5 \text{ V}$)	1012	894	1333	2000
Reverse Transfer Capacitance, pF ($V_{T2-T1} = 1000 \text{ V}$)	15.4	14.5	15	15
Reverse Transfer Capacitance, pF ($V_{T2-T1} = 5 \text{ V}$)	186	121	333	600

Switching Performance. The turn-on and turn-off switching losses (E_{ON}) and $E_{(OFF)}$ for the individual SiC power MOSFETs is reported in the datasheet to be 1.4 and 0.3 mJ for $V_{DS} = 800\text{V}$, $I_D = 50\text{A}$ and $R_G = 2.5 \Omega$ [9]. The total switching loss for the single SiC MOSFET is then 0.34 mJ when scaled to $I_D = 10\text{A}$. This is much smaller than the value obtained for the BiDFET in our preliminary switching tests. Improvements in the switching test set-up to reduce ringing noise are expected to result in smaller power losses for the BiDFET that match the individual MOSFETs.

The switching losses for a typical 1.2 kV Asymmetric Si IGBT (IXYS Product IXGA20N120A3) can be obtained from its datasheet as plotted in Fig. 11. These devices have turn-on and turn-off switching losses (E_{ON}) and $E_{(OFF)}$ of 1.27 and 3.21 mJ for $V_{DS} = 800\text{V}$, $I_D = 10\text{A}$ and $R_G = 10 \Omega$. The total switching power loss for the Si IGBT (E_{SW}) is then 4.48 mJ. This value is $2.6\times$ larger than the measured value of 1.7 mJ for the BiDFET at $R_G = 10 \Omega$ in our preliminary tests. This indicates that the BiDFET has much superior switching losses than the implementations using Si asymmetric

IGBTs. The switching losses for the implementations with Si symmetric IGBTs will be much worse [4].

The proposed BiDFET is a four-terminal device. The static and dynamic characterization experiments were conducted on test setups made for three terminal devices. Consequently, the BiDFET was connected to the three terminal fixtures using wire leads for our preliminary tests. This introduces parasitic inductance leading to ringing during turn-on and turn-off transitions. The ringing extends the duration of the current and voltage transitions, producing additional losses. The proposed device will be evaluated for switching losses on a custom test setup with four-terminal mounting in the future to extract accurate switching performance data.

Conclusions

A Bi-Directional Field Effect Transistor (BiDFET) switch has been demonstrated using two commercially available 1.2 kV SiC power MOSFET bare die devices for the first time. It was shown that the BiDFET operated with a level-shifted gate bias on one of its gate terminals can achieve a low on-state voltage drop of 0.6 V at 10A. Static characterization was conducted on the BiDFET to measure the blocking voltage, on-resistance from the output I-V curves, threshold voltage, transfer characteristics and device capacitance. The BiDFET showed the desired symmetric behavior across first and third quadrants, with blocking voltage exceeding 1.7 kV in both directions. The proposed BiDFET was demonstrated to have the lowest on-state voltage drop, of 0.6 V for a current of 10 A, at least 2.5x smaller than prior implementations involving Si IGBTs and SiC power MOSFETs. Switching tests were conducted to obtain a preliminary estimate of switching performance. The switching losses were substantially smaller than expected for implementations using Si asymmetric IGBTs.

References

- [1] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham and A. Weinstein, "Matrix Converters: A Technology Review", IEEE Trans. Industrial Electronics, vol. 49, no. 2, pp. 276-288, April 2002
- [2] P. W. Wheeler, J. C. Clare and L. Empringham, "A vector controlled MCR Matrix Converter Induction Motor Drive with Minimized Commutation Times and Enhanced Waveform Quality", Rec. 2002 IEEE Industrial Appl. Conf., pp. 466-472, 2002
- [3] M. Takei, Y. Harada and K. Ueno, "600V-IGBT with Reverse Blocking Capability", Proc. 2001 Int. Symp. On Pwr. Semicond. Dev. & ICs, pp. 413-416, 2001
- [4] B. J. Baliga, "Fundamentals of Power Semiconductor Devices", 2nd Ed., Springer Science, 2019
- [5] S. Safari, A. Castellazzi, and P. Wheeler, "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter", IEEE Trans. Power Electronics, vol. 29, no. 5, pp. 2584-2596, May 2014
- [6] H. F. Ahmed, H. Cha, A. A. Khan, J. Kim, and J. Cho, "A Single-Phase Buck-Boost Matrix Converter with only Six Switches and without Commutation Problem", IEEE Trans. Power Electronics, vol. 32, no. 2, pp. 1232-1244, February 2017
- [7] S. Mori, M. Aketa, T. Sakaguchi and T. Kimoto, "Demonstration of 3 kV 4H-SiC Reverse Blocking MOSFET" in IEEE Int. Symp. On Power Semiconductor Devices and ICs, pp. 271-274, 2016
- [8] B. J. Baliga and K. Han, "Monolithic SiC Bi-Directional Field Effect Transistor (BiDFET): Concept, Implementation and Electrical Characteristics", Govt. Microcircuit Appl. and Critical Tech Conf., 2018
- [9] Information on <https://www.wolfspeed.com/power/products/bare-die/cpm2-1200-0025b>

[10] Information on <https://www.littelfuse.com/products/power-semiconductors/discrete-igbts/pt/low-frequency/ixgh20n120a3.aspx>