Final Technical Report (FTR)

Cover Page

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Signature of Certifying Official

10.06.2023
Date

By signing this report, I certify to the best of my knowledge and belief that the report is true, complete, and accurate. I am aware that any false, fictitious, or fraudulent information, misrepresentations, half-truths, or the omission of any material fact, may subject me to criminal, civil or administrative penalties for fraud, false statements, false claims or otherwise. (U.S. Code Title 18, Section 1001, Section 287 and Title 31, Sections 3729-3730). I further understand and agree that the information contained in this report are material to Federal agency's funding decisions and I have any ongoing responsibility to promptly update the report within the time frames stated in the terms and conditions of the above referenced Award, to ensure that my responses remain accurate and complete.

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Executive Summary:

Silicon heterojunction (SHJ) and tunnel-oxide-passivated-contacts (TOPCon) solar cells are the future for silicon technology after passivated-emitter-and-rear-contact (PERC) cells. However, the tool costs (CapEx) for SHJ (TOPCon) make the cell lines more than 2 (1.5) times of the cost of the PERC, which hinders the wide adoption these new technologies despite higher efficiencies. A common challenge for both cell types is that the passivation layers are sensitive to sputter damage. Furthermore, for TOPCon cells, it is desirable to have an inline (instead of batch) process for tunnel oxide and polysilicon to maximize the throughput and thus reduce the operation cost.

This project addresses this challenge by introducing an aerosol impact-driven assembly (AIDA) deposition tool, in place of high-CapEx DC-magnetron sputtering and plasma-enhanced chemical vapor deposition (PECVD), to deposit damage-free transparent conductive oxide (TCO) layers and silicon oxide passivation layers. For TCO deposition, our AIDA system is coupled with a gas-flow-sputter (GFS) source. We started with an off-shelf gas-flow-sputter source to understand the operating principles. After the first 9 month of the project, we learned that plasma energy is a key parameter to achieve high-quality TCO films and a low target-to-substrate distance is critical to achieve this. We then completed re-designed and fabricated the second generation of the GFS source ourselves with improvements including (1) a top-mounted design that requires no extra vacuum enclosure for the source and easy to service; (2) reducing target-to-substrate distance from 14 cm to 8 cm; (3) a binary gas flow manifold for a uniform gas flow; and (4) a direct water-cooling system where the copper backing plate of the sputtering target is in direct contact with the circulating water flow through the electrodes. Our third (final) design further simplified the source to only 4 components and reduced the targe-to-substrate distance to 2.5 cm. We also improved the dark space shield design to improve the deposition time between service. We demonstrated an indium tin oxide (ITO) coating thickness of 100 nm and sheet resistance of 240 Ω/sq with a bulk resistivity of 3×10^{-3} Ω·cm. By incorporating this ITO into SHJ cells, we achieved cells with open-circuit voltage that is 10 mV higher than controls that are made with DC magnetron sputtering.

For SiO_x deposition, our AIDA system is coupled with a PECVD source. This process is successfully scaled at the project partner—Swift Coat—that deposits tunnel oxide with non-uniformity < 5% across a 6” wafer. This oxide also functions as a passivation layer as we have achieved 2.6 ms minority carrier lifetime for TOPCon cell precursor samples that were symmetrically coated with 1.5 nm-nm-thick SiO_x and 50-nm-thick n-type polysilicon. The contact resistivity of such layer stacks was measured to be less than 10 mΩ·cm, which is sufficiently low for one-sun solar cell applications. During this project, we also worked with Von Ardenne and Fraunhofer ISE to evaluate the AIDA-SiO_x. We concluded that the passivation capability of our AIDA SiO_2 is on par with the state-of-the-art thermal oxide by achieving 726 mV implied open-circuit voltage compared to their baseline process of 735 mV. In another cell experiment with a batch size of 100 wafers, TOPCon cells that incorporated with AIDA-SiO_x achieved >21% efficiency, which completes the milestone.

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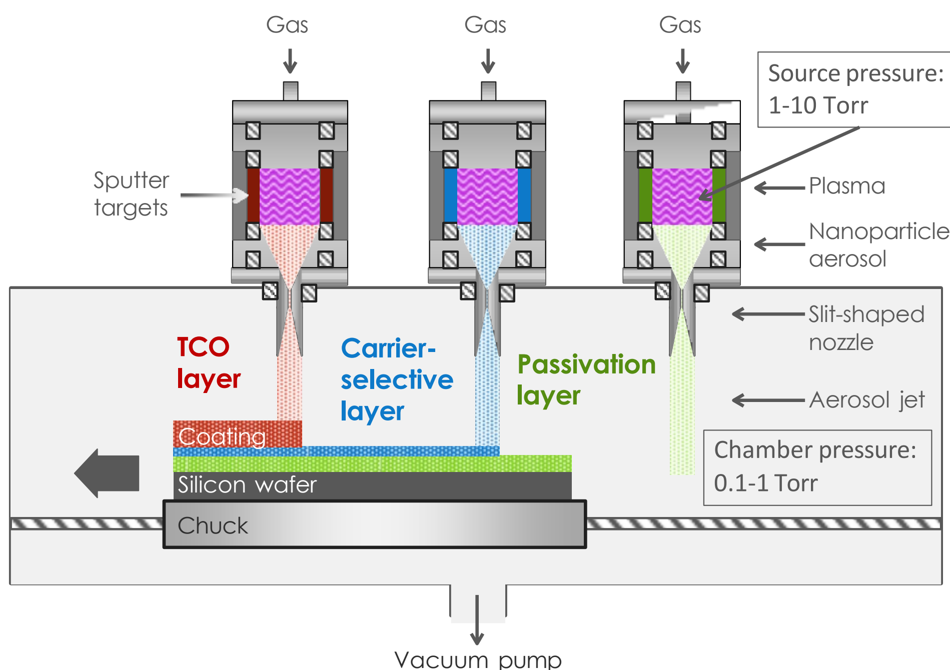
Background:

The efficiency of photovoltaic energy conversion is a decisive factor for low-cost electricity from renewable energies. In recent years, the efficiency of crystalline silicon solar cells in mass production has increased annually by about 0.5–0.6%, absolute, per year [1]. Presently, the workhorse technology—passivated-emitter-and-rear-contacts (PERC) solar cells—are reaching their efficiency limit. Therefore, in order to maintain this development speed, new technologies must be developed and transferred to industrial production. So far, silicon heterojunction cells and tunnel-oxide-passivated-contacts (TOPCon) cells are capable of reaching > 26% efficiency and are deemed as the next generation of silicon technology [2-3]. These high-efficiency solar cells use doped a-Si:H (SHJ) or poly-silicon (TOPCon, POLO) as the carrier-selective layer, but these materials absorb at least 1.5 mA/cm^2 parasitically when used in the front contact [4]. The transparent conductive oxide layer used for lateral transport in these cells is presently deposited by sputtering, which causes ion and UV damage that degrades open-circuit voltage (V_{oc}) by several tens of mV before annealing, and several mV even after annealing [5]. In addition, the contact resistivity of these heterojunction stacks is >0.2 Ohm·cm^2 and is very sensitive to the passivation layer thickness and transparent conductive oxide doping density [6], resulting in a FF loss of >2% per contact and unavoidable trade-offs between passivation, resistivity, and parasitic absorption. These trade-offs result in a narrow process window [7], which limits the yield in high-volume production. Finally, the high CapEx of the high-vacuum PECVD and sputtering tools, coupled with the yield loss, has inhibited widespread adoption of these cell technologies by cell manufacturers.



Schematic of the proposed AIDA deposition system

To reduce sputter damage, different sputter systems configurations such as rotatable magnetron sputtering [8], RAM cathode sputtering [9], and gas-flow-sputtering (GFS) were reported in the literature [10]. In a direct comparison of these

setups, Linss *et al*. found that, by testing on silicon wafers passivated with 8-nm-thick hydrogenated amorphous silicon (a-Si:H), rotatable magnetron sputtering yields 80 mV drop in implied V_{oc} (iV_{oc}) after sputtering, whereas RAM cathode or GFS yield less than 15 mV drop in iV_{oc} [8]. Although the sputter damage was mitigated in the RAM cathode or GFS sputtering, their dynamic deposition rate (DDR) was only 1/3 of the that of the tube sputtering, which hinders its application in high-volume production such as photovoltaics.

We will solve these problems by introducing a deposition technique—aerosol impact-driven assembly (AIDA)—that offers damage-free sputtering and with only rough vacuum (low CapEx). As shown in figure above, with a gas-flow (reactive) sputter source, a plasma operated at high pressure (several Torr) is confined between two metal oxide targets facing each other, and the nanometer-sized sputtered clusters are dragged downstream by a crosswise gas flow. The aerosol is then accelerated through a slit-shaped nozzle into a chamber roughly evacuated (100's of mTorr), within which wafers are translated under the nozzle. The clusters or nanoparticles deposit via inertial impaction because there are too few collisions with the background gas to deflect them (unlike at atmospheric pressure, at which small particles veer around the substrate), and the impaction speed is determined by, among other things, the pressure ratio across the nozzle and the distance to the substrate. Importantly, there is no sputter damage as the wafers are not immersed in the plasma.

In a different configuration of AIDA, in which the sputter source is replaced by a dusty PECVD source that operates at similar pressure to nucleate clusters in the plasma from precursor gases or vapors, our system will be used to deposit silicon oxide (SiO_x) layers used as a tunnel oxide passivation layer for TOPCon cells. Presently, the ultra-thin SiO_x passivation layer is often grown by dry thermal oxidation, UV/ozone, or wet chemical oxidation with hot nitric acid (HNO_3) as these oxides—in conjunction with Poly-Si—have demonstrated excellent J_0 values (< 10 fA·cm-2) [11-12]. However, this wet oxidation processes are susceptible to bath chemistry degradation during heated and continuous wafer batch processing. As the nitric acid solution is chemically reduced, the solution must be changed or spiked frequently to ensure repeatable and conformal oxide growth from batch to batch. Chemical oxidation is also not capable of depositing in-situ SiO_x and Poly-Si, requiring extra equipment and capital expenditure (CapEx) for full cell production. Our technology, if successful, would provide a low-CapEx, inline tool that is readily to incorporate with other inline chemical deposition systems to manufacture TOPCon cells.

Project Objectives:

The primary goal of this project is to enable manufacturable silicon solar cells with heterojunction contacts via an innovative deposition technique that will reduce capital expenditures (CapEx) by > 60%. It will generate the tools and processes that can readily incorporate into next generation silicon cells such as silicon heterojunction cells or tunnel-oxide-passivated-contact (TOPCon) solar cells. To achieve this goal, we introduce an aerosol impact-driven assembly (AIDA) deposition process, in place of high-CapEx plasma-enhanced chemical vapor deposition (PECVD) and sputtering, to deposit the passivation layer and electrode layers of silicon heterojunction solar cells.

The key advantages of our approach to fabricate heterojunction solar cells are: (1) AIDA possesses the materials versatility of sputtering but without any damage, and (2) AIDA is a rough-vacuum and continuous-deposition (not batch) technology. We will first prove the concept by using AIDA, in place of sputtering, to deposit transparent conductive oxide (TCO) layers with sheet resistance, parasitic absorptance, and open-circuit voltage (Voc) degradation values that compete with the present state of the art. We will similarly demonstrate passivation layers that enable the millisecond lifetimes and low full-stack contact resistivities of present state-of-the-art layers deposited by, e.g., PECVD. We will then integrate these layers into 4-cm^2 silicon heterojunction solar cells to demonstrate device performance competitive with the state of the art. By the end of the project, we will scale the hardware and process to achieve similar efficiency on 6” solar cells with a projected throughput of 3600 wafers/hr. Reliability testing, over a one-year span of the project, will demonstrate that AIDA-deposited cells can pass the IEC 61215 standard damp-heat and thermocycling tests. The go/no-go milestone is this project is to demonstrate that a solar cell with the AIDA-deposited TCO layer or the cell with the AIDA-deposited passivation layer must have higher efficiency than the reference cell, which itself must be >21% efficient.

The potential impact of the proposed project is it significantly increases the efficiency, affordability, and manufacturability of silicon cells with heterojunction contacts. It will introduce new tools and processes that lay the groundwork for >25%-efficient commercial cells. With such cells, >23%-efficient modules are expected, which will reduce utility LCOE below 0.04/kWh in average US climates (calculated with NREL’s cost model assembled by Kelsey Horowitz). The envisioned cells are enabled by a new deposition technology—AIDA—which itself has the potential to be transformative to solar manufacturing and other markets. In particular, the rough-vacuum-based deposition technique also reduces CapEx by >60%, which allows cell manufactures to quickly adopt heterojunction technology and expand without requiring crippling equipment investment. This is especially important to accelerate the expansion of PV production—and thus adoption—to meet DOE’s climate targets.

Project Results and Discussion:

Task 1: Develop TCO and passivation layers deposited by AIDA

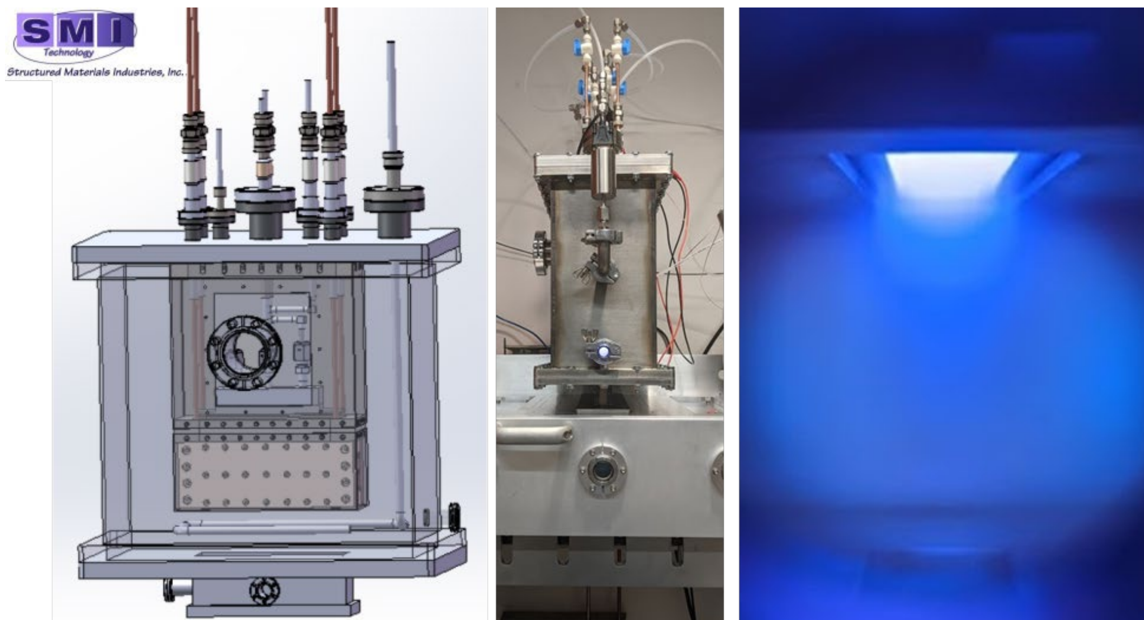


Fig. 1 CAD drawings of the 1st Gen gas-flow sputter source designed by SMI (left), the gas-flow sputter system fully installed at ASU (middle), and a photo through the vacuum view port looking at the bottom of the sputtering targets during a deposition (right).

1st Generation gas-flow sputtering source

The 1st Gen gas-flow sputtering system and all its components, ordered from Structured Materials Industries (SMI), arrived in full at ASU on January 30th, 2020, and the source was installed on February 5th, 2020 (Fig. 1 middle). To achieve a deposition, we have made several hardware changes necessary to improve the power delivery to the sputtering targets and reduce the leak rate of the vacuum chamber that houses the gas-flow sputtering source. Outlined below are some challenges we faced and the solutions we implemented to solve these problems.

In this SMI source, the two large sputtering targets are situated vertically in the middle of the vacuum chamber (Fig. 1 left) and are mounted to the two copper cooling blocks. Each copper backing plate has a water inlet and outlet to continuously flow cooling water, dissipating the excessive heat generated during the sputtering process. These four copper water-cooling tubes exit the vacuum chamber on the top flange through insulated CF vacuum chamber feedthroughs. Cleverly, these copper tubes also deliver the DC (or pulsed DC) power to the sputtering targets. These electrically powered copper tubes pass through the cavity that directs the argon sputtering gas between the targets. We found that these copper cooling tubes develop a plasma glow discharge around them when powered in the presence of argon, as shown in Fig. 2 (left). This plasma causes several problems; it reduces the power delivered to the sputtering targets, and it will erode through the water-cooling tubes, eventually rupturing. We found it is essential to shield the tubing with an electrical insulator so that the tube does not ionize the argon gas surrounding it. We used quartz sleeves for this purpose, pictured in Fig. 2 (middle), installed on the copper tubes, and they effectively suppressed the glow discharge.

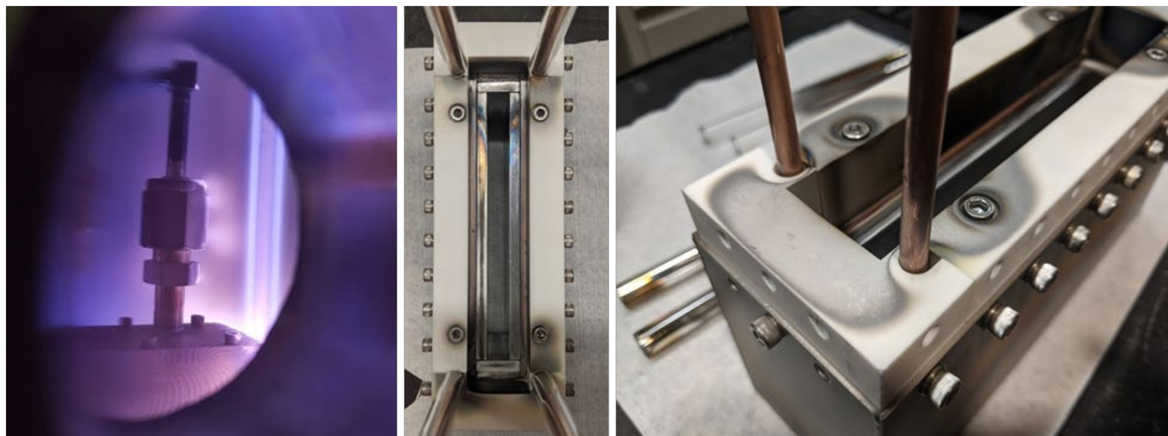


Fig. 2 A photo inside the gas-flow sputtering chamber showing the anode and plasma glow discharge around the water-cooled copper tubing during deposition (left). A view down the center axis of the sputtering targets with the quartz sleeves over the water-cooled copper tubing (middle). A photo of the four bolts and the sputtered material deposited on the white ceramic parts from the glow discharge on the bolts (right).

Another glow discharge was discovered on the 4 top bolts that hold electrical insulation blocks to the target backing copper plates. These bolts are electrically powered and exposed to flowing argon gas during operation. Fig. 2 (right) shows the four bolts and the plasma marks, which indicates the bolt material was sputtered off and deposited on the white ceramic pieces nearby. This plasma was suppressed by covering these bolts and lowering the grounded anode closer to the targets to confine the sputtering plasma between the anode and the targets. With these modifications, the source successfully operates, depositing coatings of the sputtered target material without deleterious sputtering of non-target hardware.

After successfully demonstrating deposition with aluminum targets, we swapped the metal targets with indium tin oxide (ITO) (In_2O_3/SnO_2 90/10 wt %) targets. The essential operating components in the sputtering system are the grounded anode, working gas flow, reactive gas flow, and translating substrate and substrate heater.

The grounded anode is a steel plate placed in the sputtering system just above the hollow cathode sputtering targets (ITO). It allows for a stable and dense plasma emission in the hollow target cavity by providing a path to ground for electrons in the plasma. The working gas flow of argon through the hollow cathode supplies the ionizable gas to ignite and sustain the plasma in the hollow target cavity. This working gas flow also expels sputtered material out of the hollow cathode and is the primary transport mechanism of sputtered material to the substrate. The substrate translation stage allows for the coating of 6" substrates by moving wafers at a constant speed under the 6" linear sputtering head. We installed a quartz lamp heater that can heat the substrates, up to 350 °C, before deposition or provide a post-annealing treatment in vacuum after the coating is deposited. Fig. 3 shows our initial deposition of a 100-nm-thick ITO coating on silicon substrates, which completed the first milestone of non-zero deposition.

As shown in Fig. 4 (left), we achieved uniform coating across a 5" wafer. The thickness uniformity of this coated wafer was measured using variable angle

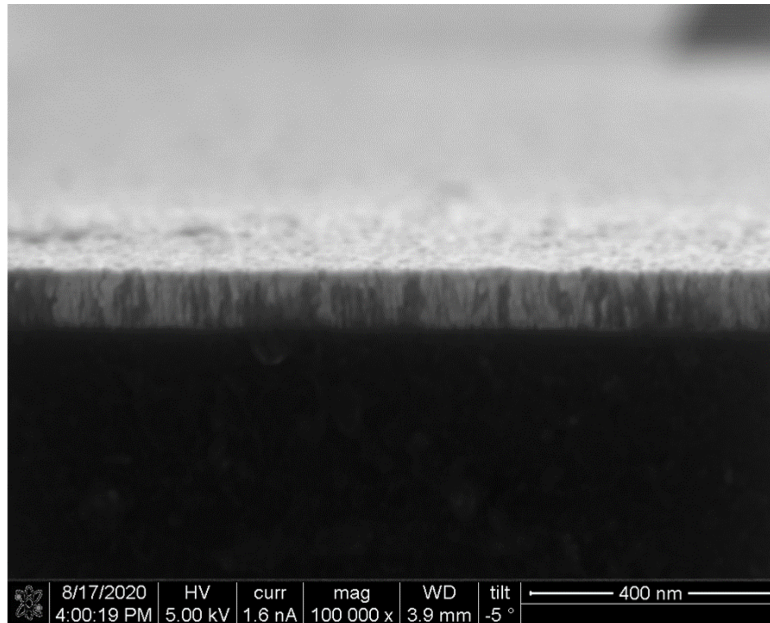


Fig. 3. A cross-section SEM image of an ITO coating deposited by the SMI 1st gen gas flow sputtering source.

spectroscopic ellipsometry mapping (VASE), with the thickness calculated at 56 points across the wafer, shown as black dots in Fig. 4 (right). The contour plot is the interpolated thickness in nanometers shown on a color scale. The thickness non-uniformity was calculated by taking all the measured points across the wafer and using Equation (1):

$$Non\text{-}uniformity = \frac{d_{max} - d_{min}}{d_{avg}} \qquad (1)$$

Where d_{max}, d_{min}, and d_{avg} are the coating's maximum, minimum, and average thickness, respectively. It shows a 7.6% non-uniformity of an ITO coating across a 5" wafer, which completed the milestone for thickness non-uniformity.

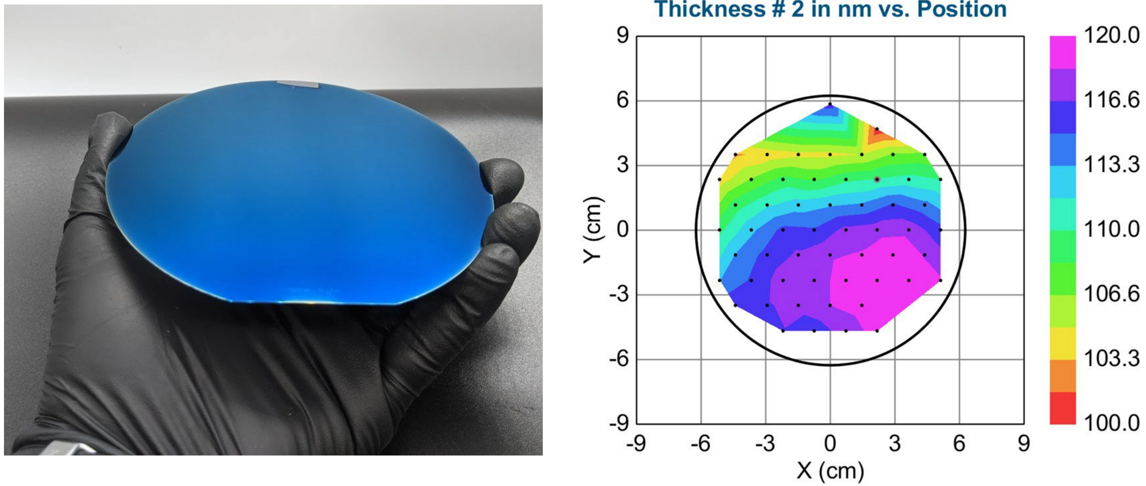


Fig. 4. A photo of a 5” silicon wafer coated with a 110-nm-thick ITO layer (left), and thickness mapping from ellipsometry measurement (right).

Fig. 5 shows that we deposited 80-nm-thick ITO coatings at room temperature with different oxygen flows on glass slides. We then annealed them at various temperatures to simulate potential cell processing conditions. Note that standard DC magnetron sputtering of ITO on an SHJ solar cell involves the room temperature deposition of ITO. Then a 200 °C anneal for 20 min after the screen-printing step to cure the silver paste. And other TOP Con-like cells may experience higher-

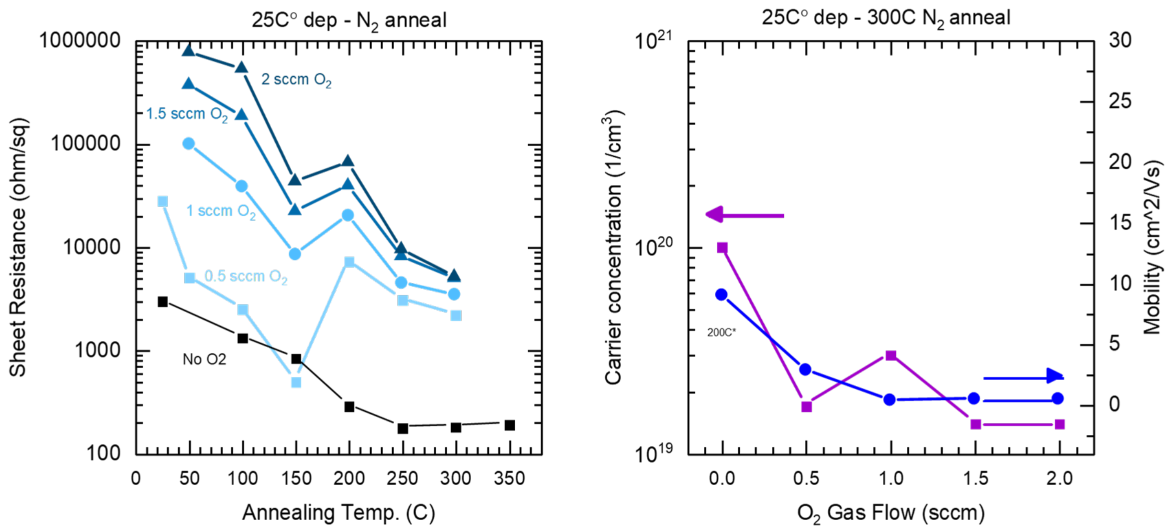


Fig. 5. Sheet resistance of 80-nm-thick ITO coatings deposited on glass at room temperature and then annealed in a nitrogen atmosphere at various temperatures (left); also shown are the mobility and carrier concentration of the coatings annealed at 300 °C

temperature treatment. Reactive oxygen gas is used to tune the density of oxygen defects in the ITO and, therefore, the carrier concentration. The post-annealing also improves the crystallinity in the coating and consequently the carrier mobility, as electrons conduct more quickly in a periodic crystal at room temperature.

We found that adding less than 0.5 sccm of oxygen during deposition was vital for improving the coating conductivity and improving coating transparency. The coating with no added oxygen had ~200 Ω/square sheet resistance but appeared brown and too absorptive as the front TCO of a solar cell. Higher oxygen flows result in sheet resistances that are too high to be used as the lateral conduction layer on the front side of one-sun solar cells. Fig. 5 (right) shows the carrier concentration and mobility as a function of oxygen gas flow for the ITO coatings annealed at 300 °C. This indicates that coatings made with oxygen gas flow over 1 sccm are not conducive enough for solar cells even after being annealed at an elevated temperature of 300 °C. This shows a decrease in sheet resistance with greater annealing temperatures, demonstrating that gas-flow sputtered ITO needs to be deposited at elevated temperature or be post-annealed to improve the conductivity, which motivated our subsequent process development.

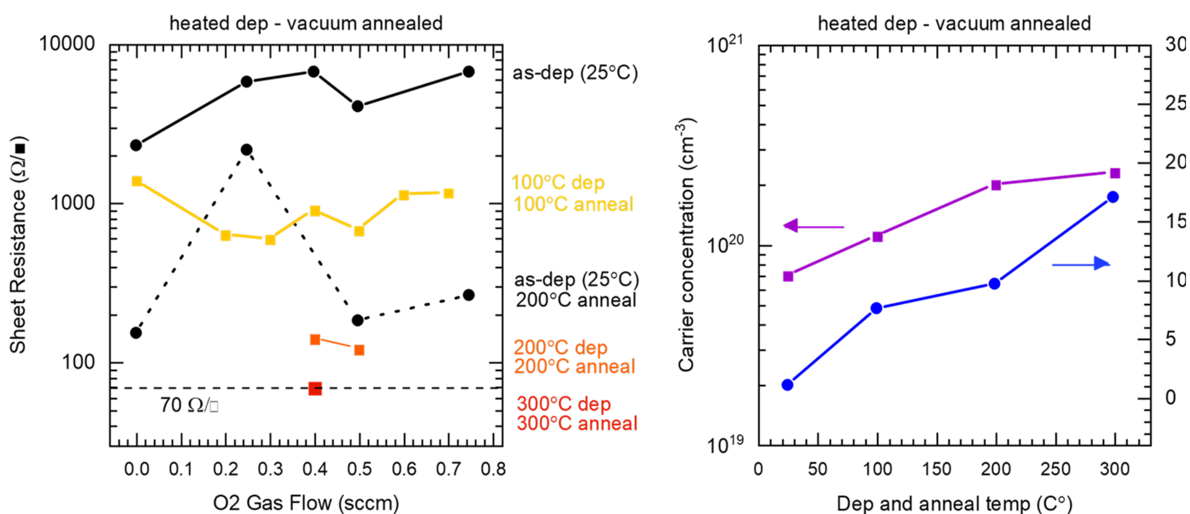


Fig. 6. Sheet resistance of 80-nm-thick ITO coatings deposited on glass at different temperatures and then annealed in-situ in vacuum (left). Also shown are the carrier concentration and mobility of the sample with the lowest sheet resistance at each temperature (right).

We then deposited and vacuum annealed ITO coatings at elevated temperatures. As compared in Fig. 6, the sheet resistance of a room temperature deposition was 7000 Ω/square, while the sheet resistance for the film deposited and annealed at 300 °C was 70 Ω/square, which achieved the TCO conductivity milestone. Hall measurements on these samples revealed that as the annealing temperature increases, both carrier concentration and mobility increase. Notably, mobilities > 10 $cm^2/V{\cdot}s$ were achieved with deposition (and annealing) temperatures greater than 200 °C. However, SHJ solar cells can only withstand a TCO deposition at 200 °C but not at 300 °C, as the amorphous passivation will likely degrade.

One thing to note is that the deposition temperature listed in Fig. 6 is the substrate temperature under the quartz heating lamp (before the process begins). As the process starts, the wafer moves towards the deposition nozzle (and away from the lamp), and it begins to cool down quickly while the ITO is being deposited. Our measurement shows that the actual substrate temperature after deposition was about

half of its initial value. This indicates there is room for hardware improvement of the substrate heater. We then fabricated another substrate heating stage and installed it for the subsequent experiments in this report.

We also explored the amount of sputtering damage introduced by gas flow sputtering. The greater the damage, the larger the iV_{oc} decreases after the sputtering process. Before the GFS ITO deposition, the iV_{oc} of the SHJ cell was 716 mV. After gas flow sputtering of ITO on both sides of the cell (65 nm on the front and 130 nm on the back), the iV_{oc} dropped by 3 mV to 713 mV, which indicates there was negligible sputter damage. Fig. 7 shows the photoluminescence image of the half-coated sample with ITO. The slight change in radiative recombination between the sputtered and non-sputtered sides confirms the damage-free deposition. This is remarkable and a great demonstration that gas-flow sputtering is a gentle and low-damage technique for depositing the TCO (ITO) layer in an SHJ solar cell. For comparison, traditional sputtering would typically result in iV_{oc} drop by at least 50 mV, leaving the cell at approximately ~650 mV before the screen-printing (annealing) process.

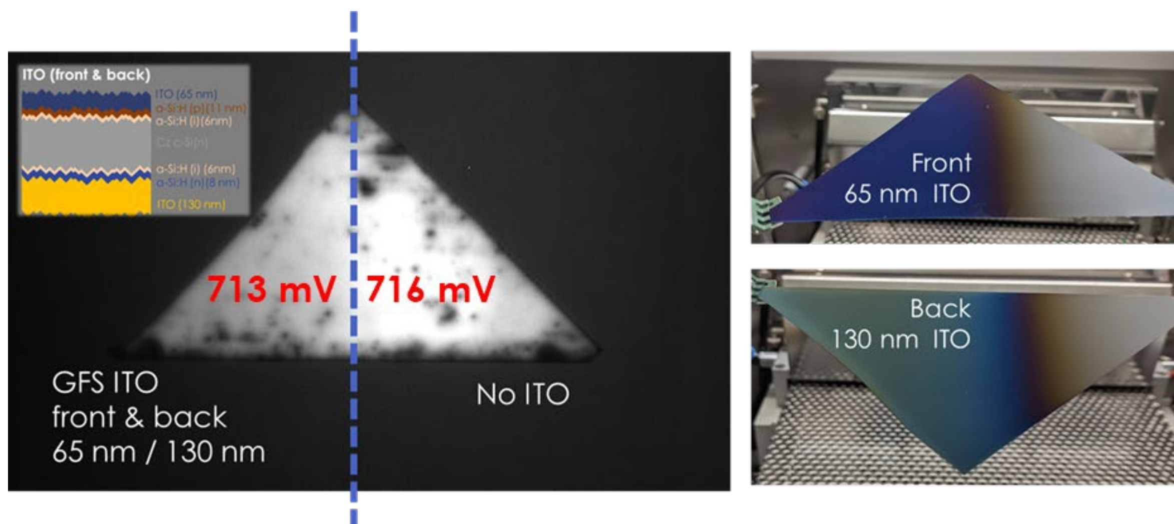


Fig. 7 Photoluminescence image of a SHJ cell precursor half-coated with GFS ITO on both sides (left), and photos of the sample after ITO deposition (right). The inset shows the layer structure of the cell precursor.

- *TCO coatings deposited by gas-flow-sputter source from SMI (Gen 1)*

Getting familiar with the SMI source, we conducted an in-depth process development to evaluate its potential. This sputtering source is characterized by a very long distance between the sputtering targets and substrate (~14 cm). This requires the source to run argon carrier gas at high flow rates (3 – 6 Standard liters per minute (SLM) at pressures of 400 – 700 mTorr to obtain) to obtain reasonable deposition rates (> 1 nm*m/min).

We first conducted a factorial design experiment with replicates to determine the most conductive indium tin oxide (ITO) deposition parameters. We varied the two most

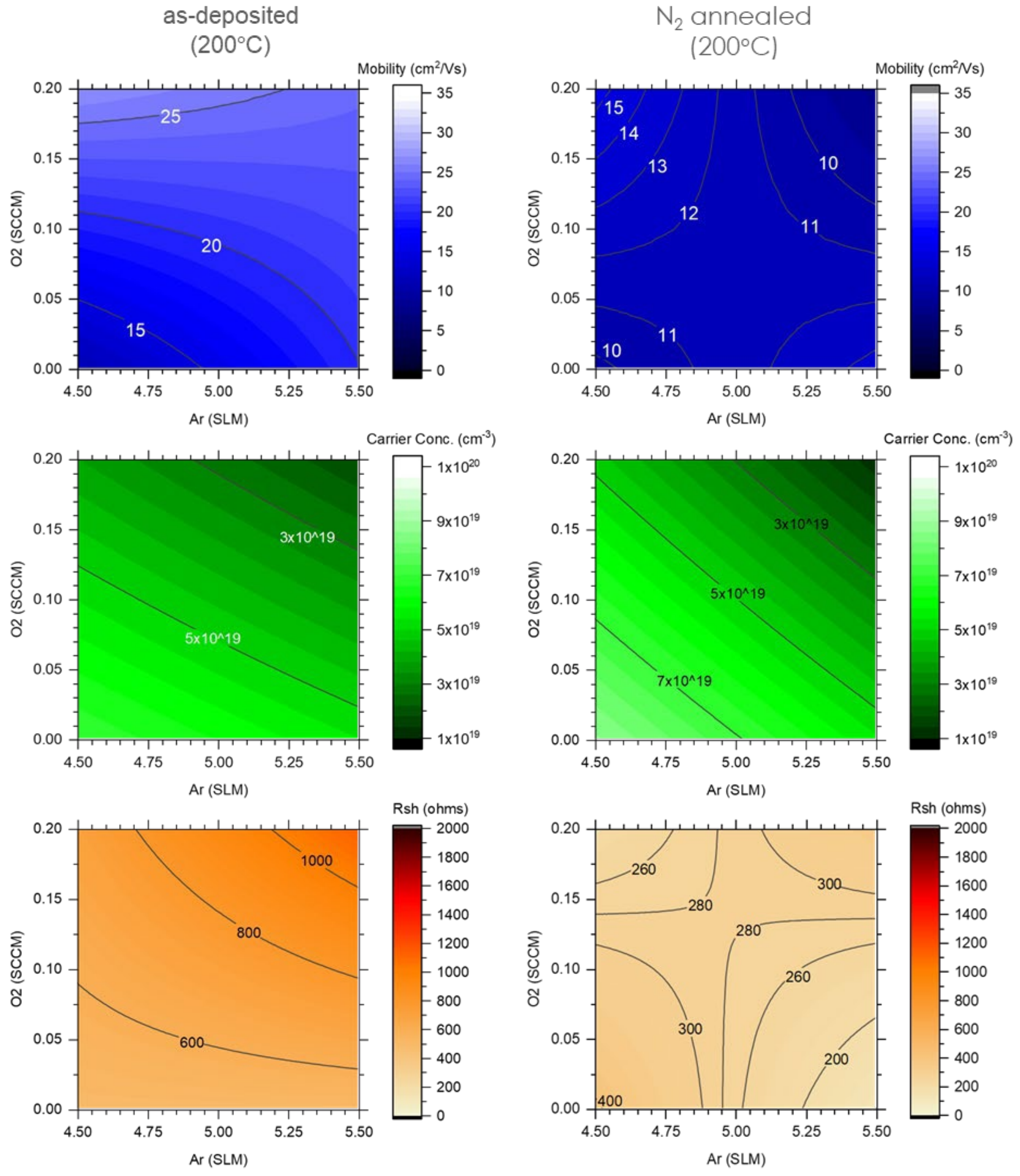


Fig. 8 Mobility (blue), carrier concentration (green), and sheet resistance (orange) of AIDA-ITO coatings as a function of argon gas flow and oxygen flow. These coatings were deposited with the SMI gas-flow-sputter source.

significant factors, the Argon gas flow (4.5 – 5.5 SLM) and the oxygen gas flow (0 – 0.2 sccm), in a 2x2 factorial design with a center point while keeping other factors constant: e.g., the hardware setup and sputtering power (2kW), deposition temperature (200°C), the sample stage height, and coating thickness (85 nm). Next, some of these samples received an annealing process in a nitrogen atmosphere for 20 min. The results of this experiment are plotted in Fig. 8. This experiment concluded

that no combination of parameters was found to achieve the high conductivity (70 ohm/sq at 70 nm thick) needed for high-efficiency silicon heterojunction solar cells.

After more experimentation and analysis, we determined that the SMI gas flow sputtering source, as designed, cannot produce highly conductive TCO coatings. This is due to the weak plasma energy that arrives at the growing thin film located 14 cm away from the sputtering targets. At these low-vacuum pressure (400 – 700 mTorr), there are too many gas collisions between the sputtering targets which thermalizes the gaseous ions by the time they reach the substrate. In this low-energy coating growth regime, the gas-flow sputtered ITO exhibits small and separated crystallites in the coating with a high density of grain boundaries, in contrast to densely packed large grains in a direct-current (DC) magnetron sputtered ITO coating. Fig. 9 shows a cross-sectional SEM images of ITO coatings deposited by the SMI source. Compared to DC magnetron sputtering, the SMI gas-flow sputtering produces films with much smaller grains. This grain boundary scattering significantly reduces the mobility of free carriers in the ITO coating. This reduced mobility is the critical challenge for producing highly conductive coatings using gas-flow sputtering.

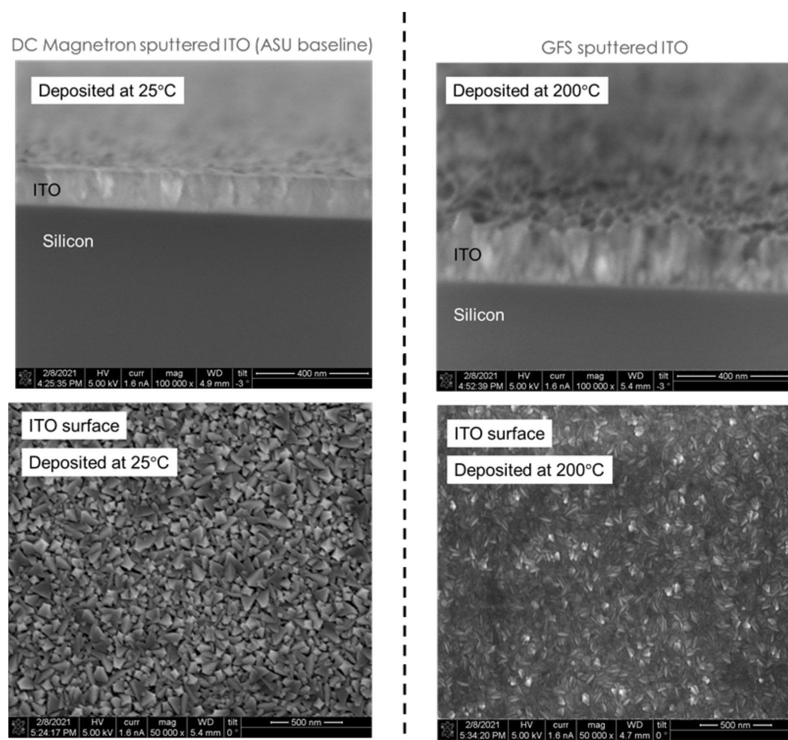


Fig. 9 Cross-sectional SEM of DC magnetron sputtered ITO and gas-flow-sputtered ITO using 5 SLM of Argon gas flow from the SMI source.

Given the low crystallinity of the deposited coating due to weak plasma energy, we tried to deposit hydrogenated Indium oxide (InO_x:H) material that can be crystallized at low temperatures to increase the conductivity. InO_x:H is an exceptional candidate as a TCO material for a high-efficiency silicon heterojunction solar cell due to its high mobility and low free carrier absorption in the solar spectrum. A unique feature of hydrogenated indium oxide, as discovered with magnetron sputtering, is that adding a small amount of water vapor into the sputtering chamber promotes amorphous coating growth on the substrate at room temperature. Subsequent annealing at 200—

300 °C crystallizes the coating and results in higher mobility (and thus conductivity). This material was sputtered from our system's sub-stoichiometric indium oxide (InOx) targets. Since In_2O_3 is electrically insulating, the oxygen-deficient targets are electrically conductive and key to enabling gas flow sputtering with a DC power supply. We could also tune the stoichiometry by flowing additional oxygen gas below the sputtering targets in the plasma. To understand the deposition, we first tried depositing coatings with just argon and oxygen gas without water vapor. By varying oxygen flows from 1 standard cubic centimeters per minute (sccm) to 40 sccm under varying conditions (substrate temperature, post-annealing conditions, etc.), we found no correlation between oxygen flow and coating conductivity. We discovered a similar trend for the ITO material deposited at the lower pressures (550 mTorr) with more experiments. Thus, a reduced gas flow (4.5 SLM) resulted in the most conductive coatings. We then introduced water vapor into the system without oxygen addition, and the results are shown in Fig. 10. It shows that the sheet resistance of a 150-nm-thick InO_x:H coating increases with increasing water vapor flow into the plasma. After subsequent annealing in air at 200 °C for 20 min, the sheet resistance of these coatings increased by an order of magnitude or greater. We also repeated these depositions on a heated substrate to promote high-mobility crystalline coating growth. We achieved the lowest sheet resistance of 1000 ohm/sq deposited at 550 mTorr with no added oxygen or water vapor. These coatings were also annealed at temperatures up to 350 °C until they crystallized, as confirmed by XRD. However, the sheet resistance remains high. After further investigation with cross-sectional SEM and Hall mobility measurements, we concluded the coating's conductivity is limited by the low carrier concentration and poor carrier mobility due to the high density of grain boundaries and small crystalline grains in the coating, just like the ITO materials.

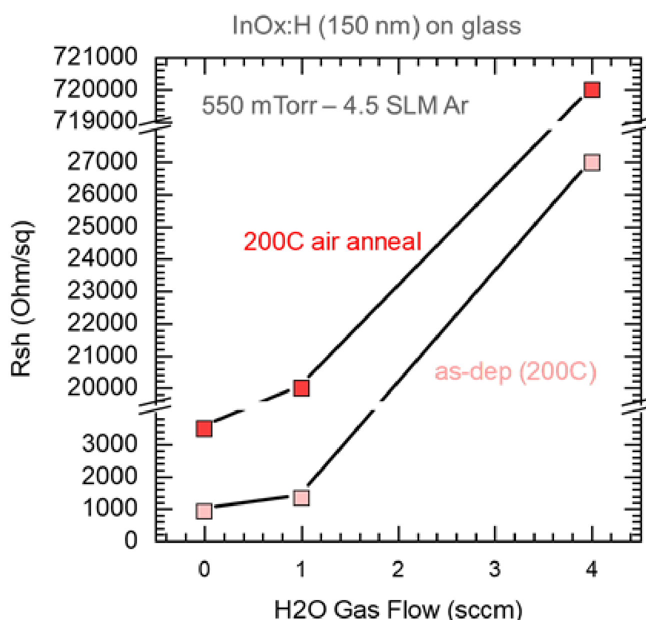


Fig. 10 Sheet resistance of gas flow sputtered InO_x:H under different water flow and substate temperatures with a constant pressure and argon gas flow.

As both materials exhibit the same issue, likely due to weak plasma energy, we believe the SMI gas-flow sputtering source is incapable of making highly conductive TCO coatings in its current design due to the sizeable target-to-substrate distance of 14 cm. We anticipate the critical factor in improving coating quality will be designing a sputtering source that can operate at a lower pressure and have the targets much closer to the substrate. Therefore, we decided that it was essential to design a new gas flow sputtering source from scratch to overcome this fundamental limitation of the 1st Gen SMI gas flow sputtering source.

2nd Generation gas-flow sputtering source

The ASU-designed gas-flow sputtering source was simplified in several ways, adding technical advantages during the coating process and facilitating assembly and maintenance of this sputtering source. Compared to the SMI source, this source has a top-mounted design that requires no extra vacuum enclosure for the source. This means only the surface of the targets is under vacuum while the power and cooling-water connections to the targets are outside the chamber in atmospheric pressure. This makes the source easy to service and reduces potential parasitic plasma elsewhere in the chamber, e.g., behind the targets that would otherwise need to be covered by a dark space shield. The target-to-substrate distance was decreased to 8 cm and improved the TCO material's dynamic deposition rate and conductivity. A binary gas flow manifold was added to the Argon gas port, ensuring a uniform gas flow along the targets' length and improving the coating uniformity. This design also incorporates a direct water-cooling system where the copper backing plate of the sputtering target is in direct contact with the circulating water flow through the electrodes. This increases the cooling efficiency on the targets and allows us to run at higher power densities comparable with traditional magnetron sputtering. This is important for scaling the sputtering source because the deposition rate increases linearly with the sputtering power density applied to the targets. Fig. 11 shows a photo of this sputtering source mounted on an AIDA tool and a schematic of a cross-section

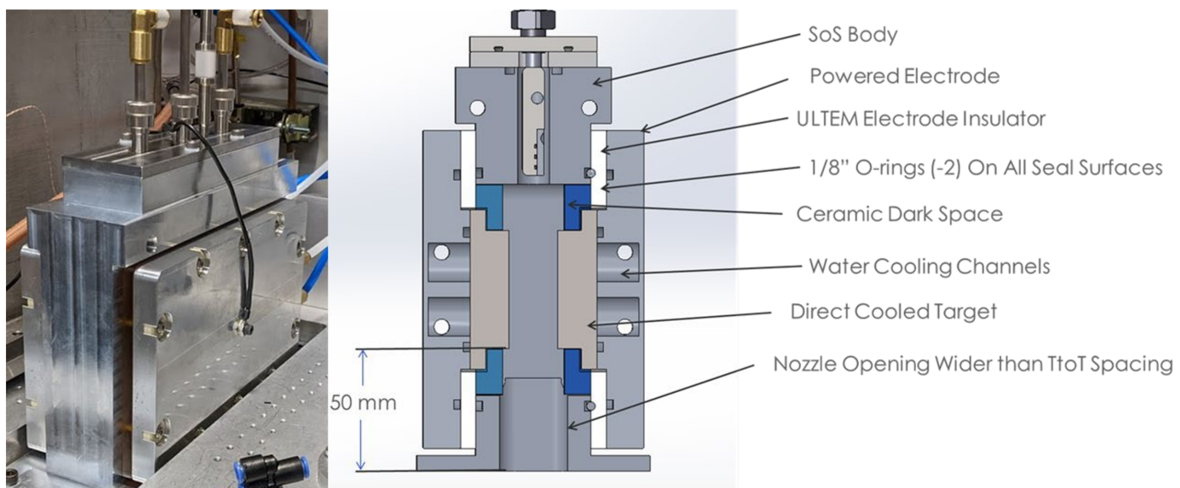


Fig. 11 Photo (left) and 3D CAD model (right) of the first-generation ASU-designed gas-flow sputtering source

view of the 3D CAD model of the source design. It also reduced the target-to-substrate distance from 14 cm to about 5 cm.

- *TCO coatings deposited by a gas-flow-sputter source designed by ASU (Gen 2)*

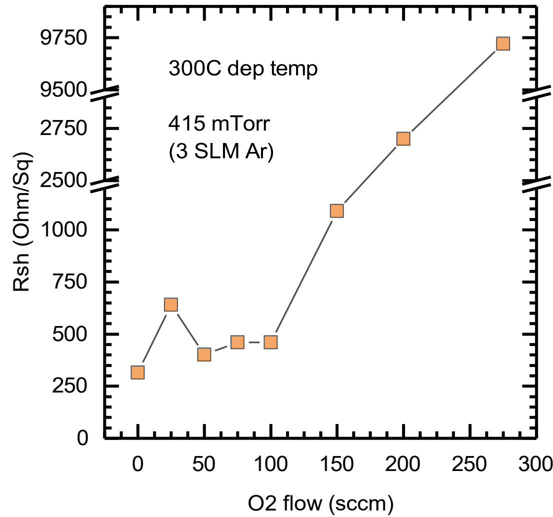


Fig. 12 Sheet resistance as a function of oxygen gas flow for ITO coatings deposited with gas-flow-sputter source designed by ASU.

Our new source design deposited 85-nm-thick ITO on glass substrates at 300°C with fixed pressure and argon gas flow settings. This allows us to adjust the oxygen gas flow introduced between the sputtering targets and substrate, to tune the stoichiometry of the material and improve its conductivity. We selected 3 SLM of argon

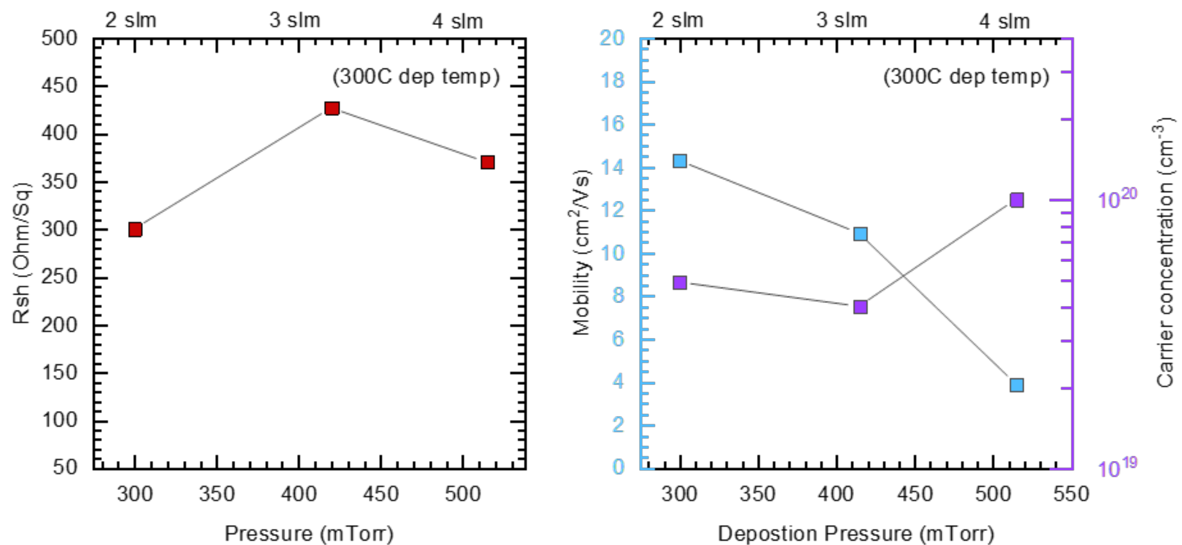


Fig. 13 Sheet resistance (left), mobility and carrier concentration (right) as a function of deposition pressure for ITO coatings deposited with gas-flow-sputter source designed by ASU.

gas flow, corresponding to 415 mTorr pressure in the sputtering chamber because it produces uniform deposition across the substrate pallet. Under these conditions, the sputtering source had a stable current and voltage with minimal arcing on the target surface. As shown in Fig. 12, the most conductive coatings were deposited with approximately 50 sccm of oxygen gas flow, resulting in a sheet resistance of 400 ohm/sq.

Next, we tested our hypothesis that lower pressures are needed to increase the coating growth energy and improve the carrier mobility in the TCO coating. Continuing this experiment, we fixed the oxygen gas flow at 50 sccm and decreased the argon gas flow to decrease the pressure in the chamber. The coating growth rate decreases with the lower gas flow, but this is compensated by adjusting deposition time so that all the coatings deposited are 85 nm thick. Fig. 13 shows the results from this experiment in that we obtained 300 ohm/sq coating sheet resistance deposited at 300 mTorr. Hall measurement results of these samples, also shown in Fig. 13, reveals that the carrier mobility increases as the deposition pressure decrease and the carrier concentration in the 10^{19} cm^{-3} range with modest mobility explains the high sheet resistance of these samples. This experiment confirms our hypothesis that we can improve carrier mobility in the TCO by decreasing the deposition pressure.

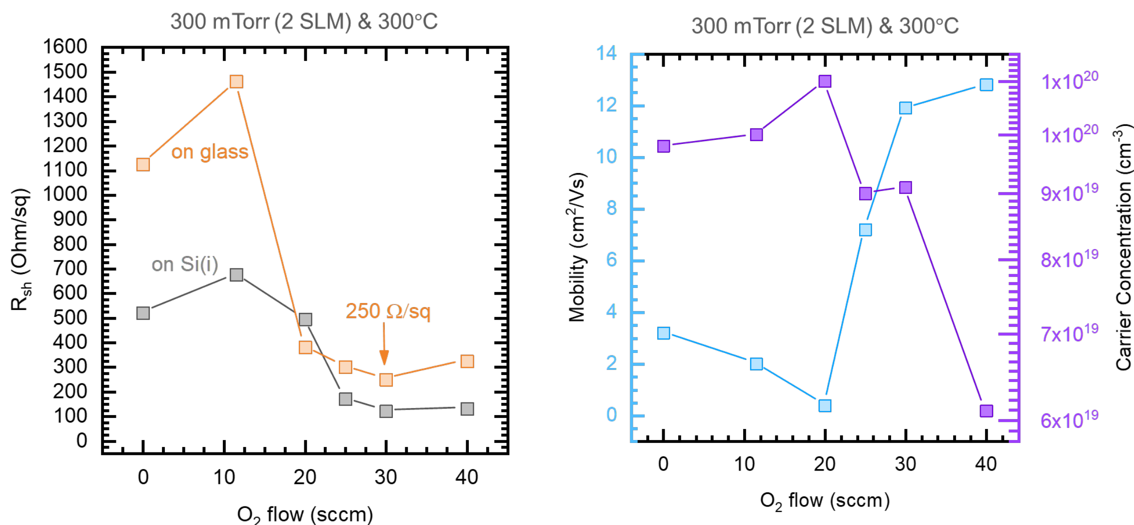
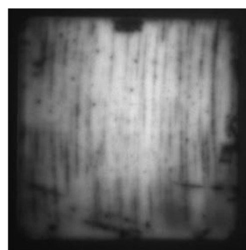


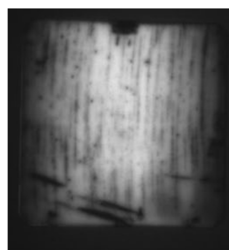
Fig. 14 Sheet resistance (left), mobility, and carrier concentration (right) as a function of deposition pressure for ITO coatings deposited with a gas-flow-sputter source designed by ASU.

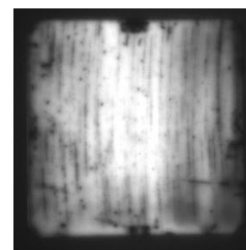
Based on this result, we ran another experiment with the decreased gas flow at 2 SLM (a corresponding pressure of 300 mTorr) and re-optimizing the oxygen flow, as a lower flow of Argon gas may have a different optimum for oxygen gas flows. As shown in Fig. 14, we found the new optimum oxygen gas flow is around 30 sccm. Fig. 14 also shows that the carrier mobility strongly increases with more oxygen gas flows, while the carrier concentration decreases dramatically. We see that 30 sccm of oxygen is the inflection point where the carrier concentration has not reduced too much. In contrast, the mobility has significantly increased, leading to the minimum sheet resistance of 250 ohm/sq for an 85-nm-thick coating. These results indicate that

the growing coating still needs more energy during deposition. And we plan to improve this further by decreasing the target-to-substrates distance, depositing at lower pressures, and considering other techniques for igniting another plasma over the substrate surface during deposition.

iV_{oc} @ 1 sun	Pre-Sputtering	Post-sputtering	200°C 20 min anneal
Gas-flow-sputtered ITO	745 mV	743 mV	743 mV
Magnetron ITO	745 mV	650 mV	730mV







Pre-Sputtering SHJ   Post GFS sputtering   200°C 20 min anneal

Fig. 15 implied V_{oc} of silicon heterojunction cell precursors at different process steps. Also shown are the corresponding photoluminescence images for the gas-flow-sputtered the sample. steps.

We also examined the sputter damage from this Gen 2 source. As shown in Fig. 15, the cell precursors have implied V_{oc} (iV_{oc}) of 745 mV. After magnetron sputtering of ITO on both sides, the iV_{oc} dropped dramatically to 650 mV because of sputter damage. Subsequent annealing at 200 °C for 20 min recovers most of the sputtering damage and increases the iV_{oc} back to 730 mV, indicating 15 mV of voltage loss caused by sputter damage. In contrast, after gas-flow sputtering, the iV_{oc} of the cell precursor stays constant (within measurement error), and annealing shows no improvement. This proves that the gas-flow sputtering process is damage-free and achieved the milestone.

A focus of developing the gas-flow sputtering source has been reducing sheet resistance by increasing mobility. We have demonstrated that the Gen 2 source can produce ITO coatings with mobilities exceeding 20 cm^2/Vs (comparable to magnetron sputtered coatings) at elevated substrate temperatures (200 °C). This source was operated in the traditional hollow cathode mode with the chamber acting as the ground and produced coatings with mobilities below 5 cm^2/Vs when the substrate is at room temperature. While it is possible to heat most silicon cells during manufacturing, it is preferable from a CapEx perspective—a significant focus of this project—to reach excellent coating properties at room temperature. Therefore, we explored an alternative operation mode that would take advantage of a plasma immersion in a positive column to facilitate the bombardment of low-energy argon ions (those with enough energy to densify the coating but not break Si-H bonds) onto the depositing coating.

To do this, we've operated the gas-flow sputtering source in a dual-source mode (using two identical Gen 2 sources) to use the positive column of a plasma generated between the two sources. The sources are electrically connected between the floating

outputs of a pulsing power supply; and we employed an evaluation Truplasma™ power supply unit loaned to us by Trumpf to power them.

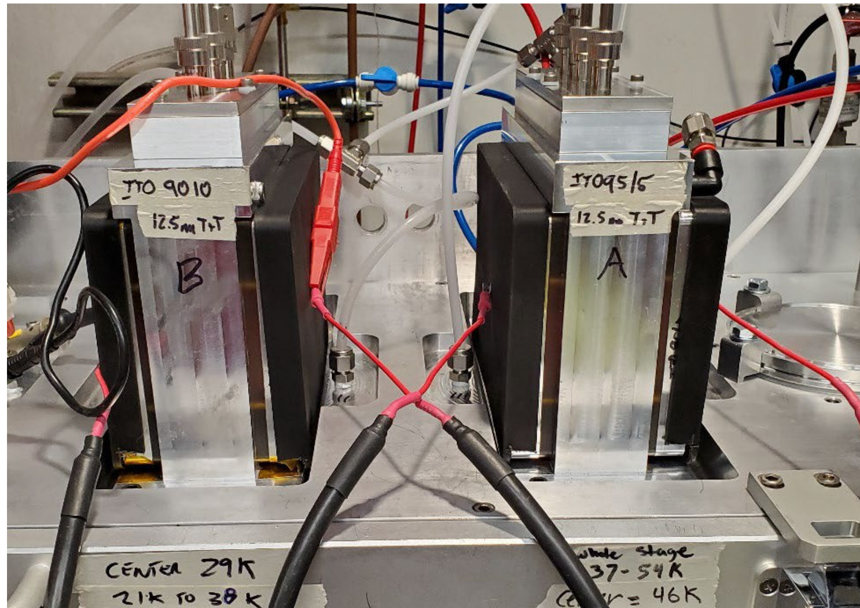


Fig. 16. ASU Gen 2 dual-source configuration hardware.

The Gen 2 dual-source configuration is shown in Fig. 16. There are two different ways in which we have operated the sources with the Truplasma™ power supply:

1. Direct DC with one source as the cathode and one source as the anode.
2. Bipolar pulsing, alternating anode/cathode between two sources at different frequencies (0.1 kHz to 10 kHz).

As shown in Fig. 17, a plasma is sustained between the two sources, and an electrically floating substrate carrier is passed through the plasma volume when operating in these modes.

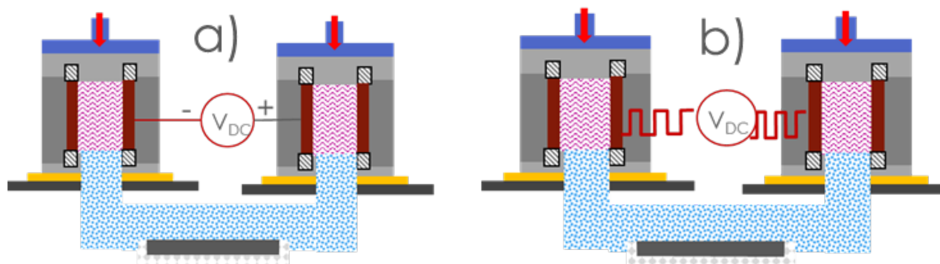


Fig. 17. ASU Gen 2 dual-source configuration for plasma immersion of substrate. a) Direct DC with a floating anode and b) bipolar pulsing alternating cathode/anode.

The plasma immersion of the substrate creates a negative electric charge on the substrate surface due to the attachment of the free electrons in the plasma. This negative charge attracts ions from the plasma to the substrate surface. The argon ions in the plasma arrive with energy directly proportional to the potential difference

between the plasma potential and the potential on the floating substrate carrier. This is different from the energetic ions that come directly off the sputtering targets in a magnetron sputtering system; those are much more energetic and are responsible for plasma damage to sensitive substrates like silicon heterojunction cell precursors. The intention is to use the energy of the "falling" argon ions to increase the adatom mobility and improve the TCO coating crystallinity and thus the coating carrier mobility.

With the setup shown in Fig. 18, we measured the bias on the substrate by measuring the potential between the floating substrate and one of the GFS source electrodes. An example of the time-resolved bias and sputter voltages at a 10 kHz pulsing frequency is shown in Fig. 19. Every half cycle, this source electrode becomes an anode; therefore, the potential difference in this half cycle represents the potential on the substrate relative to the plasma potential. The pulsing spikes the voltage each time the cathode and anode swap.

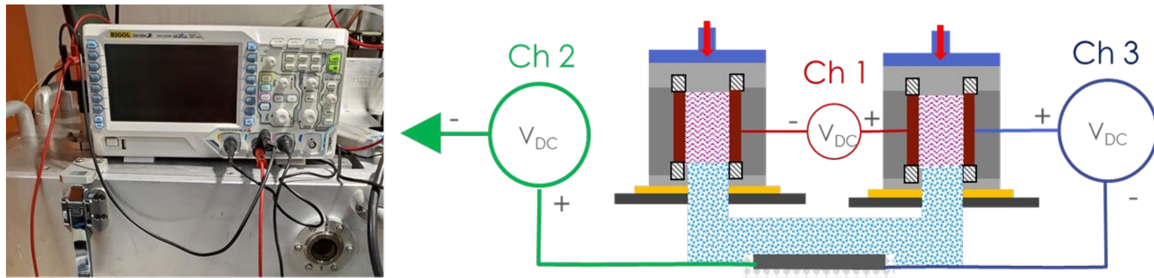


Fig. 18. Setup to measure the substrate bias with an oscilloscope. Channel 3 is the potential between the electrode and the substrate. Channel 1 measures the sputtering voltage and is used to trigger the measurement.

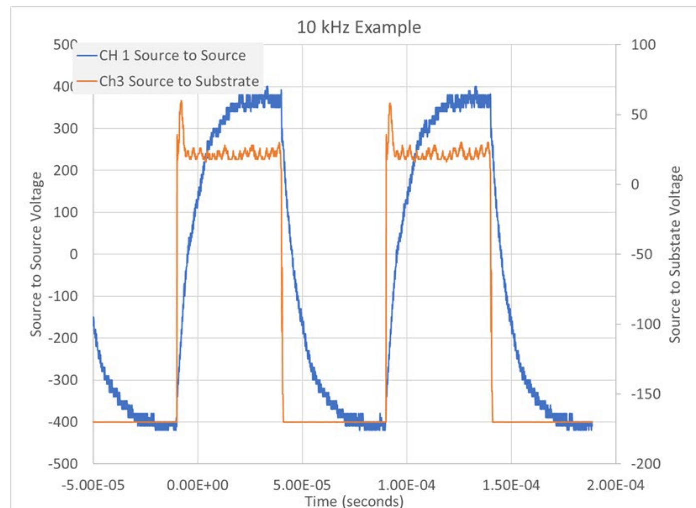


Fig. 19. Time-resolved bias and sputter voltages at 10 kHz pulsing frequency. The spike in the voltage results from the switching of the cathode to the anode. The peak voltage here is 58 V, and the average is 22 V over the pulse length.

The substrate bias's frequency and duration control the amount of ion energy delivered to the substrate. In addition, pressure plays a role in the power delivered

because gas-phase collisions thermalize the argon ions on their path to the substrate. This provides us with two process parameters to control the overall energy delivered to the growing coating: 1) the selected frequency, adjustable from 0 to 100 kHz, and 2) the gas pressure.

We measured the carrier mobility of ITO coatings deposited with different frequencies, pressures, and operating modes. We determined that the mobility could improve remarkably over the non-plasma-immersed substrate carrier. For example,

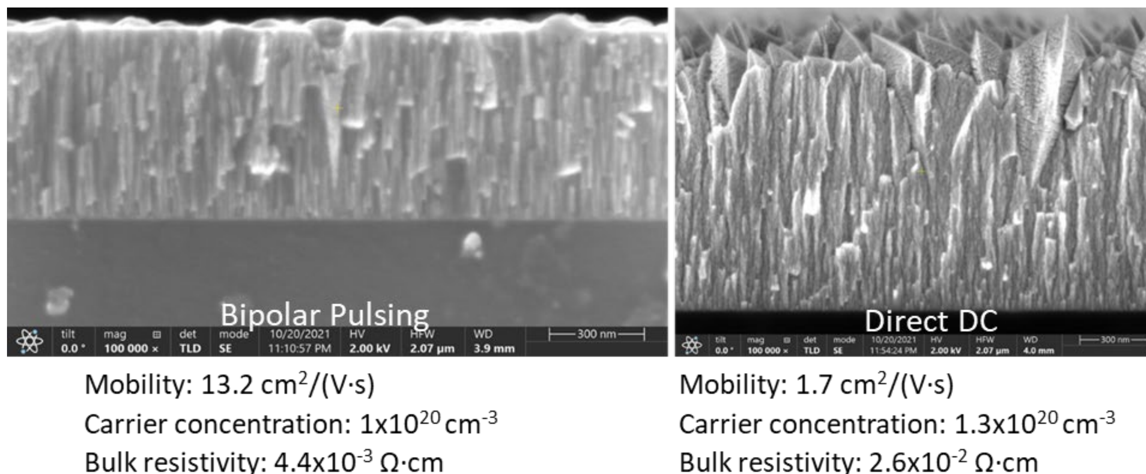


Fig. 20. SEM images and electrical properties of ITO coatings deposited with bipolar pulsing (left) and direct DC (right) modes with a 95/5 ITO target. The depositions were conducted from the same Gen 2 source at similar pressures and at room temperature.

two depositions were conducted at room temperature using the bipolar pulsing and direct DC modes. The bipolar operating frequency was set at 1 kHz, shown below to be a frequency that imparts minimal damage to amorphous silicon (a-Si:H) passivation layers and still retains improved carrier mobility. The direct DC mode also retains good a-Si:H passivation (prior reporting period) but has a carrier mobility of about 8 cm^2/Vs lower than the bipolar mode. As shown in Fig. 20, the coating morphology observed by SEM shows that the bipolar coating has a denser, tighter packed, and larger grain structure than the direct DC coating. This is consistent with the improved energy delivery to the growing coating by the bipolar pulsing and corresponds with a mobility of 13 cm^2/Vs.

Improving the conductivity of the AIDA-deposited TCO material—by maximizing the carrier mobility and tuning the carrier density as needed—is a top priority in this project. As noted above, we improved the carrier mobility of coatings deposited at room temperature to nearly 30 cm^2/Vs by operating the ASU Gen 2 source in the bipolar dual-source configuration. We also demonstrated that even higher mobilities are possible at elevated substrate temperatures. As shown in Fig. 21, operating at a substrate temperature of 180 °C, we have achieved mobilities as high as 50 cm^2/Vs, compared to a maximum value of 9 cm^2/Vs for the direct DC mode. These are excellent mobilities for coatings from 95/5 ITO targets; our next challenge is tuning the carrier density, which is usually achieved by varying the reactive gas (O_2) flow rate. Present coatings have carrier densities of 0.2–1x10^{20} cm^{-3}; this needs to be raised to about 3x10^{20} cm^{-3} to reach the target 70 Ω/sq sheet resistance.

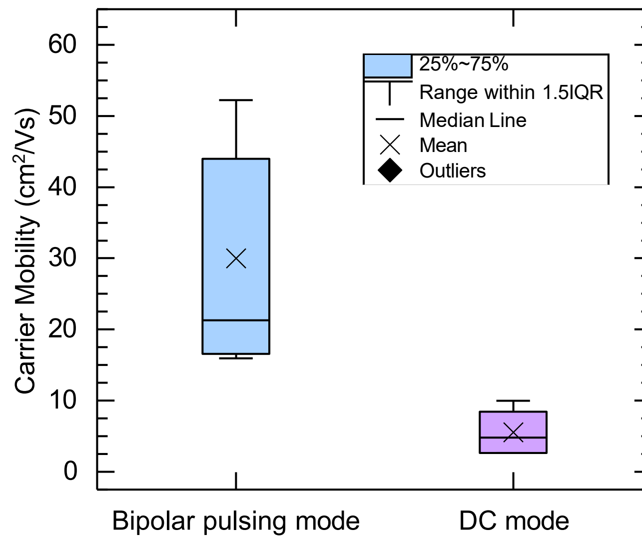


Fig. 21 The carrier mobilities of ITO coatings are deposited in bipolar pulsing and direct DC mode at 180 °C substrate temperature.

The ASU Gen 2 source has been instrumental in testing new configurations and experimental parameters for improving the TCO mobility while ensuring minimal sputtering damage to the SHJ passivation layer. However, we discovered the sputtering source could only run for 10 kWh before it needs to be removed and the dark space shield is cleaned. Thick coatings of ITO build up on the dark space shield and fill in the space between the target and the shield. Once the deposition builds up and gets close enough to the target, it triggers an arcing event. When these arcing events start occurring thousands of times per second, the sputtering plasma is not in a stable equilibrium, and therefore the deposited coating properties and thicknesses are unreliable.

3rd Generation gas-flow sputtering source

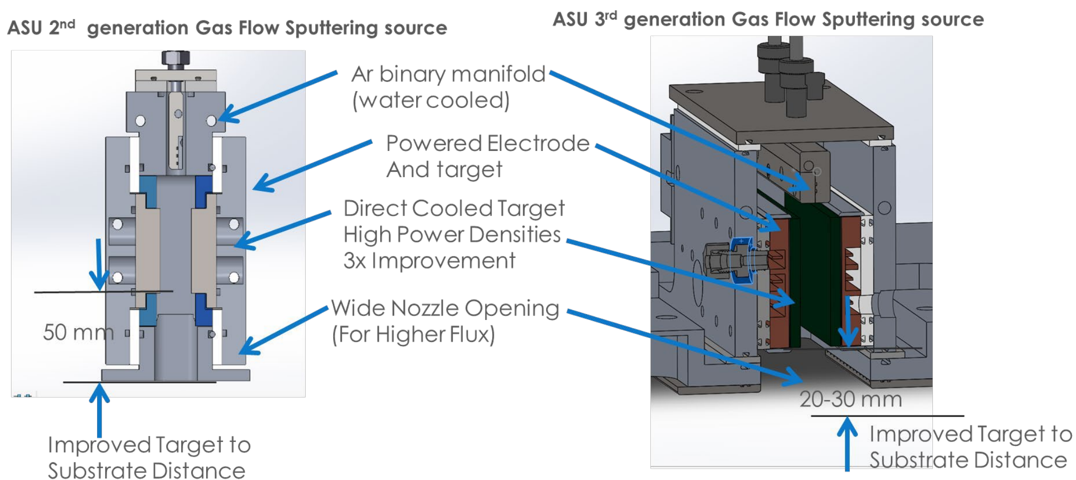


Fig. 22. 3D CAD models of the ASU Gen 2 (left) and Gen 3 (right) gas flow sputtering sources

We solved this problem and other problems by designing the ASU Gen 3 sputtering source. This Gen 3 sputtering source simplifies the Gen 2 design by following simple but essential design principles (Fig. 22). If the part does not need to be fundamentally made of a different material or needs to move, it was combined with a nearby part. This principle has boiled the original Gen 1 gas-flow sputtering design (from a vendor)

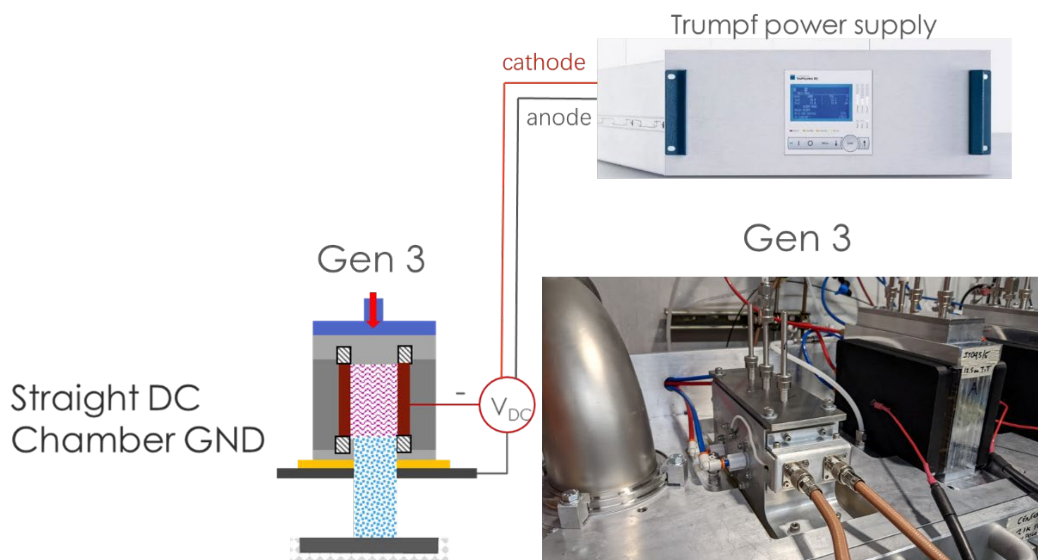


Fig. 23. ASU Gen 3 source configuration and power supply.

from around 100 parts down to just four essential components in the Gen 3 source: the body that holds the targets, the dark-space shield, the sputtering targets, and the Ar binary manifold. This innovative design allows a much closer target-to-substrate distance—down to 25 mm—which we have observed is a crucial parameter for increasing the dynamic deposition rate and the ion bombardment energy to the growing coating to increase the TCO carrier mobility (there is a balance between enough energy to provide adatom mobility, but not so much as to cause passivation damage). The dark-space shields have also been significantly reduced in size to minimize the coating buildup, and the sputtering source can now run over 100 kWh before needing to be serviced; this is 10x longer than the previous Gen 2 source. The Gen 3 source has been tested with ITO sputtering targets. The source runs stably in straight DC mode—with the grounded chamber anode—and in bipolar pulsing mode—where the anode and cathode flip flop between two different gas flow sputtering sources mounted to the chamber. This bipolar pulsing mode—and the operating and physical principles—have been described in detail in previous reports. The main benefit is that the bipolar mode increases the ITO coating conductivity by increasing the adatom mobility during the coating deposition process.

With the new Gen 3 source design, we tested the ITO coating conductivity using the simple straight DC configuration illustrated in Fig. 23. This configuration is interesting because it has the lowest capital cost of the tested configurations. But this configuration has the least plasma immersion for the growing coating and produces a TCO material with lower mobilities than more complex configurations. We designed a two-factor experiment to optimize the TCO coating conductivity by varying the Ar gas

flow and chamber pressure. These two parameters significantly impact the plasma physics and, therefore, the adatom energy delivered to the growing TCO coating. The pressure determines the mean-free path of ions in the plasma, so higher pressures typically provide less ion energy to the growing TCO coating. The Ar gas flow carries sputtered material downstream to the substrate; therefore, the deposition rate is directly related to the Ar gas flow until a high enough gas flow is reached where all the sputtered material is ejected from between the targets. For this system, this occurs at around 6 SLM of Ar gas flow.

Direct DC Design of Experiments

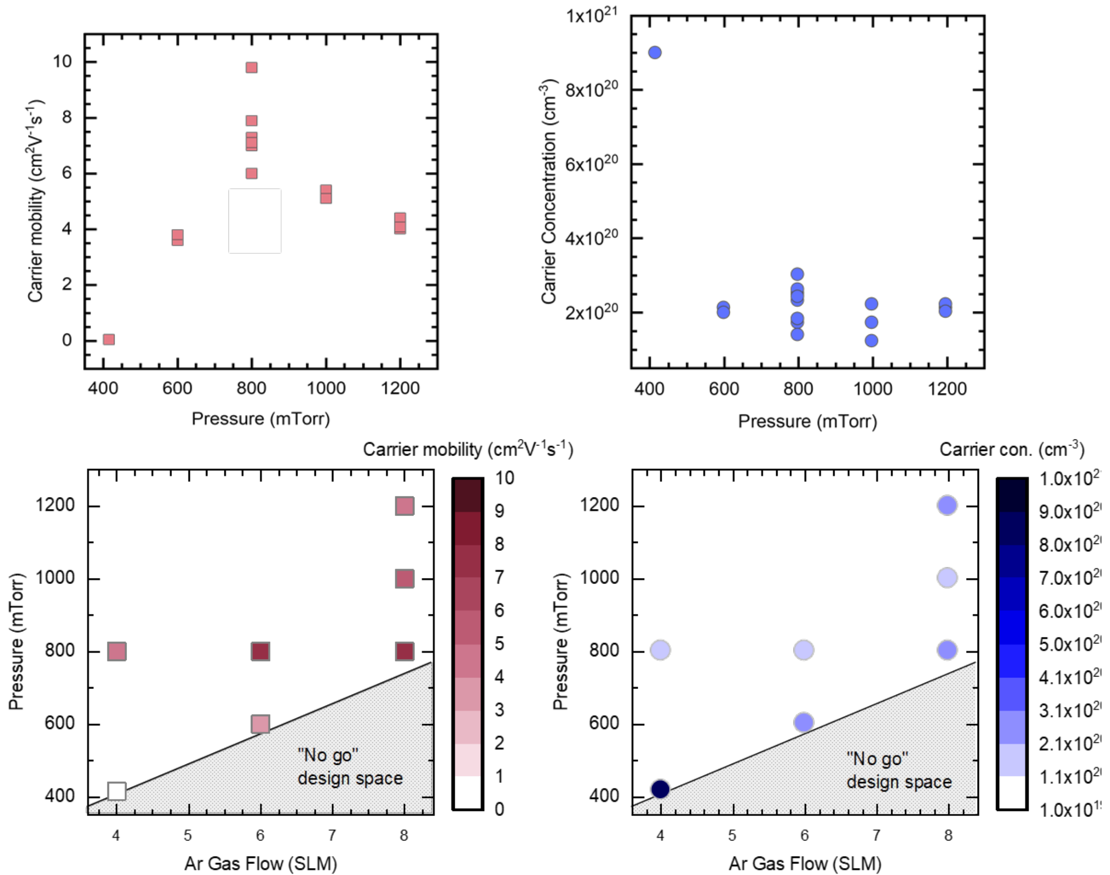


Fig. 24. ASU Gen 3 source ITO coatings on glass. Here the Ar gas flow and pressure deposition parameters are varied while the coating mobility and carrier concentration are measured. The plots on top and bottom represent the same data with different axes to highlight the ITO coating properties.

Fig. 24 shows that the Ar gas flow and chamber pressure statistically significantly affect the carrier concentration and mobility in the ITO coating. The highest mobility ITO coating, with 10 cm^2/Vs, was made at 800 mTorr with a gas flow of 6 SLM. These coatings were made on glass without adding oxygen, and both 2.5" x 5" targets received 2 kW of power total. Although the carrier concentration is oddly low without adding any oxygen during the process for sputtered ITO, DC magnetron sputtered ITO can reach nearly 10^{21} cm^{-3} carrier concentration without adding any oxygen. The

low carrier concentration is repeatable for gas-flow sputtering. We suspect this is attributed to high deposition pressures—nearly two orders of magnitude higher than the standard magnetron sputtering processes. After finding the optimum coating mobility in the straight DC mode without oxygen, we added oxygen to try and improve the coating properties, as is commonly done in DC magnetron sputtering. But unfortunately, as shown in Fig. 25, adding 0.025% oxygen (1.5 sccm) only decreases the carrier concentration while minimally increasing the mobility. This increases coating resistivity with more oxygen flow, especially when too much oxygen is added to the coating. To see how other pressures and Ar gas flow conditions are affected by additional oxygen added during the sputtering process, we selected an attractive extreme condition: the 4 SLM and 400 mTorr case. We swept two parameters, the oxygen gas flow and pressure, to find the most conductive coating properties with these two fixed parameters. Fig. 26 shows the most conducive coatings made at 400 Torr with 5 sccm of oxygen. This resulted in a coating bulk resistivity of $6x10^{-3}$ ohm-cm, which is one order of magnitude higher than the resistivity goal set for this project, $5x10^{-4}$ ohm-cm.

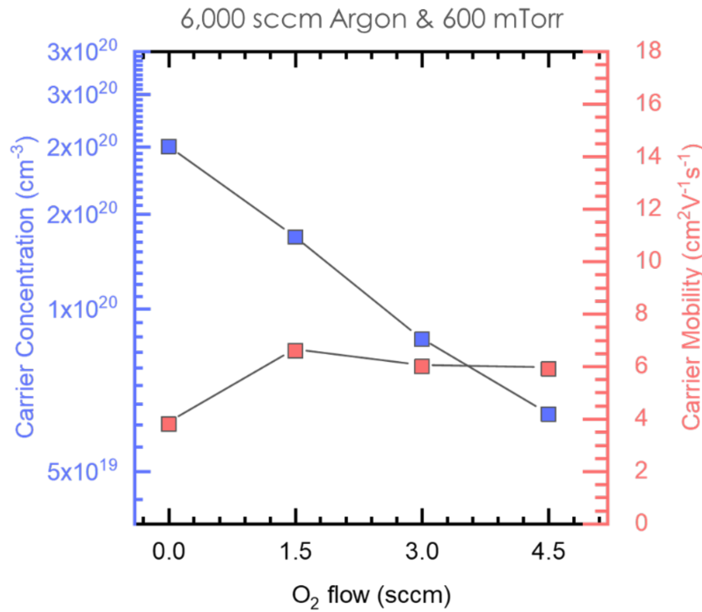


Fig. 25. ASU Gen 3 source ITO coatings on glass. This shows that even a tiny amount of oxygen significantly affects the electrical properties of the TCO coating.

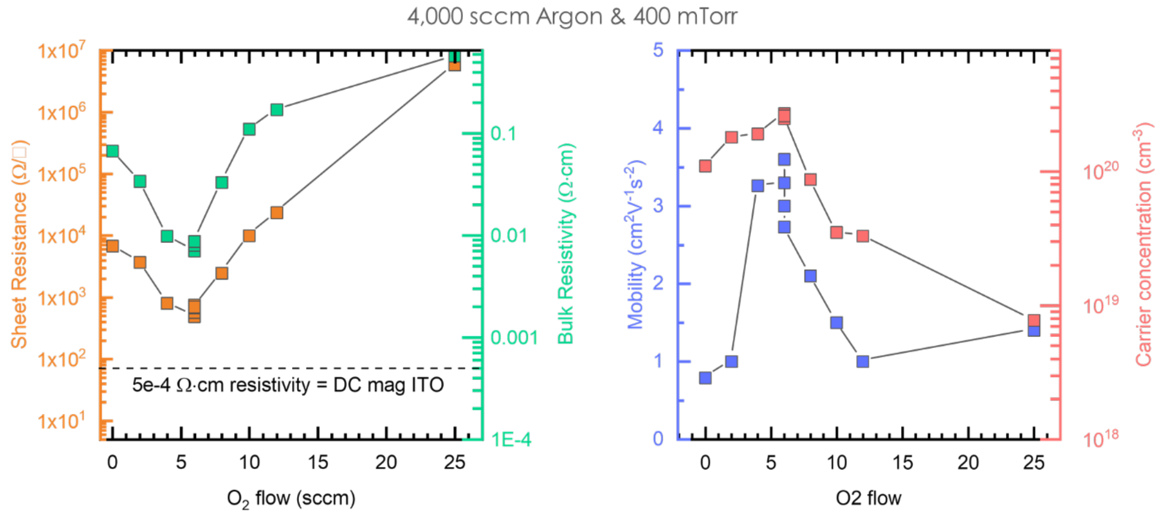


Fig. 26. ASU Gen 3 source ITO coatings on glass. Electrical properties of coatings deposited at 400 mTorr and 4 SLM of Ar are improved with 5 sccm of oxygen added during the deposition; then, the coatings become more resistive with additional oxygen.

<u>Bipolar Pulsing: Repeatability and further conductivity improvements</u>

Previously, we found that, with the Gen 2 source, replicate samples had a considerable variation from run to run. This makes it challenging to understand minor differences in the coating's electrical performance and capability. Conversely, we found that, as illustrated in Fig. 27, operating the Gen 3 source in bipolar pulsing mode produced very repeatable results, which we attribute primarily to the hardware improvements. We tested different operating parameters to find the most conductive ITO coatings deposited in this bipolar mode. Running the source at 615 mTorr with 7 SLM of Ar gas flow produced a mobility of 15 cm^2/Vs with 0.45 sccm of oxygen gas flow (Fig. 27). For this higher-mobility sample, the carrier concentration was $7x10^{19}$ cm^{-3} which is too low to achieve the project bulk resistivity goal of $5x10^{-4}$ ohm-cm (but is excellent for some applications).

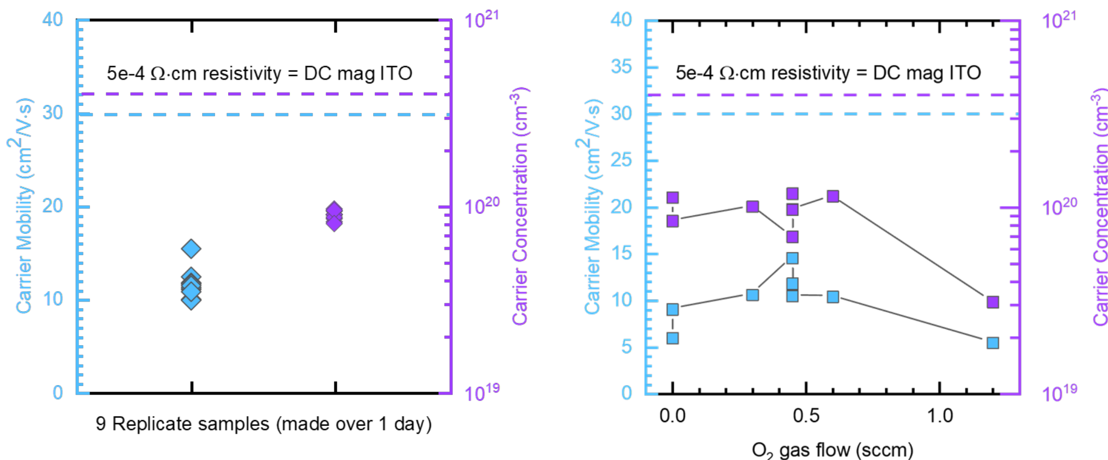


Fig. 27. The electrical properties of ITO coatings on glass were deposited at 615 mTorr and 7 SLM of Ar using the bipolar pulsing mode. (Left) these are replicate samples made without adding oxygen during the deposition. (Right) varying oxygen gas flow to improve the conductivity of the coating.

We concluded that bipolar pulsing does have a significant impact on raising the carrier mobility compared to the straight DC mode. However, the mobility is still not over the target of 30 cm^2/Vs. This cannot be compensated by increasing the carrier concentration without negatively impacting the short-circuit current of the cell because of the strong dependence of IR parasitic absorption on mobility.

To further increase the plasma emersion of the growing coatings, RF bias was added to the substrate stage. This bias ignites a plasma around the substrate stage and further increases the plasma density around the substrate. This plasma drives the stage to a negative potential due to its self-bias, as it collects more negatively charged electrons. This negatively charged plasma sheath around the substrate draws in Ar ions. It gently accelerates them towards the coating, increasing the ion flux and delivering more energy to the growing layer. Fig. 28 shows the results of an experiment where different RF bias powers were used (from 0 to 50 watts) to see their impact on the electrical properties of gas-flow sputtered ITO coatings. The carrier mobility and concentration are considerably higher for samples made with 50 watts of RF power. We also see an interesting case for the sample marked by the golden outlined symbols, which was made using double the amount of oxygen flow (0.4 sccm). This significantly increased the carrier mobility to gas-flow achieving our goal of 30 cm^2/Vs. However, this negatively impacted the carrier concentration and resulted in a bulk resistivity of $3.6 x 10^{-3}$ ohm-cm.

We also investigated sputter damage of this process. Silicon heterojunction (SHJ) solar cell precursors (i/n and i/p layers on a texture wafer) were prepared with industry-standard layer thicknesses of amorphous silicon. The samples were coated in ITO from the gas-flow sputtering source with different RF bias powers applied. With the greater substrate plasma immersion from the RF power, we checked the amount of sputtering damage, which is observed as an iV_{oc} drop. As shown in Fig. 28, even the highest power—50 watts—does not induce significant and unacceptable amounts of sputtering damage noted by the grey region labeled "DC rotary magnetron sputtering."

Note that these measurements were taken immediately after deposition and with no annealing of the samples.

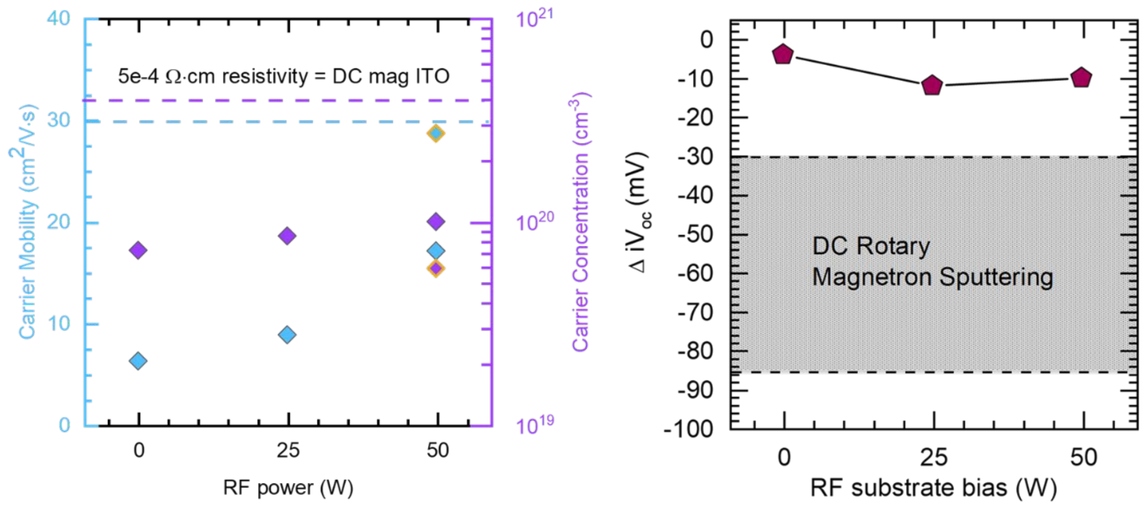


Fig. 28. Electrical properties of ITO coatings with RF bias applied to the substrate stage (0 to 50 watts) (left) and quantified sputtering damage on an SHJ cell precursor (right).

ITO coating electrical stability improvements

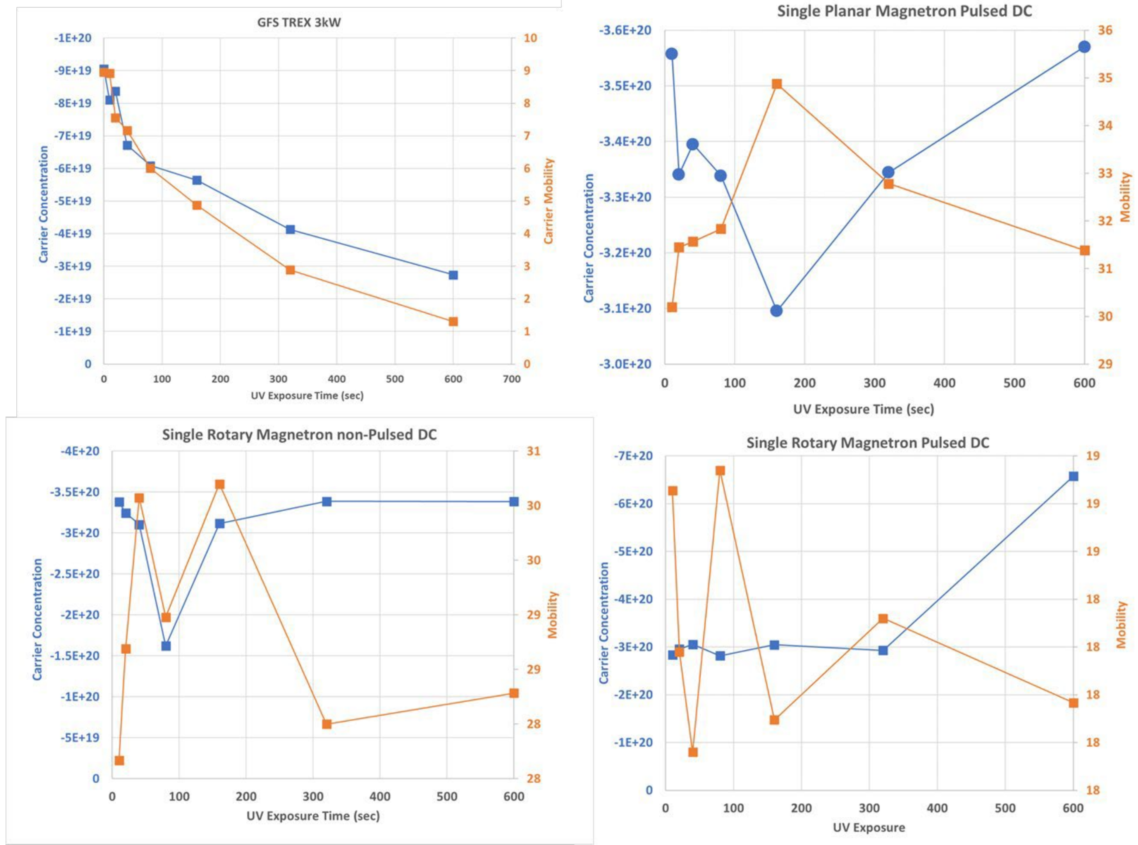


Fig. 29. ASU Gen 3 source ITO coatings on glass and various industry-standard ITO sputtering techniques exposed to an accelerated aging UV-ozone test.

An unexpected phenomenon we identified with many of our gas-flow sputtered ITO samples is that the resistivity rises over time (by as much as orders of magnitude) when exposed to the atmosphere. This is not observed when coatings are stored in a dry nitrogen atmosphere, suggesting that the oxygen or water content in the atmosphere is responsible for increasing the coating bulk resistivity. As this often takes days of atmosphere exposure to discover how much the coating conductivity degrades, we introduced an accelerated way to test the degradation mechanism by exposing the sample to a UV-ozone treatment. Fig. 29 shows the results of exposing samples of gas-flow sputtered ITO, and single planar magnetron sputtered ITO, single rotary magnetron sputtered ITO, and single rotary magnetron DC pulsed ITO. The UV-ozone treatment minimally affected the three industry-standard sputtered ITO samples, the gas-flow sputtered sample's carrier mobility and carrier concentration significantly decreased after 600 seconds of UV-ozone treatment in a higher bulk resistivity.

We discovered that depositing gas-flow sputtered ITO at 200 °C significantly improves the stability of the coatings when exposed to air and the UZ-ozone environment. Fig. 30 shows that, even after 300 seconds of treatment and three weeks of exposure to the atmosphere, the electrical properties vary very little.

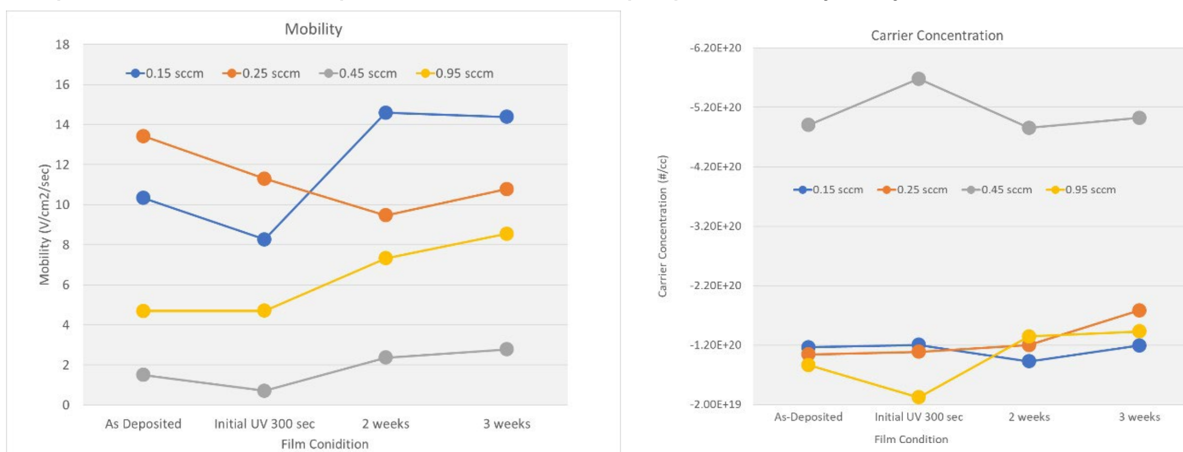


Fig. 30. ASU Gen 3 source ITO coatings on glass exposed to an accelerated aging test and then left in atmosphere for 3 weeks to determine ITO coating electrical stability.

From the experiments described above, the most conductive TCO coating made so far was reported in Fig. 28 (left) with 50 watts of RF power applied to the substrate. This resulted in a coating thickness of 100 nm and sheet resistance (R_{sh}) of 240 Ω/sq with a bulk resistivity of 3×10^{-3} Ωcm, which is six times higher than this milestone M1.2.1 (5×10^{-4} Ωcm). The deposition parameters include a total gas flow of 10 SLM Ar in bipolar mode with an operating pressure of 895 mTorr. 0.2 sccm of oxygen gas was flown through binary manifolds below the sputtering sources with a 15 mm gap between the targets.

AIDA-deposited passivation layer

Our system can also be configured to deposit SiOx as passivation layers. In this configuration, the AIDA deposition tool equipped with a dusty PECVD source, a

medium-pressure synthesis chamber (~10 Torr) is mounted on top of a low-pressure deposition chamber (~1 Torr) separated by a linear slit nozzle. Silane, helium, and air mixtures flow into the top chamber where a non-thermal plasma is ignited between two parallel plate electrodes, nucleating silica nanoparticles. This aerosol of silica and gas accelerates through the linear nozzle into the lower deposition chamber where the material impacts and adheres to the silicon substrate.

We found that the film porosity is very sensitive to the humidity of the airflow. Fig 31 shows the silica film porosity—obtained through ellipsometry using an effective medium approximation (EMA) model—as a function of humid airflow. It indicates that the silica film becomes less porous as more humid air is injected into the synthesis chamber. Under certain conditions, the silica film is as dense as 97% of bulk SiO_2 material. Compared to more porous films, the dense silica film exhibits a highly smooth surface—zero surface roughness indicated by the ellipsometry model. We felt that this dense, smooth silica film should be as good a material to provide surface passivation as thermally-grown oxides or wet-chemical oxides that are used in high-efficiency crystalline silicon (c-Si) solar cells. We thus decided to investigate these films as our first candidates for passivation layers.

We also deposited the 97% dense silica film over a 4" wafer with a nominal thickness of 4 nm, and measured 111 points across the wafer with our JA Woollam M-2000 ellipsometer equipped with a mapping stage. The result, in Fig. 31, shows that the film thickness varies between 3.6 and 4.1 nm, and the non-uniformity is less than 5%, which completes the milestone.

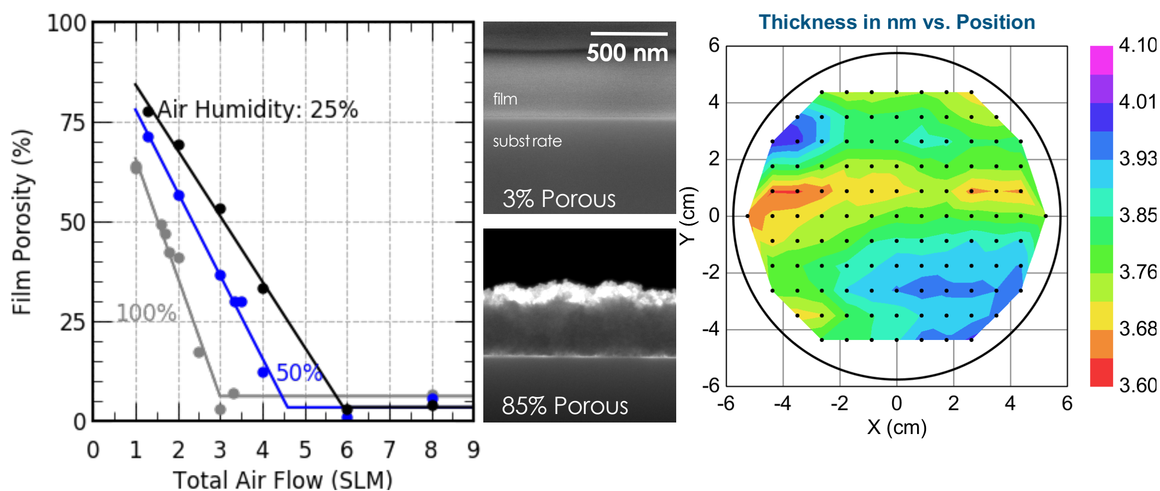


Fig. 31 Silica film porosity as a function humid air flow (left), cross-sectional SEM images of silica films with 3% and 85% porosity (middle), and thickness map of a 4-nm-thick silica passivation film over (right).

We further investigated the passivation quality of the aforementioned dense silica (SiO_x) material by depositing these films onto textured silicon wafers and measuring the effective minority carrier lifetime using a Sinton WCT-120 lifetime tester.

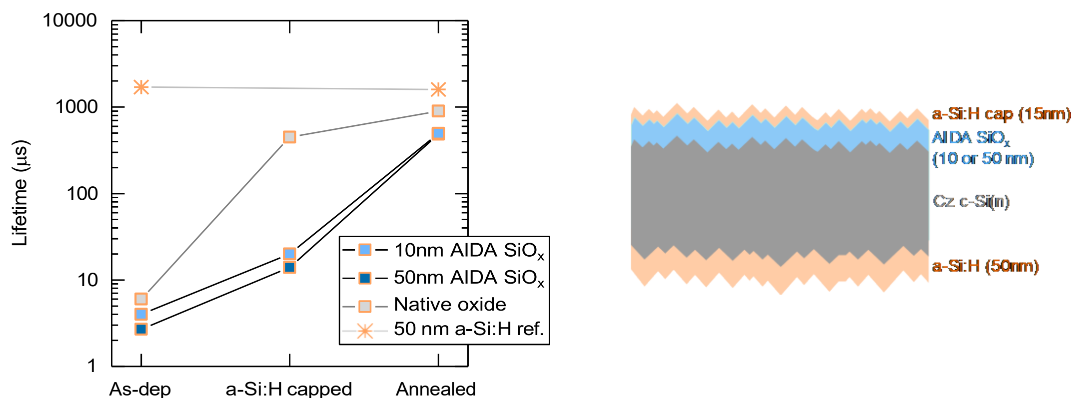


Fig. 32 Effective carrier lifetimes of lifetime samples after each process step (left). Schematic of the lifetime samples used in this experiment (right). The reference sample has 50 nm of a-Si:H on both sides, and the 'Native oxide' sample has a native oxide instead of AIDA-deposited SiO_x.

In our first experiment, shown in Fig. 32, all samples were passivated on the rear side with 50 nm of intrinsic amorphous silicon (a-Si:H) deposited with a conventional PECVD process. This prevents recombination on the rear side from limiting the overall passivation performance of the cell precursor. A reference sample was made by depositing 50 nm of a-Si:H on both sides of the silicon wafer. Another control sample was made with the same a-Si:H rear passivation, but the front side was left in the ambient atmosphere to grow a native oxide before being capped by 15 nm of a-Si:H. Two different test sample types were made, with either 10 nm or 50 nm of SiO_x deposited by AIDA, and then capped with 15 nm of a-Si:H by PECVD. After capping, the samples were annealed on a hotplate in the ambient atmosphere at 250 ºC for 10 minutes. After each step, the effective minority carrier lifetime (at an injection level of 10^{15} cm^{-3}) was measured. This gives us an insight into how the previous step may have affected the chemical passivation at the surface. As shown in Fig. 32, all samples with SiO_x have very low minority carrier lifetimes (< 10 µs) as deposited. This is observed in other silicon oxide growth techniques as well. After depositing the 15-nm-thick a-Si:H capping layer, interestingly, the sample with a native oxide gains a significant increase and approaches 500 µs lifetime, whereas the samples with AIDA SiO_x received a negligible lifetime boost. This indicates that the thin and poor-quality native oxide may have been etched during PECVD or transformed into a sub-stoichiometric hydrogenated amorphous silicon oxide, a-SiO_x:H where x~1.5, as reported by Liu *et al.* The AIDA-deposited SiO_x appears to be unchanged by PECVD process at these thicknesses [13]. After annealing the samples, an appreciable increase in lifetimes was observed across the board. Compared to the a-Si:H reference sample of 1 ms lifetime, the AIDA-SiO_x samples reached 0.5 ms, corresponding to an implied open-circuit voltage (iV_{oc}) of 677 mV. This can be attributed to hydrogen diffusing from the a-Si:H layer to the c-Si/SiO_x interface, increasing the chemical passivation and thus the minority carrier lifetimes. A key

takeaway is that the AIDA SiO_x can be as thin as 10 nm and still have similar passivation performance to thicker AIDA SiO_x layers.

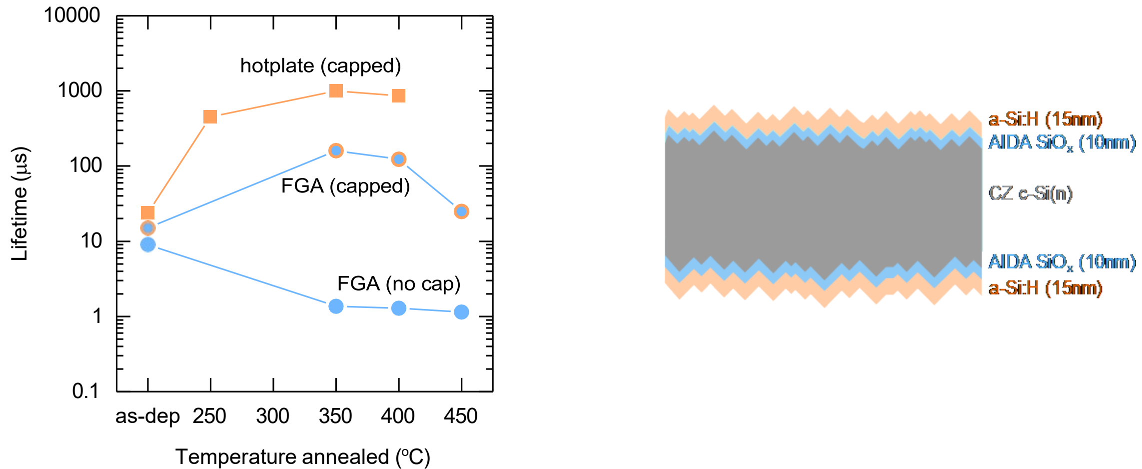


Fig. 33 Effective minority carrier lifetimes of lifetime samples that underwent different annealing conditions and temperatures (left). Schematic of the lifetime samples (right). Some samples (labeled “no cap”) were annealed without the 15-nm-thick a-Si:H capping layer.

In a follow-up experiment, shown in Fig. 33, the second set of samples were symmetrically passivated with 10 nm of AIDA SiO_x and some were then capped with 15 nm of a-Si:H, again deposited by PECVD. (Note that these a-Si:H layers can later be deposited by AIDA if desired, but we're focused on understanding the passivation potential of the SiO_x layers at the moment and, based on previous work, knew that we would need to hydrogenate them.) All samples were annealed at the designated temperature for 10 minutes, and their lifetime was measured. Fig. 33 shows the effective minority carrier lifetimes as a function of annealing time and ambient. Similar to the previous experiment, the as-deposited minority carrier lifetimes are very low (~10 µs). After annealing, the sample with the greatest increase in lifetime are the ones that received capping layers and were annealed on a hotplate in an ambient atmosphere. When annealed at 350 ºC, the lifetime is above 1 ms with an iV_{oc} of 695 mV. This is the highest minority carrier lifetime we have achieved so far with AIDA SiO_x and is approaching many state-of-the-art reports in the literature. This is attributed to hydrogen diffusing to the c-Si/SiO_x interface, enhancing the chemical passivation. Samples capped with a-Si:H were also annealed in a rapid thermal annealing (RTA) furnace under a forming gas atmosphere. This step, known as a forming gas anneal (FGA), uses a gas mixture of 5% H_2 in N_2. This was anticipated to create a hydrogen overpressure and diffuse even more hydrogen atoms to the c-Si/SiO_x interface, further increasing the chemical passivation. The FGA treatment increased the lifetime to about 100 µs on the samples capped with a-Si:H. However, for the uncapped samples, the lifetimes were degraded to about 1 µs after the FGA. These interesting results were unexpected and contrast findings by Mazzeralla *et al.* (no known relation to the cheese). Mazzeralla *et al*. deposited SiO_x by PECVD and performed similar capping and annealing procedures in a forming gas atmosphere. They found that an FGA treatment improves minority carrier lifetimes regardless of

whether the sample is capped with a-Si:H or not [14]. They achieved an effective minority carrier lifetime of 1.6 ms and an iV_{oc} of 686 mV. One explanation may be that PECVD SiO_x and AIDA SiO_x have different bonding, structures, or stoichiometries. This could cause them to react differently to the energetic reducing environment supplied by the forming gas at elevated temperatures. We did FTIR (not shown here) on similar dense AIDA SiOx films and found prominent Si-OH vibrational modes. These silanol bonds are not found in silicon oxide grown thermally or by chemical oxidation and could be responsible for the different results seen in the FGA experiment.

High-resolution transmission electron microscopy (TEM) was performed on a 120-nm-thick AIDA SiO_x layer deposited on an HF-cleaned silicon wafer. The cross-section sample was prepared using a FIB lamella lift-out technique, attached to a copper grid, and thinned to electron transparency for imaging. Fig. 34 is an overview of the sample and shows the film is very dense with no voids or gaps through the entire AIDA SiO_x layer. It also confirms that these dense AIDA SiO_x coatings have very low surface roughness—in agreement with zero surface roughness as measured by ellipsometry. A magnified view of the c-Si/SiOx interface shows some crystalline defects but, encouragingly, is free of voids or gaps. Also, there are no clear crystallinity in the AIDA SiO_x coating, and the coating appears to be completely amorphous. We will, in future quarters, image much thinner SiO_x layers, including those capped with a-Si:H. We will also begin contact resistivity measurements after adding a doped layer on top of thin SiO_x layers.

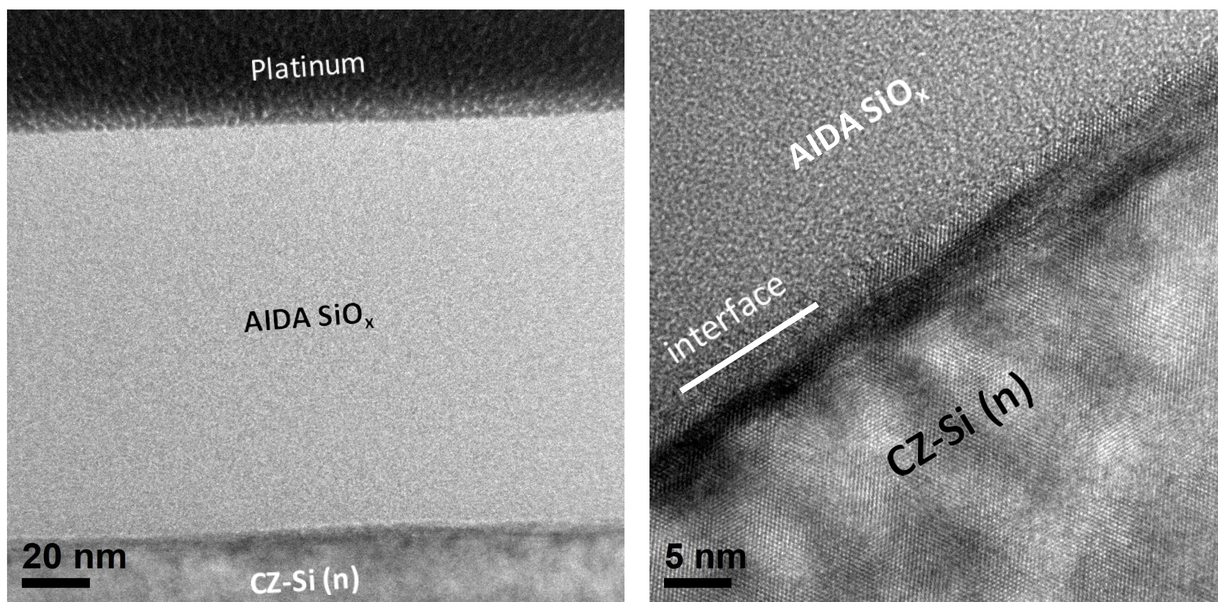


Fig. 34 High-resolution transmission electron microscopy cross section of an as-deposited AIDA SiO_x layer with a thickness of approximately 120 nm. The platinum cap is a protection layer deposited during the TEM sample preparation process.

Task 2: Demonstrate AIDA-deposited silicon heterojunction cells on 4-cm^2 devices

Silicon cells with AIDA-deposited transparent conductive oxide layer

While optimizing the AIDA-TCO process, we also integrated it into our baseline silicon heterojunction cells by replacing the magnetron-sputtered front ITO with gas-flow-sputtered ITO. In this experiment, the front ITO layer was deposited using the SMI gas-flow sputtering source with 200 °C substrate temperature, 5 SLM argon gas flow, 600 mTorr pressure, and 0.45 sccm oxygen. We also investigated the effects of annealing ambient.

The most encouraging discovery from this experiment is the cells with gas-flow-sputtered ITO has a Voc of 706 mV, 10 mV higher than the baseline cells with magnetron-sputtered ITO. This demonstrates the advantage of using this low-damage sputtering process for silicon heterojunction cells. Fig. 35 shows the device results. The ITO deposited here is still plagued by the conductivity issues described

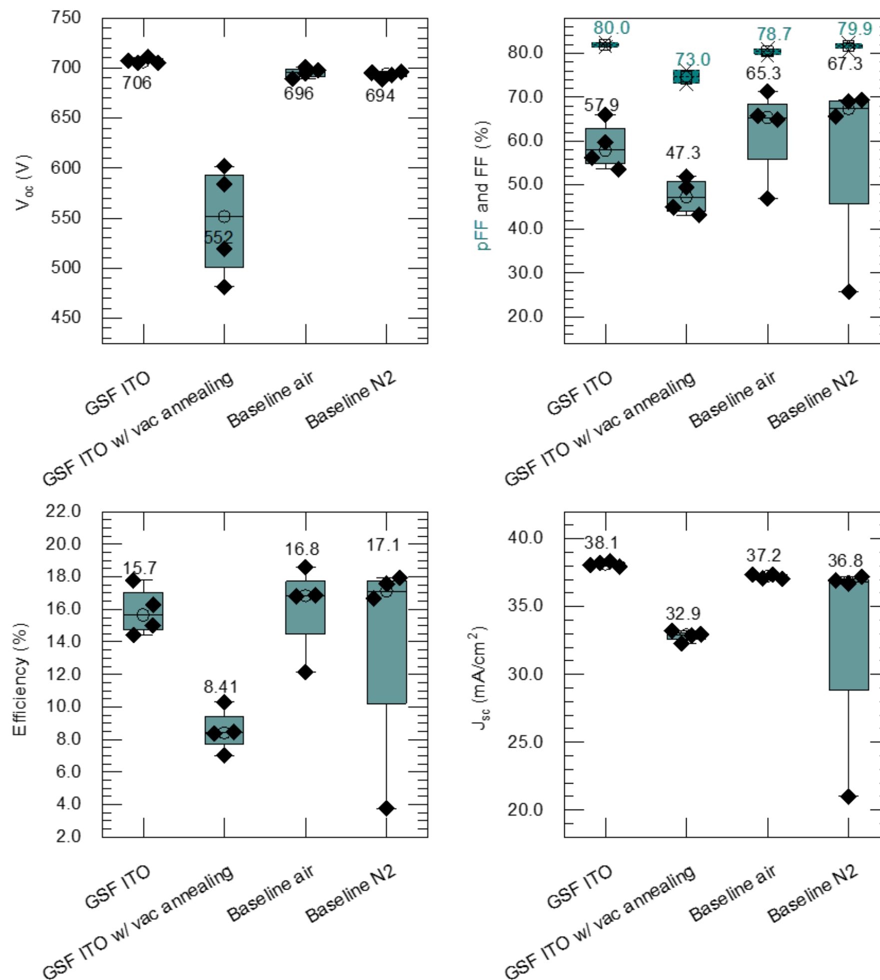


Fig. 35 Current-voltage characteristics of silicon heterojunction cells with gas-flow-sputtered ITO and magnetron-sputtered ITO.

previously, and it has sheet resistance greater than 300 ohms/sq. Given the finger

spacing of 2.2 mm, this large sheet resistance results in poor FF (< 60%), much lower than the baseline device. Note that the FF of the baseline cells was lower than normal (> 75%), resulting from bad printing in this batch. We also conducted another batch of cells and re-designed the finger spacing reduced to 1.1 mm. We achieved the best efficiency of 19%, with FF of 70%. Once the conductivity of the TCO is improved, this will be the key enabler for making more efficient silicon solar cells than can be made with traditional magnetron sputtering.

We continued progressing the mobility, carrier density, and stability of gas-flow sputtered ITO films with Gen 3 source, though the best resistivity remains slightly higher than the target value. Nevertheless, we made SHJ solar cells with the front and back TCO layers deposited by gas-flow sputtering to see how the cells' performance was impacted. For this batch of cells, we used the most conductive recipe so far, with a bulk resistivity of 2×10^{-3} Ohm-cm. The experiment included a batch of control cells with standard DC magnetron sputtered ITO on the front and back of the device. A second group had gas-flow sputtered (GFS) ITO on the front and back of the device with no DC sputtering, and a third group had the front side of the device coated with DC magnetron sputtered ITO and the backside of the device coated with GFS ITO.

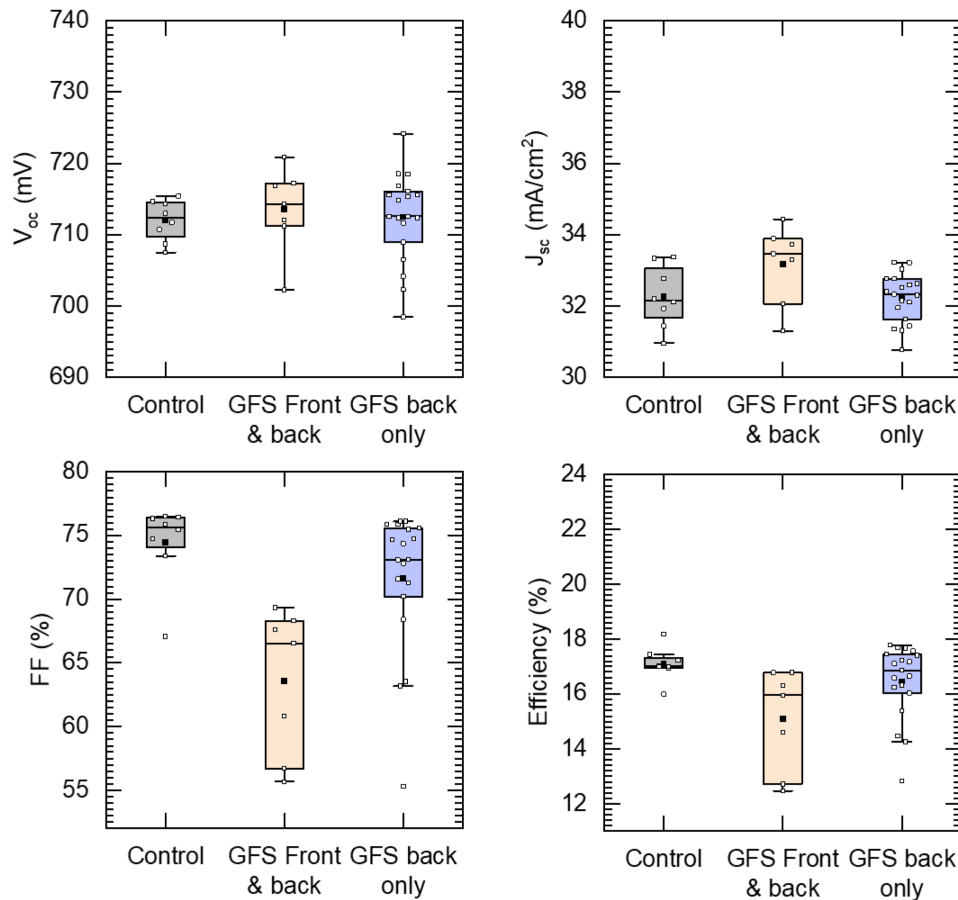


Fig. 36. ASU Gen 3 source ITO coatings used in SHJ solar cells with performance that rivals the batch of control SHJ cells (plotted on the left side).

This last configuration is exciting because the device's rear side can be much more resistive—and often is made on purpose by adding extra oxygen to lower the carrier

concentration—to decrease the parasitic absorption in the layer and improve the device J_{sc}. Therefore, the GFS ITO is a realistic and suitable candidate for replacing the rear layer without significant loss of device performance.

Fig. 36 shows that the batch that received the GFS sputtered ITO had comparable V_{oc} to the control samples, though the variation is higher. The J_{sc} of all devices is also similar. Still, the batch with GFS ITO on the front is slightly higher because of the reduced parasitic absorption stemming from the lower carrier concentration in the front TCO coating. All J_{sc} values are also artificially lower than their actual values due to the shading of the contact busbar during the measurement process. The FF of the samples with GFS ITO on the front side suffers from the higher cell sheet resistance of that layer, but the batch of samples with GFS ITO only on the back side rival those of the control samples. This results in the batch of solar cells with GFS ITO only on the rear side having efficiencies as high as the control samples. This demonstrates that GFS ITO can be incorporated into an SHJ cell structure and still perform as well as the current state-of-the-art SHJ cell manufacturing methods. Although the overall efficiencies are not high, due in part to the artificially low J_{sc} from the measurement technique, this result shows that there is a realistic pathway to substantially decrease the CapEx of ITO sputtering (by switching to rough-vacuum-only AIDA tools) if we can further increase the mobility and carrier densities of the films.

Silicon cells with AIDA-deposited passivation layer

Initial attempts using a double-side TOPCon structure with TCO

Envisioning the use of AIDA SiO_x as a tunnel oxide, we further reduce the oxide thickness and check its passivation quality in conjunction with polysilicon contact. In this experiment, after depositing AIDA SiO_x with thicknesses of 1.5 nm, 4 nm, and 6 nm on textured n-type CZ wafers, we used PECVD to deposit 50-nm-thick a-Si:H and then annealed the samples at 850 °C for 30 minutes to crystallize the a-Si:H into polysilicon. For n-type polysilicon, the lifetime of such a cell precursor, as shown in Fig. 37, achieved 2.6 ms for the sample coated with 1.5 nm-nm-thick SiO_x. This further demonstrates that AIDA-SiO_x has excellent surface passivation quality and is on par with (if not excel) the state-of-the-art. We also conducted the experiment with p-type polysilicon. However, the lifetime was in microseconds range. This is due to the poor quality of p-type polysilicon in particular the boron doping which can create defects within the SiO_x.

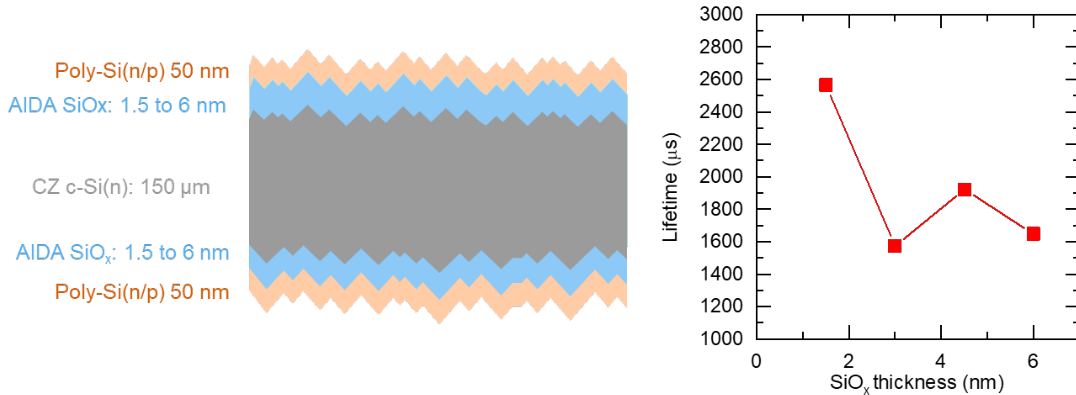


Fig. 36. A schematic of the lifetime test structure (left), and effective minority carrier lifetime as a function of SiO_x thickness (right).

Since AIDA-deposited SiO_x has fulfilled the passivation requirement, we then probed the contact resistivity when it is used in conjunction with poly-Si contacts. To do that, we performed transfer length measurements (TLM) to determine the contact resistivity for a series of SiO_x thicknesses with either n- or p-type polysilicon. The TLM test structure is shown in Fig. 38, we first symmetrically passivated the silicon wafer with either 1.5 or 3 nm silica, and then deposited 50-nm-thick n- or p-type hydrogenated a-Si:H using PECVD and subsequently annealed the samples at 850 ˚C in a tube furnace for 30 minutes. We then sputtered 70-nm-thick ITO and 200-nm-thick silver through a shadow mask that defines the TLM pads. TLM measurements were measured with four probes by setting the current and measuring resistance.

As shown in Fig. 38, for samples with n-type polysilicon, the whole-stack contact resistivity increases with SiO_x thickness which is similar to other reports that studied TOPCon and POLO contacts [11, 15-16]. However, unlike previous reports, the contact is still quite conductive even when the SiO_x thickness is 3 nm, which is beyond the thickness limit that electron tunneling can happen. Indeed, even for a 6 nm SiO_x layer the contact resistivity is about 0.04 $\Omega\cdot cm^2$, which would result a calculated fill factor (FF) loss of only 0.21%. All these resistivity number are well below 0.1 $\Omega\cdot cm^2$, which is the best contact resistivity that a-Si:H contacts have been reported to achieve (0.5% FF loss). In a similar manner, the contact resistivity for contacts with p-type polysilicon is also about 0.03 $\Omega\cdot cm^2$ for a SiO_x thickness of 1.5 nm. However, for thicknesses greater than 1.5 nm we were unable to obtain an accurate contact resistivity measurement for reasons that are still unclear and need further investigation. As the project progressed, we recognized that the current path in the TLM structures was likely traveling from the electrode through the sheet of the poly-Si and not through the full contact stack leading to the low contact resistivity.

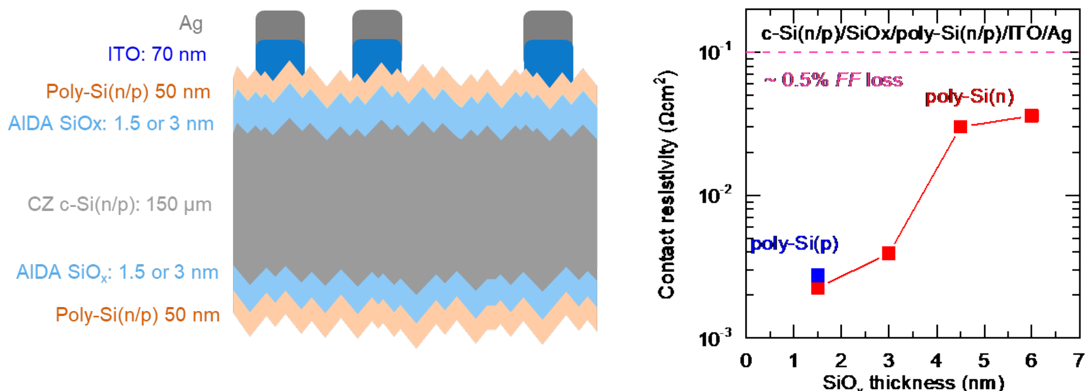


Fig. 38. A schematic of the TLM structure used to probe the whole-stack contact resistivity (left), and contact resistivity as a function of silica thickness (right).

Given the promising passivation and contact resistivity of the poly-Si/AIDA-SiO_x stack, we attempted fabrication of a TOPCon-like solar cell, as shown in Figure 39. We used double side-textured, n-type silicon wafers and deposited either 1.5 or 3 nm SiO_x. The wafers were then deposited with 50-nm-thick n- and p-type a-Si:H layers on the front and back side, respectively, and then annealed in a tube furnace at the condition mentioned before. The front side was sputtered with 70-nm-thick ITO (not typical for a TOPCon cell—but the front metallization for such cells is still being researched by the community), whereas the rear side was sputtered with 150-nm-thick ITO and 200-nm-thick silver. The cell was then screen printed with metal grids using low-temperature paste on the front side, and finished with a hot-plate annealing at 200 °C for 20 min. The sputter mask has 2 cm × 2 cm openings that define the cell area. In essence, these cells resemble a standard silicon heterojunction solar cell with all the hydrogenated amorphous silicon contacts are replaced by our AIDA-deposited SiO_x passivation layer and a polysilicon carrier-selective layer.

Fig. 39 also shows the current-voltage characteristics of these cells as a function of SiO_x thickness. We achieved 16% cell efficiency on the first try of making these TOPCon solar cells. The J_{sc} is below 34 mA/cm^2, which is due to the parasitic absorption from the non-optimized 50-nm-thick polysilicon layer. The V_{oc} of our TOPCon-like devices are consistently low, around 600 mV for all SiO_x thicknesses. Given the relatively high and constant implied V_{oc} of 640 mV V_{oc} after poly-Si crystallization (before sputtering), there are two possible explanations for the low V_{oc} of these devices: either the contacts are not selective towards their respective carrier types or there is damage to the contact induced by the sputtering of the ITO layers that is not recovered during the annealing of the silver paste. The first case seems unlikely as the polysilicon contacts are heavily doped and thus they should allow for a high selectivity. The second case appears much more likely as sputter damage will reduce the iV_{oc} of the device, thus limiting the maximum V_{oc} that can be extracted. We also performed external radiative efficiency measurement on these finished cells (not shown), and confirmed it is due to sputter damage, as the iV_{oc} on the finished cells are about the same as the V_{oc}. While SHJ devices also receive some sputter damage, the damaged layers recover after the annealing of the silver paste due to the movement of hydrogen from the hydrogenated amorphous silicon throughout the contact. Our TOPCon-like devices lack this hydrogen reservoir and thus there is no

way to recover from the sputter damage. The gap between implied FF and pseudo FF also indicates damage during the sputtering process. All these motivate us to integrate the damage-free AIDA-ITO into this solar cell.

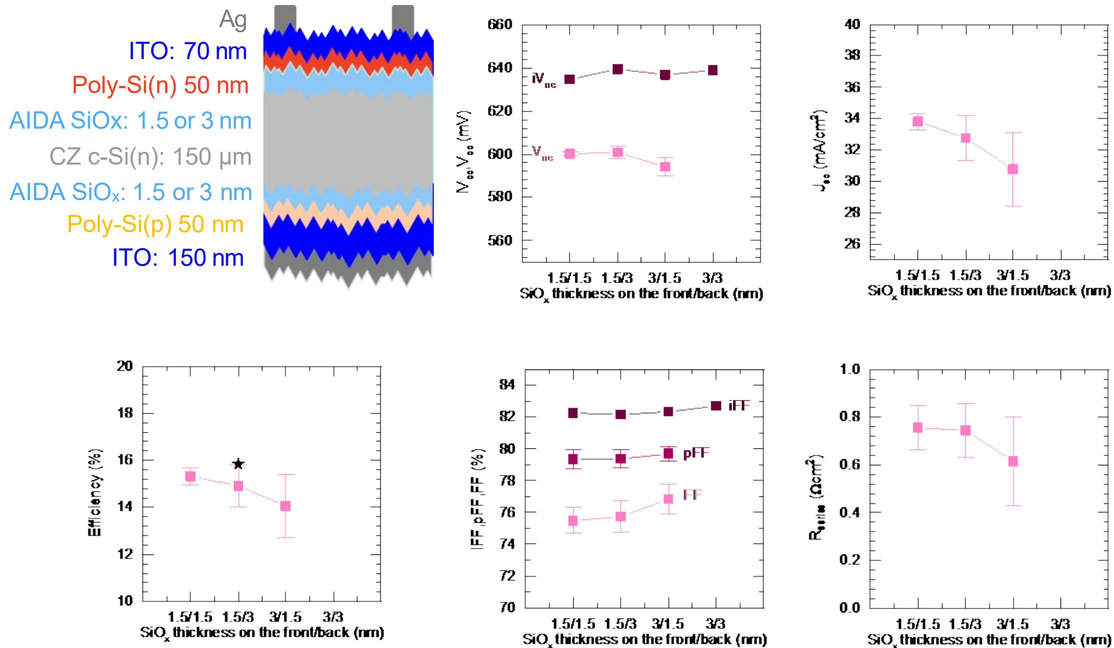


Fig. 39. A schematic of the TOPCon-like cell structure and current-voltage characteristics of the cell.

Before we integrated the AIDA-ITO into cells, we further tested whether we could improve the iV_{oc} of our double-side TOPCon devices through hydrogenation. To hydrogenate the cell precursor, one need a hydrogen reservoir. Therefore, we tested different reservoir candidates such as a sacrificial silicon nitride (SiN_x) layer, hydrogen plasma process, and hydrogenated indium oxide (IO:H) and the results were summarized in Fig. 40. After crystallization of the a-Si:H layer, all the cell precursors have consistent iV_{oc} around 640 mV. With the SiN_x layer (deposited by PECVD) the samples were annealed for 10 minutes in a FGA atmosphere, and the iV_{oc} exceeded 670 mV which is 30 mV higher than pre-hydrogenated state. However, after etching the sacrificial SiN_x layer in HF, the iV_{oc} dropped to below 600 mV, which is lower than the pre-hydrogenated state. We initially believed that this drop was due to the etching of either the polysilicon or silicon oxide layers during the HF process. To test this hypothesis, we submerged a reference cell precursor (without SiN_x) in HF for 10 minutes and found that the iV_{oc} only decreased by 10-15 mV (not shown). We also repeated this experiment by adding SiN_x back to the precursor and re-hydrogenated the iV_{oc} back to 640 mV. However, it drops again back to ~570 mV after etching off the SiN_x layer. We also tested a hydrogen plasma step (using a PECVD tool) on the polysilicon contacts for hydrogenation. We found that the iV_{oc} dropped 10 mV after 30 seconds hydrogen plasma treatment but 70 mV after 60 seconds treatment. We further tested whether the hydrogen-rich IO:H can be used as the hydrogenation source for the polysilicon contact as well as the electrode in the contact. As shown in Fig. 40, after sputtering, the iV_{oc} dropped to around 570 mV but recovered to 635 mV after subsequent anneals at 350 °C. This indicates that the IO:H could be a better

alternative to ITO in our TOPCon-like solar cell as it provides both lateral transportation and hydrogenation to recover the iV_{oc} loss. We would also investigate using our gas-flow-sputter system to deposit IO:H in future.

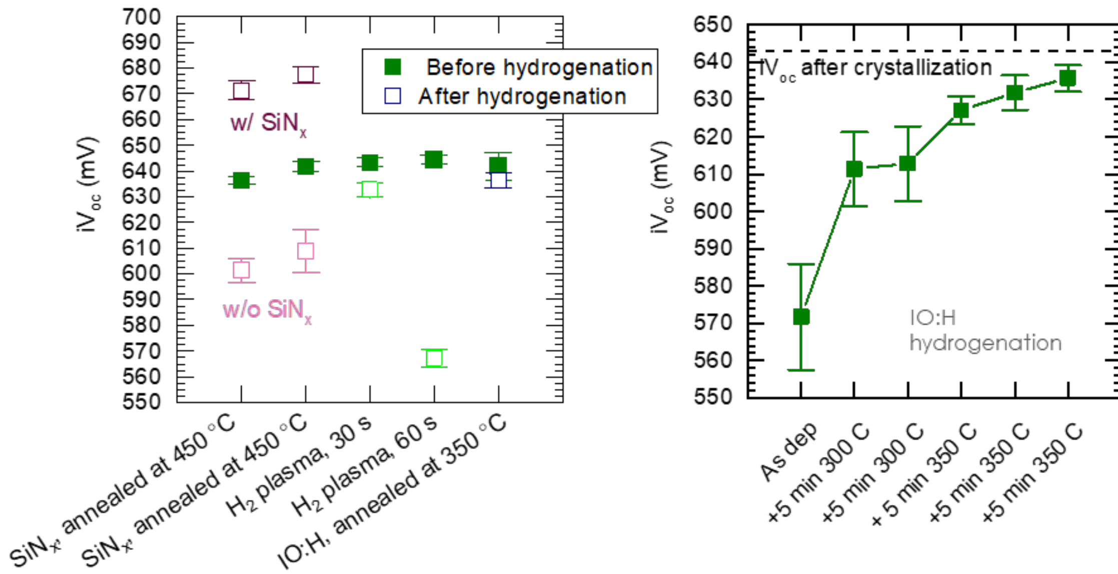


Fig. 40. iV_{oc} of a double-side TOPCon cell precursor with different hydronation methods (left), and iV_{oc} progression with IO:H hydrogenation (right).

To test whether IO:H is suitable our TOPCon-like solar cells, we also measured the contact resistivity of the full stack consisting of c-Si/SiO_x/poly-Si/IO:H/Ag with TLM and the results are shown in Fig. 41. For the hole-contact TLM sample, the sheet resistance calculated from the TLM measurements was approximately 130 Ω/square (similar to that of the p-type wafer) while a four-point-probe measurement on the p-type polysilicon layer indicated a sheet resistivity of approximately 1000 Ω/square. This confirms that the current was travelling through the polysilicon layer, and the extracted contact resistance represents the whole-stack contact resistance. For the hole contact, the contact resistivity in the as-sputtered state was 0.010 $\Omega\cdot cm^2$ and rose to 0.21 $\Omega\cdot cm^2$ after the 350 °C anneal. This contact resistivity value is comparable to our standard silicon heterojunction devices. For the electron contact, TLM measurements revealed a sheet resistance of 340 Ω/square which is similar to what we found with a four-point-probe measurement on the n-type polysilicon layer. This sheet resistance is also close to what we typically measured on our n-type silicon wafers, so there are two likely cases: the current travels through the Ag/IO:H electrode and across the n-type polysilicon layer; or the current travels through the entire contact stack with some current flowing through the n-type polysilicon layer and some through the wafer. While we attempted to etch back the polysilicon in an SF_6 environment, we found that contact resistivity increases drastically leading us to modify our contact resistivity measurement structures in future iterations of this process. Nevertheless, the extracted contact resistivity in the as-sputtered state was 0.017 $\Omega\cdot cm^2$, which is well below the tolerable value of 0.1 $\Omega\cdot cm^2$, but rose to approximately 10 $\Omega\cdot cm^2$ after annealing at 350 °C which would lead to a massive *FF* loss.

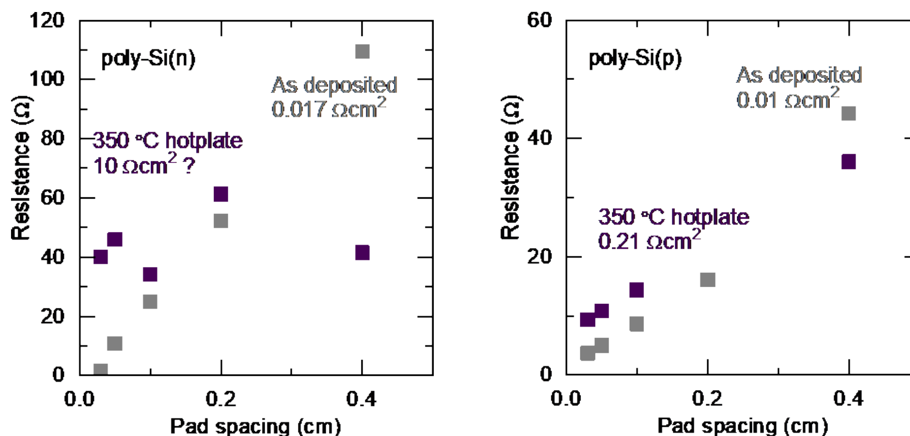


Fig. 41. TLM measurements of n-type (left) and p-type contact stack, consisting of c-Si/SiOx/poly-Si/IO:H/Ag. The extracted contact resistance for electron contact stack is 0.017 $\Omega\cdot cm^2$ before annealing and 10 $\Omega\cdot cm^2$ after annealing, whereas for hole contact stack, the contact resistance is 0.01 $\Omega\cdot cm^2$ before annealing and 0.21 $\Omega\cdot cm^2$ after annealing.

Sample exchange with Von Ardenne to process TOPCon cells

The primary challenge that we faced in meeting these milestones with our AIDA SiO_x passivation layer is access to a high-efficiency TOPCon baseline into which we can incorporate that layer. We don't have a high-efficiency PERC front side available at ASU, and thus, in previous quarters, we attempted to use a p-type TOPCon front side (with a thin poly-Si layer and TCO) or a p-type silicon heterojunction front side. Both were challenging to implement, resulting in cells that were limited not by the AIDA SiO_2 layer of interest but instead by those front sides. A new opportunity and route became available to us, one that is both more likely to be successful and demonstrates market traction of the technology developed in this project.

We worked with Von Ardenne to incorporate AIDA SiO_x into TOPCon cells as the tunnel oxide passivation layer, using Fraunhofer ISE's TOPCon cell baseline process. Von Ardenne is a manufacturer of vacuum coaters with sales into the solar cell market. Von Ardenne has a customer who is ready to purchase a TOPCon cell line, and, while Von Ardenne has developed a sputtering process and coater for the poly-Si layers, it does not presently have a vacuum-deposited solution to offer for the SiO_2 passivation layer. That is why Von Ardenne approached ASU and Swift Coat about sampling.

In the first experiment, shown in Fig. 42, we aimed to identify the optimum crystallization temperature for best passivation. We deposited our AIDA SiO_x in Swift Coat's tool (labeled as "OX-V3") on both sides of n-type float-zone silicon wafers for lifetime tests. These were compared to two other oxides: Fraunhofer ISE's baseline thermal oxide ("ISE") and another undisclosed plasma-based oxide from Von Ardenne or one of their partners ("OX-V2"). These wafers subsequently underwent the same a-SiC_x(n) deposition and were divided into four groups for different annealing temperatures, ranging from 850 °C to 980 °C, to crystallize this layer into poly-Si.

Sample ID	Oxide		a-SiCx(n)	Anneal			
				850°C 10'	900°C 10'	950°C 10' (ISC)	980°C 30' (ISC)
1	ISE	TO1	done	x			
2	ISE	TO1	done		x		
3	ISE	TO1	done			x	
4	ISE	TO1	done				x
5	ISE	TO2	done	x			
6	ISE	TO2	done		x		
7	ISE	TO2	done			x	
8	ISE	TO2	done				x
~~9~~	~~broken~~						
10	OX-V2	P1	done	a)	b)		
16	Ox-V2	P1	done			a)	b)
11	OX-V2	P2	done	a)	b)		
12	OX-V2	P2	done			a)	b)
13	OX-V2	P3	done			a)	b)
14	OX-V2	P3 (ms only)	done	a)	b)		
~~15~~	~~broken~~						
17	broken?		done				
18	OX-V3	P4	done	a)	b)		
19	OX-V3	P4	done			x	
20	OX-V3	P4	done				x
21	OX-V3	P5	done	x			
22	OX-V3	P5	done		x		
23	OX-V3	P5	done			x	
24	OX-V3	P5	done				x
~~25~~	~~broken~~						

Fig. 42. Experiment plan comparing different oxides as a tunnel oxide passivation layer with TOPCon lifetime test structures.

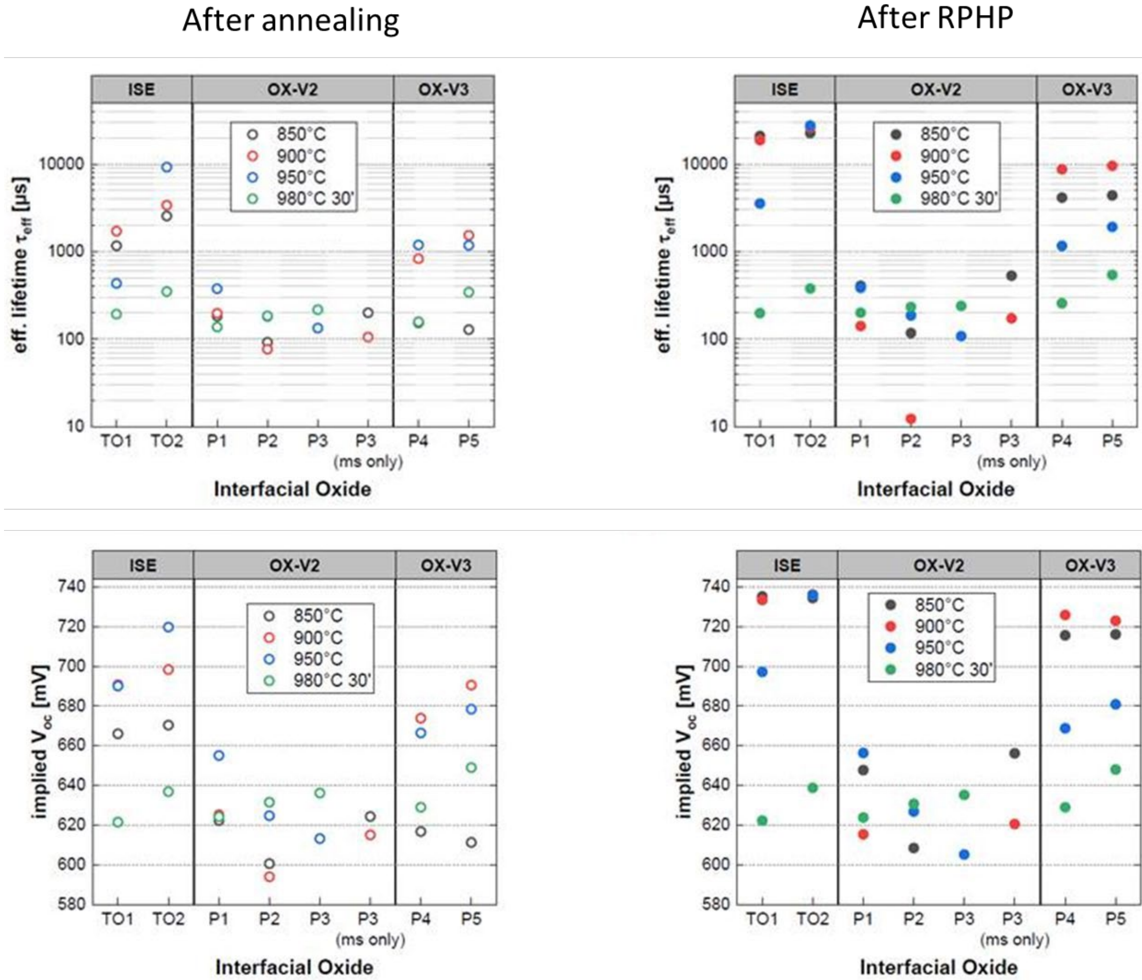


Fig. 43. Lifetime and iV_{oc} of TOPCon lifetime test structures made with three different oxides after thermal annealing (left) and after remote plasma hydrogen passivation (RPHP) treatment (right).

As the shown in Fig. 43, after annealing, our AIDA SiO_2 achieved a best lifetime approaching 2 ms and an iV_{oc} of 690 mV—outperforming the other plasma-based oxide and within 10 mV of all but one sample of Fraunhofer ISE's baseline thermal oxide. The optimum annealing temperature for our AIDA SiO_2 is 900 °C, close to that of Fraunhofer ISE's baseline thermal oxide. As known from Fraunhofer's papers, the passivation quality can improve upon remote plasma hydrogen passivation (RPHP) treatment. All the lifetime samples were further subject to such a RPHP process, and the results are also shown in Fig. 43. The lifetime of the plasma-oxide (OX-V2) sample stays the same, whereas the lifetime of Fraunhofer ISE's thermal oxide samples increased to >10 ms, resulting in iV_{oc}s of about 735 mV—as they typically achieve with RPHP treatment. Encouragingly, our AIDA SiO_2 also exhibited a remarkable increase in lifetime, with two samples achieving 10 ms (726 mV iV_{oc}) with the optimum 900 °C annealing temperature. This demonstrates that the passivation capability of our AIDA SiO_2 is nearly on par with the state-of-the-art thermal oxide and could be a competitive alternative to thermal oxide for TOPCon cells.

While processing this batch, we also made a control sample that we made into a contact resistance test structure. We deposited a-Si:H(n) at ASU on this sample and annealed at 850 °C for 30 min. The lifetime of the sample is above 1.5 ms (not shown), which is what we expected from our baseline processes. We further sputtered either silver or aluminum in a TLM pattern to extract the contact resistance. While industrial TOPCon cells use a high-temperature paste for real metallization, the sputtered metals still provide a reasonable check of the contact resistance since the majority of the resistance is expected to arise from transport across the oxide layer. Fig. 44 shows the resistance versus pad spacing for samples with either sputtered silver or aluminum. In either case, the calculated contact resistivity (< 20 mΩ·cm^2) is extremely low and should not lead to significant fill factor losses in one-sun TOPCon cells.
we are presently working with Von Ardenne and Fraunhofer ISE on subsequent experiments to fabricate TOPCon cells with our AIDA SiO_x layers.

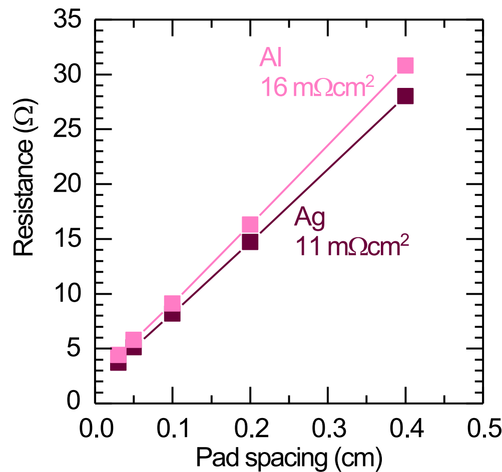


Fig. 44. Resistance versus pad spacing for TOPCon TLM test structures with sputtered silver or aluminum.

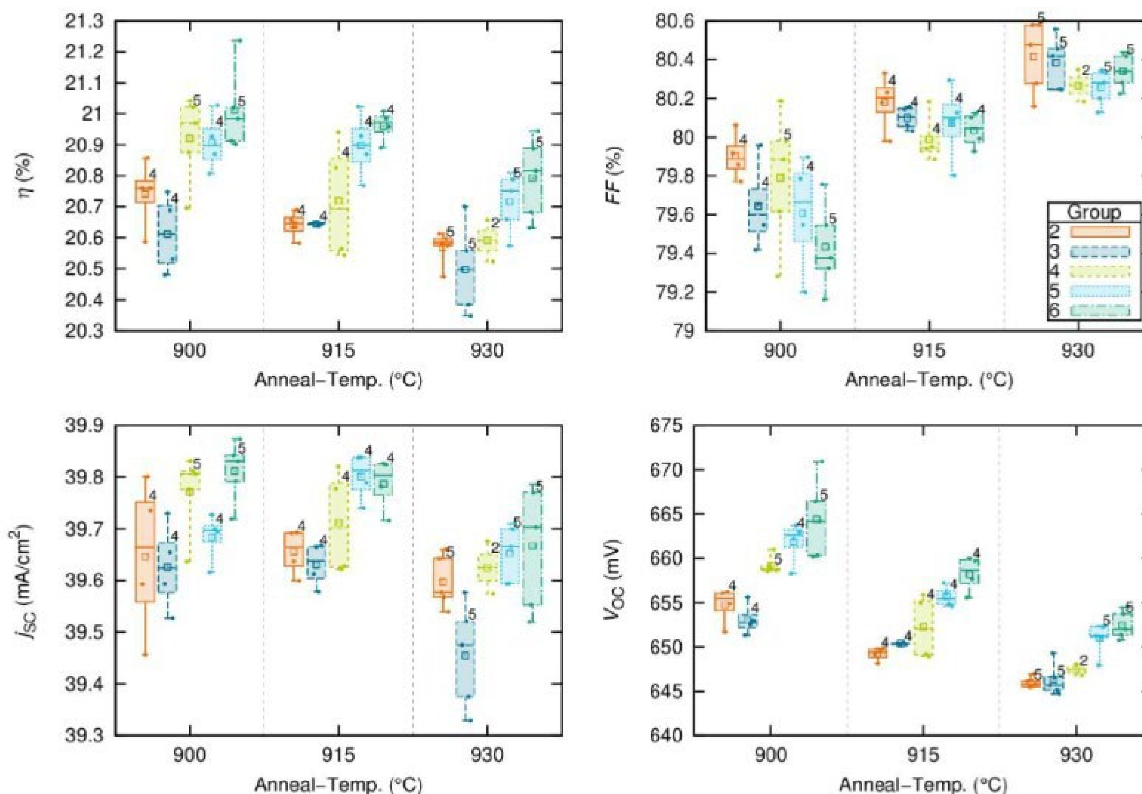


Fig. 45. Performance of 100 full-area TOPCon cells (PERC front side, TOPCon rear side) with AIDA SiO_x passivation layers. The SiO_x thickness increases from Group 2 (0.93 nm) to Group 6 (1.76 nm).

Given the promising lifetime and contact resistance results, we arranged a second experiment that made a batch of 100 full-area, M2-sized cells. We received 100 textured n-type CZ silicon wafers whose front side received a BBr_3 diffusion at Fraunhofer ISE. The samples were coated with AIDA-SiO_x at Swift Coat and then returned to the equipment manufacturer, where they received sputtered n-type amorphous silicon (a-Si(n)). They were then sent to Fraunhofer ISE for crystallization (with a split having three temperatures), metallization, and characterization.

The cell results are summarized in Fig. 45. Several of these cells met the GNG milestone of 21% efficiency with either an AIDA passivation layer or an AIDA TCO. This confirms our long-held hypothesis that our cell results at ASU within this project have been limited by our ability to make an SHJ front side that is process-compatible with our TOPCon rear, and not by the TOPCon contact itself. For all explored AIDA SiO_x thicknesses, the FF is good and the sheet resistance is low (~0.4 Ωcm²). This confirms our contact resistance measurements at ASU which showed that, even for SiO_x thicknesses up to 3 nm, the contact resistivity is less than about 30 mΩcm² (which is unexpected at thicknesses greater than about 2 nm for wet and thermal oxides). More particularly, the contact resistivity of reference samples from this experiment that remained at ASU was below 10 mΩcm² for all explored thicknesses. The J_{sc} is also very good at nearly 40 mA/cm².

The cells are thus limited by the V_{oc}. To understand this, it is instructive to consider the reference samples that stayed at ASU. These wafers received 20 nm of our in-house PECVD a-Si(n) and were annealed at 850 °C to crystallize the a-Si(n) into poly-

Si(n). We then measured the lifetime of these samples, shown in Fig46. (Since we used half wafers for this experiment, we were only able to make one lifetime measurement on each sample; hence the lack of statistics,) The lifetimes of the control samples are all relatively low, with a peak of 0.36 ms and a slight dependence on SiO_x thickness that is replicated in the cell V_{oc}s. While the finished cells had a different poly-Si layer (deposited at the equipment manufacturer instead of ASU) and a different crystallization process (at ISE instead of ASU), this suggests that the V_{oc} of the cells is limited by the iV_{oc}, as is normal in silicon cells with functioning contacts. As ISE measured up to 10 ms lifetime with our AIDA SiO_x layers in the previous experiment, which studied only lifetime structures and used their hydrogenation treatment, we know we have the scope to improve this and bring the V_{oc} up to 720 mV or even higher. The manufacturer's sputtered poly-Si had not been tested in combination with the AIDA SiO_x prior to these cells and ISE used too-high crystallization temperatures (we are unsure why), so figuring out the cross-term interactions between the AIDA SiO_x, the sputtered poly-Si, and the crystallization gives considerable opportunity to realize this V_{oc} improvement. Nevertheless, this collaborative experiment proves that the AIDA-oxide is functioning as passivation layers and can be readily integrated into state-of-the-art solar cells.

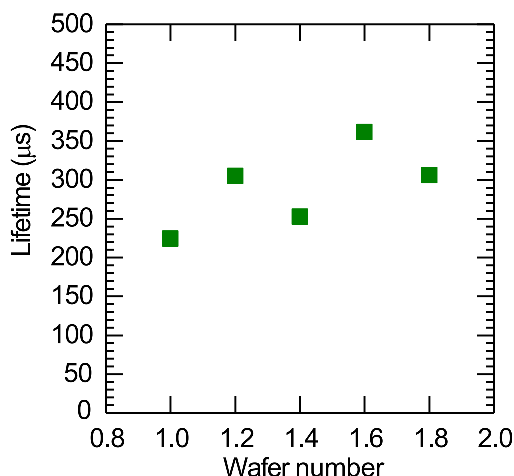


Fig 46: Lifetime of symmetric TOPCon control samples that remained at ASU and received ASU's baseline poly-Si(n).

<u>Integrating AIDA-deposited ITO into in-house TOPCon cells</u>

Previously, we fabricated TOPCon-like solar cells with AIDA-SiO_x as a passivation layer. We identified that the magnetron-sputtered ITO introduces sputter damage to the poly-silicon contact layer. Here, we also apply our low-damage AIDA-ITO onto TOPCon solar cells. We fabricated solar cells consisting of an n-type silicon wafer sandwiched between contacts consisting of AIDA-deposited SiO_x, n- or p-type polysilicon (poly-Si), and indium tin oxide (ITO). The poly-Si layers were deposited at 250 °C in a PECVD cluster tool in amorphous phase and then annealed in a nitrogen environment at 850 °C for 30 minutes to crystallize. The front poly-Si was n-type and the rear poly-Si was p-type. ITO was deposited using either traditional magnetron sputtering or our gas-flow sputtering system with the SMI source. For the rear of the

cell, sputtered Ag was deposited as the electrode whereas the front side was completed with screen-printed Ag paste, similar to a heterojunction cell. As shown in Fig 47, cells with V_{oc} averaging 600 mV and short-circuit current density (J_{sc}) of 36 mA/cm^2 were achieved using AIDA-deposited SiO_x and gas-flow-sputtered ITO. Compared to cells deposited with magnetron sputtering, cells with GFS ITO had a much lower drop from iV_{oc} to V_{oc} of ~20 mV, indicating less sputter damage from these layers. These cells also had the highest J_{sc} compared to standard magnetron-sputtered ITO. The fill factor of all cells were low, below 70%, indicating either an issue with the poly-Si/ITO interface or the sheet resistance of the ITO itself.

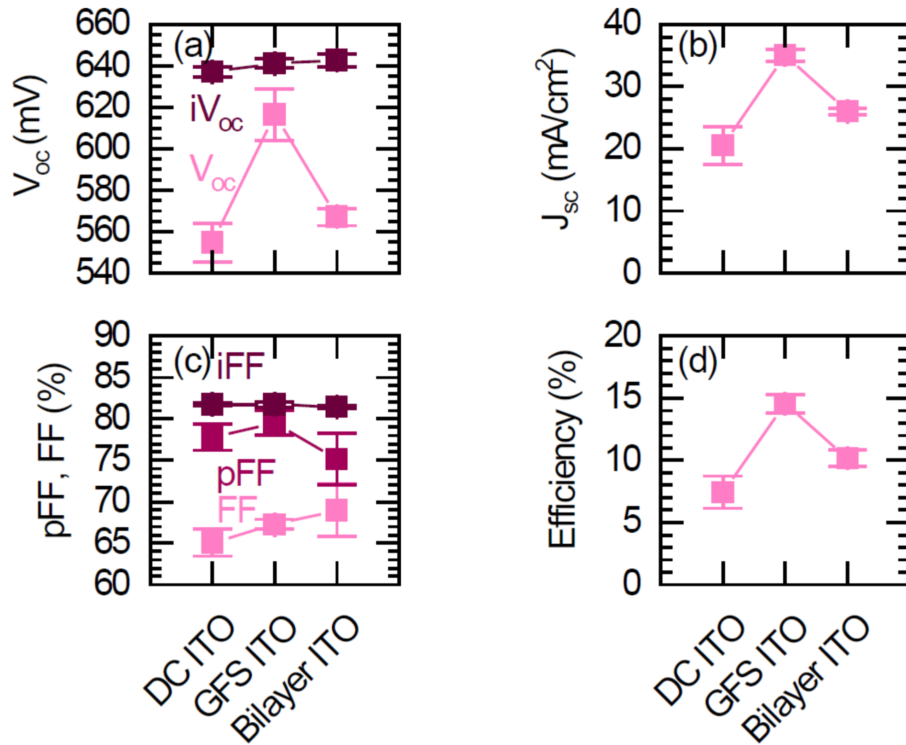


Fig. 47. Cell results for double-side TOPCon cells with either DC-sputtered ITO, gas-flow sputtered ITO, or a bilayer of both layers.

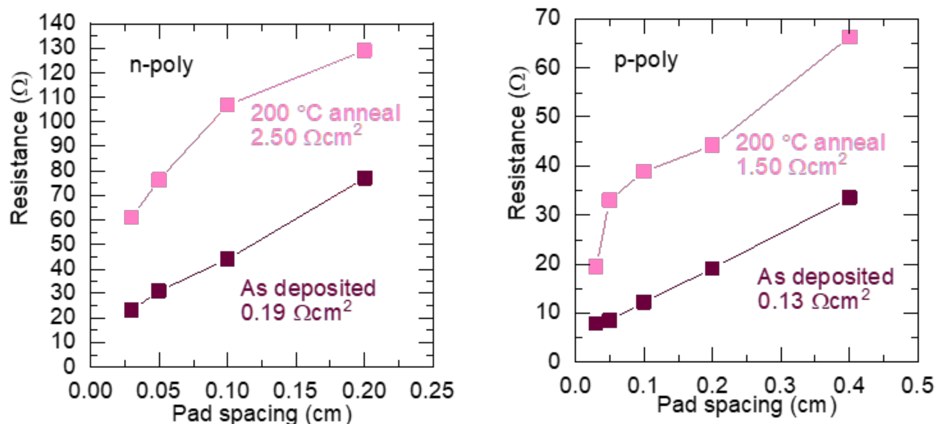


Fig. 48 Contact resistance versus pad spacing for AIDA SiO_x/poly-Si/GFS ITO contacts.

To investigate the contact resistance, using the same GFS ITO as on the cells, we fabricated test structures and measured the corresponding full-stack contact resistivity consisting of AIDA SiO_x/poly-Si/GFS ITO/Ag. As shown in Fig. 48, before annealing, contacts with either doping type of poly-Si had contact resistivities below 0.2 $\Omega \cdot cm^2$ and the values are comparable to our standard silicon heterojunction solar cells. After annealing at 200 °C in ambient, the contact resistivity increases significantly and the resistance versus pad spacing is no longer linear. This is evident that the low fill factors above are mostly caused by the high contact resistance between the poly-Si and GFS ITO but does not completely rule out a high sheet resistance in the GFS ITO.

To investigate whether we could reduce the contact resistance by increase the doping of the poly-silicon contact, we also performed ex-situ doping of our p-type poly-Si using spin-on dopants consisting of either gallium or boron dopants. These cells also used AIDA-SiO_x as the passivation layer. As shown in Fig. 49, we achieved our best efficiency of 17.1% using a gallium spin-on dopant annealed at 850 °C, which is 1% higher absolute compared to our previous record. This improved efficiency is the result of improved FF just under 74% and a J_{sc} around 38 mA/cm^2 but the V_{oc} is still low around 605 mV. This is likely caused by the sputter damage induced during the magnetron sputtering of the ITO layers. If integrated with GFS ITO, we expect higher V_{oc} and efficiency.

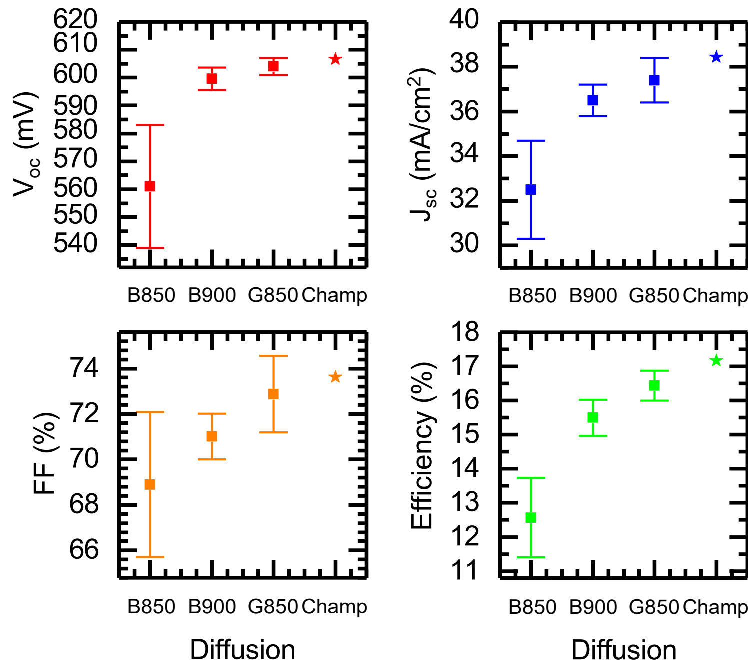


Fig. 48 Cell results using AIDA SiO_x passivation layers and spin-on dopants for the p-type poly-Si layer.

<u>Replacing the p-type TOPCon structure with standard SHJ contacts</u>

In another attempt to test the quality of our SiO_x contacts, we swapped out the front p-type TOPCon structure with our standard p-type SHJ contact. The front of these cells consisted of a stack of a-Si:H(i)/a-Si:H(p)/ITO/Ag-paste while the rear consisted of our stack of SiO_x/poly-Si(n)/Ag. Since we had previously observed that the contact resistivity of our SiO_x/poly-Si(n) contact remained relatively constant even up to 5 nm, we varied the thickness of the SiO_x layer from 1.6 to an extreme 11 nm. We also included our standard baseline SHJ cell for comparison. In this same experiment, we made sister samples to measure the contact resistivity. Fig. 49 shows the cell results (V_{oc}, FF, J_{sc}, efficiency) of this experiment. Nine 2 cm × 2 cm cells were measured per wafer and averaged. Error bars are the standard deviation of the 9 cells.

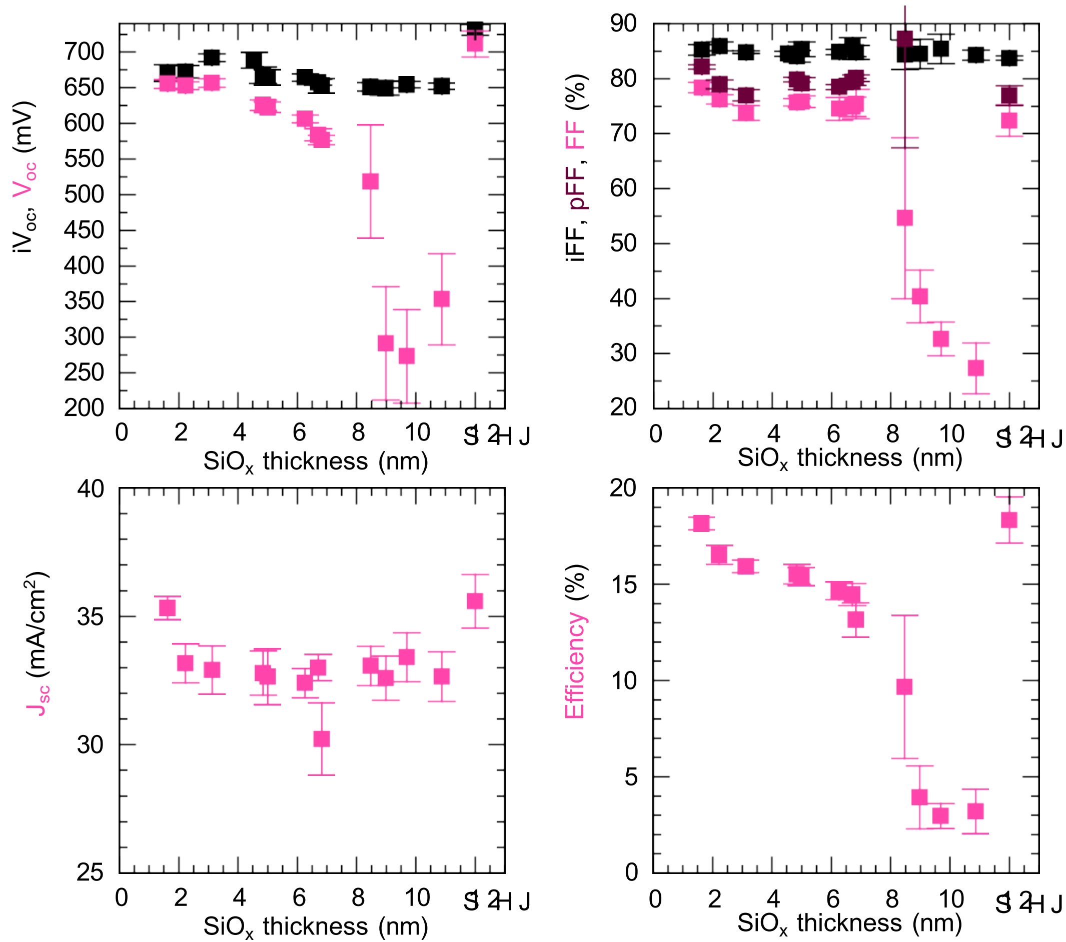


Fig. 49. Cell results of SHJ/TOPCon hybrid cells with increasing AIDA SiO_x thickness, plus an SHJ reference cell.

The V_{oc} follows the trend in iV_{oc} up to an SiO_x thickness of 6 nm. In these TOPCon structures, the phosphorus of the poly-Si layer partially diffuses into the silicon wafer during crystallization, leading to an electron-conductive surface and band bending that facilitates electron extraction. As the SiO_x layer thickens, it limits this phosphorus diffusion and the iV_{oc}–V_{oc} gap grows, even dropping below 400 mV. The SHJ control sample had a higher V_{oc} than the best hybrid cell by nearly 60 mV due to the superior passivation of the amorphous silicon contact.

Remarkably, there is very little variation in the FF for all thicknesses up to 6 nm. This is a unique result, as the leading theories for transport in these contacts is direct tunneling through the SiO_x layer when it is thinner than 2 nm or transport through pinholes in the SiO_x for thicker layers around 3 nm. Typically, pinhole formation occurs for SiO_x layers annealed at temperatures above 1000 °C; we annealed our contacts at 850 °C for all thicknesses. It is likely we have a unique oxide that forms pinholes even at these lower temperatures, and we have plans in place to perform TEM on these layers to confirm this hypothesis. Above 6 nm, the FF rapidly decreases, indicating that any pinholes are likely pinched off. For the SHJ control, the FF is 6% lower than the best hybrid cell because SHJ contacts tend to have higher contact resistivity than TOPCon contacts by at least an order of magnitude.

With SiO_x thicknesses below 6 nm, the cell efficiency follows the trend of reduced V_{oc}, while above 6 nm the efficiency follows the drop in FF. The best cell efficiency in this batch was 18.6% for an SiO_x thickness of 1.63 nm, which is an improvement of 3% absolute over our previous best and comparable to the SHJ references. The low-hanging fruit in improving the efficiency of these devices is in improving the V_{oc}, per the discussion above for TOPCon cells.

With the co-deposited sister wafers, we made Cox and Strack structures to measure the contact resistivity for all SiO_x thicknesses. Fig. 50 shows the contact resistivity as a function of thickness. The contact resistivity remains constant below 10 $m\Omega \cdot cm^2$ up to 4.5 nm, then rapidly increases, causing the same tried in the cell FF. Beyond 5 nm, the resistance versus pad area become non-linear and contact resistivity is impossible to calculate.

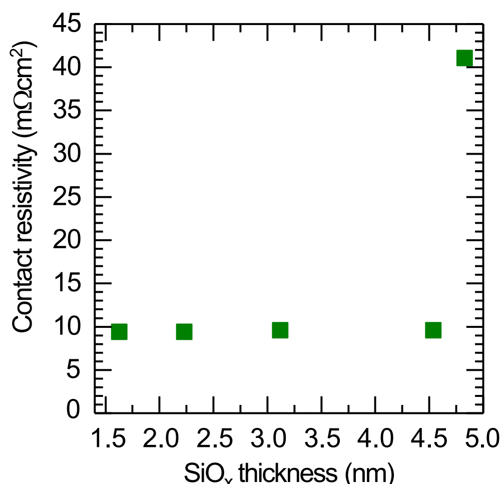


Fig. 50. Contact resistivity as a function of SiO_x thickness.

Hybrid cells with planar rear

In an attempt to reach higher efficiencies with our hybrid solar cells, we decided to change the rear surface of the c-Si wafer from a textured surface to a planar surface. Passivation of planar surfaces with SiO_x/poly-Si tends to be higher when compared to textured surfaces because the planar surface has a lower density of dangling bond defects. In addition, planar surfaces are more representative of the industry-standard TOPCon as cells undergo a rear etch after boron diffusion to remove the wrap around boron layer. To simulate this effect, we etched the wafers in KOH. In this experiment we used two different thickness of AIDA SiO_x (1.75 and 2.23 nm) that were approximately the same as the best cells from the previous experiment on textured wafers. We also included a cell with 0 nm of SiO_x and a native SiO_x as controls to confirm AIDA SiO_x provides a higher quality cell.

Fig. 51 shows the cell results of this batch of cells. Compared to the experiment performed on textured wafers, the iV_{oc} of these cells is 30-40 mV higher with both samples with AIDA SiO_x achieving iV_{0c} above 700 mV. This translates to a V_{oc} above 680 mV again 30 mV higher than the textured cells. The iFF, pFF, and FF between the two batches are the same indicating that the contact resistivity will be approximately the same (we did not complete contact resistivity measurements in this batch due to wafer availability at the time). The average J_{sc} around 35 mA/cm^2 of this

batch is similarly low like the textured batch which we mentioned previously is a result of parasitic absorption in the thick a-Si:H(p) layer on the front and not an issue with the SiO_x/poly-Si(n) contact. To prove this, Fig. 52 shows the EQE and 1-R results of these cells showing a J_{sc} loss of approximately 3.5 mA/cm^2 in the region from 300-600 nm which is all parasitic absorption in the front of the cell. Finally, the efficiency of these cells averaged above 18% with the best cells at 1.75 and 2.23 nm had efficiencies of 19.2 and 18.9%, respectively, which is an improvement of 0.3% absolute over the best cell in the textured batch. While we did not achieve a cell with efficiency above 20% using our hybrid cell structure, this is not the fault of the SiO_x/poly-Si contact as results discussed above show.

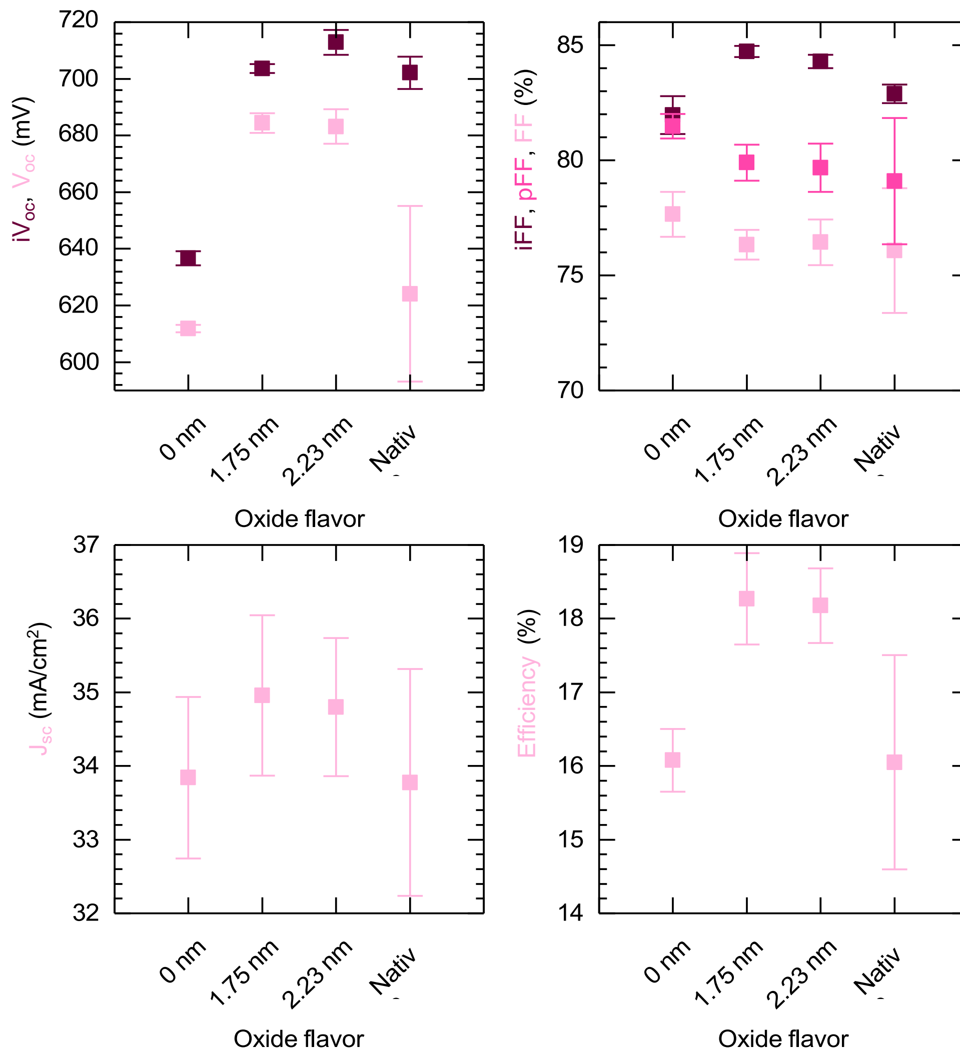


Fig. 51. Hybrid cell results with a planar rear surface.

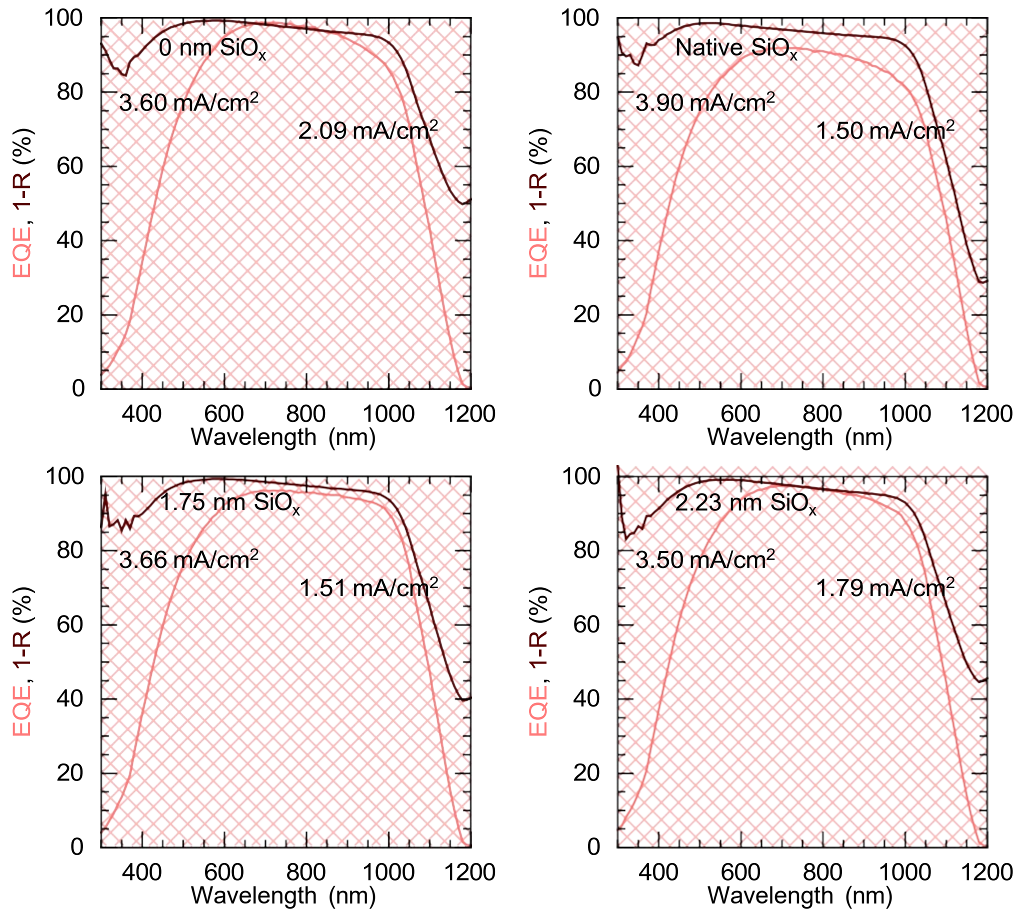


Fig. 52. EQE and 1-R for cells made with a planar rear.

Task 3: Scale processes to 6" wafers with technoeconomic analysis

Hardware and process scaling

To meet the milestones associated with the scaling of the processes Swift Coat worked to scale up and improve on the hardware associated with both the SiO_2 passivation layer and the ITO TCO. The goal is depositing a uniform coating of each layer across at least a 6-inch-wide wafer.

For the SiO_2 passivation layers, Fig. 53 (left) shows the thickness mapping as measured with ellipsometry of a SiO_2 layer, deposited on a Si wafer, with an average thickness of 7.79 nm and a thickness non-uniformity of ±15.9%. The thickness over the full wafer ranged from 6.83 nm to 9.31 nm. The right side of the figure shows the same data replotted as the % deviation for the average thickness across the wafer. It is clear from that the largest deviations are at the front and back of the wafer. These are likely due to the turn-around points in the small test chamber being too close to the nozzle and excess deposition occurring when the wafer changes direction of motion under the nozzle. If the uniformity is considered just across the center line of the wafer at Y-Position = 0, the non-uniformity is decreased to 4.8%. This position

should be more indicative of the expected results for a system with a continuously translating wafer under 1 or more sources.

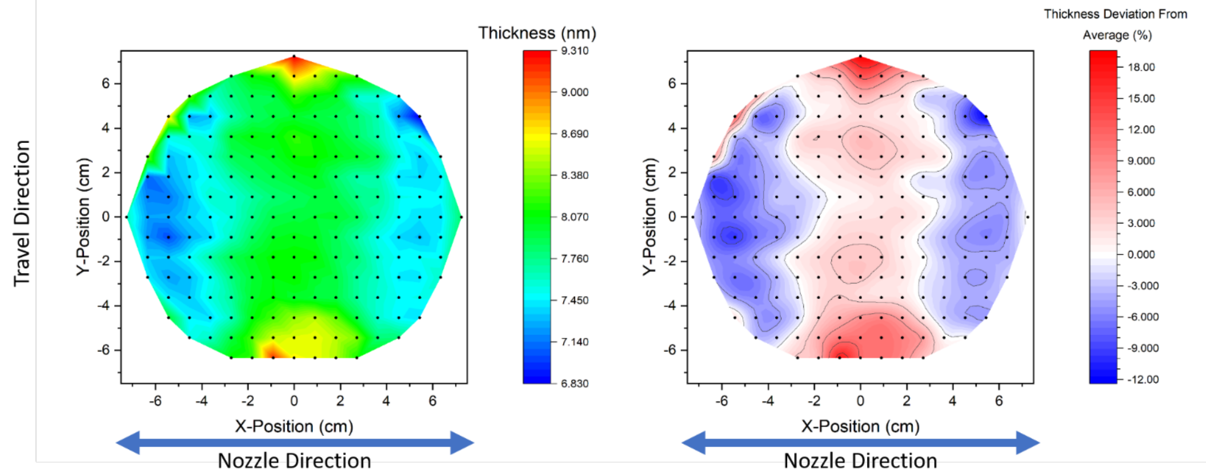


Fig. 53. AIDA deposited SiO2 passivation layer thickness map. Left: Actual layer thickness Right: Thickness deviation from average.

In addition to meeting the stated milestone of <20% non-uniformity for a < 10nm-thick SiO_2 passivation layer across a 6-inch wafer, Swift Coat further expanded the passivation layer deposition process to a 0.5 m-wide source. This system shows good uniformity across its full deposition width as illustrated in the Fig. 54. It shows that the thickness of a SiO_2 layer as measured across a 12-inch wafer. Although the measurements in this figure are of a thick film, the uniformity of the deposition from this source was found to be consistent for differing layer thicknesses. The system that the 0.5 m source is installed on allows the simultaneous deposition of up to 6 solar wafers at a time with an estimated throughput for a commercial system of more than 10,000 wafers per hour. This system was used for a majority of the passivation depositions in the latter half of this project including all of the samples sent to Von Ardenne that we presented previously in this report.

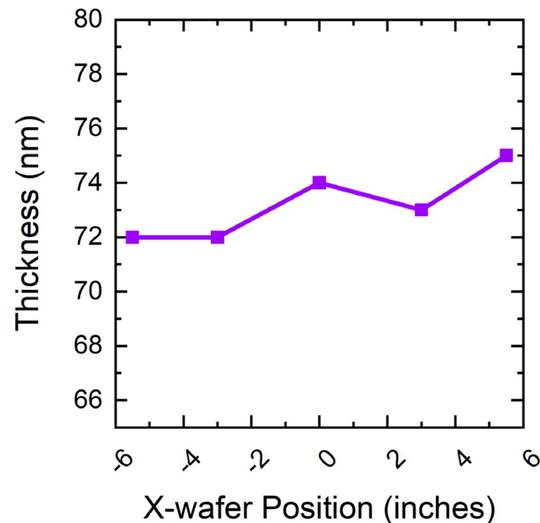


Fig. 54. Thickness of an SiO_2 layer across deposited by the 0.5m source measured across a 12in wafer parallel to the source direction.

On the TCO side of this project Swift Coat designed and tested 3 different version of a lager GFS source with the goal of scaling both the uniform deposition width of the sources developed at ASU and the deposition speed. One of these 3 sources is a scaled-up version of the latest generation of ASU sources and the other two are of Swift Coats own design.

The first Swift Coat designed GFS source took the target width from 5 inches on the latest ASU versions to 8-inch wide. Fig. 55 shows pictures of this first-generation Swift Coat source. In addition to scaling the width of this source it also has some advantages over the ASU designs. By placing the targets inside of the main chamber, the target to substrate distance can be reduced considerably compared with the ASU sources and can easily be adjusted. This source also has much more ease of scalability as many of the parts can be used for varying target sizes.

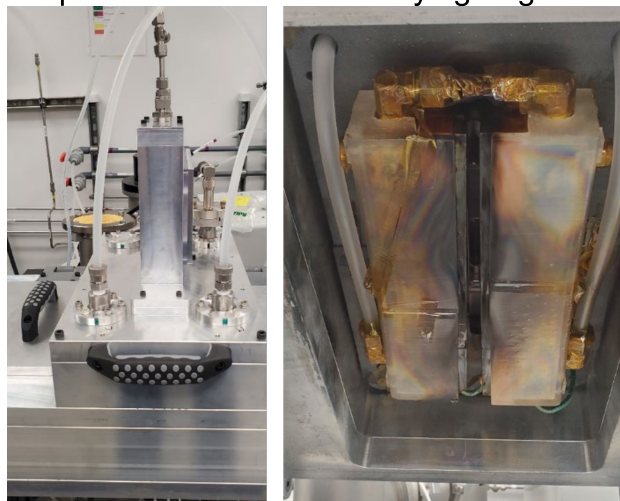


Fig. 55. Pictures of the first-generation Swift Coat GFS source. Left: outside of the source, and right: Inside of the source from substrate perspective.

The Gen 1 Swift Coat source did give a lager uniform width than the smaller ASU sources however it also had some reliability issues due to the water and power connections being in the vacuum chamber. This led to many electrically hot surfaces that were prone to arcing.

Due to the failures of the Gen 1 Swift Coat source a new approach was tried by scaling the Gen 3 ASU source up to a larger dimension. This Gen 2 Swift Coat source had targets that are 400-mm wide, intending to render a uniform deposition zone of about 300-mm wide. The difference between the target length and uniform deposition zone was expected due to the performance of the smaller ASU sources. This new design incorporated the learning from the ASU sources by incorporating binary gas manifolds for both the Ar coming through the source and the O_2 coming in between the source and the substrate. Fig. 56 shows a diagram of the Gen 2 Swift Coat GFS sputter source.

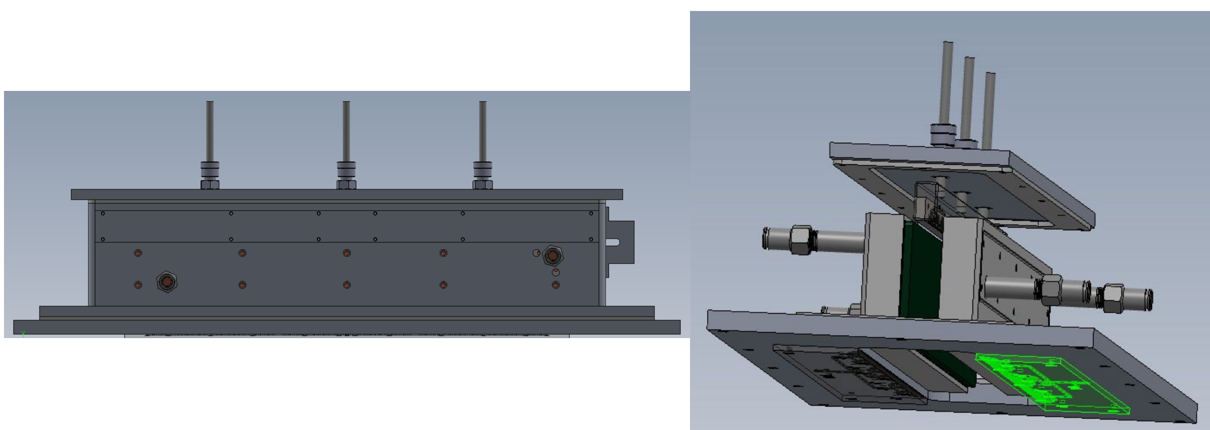


Fig. 56. Diagrams of the Gen-2 Swift Coat GFS source. On the right-hand image the main body has been removed to revel the binary gas distribution manifolds (highlighted in green).

The reason for this new source design was to take advantage of the learning that ASU smaller scale sources had provided to that point while still aiming for a larger deposition area. Upon initial testing of the Gen 2 Swift Coat source, it was found that the deposition had a very unexpected thickness profile with the center of the source having a significantly lower deposition rate than the area on either side of it. The M shaped profile can be seen in Fig. 57. The sever, >40% non-uniformity was able to be somewhat alleviated by decreasing the Ar gas flow but at the expense of deposition rate. Later, as shown in Fig. 58, changing the Ar gas inlet such that the Ar flow could be separately controlled though three equal width sections along the width of the source improved the uniformity and when the center flow was lessened compared to the outer edges a 230-mm wide area was able to be coated with less than 10% was able to be achieved, limiting the M shaped profile while maintain the higher dep rate since the over all gas flow was maintained.

While the uniformity of the Gen 2 source showed promise it came at the cost of a significantly more complex system with extra gas flow control required and brazed targe cooling blocks that proved to be a manufacturing hurdle. It was also found, similar to the smaller ASU versions, that after moderately long deposition periods the space between the targets and the dark space shielding would get filled with deposited

material. When this happened, the source would start arcing, leading to low quality and low-rate depositions. The source would then need to be disassembled and cleaned to remove this material. Due to the berried nature of the targets this was a complex and time-consuming process prone to introducing vacuum leaks on this large-scale source.

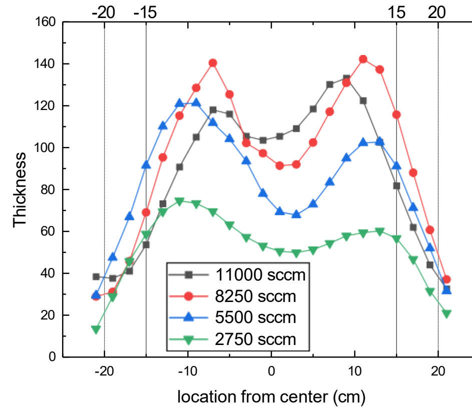


Fig. 57. Illustrating the effect of total gas flow on the highly non-uniform deposition profile of the Gen 2 Swift Coat GFS source.

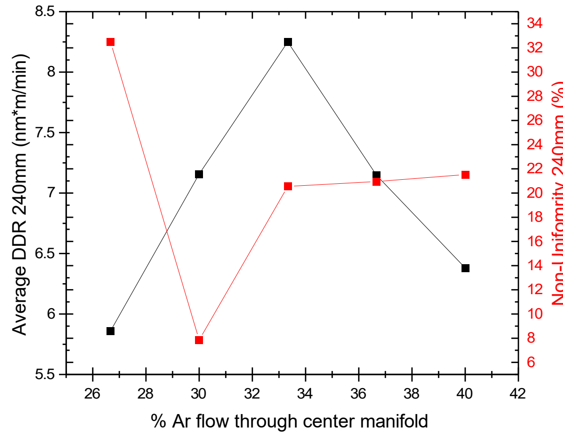


Fig. 58. Graph of the DDR and thickness non-uniformity of the Gen 2 Swift Coat GFS source when the relative distribution of Ar through the center and edges of the source is varied.

To attempt to overcome these deficiencies in the first- and second-generation Swift Coat sources a third design was made. This design was largely a slightly larger version of the Gen 1 source with a redesigned water and power delivery system to alleviate the arcing points seen in the former. The Gen-3 Swift Coat GFS source incorporated the in-chamber and nozzle-based Ar distribution. It also incorporated a scaled binary oxygen distribution system similar to the ASU based sources. Fig. 59 shows both a photo and cross-sectional diagram of the Gen 3 Swift Coat source. This source has proved to be both the most reliable of the large sources but also to produce the best dynamic deposition rate and best material quality of the three. In each case, at the

end of this project, it is shown to be approaching the state-of-the-art magnetron sputtered ITO films over an width of grater than 6 inches. This is all while maintain the rough vacuum advantages of gas flow sputtering.

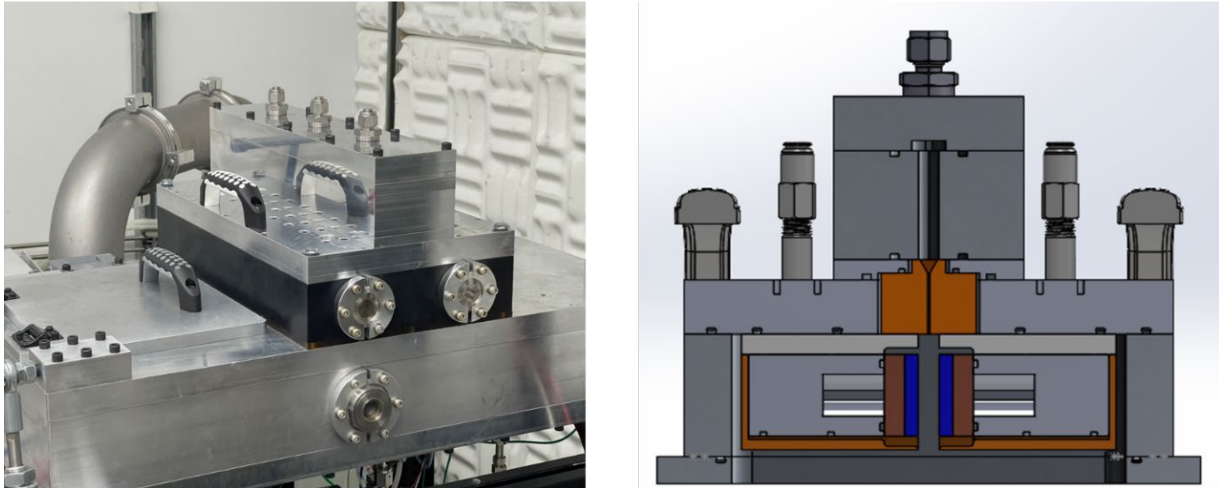
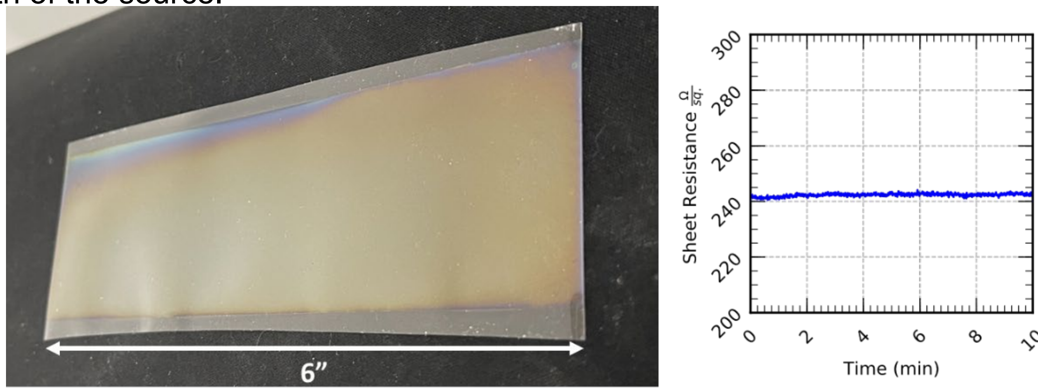


Fig. 59. Swift Coat's 300mm ITO deposition source. The system expands on ASU's design with modifications for improved non-uniformity, increased DDR, and long run times. (a) Photograph of the source integrated into Swift Coat's SC300 disposition system. (b) Cross-section of the 300mm ITO deposition source.

The ITO film uniformity deposited by the Gen-3 Swift Coat source are shown in Fig. 60. It shows a 6-inch-wide substrate with 85nm of ITO deposited on it. The sheet resistance of this film was about 250 Ω/square or about 3 times the requirement for the top side of a silicon solar cell. The graph to the right of the figure illustrates that the sheet resistance of the film is stable over the course of 10 minutes. This is in contrast to films deposited at room temperature with standard DC sputtering techniques on the smaller ASU sources. Finally, the bottom image in shows a 300 mm Si substrate with an ITO coating that has a thickness non-uniformity of 8.5% over the width of the source.



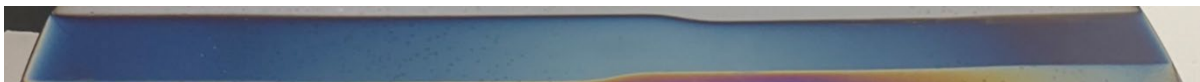


Fig. 60. (Left) Uniform deposition of an 85nm thick ITO film deposited by the Gen 3 Swift Coat GFS source. (Right) Sheet resistance as a function of time for the film shown on the left. (Bottom) A thick ITO film on 300mm Si with a thickness non-uniformity of 8.5%

In addition to scaling the GFS sources in deposition area Swift Coat also was working to enhance the deposition speed to allow for the better integration with commercial solar cell processing. As shown in Fig. 61 the 3rd generation Swift Coat source has a very stable and saleable deposition rate. On the left of the figure, it is shown that the DDR from this source scales nicely with power which is helpful for matching the deposition rate to the run speed of a given coating line. The center shows that over 30 different runs covering over 3 months of baseline depositions confirming a very repeatable deposition rate.

Finally, the third panel in Fig. 61 shows that DDR normalized to the linear power density applied to the source. This normalized DDR allows us to compare the ASU and Swift Coat sources more directly to state-of-the-art rotary magnetron sputtered ITO. From this graph, one can tell the Gen 3 Swift Coat source has significantly higher Normalized DDR compared to the smaller ASU and Gen 1 swift coat sources. It is thought that this is at least partially due to the reduced end effects which give a lower dep rate due to worse confinement of the electrons and so lower plasma density as the total length of the source increases. If this trend were to continue than the GFS sputter source could easily be at or above the SOA with a source of 1m in length on par with commercial rotary magnetrons.

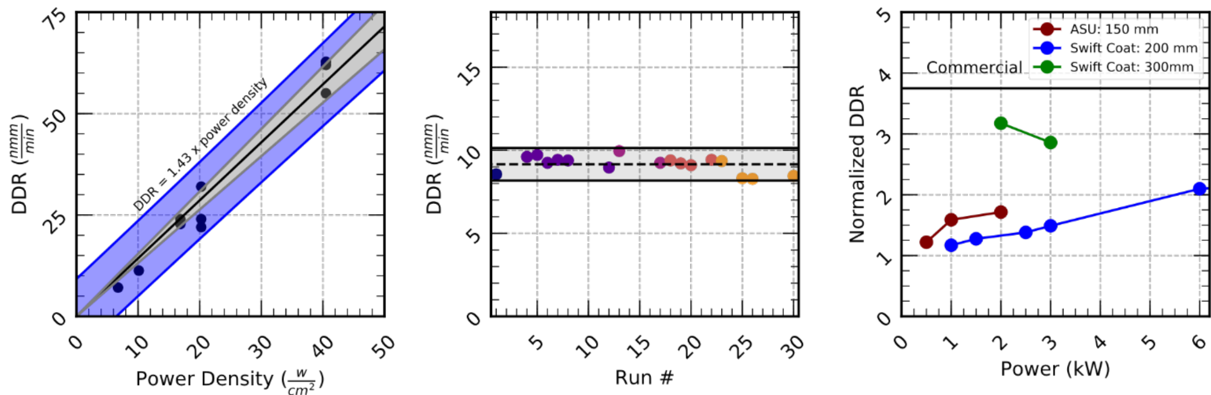


Fig. 61. Performance summary of Swift Coat's 300mm TCO deposition source. (Left) Plot of dynamic deposition rate vs. power density. DDR's > 65nm m/min have been demonstrated. (Middle) run number vs DDR for 30 runs of a baseline process conducted over 3 months of testing. The plot indicates good process repeatability. (Right) Plot of applied power vs. normalized DDR for the ASU source (red), Swift Coat's 200mm source (blue) and Swift Coat's 300mm source (red). The plot indicates that the latest version of the source has normalized DDR's approaching commercial magnetron sputtering processes.

We also performed technoeconomic analysis, especially the CapEx on our system. Based on interviews with cell manufacturers and tool vendors, a 200 MW TOPCon manufacturing line costs approximately $4.8M. The LPCVD tool in that line that deposits the tunnel oxide accounts for approximately 12%, or $575k, of the total cost. Part of the work in developing AIDA as a method for producing a tunnel oxide has been evaluating various SiO_x precursors and their impact on performance and cost. Initially it was believed that liquid SiO_2 precursors like TMMS, TEOS, or HMDSO would provide superior economics when compared to gaseous precursors like silane (SiH_4),

as the price of liquid precursors per gram of material produced is generally much (10X) less expensive than gaseous precursors. However, while it remains true the material costs for liquid precursors is much less than that of silane, the same cannot be said for the capital expense. The liquid precursors require expensive ($250k) liquid chemistry delivery systems, expensive mass flow controllers, and expensive exhaust handling that is not required when using highly diluted silane. Our model indicates that the cost per wafer was primarily driven by the capital expense and, when comparing the low-materials-high-capex liquid precursor system to the high-materials-low-capex gaseous system, the gaseous system provided the same or better cost per wafer at a much reduced CapEx of $315k. When compared to the $575k cost of a commercial system, an AIDA system is ~55% of the cost—meeting the requirements of milestone M3.1.1.

AIDA deposition system component cost breakdown		
Electrical work (10% of active source cost)	$	22,860.00
Installation (20% of active source cost)	$	45,720.00
Gas line plumbing (15% of active source cost)	$	34,290.00
1m wide, 2m long chamber	$	75,000.00
Throttle valve	$	5,000.00
Main Chamber pump	$	25,000.00
Load lock pump	$	7,000.00
Unload pump	$	7,000.00
Load & Unload Chambers	$	25,000.00
Filter	$	1,200.00
Cold Trap	$	1,200.00
Foreline	$	1,000.00
Frame	$	800.00
Cost Per System	$	251,070.00

AIDA spray head component cost breakdown		
Generator	$	8,150.00
MFCs	$	28,000.00
Heating lines/controllers	$	6,000.00
Pressure Sensors	$	1,500.00
Spray head chamber	$	12,000.00
PLC & automation components	$	1,500.00
Total	$	57,150.00

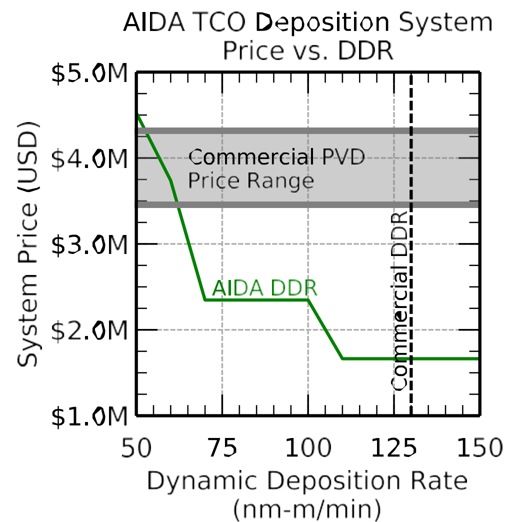


Fig. 62. Cost breakdown of an AIDA system used for TCO deposition (left), and system cost as a function of dynamic deposition rate (right).

A 200 MW SHJ cell manufacturing line costs approximately $11.5M. The PVD tool that deposits TCO on both sides of the cell accounts for 30% of that total cost at ~$3.5M. An AIDA-based TCO deposition system has the potential to significantly decrease this cost. The AIDA system comprises two types of components: the deposition chamber and the spray head, with several spray heads being mounted on each deposition chamber. The costs for each of these components are shown in Figure 62. Each spray head has a maximum dynamic deposition rate (DDR) it can achieve. To increase the effective DDR, multiple spray heads can be placed in series. The effect of this is that the total capex required to integrate an AIDA TCO deposition system will be heavily influenced by the DDR. Figure 62 also shows the system price of an AIDA-TCO deposition system as a function of DDR (green line). Also included in the plot is a range for the price of state-of-the-art PVD systems of equivalent throughput (grey area) and the typical DDR of a commercial system (black-dashed line). As shown in the plot, to be cost-competitive with commercial PVD systems, the spray heads need to be able to reach DDRs of >55 nm-m/min. We note that, for both

the TCO and tunnel oxide deposition, we have included installation and infrastructure costs in our calculation whereas the price estimates provided by industry do not.

Significant Accomplishments and Conclusions:

In this project, ASU explored three versions of gas-flow-sputter sources. We learned that the plasma energy dictates the grain size and quality of these gas-flow-sputtered films. On both the lab-scale version and 300-mm-wide scaled version of GFS AIDA system, we achieved 85-nm-thick ITO films with sheet resistance of 250 Ω/square. Although this number is still about 3 times higher than the project target, it can already finds its application on the rear side of solar cells (as we demonstrated in the project) or some other applications such as perovskite solar cells (which has lower current density due to higher bandgap) or LEDs that don't require high conductivity. The non-uniformity of our AIDA process, whether coupled with GFS source for TCO deposition or PECVD source for silicon oxide deposition, have been demonstrated <10% across 300-mm-wide area. This is sufficient for silicon solar cell application intended for this project. However, based on the design principle, we anticipate the process uniformity can be maintained when further scaling this process for other applications, e.g. glass coatings. The GFS ITO also shows low sputter-damage, as, compared to a DC magnetron sputtering that usually introduces > 50 mV drop in iV_{oc} on silicon heterojunction cell precursors after sputtering, AIDA-ITO results < 10 mV iV_{oc} drop. This soft ITO deposition could also find its application on other materials that are susceptible to sputter damage, e.g. perovskite solar cells.

As for the silicon oxide passivation layers, we demonstrated that AIDA-oxide functions as a tunnel-oxide passivation layer by achieving 2.6 ms minority carrier lifetime on double-side textured silicon wafers and 10 ms on polished float zone wafers. The best contact resistivity of the corresponding layer stack is less than 10 $m\Omega \cdot cm^2$, which is sufficiently low for one-sun solar applications. We also demonstrated 21%-efficient TOPCon solar cells that incorporates AIDA-SiO_x as a passivation layer. These results also show that the AIDA-SiO_x can be readily integrated into TOPCon cell production lines. Our technoeconomic analysis reveals that AIDA system roughly saves 45% CapEx compared to a commercial LPCVD tool. The inline nature of our process opens the opportunity for process integration with higher throughput and could potential lower operational cost of TOPCon solar cells.

Path Forward: Future work on the two AIDA deposition sources—one based on PECVD and one based on sputtering—developed in this project should be geared towards refining hardware and processes to (i) exceed the performance of SiO_2 tunnel passivation layers and TCO electrodes in TOPCon and SHJ solar cells, (ii) "harden" the equipment for manufacturing 5,000 wph with high yields, and (iii) engage solar cell manufacturers in joint-development agreements or other product testing arrangements.

Products:

Z. Leuty, M. George, M. Garcia, Z. Yu, and Z. Holman, "High mobility soft sputtered ITO coatings by dual gas-flow sputtering," (submitted).

Z. Leuty, W. Weigand, J. Ochoa, J. Carpenter, Z. Yu, M. Bertoni, and Z. Holman, “Ultra-high throughput inline deposition of silicon oxide for polycrystalline silicon passivating contacts,” (submitted).

Project Team and Roles:

- Zhengshan Yu, Assistant Research Professor, Arizona State University: Manage process development, design experiments, and prepare reports to DOE
- Mark George, Research Scientist, Arizona State University: Hardware design and process development for lab-scale deposition tool.
- Zachary Leuty, PhD student, Arizona State University: Hardware design for lab-scale deposition tool, perform deposition and experiments
- William Weigand, PhD student, Arizona State University: Integrate AIDA process to solar cells
- Mark Li, PhD student, Arizona State University: AIDA depositions and coating characterization
- Peter Firth, CEO, Swift Coat Inc: Hardware design for the full-size deposition tool
- Ty Newhouse-Illige, Thin Film Engineer, Swift Coat Inc: process development for the full-size deposition tool

References:

[1] M. Hermle, F. Feldmann, M. Bivour, J. Goldschmidt, and S. Glunz, “Passivating contacts and tandem concepts: Approaches for the highest silicon-based solar cell efficiencies,” *Applied Physcis* Reviews, vol. 7, 021305, 2020.

[2] K. Yoshikawa et al., "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," *Nature Energy*, Article vol. 2, p. 17032, 2017, doi: 10.1038/nenergy.2017.32.

[3] F. Haase, C. Hollemann, S. Schafer, A. Merkle, M. Rienacker, J. Krugener, R. Brendel, and R. Peibst, "Laser contact openings for local poly-Si-metal contacts enabling 26.1%-efficient POLO-IBC solar cells." *Solar Energy Materials and Solar Cells*, 186 (2018): 184-193.

[4] Z. C. Holman, A. Descoeudres, L. Barraud, F. Z. Fernandez, J. P. Seif, S. De Wolf, et al., "Current losses at the front of silicon heterojunction solar cells," *IEEE Journal of Photovoltaics*, vol. 2, pp. 7-15, 2012.

[5] B. Demaurex, S. De Wolf, A. Descoeudres, Z. Charles Holman, and C. Ballif, "Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering," *Applied Physics Letters*, vol. 101, p. 171604, 2012.

[6] M. Leilaeioun, W. Weigand, M. Boccard, Z. J. Yu, K. C. Fisher, and Z. C. Holman, "Contact resistance of the p-type amorphous silicon hole contact in silicon heterojunction solar cells," *IEEE Journal of Photovoltaics* 10, no. 1 (2019): 54-62.

[7] J. Shi, Z. Yu, A. Leilaeioun, K. Fisher, and Z. Holman, "Effects of amorphous silicon thickness variation on infrared-tuned silicon heterojunction bottom cells." *Proceedings of IEEE 46th Photovoltaic Specialists Conference (PVSC)*, pp. 0750-0755, 2019.

[8] V. Linss, M. Bivour, H. Iwata, and K. Ortner. "Comparison of low damage sputter deposition techniques to enable the application of very thin a-Si passivation films." *AIP Conference Proceedings*, vol. 2147, no. 1, p. 040009. AIP Publishing LLC, 2019.

[9] J. Jeong, H. Kim, J. Lee, J. Lee, H. Bae, and Y. Tak. "Characteristics of ITO electrode grown by linear facing target sputtering with ladder type magnetic arrangement for organic light emitting diodes." *Thin Solid Films*, 517, no. 14 (2009): 4043-4046.

[10] J. Mahrholz, S. Shikolenko, B. Szyszka, and T. Jung, "Deposition of amorphous silicon films by gas flow sputtering (GFS)", *Proceedings of the 24th Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2009, pp. 2879-2883.

[11] F. Feldmann et al., "A Study on the Charge Carrier Transport of Passivating Contacts," *IEEE Journal of Photovoltaics*, vol. 8, no. 6, pp. 1503-1509, 2018, doi: 10.1109/jphotov.2018.2870735.

[12] A. Moldovan, F. Feldmann, M. Zimmer, J. Rentsch, J. Benick, and M. Hermle, "Tunnel oxide passivated carrier-selective contacts based on ultra-thin SiO 2 layers," *Solar Energy Materials and Solar Cells*, vol. 142, pp. 123-127, 2015, doi: 10.1016/j.solmat.2015.06.048.

[13] W. Liu, F. Meng, X. Zhang, and Z. Liu, "Evolution of a Native Oxide Layer at the a-Si:H/c-Si Interface and Its Influence on a Silicon Heterojunction Solar Cell," *ACS Applied Materials & Interfaces,* vol. 7, pp. 26522-26529, 2015/12/09 2015.

[14] L. Mazzarella, S. Kolb, S. Kirner, S. Calnan, L. Korte, B. Stannowski*, et al.*, "Optimization of PECVD process for ultra-thin tunnel SiOx film as passivation layer for silicon heterojunction solar cells," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 2955-2959.

[15] J.-I. Polzin, F. Feldmann, B. Steinhauser, M. Hermle, and S. Glunz, "Realization of TOPCon using industrial scale PECVD equipment," AIP Conference Proceedings, vol. 1999, no. 1, p. 040018, 2018/08/10 2018.

[16] C. Hollemann, F. Haase, S. Schäfer, J. Krügener, R. Brendel, and R. Peibst, "26.1%-efficient POLO-IBC cells: Quantification of electrical and optical loss mechanisms," Progress in Photovoltaics: Research and Applications, vol. 27, no. 11, pp. 950-958, 2019/11/01 2019.