Al-Rich AlGaN High Electron Mobility Transistor Gate Metallization Study up to 600°C in Air

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We report a comparative study of three rectifying gate metals, W, Pd, and Pt/Au, on ultrawide bandgap $Al_{0.86}Ga_{0.14}N$ barrier / $Al_{0.7}Ga_{0.3}N$ channel high electron mobility transistors for use in extreme temperatures. The transistors were electrically characterized from 30°C to 600°C in air. Of the three gate metals, the Pt/Au stack exhibited the smallest change in threshold voltage (0.15 V, or 9% change between the 30°C and 600°C values, and a maximum change of 42%), the highest on/off current ratio (1.5×10^6) at 600°C, and a modest forward gate leakage current (0.39 mA/mm for a 3 V gate bias) at 600°C. These favorable results showcase AlGaN channel HEMTs' ability to operate in extreme temperature environments.

Wide and ultra-wide bandgap (WBG/UWBG) semiconductor materials are the enabling technology to realize transistor operation in extreme temperature environments. Their benefits, outlined by Neudeck [1] include reduced thermionic emission-mediated gate leakage and reduced intrinsic carrier effects. Materials such as SiC[2], GaN[3], AlInN/GaN[4], Ga_2O_3[5, 6], and AlGaN[7-10] have been investigated for use in high temperature electronics. Of these, UWBG AlGaN semiconductor devices have great promise to operate in extreme temperatures, with bandgaps reaching up to 6.2 eV and relatively temperature-invariant carrier transport compared to their binary counterparts.[11] Prior reports of Al-rich AlGaN transistors operating at high temperatures highlighted benefits such as large on/off ratios,[7] minor changes in drain current,[9] and operation with minimal changes over a large temperature range.[10]

A major challenge for any transistor operating in elevated temperatures is degradation of gate metal.[12] Prior studies on III-N materials have utilized gate metals such as Ni/Au,[4, 9] Pd/Ni,[13] and various Ni, Pt, Ti, and Au stacks.[14] Oftentimes, elevated temperature device experiments are performed under vacuum[12] or in an inert atmosphere such as nitrogen,[14] but in end-use applications such control of ambient conditions is not always realizable. In air and at elevated temperatures, the gate metals can readily oxidize, which drives modifications to their electrical and mechanical properties. For example, during testing in air Carey[7] observed a metal reordering and oxidation of the commonly used Ni/Au stack for temperatures above 300°C. To enable transistor operation in extreme temperatures and air, an experimental evaluation of gate metallization schemes is needed.

In this study, we examined three Schottky metal stacks, W, Pd, and Pt/Au as gate metallization to Al-rich AlGaN high electron mobility transistors (HEMTs). The Pt and Pd were selected for their large Schottky barrier heights,[15] and W was selected for its high melting point. These transistors

were tested in air from room temperature to 600°C (chuck temperature). The goal was to demonstrate stable electrical properties including threshold voltage (V_{TH}), and on/off current ratio (I_{ON}/I_{OFF}) over a wide temperature range. Furthermore, the gate metal needed to be mechanically stable (i.e., to not delaminate) throughout testing. The favorable results showcase AlGaN channel HEMTs ability to operate in extreme environments and the gate metallization results of this study could potentially be applied to other materials.

Epitaxial structures were grown using metal organic chemical vapor deposition (MOCVD) on 2-inch diameter sapphire substrates with previously prepared AlN templates. First, a 5000 Å thick $Al_{0.7}Ga_{0.3}N$ channel layer as grown followed by a 300 Å $Al_{0.86}Ga_{0.14}N$ barrier layer. Figure 1a presents the epitaxial structure. Post-growth characterization using contactless sheet resistance measurements indicated values ~ 3600 Ω/square, while capacitance-voltage measurements showed V_{TH} = -3 V and two-dimensional electron gas (2DEG) charge concentration of 8×10^{12} cm^{-2}.

Throughout wafer fabrication, standard contact lithography was used for all patterning and electron-beam deposition was used for all metallization steps, unless otherwise noted. Prior to each metal deposition, the wafer was cleaned with oxygen plasma followed by hydrochloric acid. Ohmic metal consisting of 250 Å Ti / 1000 Å Al / 150 Å Ni / 500 Å Au was deposited and underwent rapid thermal annealing at 1100°C for 30 s in nitrogen (~1 Torr). Next, three individual gate metal stacks, (1) 2000 Å W, (2) 2000 Å Pd, and (3) 200 Å Pt / 2000 Å Au, were deposited in the gate areas. Furthermore, wherever there were Ohmic metal contacts, an additional layer of the gate metal was also deposited over the Ohmic metal. The W gate was sputter-deposited, while the other gates were evaporated. The three types of gates were repeated side-by-side across the wafer to allow for electrical comparison between spatially adjacent devices. A 1000 Å thick SiN passivation layer was blanket deposited by Plasma-enhanced chemical vapor deposition, then patterned and etched with reactive ion etching (CF_4 and O_2 plasma) to open electrical access points to the source, gate, and drain. The resulting transistors were circular with a central drain, an exterior source, and a gate in-between (Figure 1b) and had gate lengths of 4.5 µm, and equal gate-to-drain and gate-to-source spacings of 2.75 µm. The gate width, taken at the midline of the gate, was 0.66 mm. The initial specific contact resistance of the Ohmic contacts was 2.5×10^{-2} Ωcm², measured by circular transmission line method.[16]

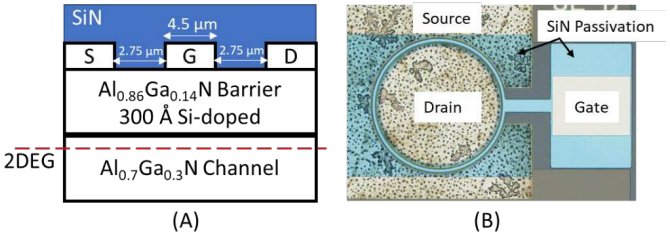

Figure 1. (A) Cross-sectional view of AlGaN HEMT active area. (B) Microscope view of HEMT prior to thermal testing.

A total of nine transistors were tested. The completed wafer was diced into individual test die, and three spatially co-located die were selected for over-temperature testing. Each die included a W-

gated, a Pd-gated, and a Pt/Au-gated transistor. On-wafer testing was performed on a Signatone 1160 probe station capable of characterizing samples from room temperature to 600°C in air. Throughout this report, the chuck setpoint (monitored by an internal thermocouple) rather than the device temperature are given; the low thermal conductivity of the sapphire substrate has been shown to offset (reduce) the actual device temperature by as much as 70°C.[10] A 15-minute delay time after each setpoint ensured the device temperature stabilized prior to electrical test. DC electrical characterization was performed with a Keysight B1500A semiconductor device analyzer. Electrical sweeps included (1) I_D-V_D (drain current vs. drain voltage) at gate biases of -5 V to 4 V in steps of 1V and a source bias of 0 V and (2) I_D-V_G (drain current vs. gate voltage) at respective drain and source biases of 10 V and 0 V.

The extracted V_{TH} (defined as the gate voltage where I_D > 150 µA/mm), I_{ON}/I_{OFF}, and forward gate current (measured at V_G = 3 V and V_{DS} = 10 V) over temperature are presented in Figure 2 and key results are summarized in Table I. The Pt/Au stack exhibited high average V_{TH} stability throughout the investigated temperature range, with only an average 0.15 V increase when comparing 30°C and 600°C data, ~ 9% change from its starting value. However, the Pt/Au contact also exhibited the largest V_{TH} standard deviation, and the average V_{TH} had a range of 0.67 V, between -2.29 V and -1.62 V, changing as much as 42% from the starting V_{TH}. In contrast, the Pd and W gate metals exhibited drops of 0.86 V (50% change) and 2.7 V (160% change), respectively. The large threshold shift exhibited by the W transistors are due to all three failing at 600°C. The Pd and Pt/Au stacks exhibited similar I_{ON}/I_{OFF} behavior over temperature, both with 30°C averages of 2×10^8; these declined with temperature down to 1.5×10^5 and 1.5×10^6, respectively, at 600°C. The W gate metal had comparatively lower I_{ON}/I_{OFF} throughout the entire temperature range, with averages of 2.8×10^5 at 30°C and 8.8×10^2 at 600°C. The lower initial I_{ON}/I_{OFF} of the W gated switches was attributed to sputter deposition induced damage, which increased the off-state leakage current, thereby degrading the I_{ON}/I_{OFF} ratios. With rising temperature, an increasingly large forward gate leakage current ($I_{G,F}$) was observed in the W gated devices (over 0.9 mA/mm at its peak), while the Pd and Pt/Au gates exhibited a preferably less severe increase (0.45 mA/mm peak for both). Lower $I_{G,F}$ values allow for higher gate biasing without the deleterious effects of gate leakage. Notably, the Pt/Au and Pd metals showed reasonable mechanical stability during testing, whereas the W suffered delamination. Of the three metals examined in this study, the Pt/Au stack exhibited the smallest change in V_{TH}, large I_{ON}/I_{OFF}, and relatively modest $I_{G,F}$, and so was determined to be the best choice for high operating temperature gate metal.

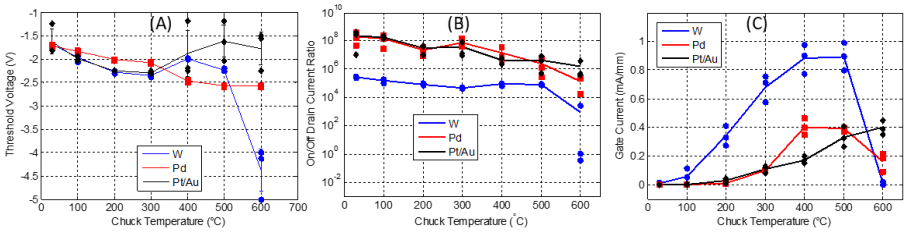

Figure 2. Extracted (A) V_{TH} (bars showing standard deviation), (B) I_{ON}/I_{OFF}, and (c) $I_{G,F}$ at 3 V gate bias for each gate metallizaton on the three tested die from 30°C to 600°C chuck temperature. For all plots, drain-to-source bias (V_{DS}) was 10 V.

Table I. Summary of key characterization results for the investigated gate metals.

Gate Metal	ΔV_{TH} (V) T_{Chuck} = 30 *vs*. 600°C	I_{ON}/I_{OFF} T_{Chuck} = 600°C	$I_{G,F}$ @ V_G=3 V (mA/mm) T_{Chuck} = 600°C
W	-2.69 (Failure)	8.8×10^{2} (Failure)	0 (Failure)
Pd	-0.86	1.5×10^{5}	0.17
Pt/Au	0.15	1.5×10^{6}	0.39

A representative Pt/Au gated device is examined in greater detail in Figure 3, which shows characteristic sweeps from 30°C to 600°C. In Figure 3a, the I_D-V_{DS} sweeps reveal (1) the on-state drain current decreases over temperature by 38% and (2) the Ohmic contacts improve with increasing temperature. First, we attribute the decrease of I_{DS} with increasing temperature to a thermally-induced reduction in electron mobility. In prior work and for a similar AlGaN epitaxial structure, from room temperature to 500°C the mobility dropped from 145 cm²/Vs to 45 cm²/Vs,[10] roughly a 70% decline. However, in this work the impact of the mobility degradation is offset by the improvement in Ohmic contacts. At 30°C, the source and drain contacts exhibit Schottky-like behavior shown by the non-linear I-V sweep in the linear region of the voltage transfer characteristic. As the temperature rises, the sweeps become linear due to increased thermionic emission-mediated conduction at the metal-semiconductor interface of the Ohmic contacts. These combined effects of improved contacts and mobility degradation produced only a modest decline in drain current.

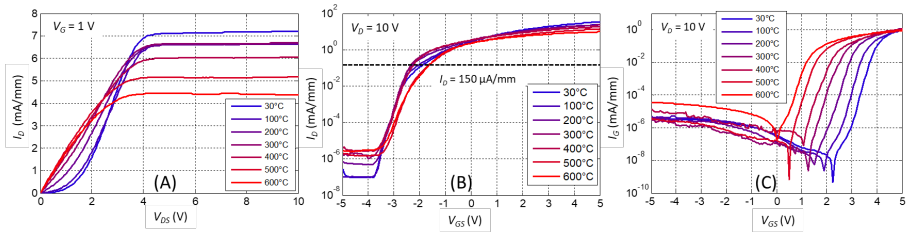

Figure 3. Over-temperature current voltage sweeps of the Pt/Au-gated transistor for (a) I_D-V_D at a 1 V gate bias, (b) I_D-V_G for a 10 V drain bias, (c) I_G-V_G for a 10 V drain bias.

Figure 3b displays the I_D-V_{GS} sweep measured with a drain bias of 10 V. The threshold voltage current limit is indicated by the dashed line. The plot shows that V_{TH} becomes more positive with rising temperature, after an initial decline, agreeing with the results in Figure 2a. The cause of V_{TH} shift above 300°C requires more investigation, but the role of thermionic emission at the resistive Ohmic contacts is a possible contributing factor. The transistor's off-state leakage current, observed at gate biases of less than -4 V, rises from 9×10^{-8} mA/mm at 30°C to 3×10^{-6} mA/mm at 300°C, and then exhibits only minor changes at higher temperatures. The combined relative invariance of both the off-state leakage current and on-state drain current are responsible for the

stable I_{ON}/I_{OFF} ratios discussed earlier. Furthermore, the favorable off-sate leakage behavior showcases the applicability of AlGaN channel HEMTs for use in extreme temperatures. In comparison, other technologies like GaN[3] and Ga_2O_3[6] have exhibited orders-of-magnitude increases in off-state leakage current over similar temperature ranges, although gate optimization could further improve these technologies' performance. Figure 3c illustrates the temperature evolution of gate current; the forward gate leakage turn-on voltage reduces with temperature. However, the absolute current remains less than 1.5 mA/mm for the entire range examined. After cooling back down to 30°C, the transistors did not return to their initial values. The drain current was reduced to an average of 18% of the original value, which shifted the threshold voltage positive. Since the gate metal was also deposited over the Ohmic metal contacts, we suspect that the interactions with the overlying gate metal degraded the Ohmic contacts during the over-temperature testing.

In Figure 4a the voltage transfer characteristic plots of the Pt/Au gated sample measured at a chuck temperature of 600°C showcase the AlGaN HEMT extreme temperature operability. Microscope images of the transistor before and after the 30°C to 600°C characterization are provided in Figure 4b-c, which show no change in edge acuity, indicating mechanical stability of both the gate metal and Ohmic contacts.

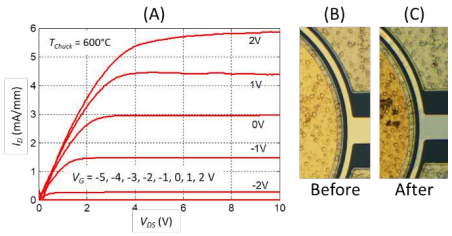

Figure 4. Results of the Pt/Au gated transistor. (A) Voltage transfer characteristic curves taken at a chuck temperature of 600°C. (B-C) Microscope images before and after the over-temperature characterization showing no change in edge acuity.

In summary, gate metals of W, Pd, and Pt/Au on Al-rich AlGaN HEMTs were electrically characterized from 30°C to 600°C in air. Of the three gate metals, the W delaminated at 600°C, causing electrical failure, while the Pt/Au and Pd were mechanically stable throughout testing. The Pt/Au stack exhibited the most favorable results, with the smallest change in V_{TH} between the 30°C and 600°C values (0.15 V, or 9% of its starting value, and a maximum change of 42%), the highest on/off current ratio (1.5×10^6) at 600°C, and a modest $I_{G,F}$ (0.39 mA/mm for a 3 V gate bias). The favorable results showcase AlGaN channel HEMTs ability to operate in extreme environments.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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