Final Technical Report (FTR)

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Submitting Official Signature		

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Executive Summary: Thin film cadmium telluride is one of the most successful photovoltaic technologies on the market today. Second only to silicon in yearly output and accounting for 40% of U.S. utility-scale photovoltaic installation, CdTe is known for its ease of manufacture, ideal bandgap, and low levelized cost of energy. Despite its commercial success, CdTe underperforms compared to its theoretical potential. The current world record CdTe device is only 21.0% compared to a theoretical maximum of 33.1%. This significant discrepancy in efficiencies can mostly be attributed to the poor open-circuit voltage of CdTe devices. Compared to silicon technologies, CdTe has a large voltage deficiency, exceeding 250 mV.

While copper doping has traditionally been used for CdTe devices, it has proven to be incapable of sufficiently doping CdTe. Copper typically dopes CdTe in the 10^{14} to 10^{15} holes/cm^3 range where most models predict that 10^{16}–10^{17} is needed. Additionally, interstitial copper is a fast diffuser in CdTe, and can lead to numerous stability issues. As an alternative to copper, this work explores arsenic as a dopant for CdTe. Using a novel arsenic doping technique, hole concentrations greater than 10^{15} cm^{-3}, microsecond lifetimes, and increased radiative efficiency are achieved. These are important prerequisites to achieving higher voltages.

Achieving high doping levels alone is not sufficient to achieve higher device performance. A well-passivated and carrier selective contact is needed to ensure that electron-hole pairs do not recombine and are extracted as useable energy. Aluminum oxide has been shown to passivate CdTe surfaces. This work illustrates the explorations of using Al_2O_3 as a passivation layer, pairing it with highly doped amorphous silicon as a hole contact, resulting in excess-carrier lifetimes up to 8 µs, the highest reported to date for polycrystalline Cd(Se)Te.

Although the inclusion of arsenic doping and an aluminum oxide back contact are each explored separately, the combination of both methods result in massive improvements to the carrier lifetime, interface passivation and radiative efficiency. Through this combination, microsecond lifetime and External Radiative Efficiency of over 4% are achieved. The excellent ERE values measured here are indicative of large quasi-Fermi level splitting, leading to an implied voltage with multiple device structures of nearly 1 V and an implied voltage of 25%.

Finally, while CdSeTe serves as a more promising photovoltaic absorber candidate compared to CdTe, certain difficulties remain which must be addressed. Careful selection of processing conditions is shown to create a dense and large-grained film while eliminating wurtzite-phase crystal growth, which has been shown to degrade device performance. Surprisingly, as-deposited CdSeTe is shown to be n-type or nearly intrinsic rather than the previously supposed p-type. This necessitates additional steps to account for very poor hole conductivity, which can produce zero-current devices if not addressed. Challenges notwithstanding, CdSeTe absorbers are shown to be a key component in devices capable of a photovoltaic conversion efficiency of greater than 25%.

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BACKGROUND: The goal of this research is to demonstrate record efficiencies for CdTe based polycrystalline devices with processes suitable for large-scale industrial processing. The target is to demonstrate efficiencies of at least 21% at the end of the project and potentially 25%. To achieve such efficiencies, three metrics are critical: (a) carrier concentration in absorber greater than 10^{16} cm^{-3}; (b) minority carrier lifetime greater than 10 ns with doping, and (c) interface recombination less than 1000 cm/s in a device structure. The carrier-concentration metric is particularly critical because current values in the 10^{14} cm^{-3} range are a major limitation to the voltage of CdTe cells, and hence their efficiency. Hence, the overall thrust of the project is to increase the absorber carrier concentration with judicious doping of group-V elements, initially arsenic, with high carrier lifetime and low interfacial recombination.

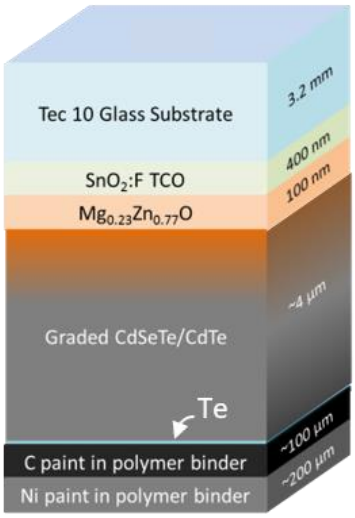

Figure 1: Schematic of (not to scale) baseline film stack. Best efficiency for such a device is recorded at 20.14% with AR coating

Substantial progress has been achieved for fabrication of higher efficiency CdTe-based photovoltaic devices using Se based graded ternary alloys for p-type absorber deposition. The baseline capability at Colorado State University has demonstrated cells with efficiency exceeding 20% using a 1.4eV absorber layer. The open-circuit voltage for such device is typically measured at about 850 mV and short-circuit current above 28 mA/cm^2. With some optimization a voltage of 880 mV has been achieved with efficiency greater than 19%.

The doping and lifetime in baseline CdTe cells are: 10^{14} cc^{-1} by capacitance vs voltage measurements for doping and typically 2-4 ns lifetime. Since all the parts of the cell except TCO-coated glass are fabricated in-house, significant optimization in device fabrication process has been employed to meet the proposed project goals. The cell structure consists of a TCO front contact, $Mg_xZn_{1-x}O$ (MZO) buffer, graded CdTe-$CdSe_xTe_{1-x}$ (CST) absorber, $CdCl_2$ passivation of the deposited film stack and Cu/Te combination to form the back contact. A schematic (not to scale) of this device structure is shown in figure 1. The efficiency was measured with anti-reflection (AR coating).

The primary objective of the project is to produce CdTe-based solar cells that utilize group-V element doping (i.e. arsenic) to increase the absorber carrier concentration to the mid-10^{16} cc^{-1} range to significantly increase the cell voltage by 100 mV and increase the cell efficiency to 21%. In addition to the successful doping, the project will require that

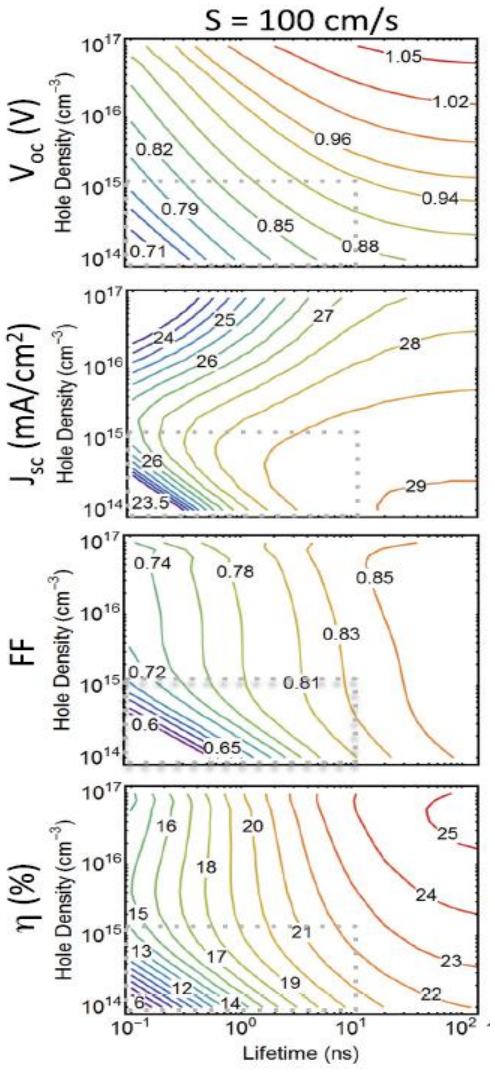

Figure 2: Calculated impact of hole density and lifetime on cell parameters (*Kanevce et al*)

a bulk lifetime above 10 ns be maintained, that there is a minimal hole barrier at the back interface, and that interfacial recombination velocity be reduced to ~1000 cm/s.

Voltage deficit in CdTe-based photovoltaics is a primary issue and needs to be addressed to achieve higher conversion efficiency. The highest open-circuit voltage reported for polycrystalline CdTe device is about 890 mV which is much lower than the limit for 1.5 eV material of about 1.2 V. As per simulation results published by *Kanavace et al* (figure 2), hole density of 10^{16} cc^{-1} should reduce the voltage deficit paving way for polycrystalline CdTe devices with over 1 V open-circuit voltage (Kanevce et al. 2017). We have demonstrated recombination velocity of ~80 cm/s and a bulk recombination lifetime of 1.4 µs with our polycrystalline CST absorber films without arsenic doping.

Film Deposition and Device Fabrication: To further the understanding of arsenic doping on CdTe based photovoltaic devices, over 700 small area research devices with arsenic doping have been fabricated, measured for performance, and extensively characterized. These devices were fabricated using two different inline deposition systems equipped with multiple heating and sublimation sources. The primary deposition system called the Advanced Research Deposition System (ARDS) (Swanson et al. 2016) had 9 process stations while the second system had 2 processing stations and is called the Research Test Chamber (RTC). An advanced co-sublimation source was installed in each of these

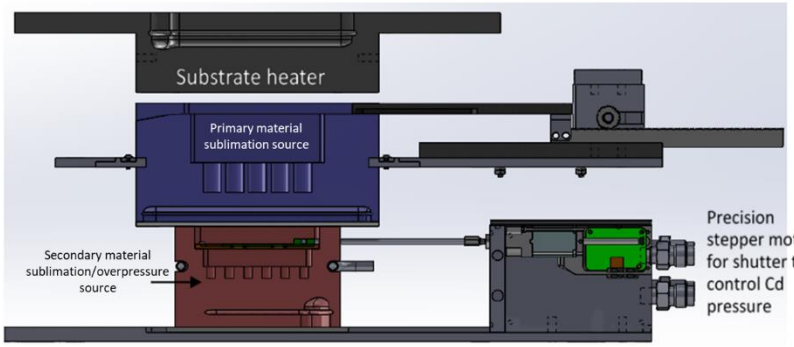

Figure 3: CAD cross section of the described co-sublimation hardware.

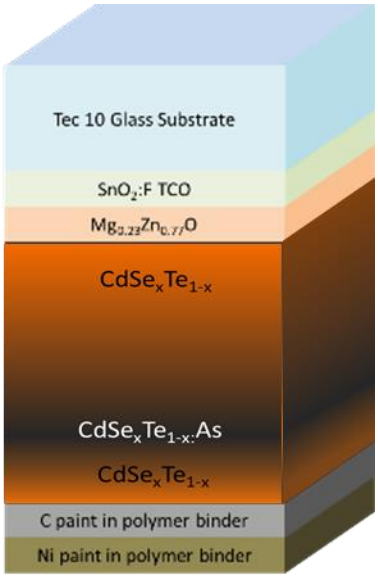

Figure 4: A schematic of device structure discussed in this section (not to scale)

systems. Advanced co-sublimation, as the name suggests, is designed and developed for simultaneous sublimation of two different materials in a controlled fashion to deposit the desired composition of the respective materials on the substrate (Munshi et al. 2018). A schematic of such a co-sublimation source is shown in figure 3. This arrangement enabled researchers to deposit arsenic doped source charge (CdTe:As or $CdSe_xTe_{1-x}$:As) under cadmium overpressure for enhanced incorporation of arsenic in the film and achieve desired activation of dopants.

PROJECT OBJECTIVES: There are several studies that we have used to improve our scientific understanding and refine our device fabrication process aimed to achieve the final objective of this project. These results are discussed in detail later in this report.

At the Go/No Go point of the project the following proposed milestones have been met.

- ✓ Demonstrate carrier concentration >10^{16} cc^{-1}
- ✓ Recombination lifetime τ > 10 ns
- ✓ Go/No Go Metric – device efficiency η = 20%

In addition, at 24 month point of the project –

- ✓ Demonstration of surface recombination velocity S < 10^4 cm/s

PROJECT RESULTS AND DISCUSSION:

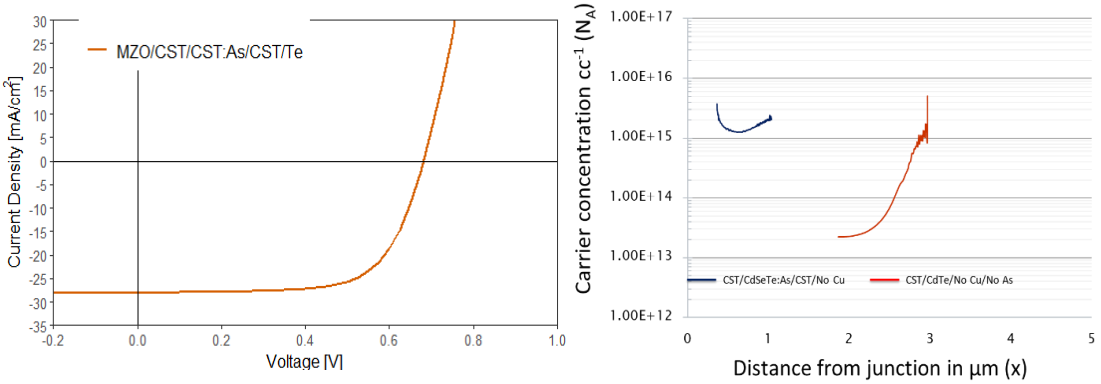

Figure 5: (left) J-V curve for a device fabricated using the device structure shown in figure 4, and (right) C-V curve showing comparison of carrier concentration vs distance from junction for a device with Arsenic doping (blue) and one with no doping (red). The device with no doping is from a different substrate.

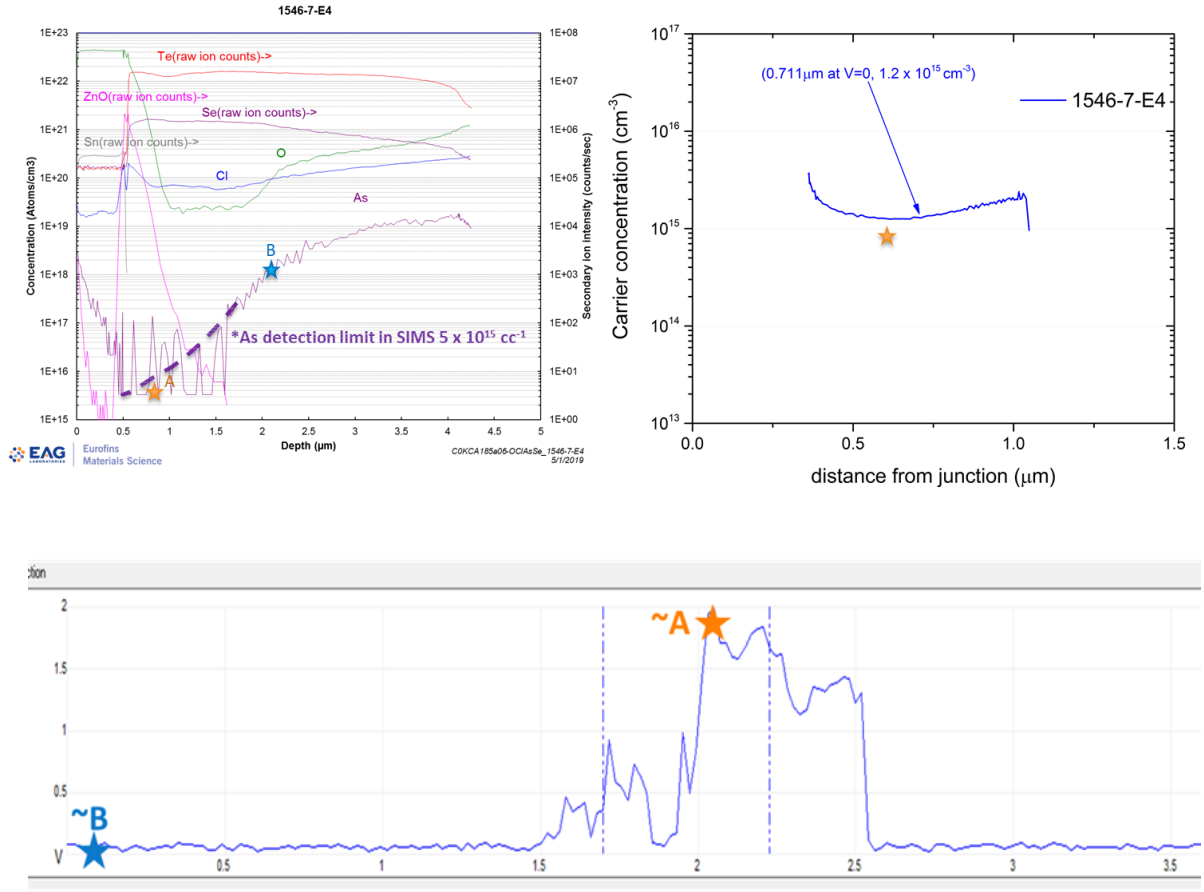

Figure 6: (top left) SIMS profile of the device structure under investigation, (top right) C-V curve showing carrier concentration of the arsenic doped device, and (bottom) the scanning capacitance microscopy scan of the device across the thickness of the device.

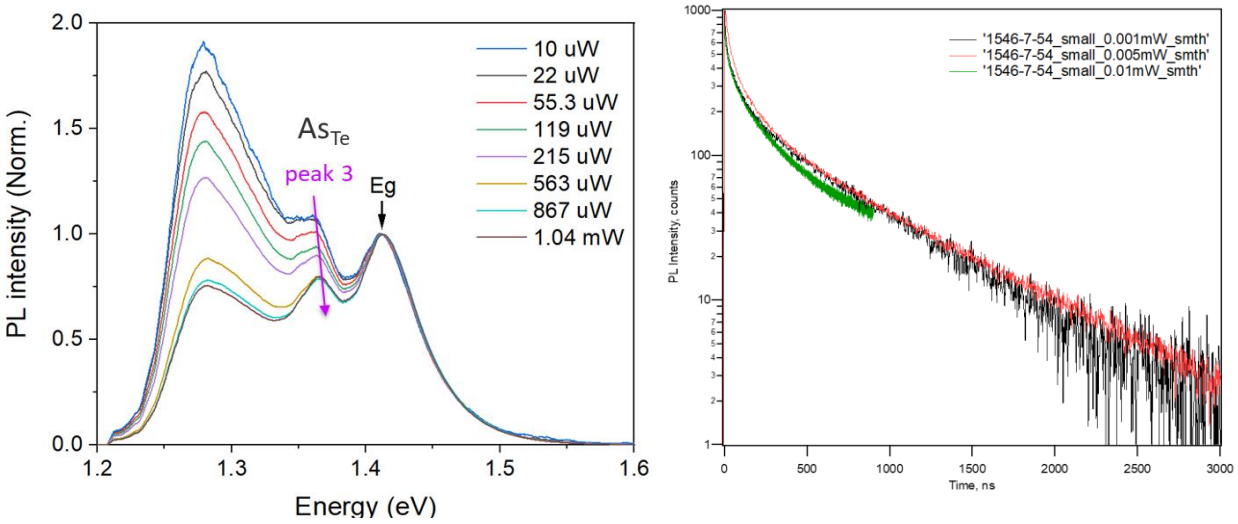

Figure 7: (left) room temperature PL measurement showing distinct As_{Te} peak, and (right) TRPL decay curves showing recombination lifetimes of about 620 ns.

Results from the same substrate: During the recent quarterly feedback, it was requested to provide data from one sample. This is provided in this section and the sample is 1546-7 in our records. The device structure as shown in figure 4 was fabricated. Here a CdSexTe1-x (x=0.4) in source charge) film was deposited on MgxZn1-xO transparent buffer layer. Following that, the substrate was transferred to another inline system

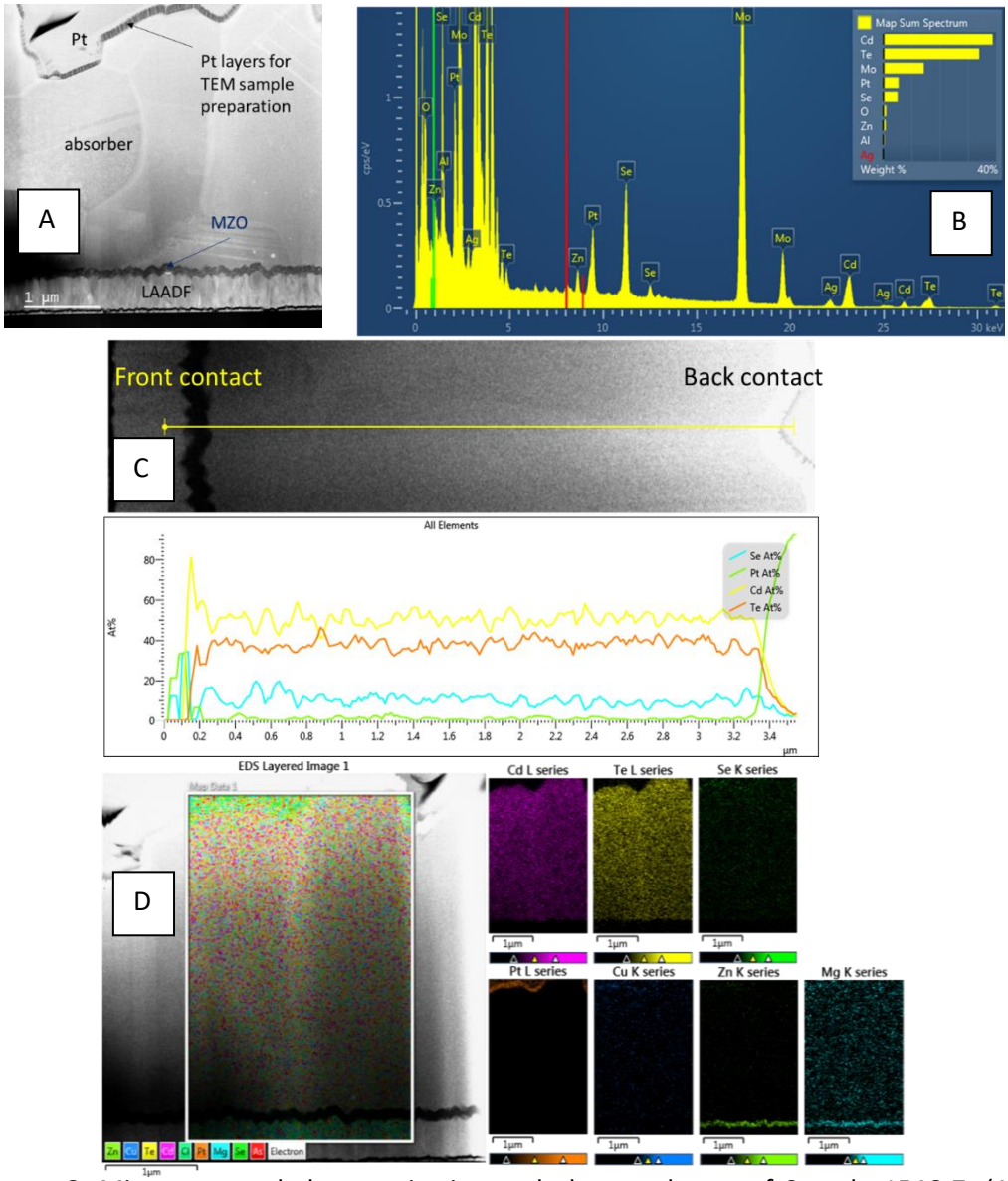

Figure 8: Microstructural characterization and elemental map of Sample 1546-7. (A) Sample has large grains and low density of stacking fault, (B) The red and green lines are Cu peak locations, no Cu detected in the film; Mo signal comes from the TEM grid, (C) In the absorber region, line profile shows 50%Cd with 40%Te and 10%Se (atomic percentage) uniformly distributed. It confirms with EDS map that there is no pure CdTe layer. (D) EDS shows Cd Te and Se distribute almost uniformly. The EDS map doesn't show pure CdTe layer in absorber.

equipped with the co-sublimation source shown in figure 3 that was loaded with $CdSe_xT_{1-x}$:As (x=.40 in source charge). Doped source charge was fabricated at Washington State University and had ~ 1E20 cc^{-1} As in the source material.

CdTe:As and CdSeTe:As source materials were prepared by the High Pressure Bridgman (HPB) growth technique, performed at Washington State University, to melt CdTe, CdSe, and Cd_3As_2 with Cd overpressure as described in (Al-Hamdi et al. 2020). When it was fabricated, it was initially hypothesized that the arsenic would be completed dissolved as monoatomic arsenic. If this were the case, then as the source material sublimated, single arsenic adatoms would impinge upon the growing film to become As_{Te}. To investigate possible sources of the defect-heavy films, these source materials were studied using a Scanning Electron Microscope (SEM) equipped with Energy Dispersive X-Ray Spectrometry (EDS). It was soon discovered that arsenic was not dissolved into the source material as single atoms but rather had a tendency to cluster into areas of high Cd_3As_2 concentration, as the EDS maps in Figure 9 for CdSeTe:As and Figure 10 for

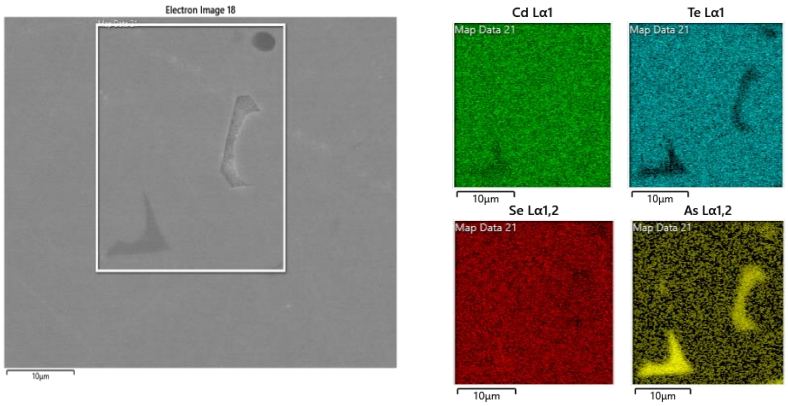

Figure 9 - SEM/EDS map for CdSeTe:As source charge showing areas of high arsenic concentration, microscopy images taken by University of Illinois at Chicago.

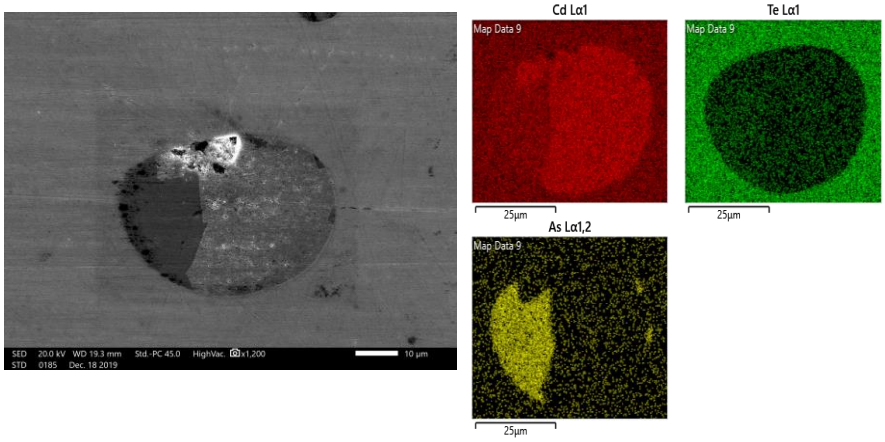

Figure 10 - SEM/EDS map for CdTe:As source charge showing areas of high arsenic concentration, microscopy images taken by University of Illinois at Chicago

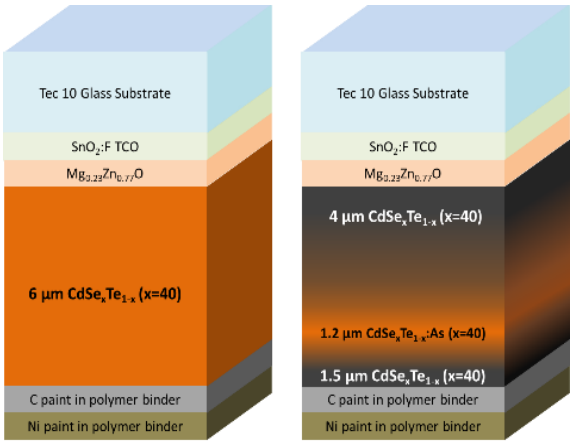

Figure 11. Schematic of fabriacated devices. (Left) device with no doping and copper doping, (right) device with arsenic doping. (not to scale)

CdTe:As display. These findings are corroborated by literature, where Burton et al similarly found arsenic clusters in MBE-deposited films (Burton et al. 2018).

In figure 5 (left), the J-V curve for this device is shown while the plot in figure 5 (right) shows a C-V curve where the bottom of the curve for an undoped device (red) shows carrier concentration of about 1E14 cc^{-1} while the one with arsenic doped CdSeTe layer has a carrier concentration of 1E15 cc^{-1}.

To reliably measure the doping concentration in these devices, one of the devices from the same substrate was sent to EAG Laboratories for scanning capacitance microscopy (SCM). In addition, SIMS analysis of the device was performed. To overcome this limitation of the roughness, the films were delaminated at the front junction and the SIMS measurement were performed from the front junction. This substantially reduced the effect of roughness on the SIMS result. It can be seen from figure 6, the As incorporation reached ~1E19 cm^{-3}.

Devices from this substrate were further studied at the National Renewable Energy Laboratory by Dr. Darius Kuciauskas and Dr. Siming Li using room temperature photoluminescence and time-resolved photoluminescence (TRPL). Using photoluminescence (figure 7 left), a defect peak was identified that represents emission from As_{Te} which is the arsenic form most suitable for this application. This further emphasizes that the arsenic in the deposited film with our process is sufficiently doping the device. Figure 7 (right) shows TRPL decay curves and the recombination lifetime here was measured to be about 620 ns. The green curve is from a measurement that had to be abandoned during collection since the decay time was longer than the laser pulse. The high lifetime is due to band bending caused by the grading of carrier concentration.

The same sample was also characterized by STEM (scanning transmission electron microscopy) at UIC and the results are presented below:

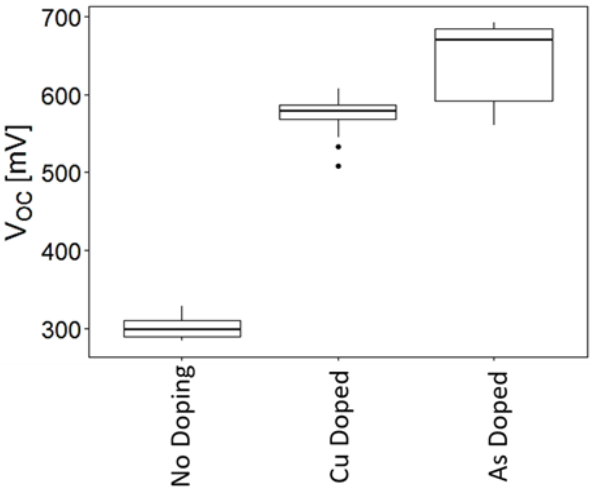

Figure 12: Measured open-circuit voltage on device with no doping, copper doping and arsenic doping.

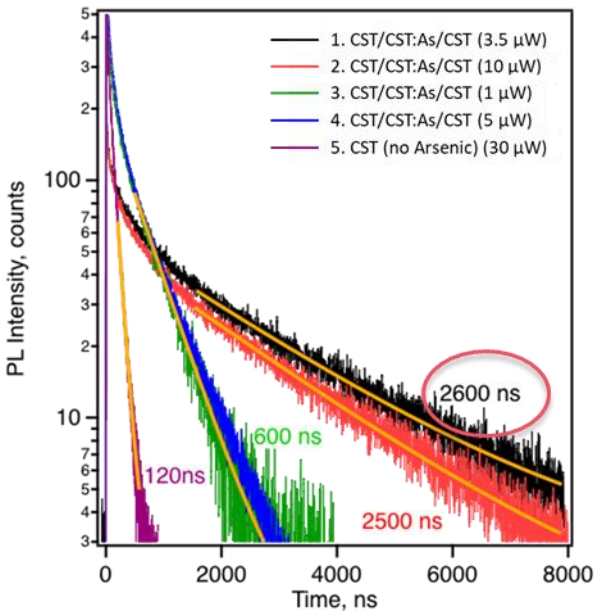

Fig. 13. Low-injection 1PE TRPL for device listed in the legend.

These results clearly show that the approach used in our process of depositing arsenic doped source charge in Cd-overpressure and then using $CdCl_2$ passivation as a means of diffusing the arsenic in the film results in high carrier concentration and high lifetimes. No segregation of arsenic at the grain boundaries or interfaces has been observed. This approach provides the most promising method of doping CdTe-based devices with arsenic to achieve the proposed goals of device efficiency >21% (potentially 25%) with an open-circuit voltage greater than 950 mV.

<u>Electrical characterization of other devices -</u>

Many devices were fabricated and studied. To understand the effect of arsenic doping and to compare the performance to Cu doped and undoped devices, similar films with arsenic doping and Cu doping were fabricated. A schematic of these device structures is shown in figure 11.

Devices with arsenic doping showed improvement in open-circuit voltage (V_{OC}). As showed in figure 12, doping with copper improved the average V_{OC} from ~300 mV to nearly 600 mV. Arsenic doped devices showed a V_{OC} of about 650 mV. Two devices were examined using capacitance-voltage (CV) and showed carrier concentration of $1.28x10^{15}$ cc^{-1} and $4.2x10^{15}$ cc^{-1}. This is substantially higher than $2.35x10^{14}$ cc^{-1} observed with the Cu doped device. Some devices were characterized using scanning capacitance microscopy (SCM) to measure the carrier concentration further away from the depletion region. The carrier concentration at about 3 µm from the junction was measured at about $1x10^{18}$ cc^{-1}. When this was compared to secondary ion mass spectroscopy (SIMS) profile it showed a very high arsenic dopant activation.

Low-injection time-resolved photoluminescence (TRPL) decays measured with excitation at 640nm are shown in Figure 13. After pulsed laser

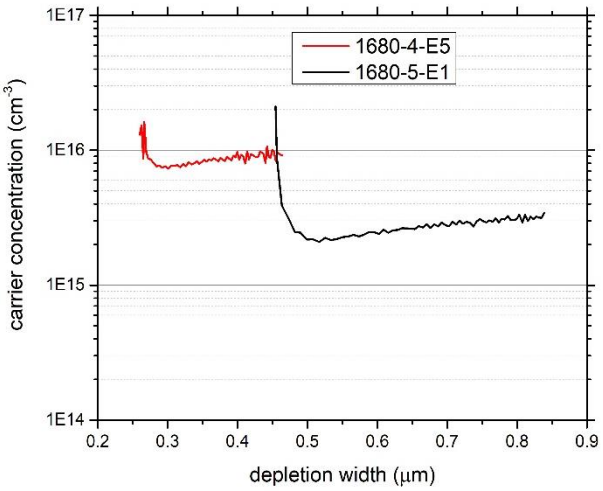

Figure 14: Capacitance-Voltage plot showing high carrier concentration with arsenic doping.

excitation, electrons drift in the space charge field to the MZO interface and holes drift to the back contact. After quasi-equilibrium is established (drift/diffusion dynamics is over) we observe the slower component of the decay. Lifetime values for such "τ_2" dynamics are indicated in the figure 13. Decays at two injections are shown for samples 1 and 2 (2.5-2.6 µs) and samples 3 and 4 (600ns), where near-identical TRPL confirms low injection condition. **Qualitatively, data in figure 13 indicates that bulk lifetime exceeds 200 ns for samples 1-4, and front interface recombination velocity was ~100 cm/s for samples 3 and 4 and <100 cm/s for samples 1 and 2.**

Carrier concentration of 1E16 cm^{-3} have been measured on devices with shorter $CdCl_2$ times. Carrier concentration of 1E16 cm^{-3} have also been seen at V=0 in devices. Figure 14 shows carrier concentration for these devices.

Champion Device: Another important milestone that has been achieved using a $CdSe_xTe_{1-x}$/CdTe graded absorber device with copper doping was the demonstration of 20.14% efficiency. The J-V plot for this is shown in figure 15 along with its performance parameters. **This also meets the Go/No Go metric proposed at the start of this project. Many devices with efficiencies greater than 19% without AR coating have been demonstrated. Many substrates with average efficiency greater than 18.2% have also been demonstrated. These substrates have 25 devices each.**

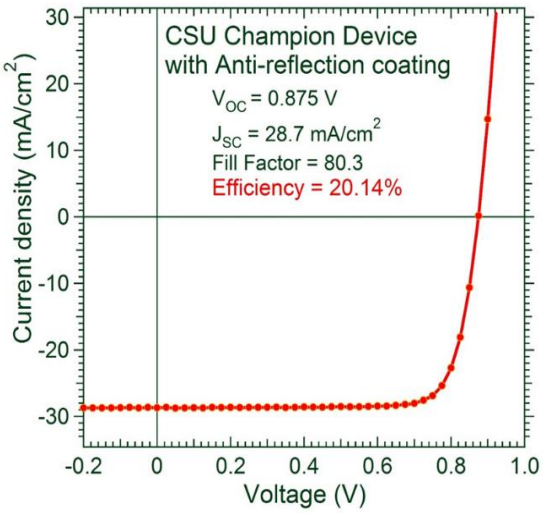

Figure 15: CSU Champion Device with AR coating demonstrated efficiency >20%

<u>Understanding the effect of thickness and overpressure conditions</u>: A few experiments were recently performed to evaluate specifically the effect of thickness of the arsenic doped absorber film and later the effect of amount of Cd overpressure during deposition of such films. These absorbers had the structure CST/CdTe/CST:As/Te. In these devices the CST:As was used to make a doped layer at the back in place of the normal copper doping.

As can be observed from figure 16, a thinner layer of arsenic doped CST layer has better device performance as compared to a thicker device. However, in this particular case, the device performance with arsenic doped film was not comparable to the baseline which was later improved. It is noted that the buffer layer used in the front is MZO doped with Ga (GMZO).

Following up on this study, devices were fabricated with a similar variation in arsenic doped film thickness deposited under two Cd-over pressure conditions. Figure 17 shows

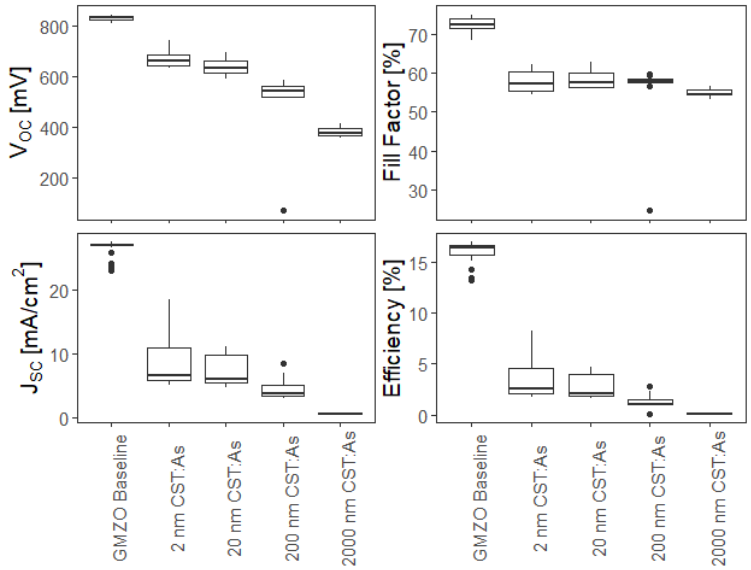

Fig. 16. Boxplot showing a CdSeTe/CdTe control device as compared to identical device structure with varying arsenic thickness of arsenic doped layer deposited at the back of the device.

a distinct trend where a thinner CST:As layer at the back with higher Cd-over pressure is favorable for improved device performance. Here devices with 'No Cd OP' meaning no cadmium overpressure were fabricated with the Cd vapor source operating at 190°C while the ones with cadmium overpressure (w/Cd OP) had the cadmium source operating at 210°C.

These results show a clear indication towards deposition of thinner arsenic doped layer at optimal Cd vapor pressure

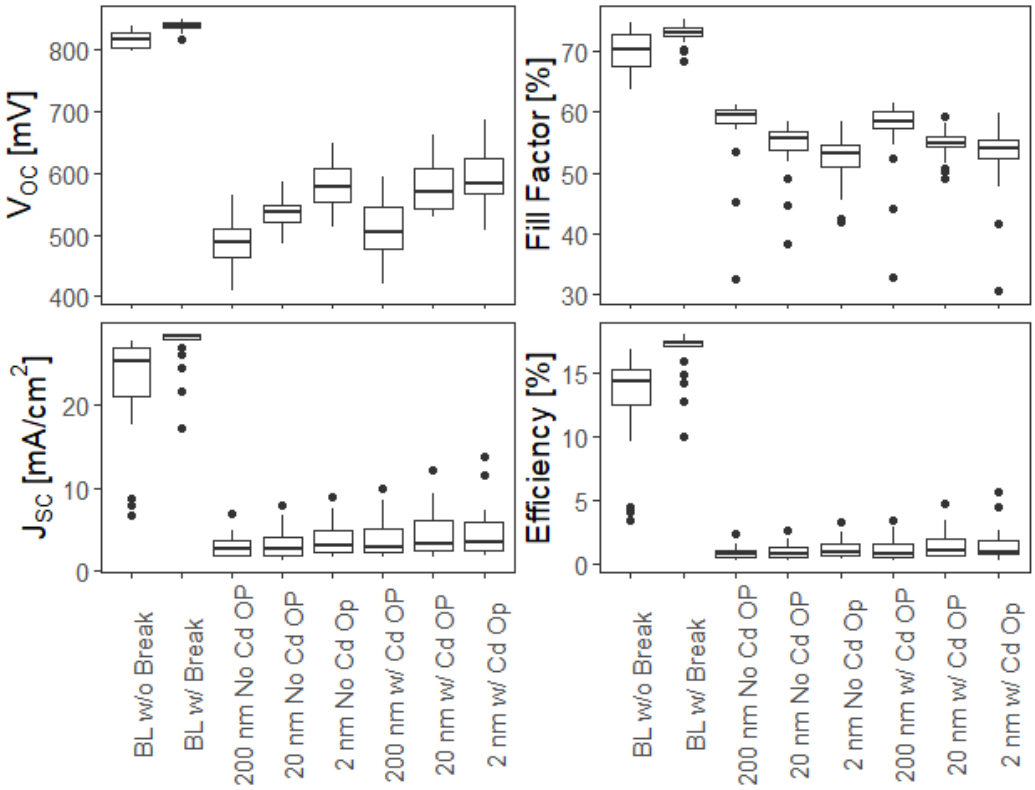

Fig. 17. Boxplot showing a CdSeTe/CdTe control device as compared to identical device structure with varying arsenic thickness and Cd-overpressure during arsenic doped layer deposition at the back of the device.

to be a necessary process step in fabrication of well performing arsenic doped devices. The experiments with Cd overpressure in Fig.16 were done immediately after the no Cd overpressure condition and resulted in changes in the Cd pellets. These changes were subsequently removed by longer operation under Cd overpressure conditions. With such optimization, devices were fabricated on identical device structures. It is important to note that the $CdCl_2$ passivation treatment at 450°C is performed after the deposition of the CST:As film. While arsenic doping was almost an in-situ process and $CdCl_2$ treatment at 450°C was performed after arsenic deposition. This also suggests that arsenic is a substantially more stable dopant since Cu doped film exposed to such temperatures would be highly detrimental to its performance. The stability of As doped layer in $CdCl_2$ treatment has later been repeated by our group validating the repeatability of the process.

Verification that doping improves performance:

The device structure was –MZO/CST 0.5 micron/CdTe 3 microns/5 nm of CST:As/Te/C/Ni_{-x}

Cells and related structures: Several different device structures were fabricated with varying film thicknesses and stack configuration. Performance of some devices is shown in figure 17. The device performance shown in figure 18 has the best device performance observed so far in this study with arsenic doping. **Device efficiency of this device was observed to be 16.8%**. These results demonstrate that significant optimization of the process and the device structure will be needed to demonstrate the benefit of increased carrier concentration due to As.

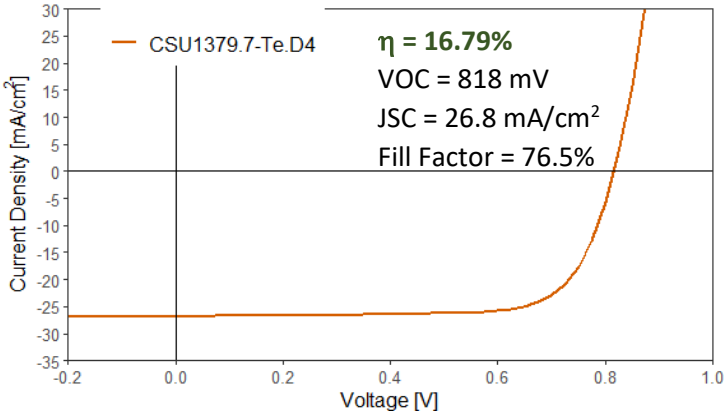

Fig. 18. J-V curve for the best performing arsenic doped device fabricated in this study.

Determination of the optimal source materials for higher absorber carrier density: Three different source materials have so far been used in these experiments that contained arsenic as a dopant in varying proportion in the source charge. So far CdTe:As with 10^{18} cc^{-1} arsenic in the source charge seems to be optimum within the studied materials but they may be specific to particular process under study.

Analysis of choice of device structure – After initial results were achieved in this project, the device structure was altered to include doping of $CdSe_xTe_{1-x}$ layer as the primary doped layer replacing the initial idea of using CdTe:As as the primary doped layer. The justification for such a change was identification of potential of As being a more efficient dopant in $CdSe_xTe_{1-x}$ than CdTe. This hypothesis was verified using first

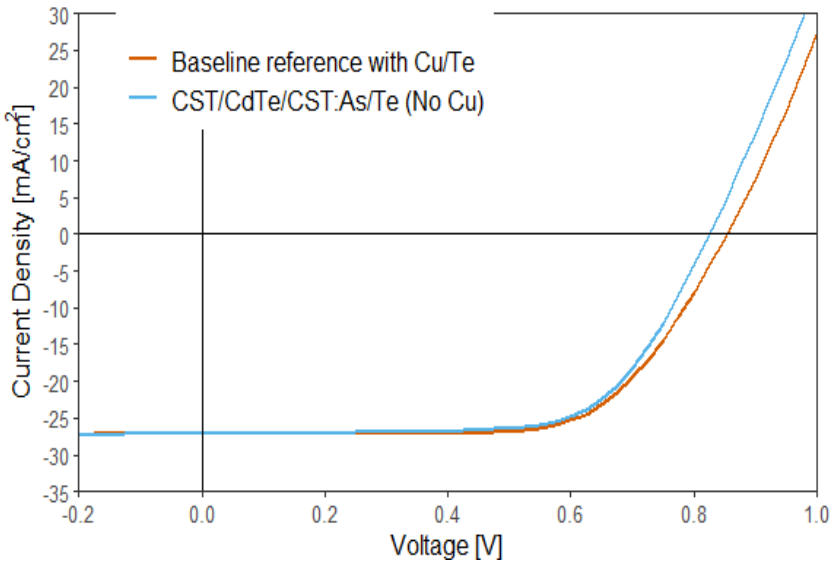

Fig. 19. J-V plots comparing performance of CST/CdTe device structure with copper and arsenic doping. Arsenic doping here shows lower Voc but a relatively higher fill-factor.

principles Density Functional Theory simulation to identify the energetics associated with As doping of both these material candidates.

Doping $CdSe_xTe_{1-x}$ (CST) with As, can allow As to occupy either Selenium site (As_{Se}) or Tellurium site (As_{Te}). This work therefore uses first principles approach to study the behavior of As_{Se} and As_{Te} in $CdSe_{0.11}Te_{0.89}$ bulk. Density Functional Theory (DFT) with Linear Combination of Atomic Orbitals (LCAO) basis sets have been used to simulate the As doped $CdSe_{0.11}Te_{0.89}$ structure consisting of 54 atoms. The simulations have been performed using Synopsis QuantumATK software and this is one of the first uses of this approach demonstrated for the study of $CdSe_xTe_{1-x}$ material. The energetics has also been calculated to understand the stability of As going into Se and Te sites.

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DFT calculations revealed that for As_{Te}, there was a release of energy=0.56 eV/atom, while for As_{Se}, the release of energy was 1.36 eV/atom, making Se more preferred choice for As atoms to go to in CST compounds. A similar calculation was done for As_{Te} in CdTe, where the energy release was 0.77 eV/atom.

This clearly proves the hypothesis that $CdSe_xTe_{1-x}$ is a better candidate for As doping when compared to CdTe and thus the project used this device structure for the experiments and studies.

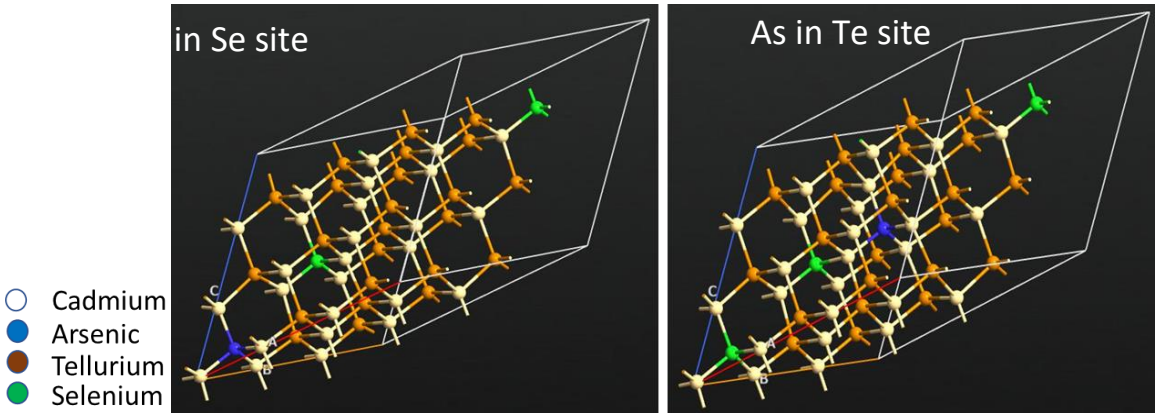


Figure 20: Computational model of CdSexTe1-x with SeAs occupying Se site and As occupying Te site. The 54-atom model was developed and computational analysis was performed using Synopsys QuantumATK.

SCAPS device simulation to understand limitation – In many devices with As doping at the back, loss of current in the devices has been observed. Device results, characterization, microscopic and elemental analysis, etc. show that the films and devices fabricated have all the desired characteristics that would lead to devices with efficiency greater than 21% and demonstrate open-circuit voltage >1V. However, such performance has not yet been achieved and the underlying reasons to overcome such limitations are being identified and means of mitigating them are being extensively explored.

This has also been modeled using SCAPS one dimensional simulation. This simulation result is shown in figure 21. It was observed that as the lifetime at the back of the device was decreased, a reduction in short-circuit current (J_{SC}) was observed. A lower V_{OC} was also observed, this aligns well with the experimental results.

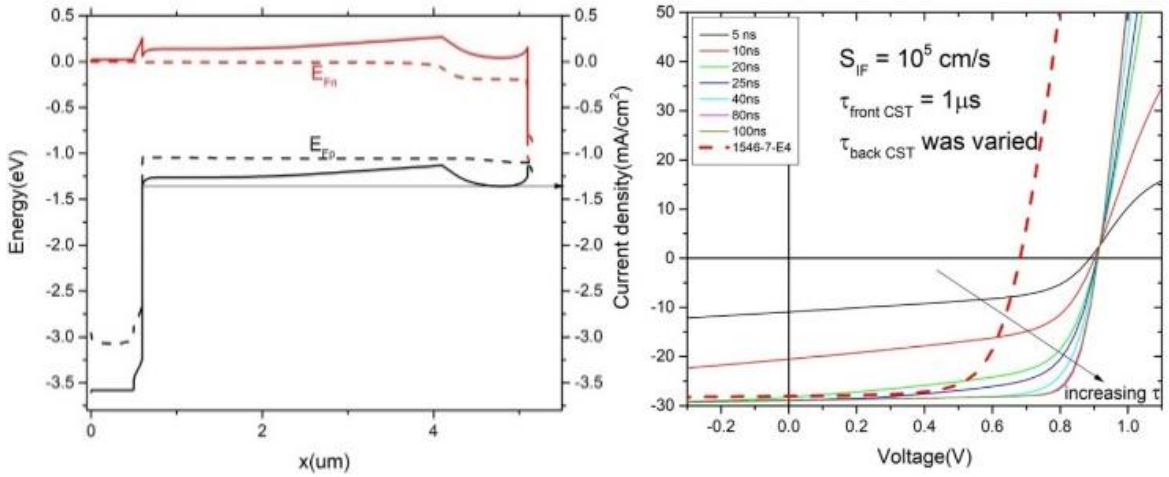


Fig. 21. SCAPS model of arsenic doped device and effect of increasing interface recombination velocity at the MZO/$CdSe_xTe_{1-x}$ interface.

DFT results for graded $CdSe_xTe_{1-x}$/CdTe interface - Grading Se in CdTe using $CdSe_{0.4}Te_{0.6}$ (CST 40) and $CdCl_2$ treatment have shown better devices performance in CST 40/CdTe solar cells. This work therefore uses first principles approach to study the band alignment of graded Se in CdTe. Density Functional Theory (DFT) with Linear Combination of Atomic Orbitals (LCAO) basis sets was used to simulate the graded CST40/CdTe interface. The simulations have been performed using Synopsys QuantumATK software. DFT coupled with the Green's function method was implemented to accurately describe the CdTe/Te interface using semi-infinite boundary conditions as oppose to periodic boundary conditions used in conventional DFT slab-models. Understanding these interfaces and their effect on device behavior will be important for optimization of device structure for the final deliverable under this project.

Figure 22 (a)-(f) describes the grading of Se in CdTe. The model tried to emulate the SIMS result shown in figure 6. The following assumptions were made while simulating the Se graded structure:

- The CST film was CST 37.5 ($CdSe_{0.375}Te_{0.635}$) instead of CST40 to begin with.
- The concentration of Se grading was assumed to decrease uniformly (6.25%/2 unit cells) as we move further into the CdTe film.
- The Se atoms at Te site were substituted randomly.
- CST 37.5 and CdTe were oriented (111) in the model. This was done as CST and CdTe films have preferred (111) (XRD results).

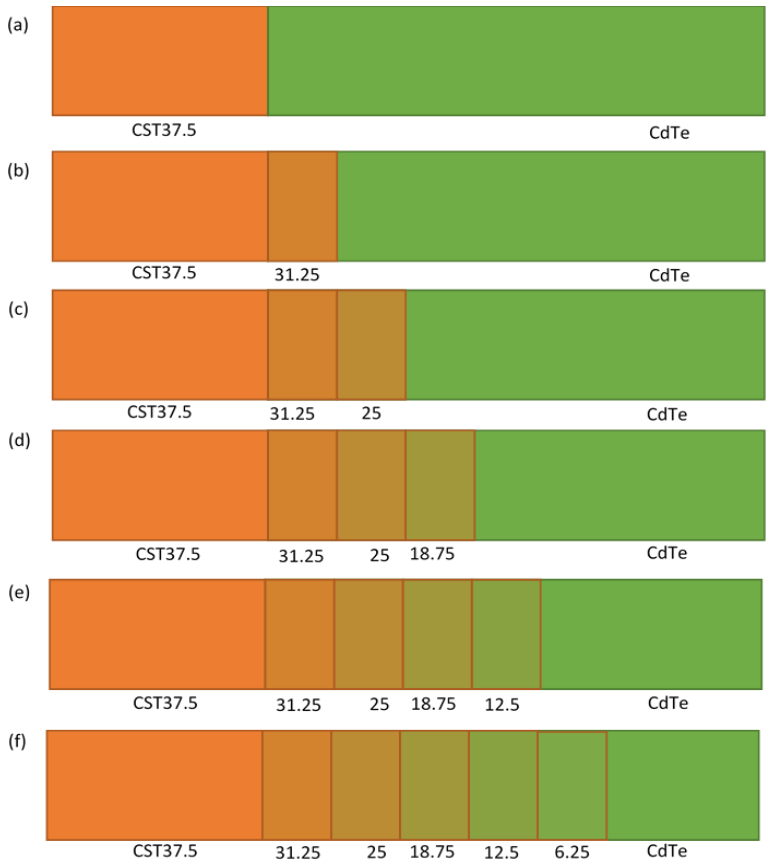


Fig. 22. (a)-(f) showing the Se grading decreasing uniformly in CdTe. The number indicates the % Se atom.

Overall, the model is a first order approximation of Se grading in CdTe.

The band alignment for all the above graded Se CdTe is shown in Figure 22 (a)-(f), corresponds to the structures in Figure 23 (a)-(f) respectively.

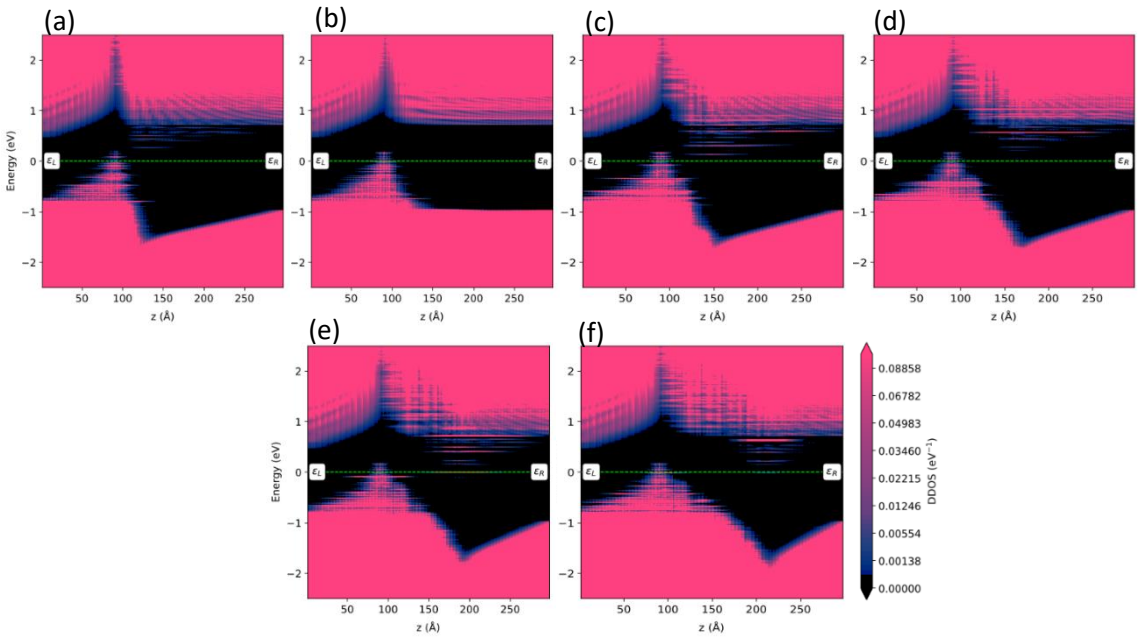


Figure 23. (a)-(f) showing the band alignment for corresponding Se graded structure shown in figure 22 (a)-(f).

The band alignment results shows a pickup in the conduction band. This suggests that grading CST is acting as an electron reflector. Also there is a dip in the Valence band which is dependent on the length of Se grading in CdTe. This magnitude of the energy dip in the valence stays constant but keeps shifting to the point where Se was graded. However, valence band becomes flat for CST37.5/31.25(graded Se)/CdTe case. More simulations are underway at this point to understand this mechanism.

Experimental studies to optimize arsenic dopant activation - Farrell *et al* provided convincing evidence that arsenic incorporation is heavily affected by the presence or absence of cadmium overpressure during film growth. Based on these results, Co-sublimation was utilized to fabricate films under cadmium overpressure. In this configuration, two sublimation sources were installed one on top of the other. The sources were thermally isolated so they could each maintain different temperatures, but the upper source had channels bored into it to allow the vapor from the lower source to reach the

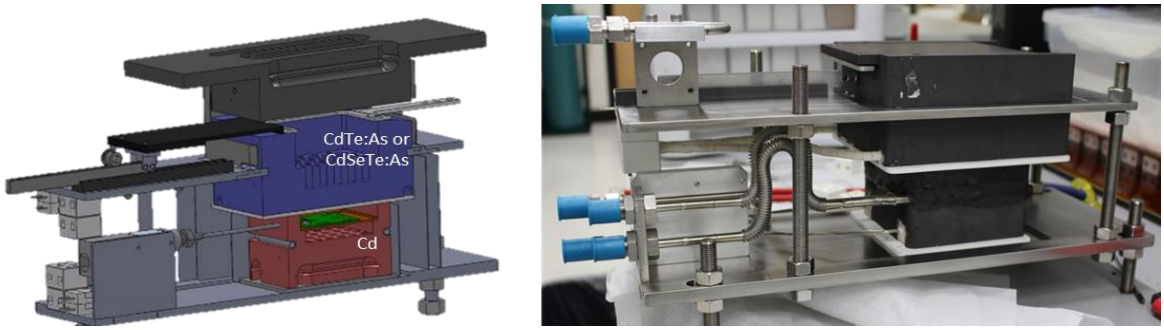


Figure 24 - Co-sublimation hardware used in arsenic doping experiments

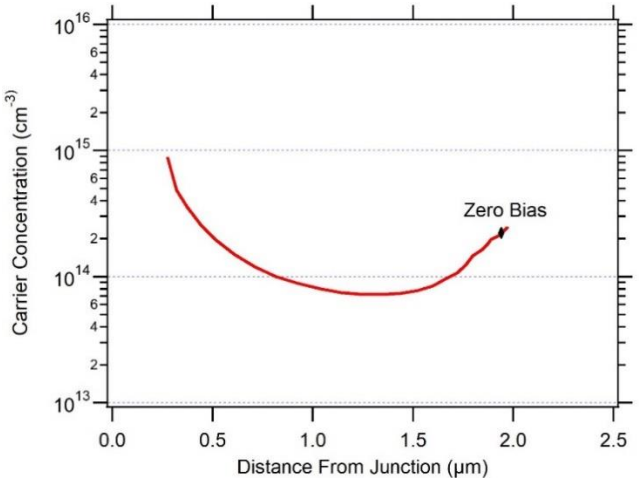


Figure 25 - CV profile for the 16.8% MZO/CdSeTe/CdTe:As arsenic-doped device (1379-7) showing acceptor concentration of approximately $10^{14}cm^{-3}$.

substrate. Further details of the co-sublimation source may be found in [106] and Figure 24 shows a diagram and photo of the source hardware. The top source was loaded with the primary absorber material— either CdTe:As or CdSeTe:As.

The lower source was loaded with elemental cadmium. This method was met with initially encouraging results, as a 16.8% efficient device was fabricated, the JV curve of which is shown in Figure 26, both with and without a tellurium back contact. Several notable features deserve discussion. First, a 16.8% efficient device, particularly one fabricated so early in the experimental cycle, was encouraging. 16.8% conversion efficiency already places this device in the upper tiers of CdTe performance. While a great deal of additional improvement would be required, these samples showed that arsenic doped CdSeTe/CdTe holds promise. Secondly, while the overall performance is impressive, the open-circuit voltage remains lower than would be expected from a well-optimized copper-doped sample. Finally, the sample without the tellurium back contact shows a substantial kink, which reduces the V_{OC} and FF of the device. The thin layer of evaporated tellurium deposited as the hole contact for CdTe has been thought to reduce the barrier to hole extraction and remove the "kink." If the back few nanometers of CdTe were doped-highly enough, the hole barrier would likely not be present and there would be little to no difference in performance between the two samples shown in Figure 26. The fact that there is a large difference in performance provides possible evidence that the back surface is not highly doped. Nonetheless, these promising results warranted further investigation, to see if the arsenic incorporation and/or high levels of doping might explain the encouraging early results.

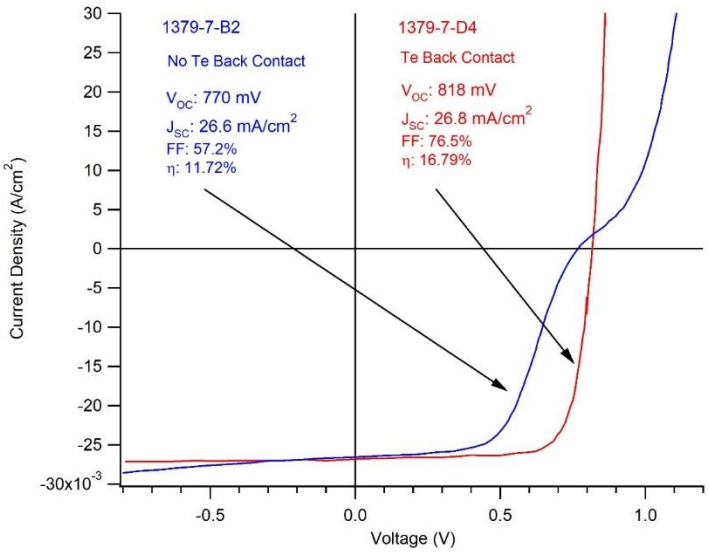


Figure 26 - JV curve for a 16.8% CdSeTe/CdTe:As device with and without tellurium

Arsenic Incorporation **-** To measure the arsenic incorporation in CdTe films deposited from an arsenic-containing source, and to measure the response as a function of cadmium overpressure, a series of films were fabricated while the cadmium source temperature was gradually increased. SIMS measurements were performed on each sample and the arsenic incorporation was compared. This comparison is shown in Figure 27 below. Unlike Farrell's work using MBE, the amount of cadmium overpressure does not appear to significantly alter the amount of arsenic incorporation in polycrystalline films deposited using co-sublimation. Indeed, the insert in Figure 27 shows a zoomed-in view of a section of the curve, where the curves for all four cadmium overpressures tested overlay one another. It should be noted that the difference in sputtering time between the sample without Cd overpressure and the other samples is due to a difference in sample thickness rather than a significant difference in the sputter rate. When compared against a CdTe:As standard of known incorporation produced at NREL, these signals could be correlated to arsenic incorporation of 1018 atoms/cm^3, indicating approximately a 1% incorporation rate from the source charge of 1020 atoms/cm^3.

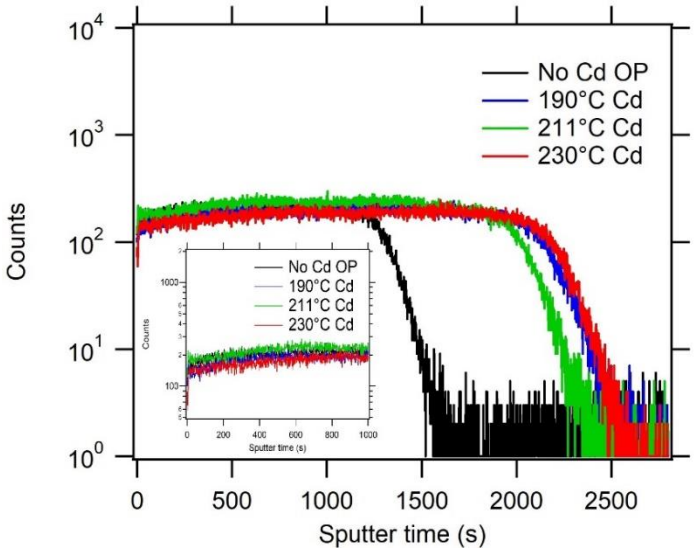


Figure 27 - Arsenic profiles of MZO/CdTe:As films deposited under varying cadmium overpressures, obtained using SIMS. SIMS measurements performed at Colorado School of Mines.

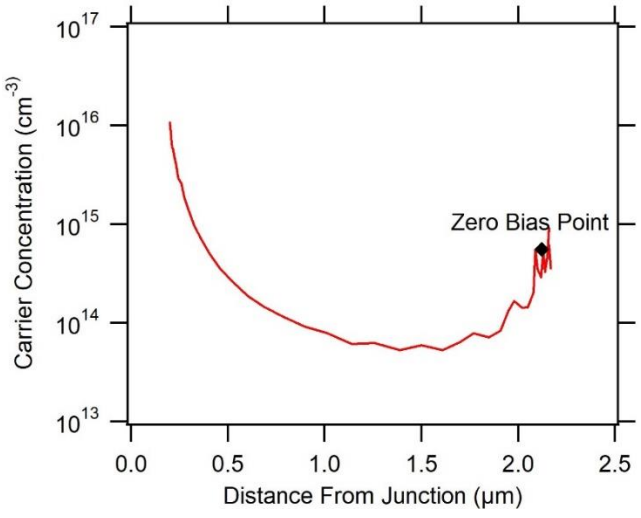


Figure 28. CV Profile of a MZO/CdSeTe:As/CdTe/CdSeTe device (1732-8R)

Acceptor Concentration **-** Next, utilizing CV, the carrier concentrations of multiple CdTe, CdSeTe, and graded bilayer samples were measured. First, the 16.8% CdSeTe/CdTe:As device shown in figure 27 was measured using CV. The acceptor concentration was found to be quite low — between 7x10^{13} and 2x10^{14} cm^{-3} depending on whether the belly of the curve or the zero bias point is used, as seen in Figure 28. In

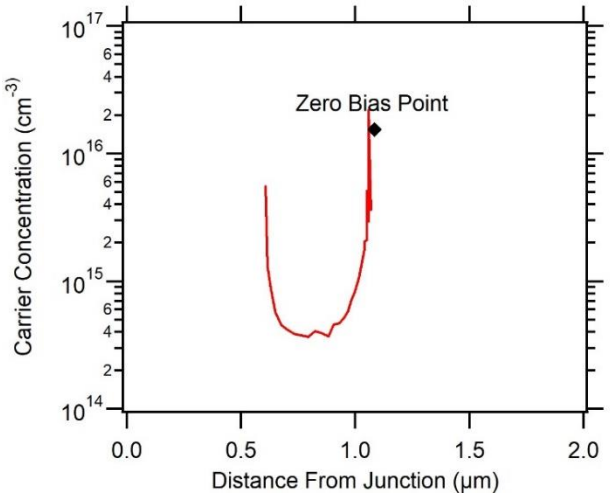


Figure 29 - CV Profile of a MZO/CdSeTe:As device (1886-3)

either case, this is comparable to the intrinsic doping found in a sample with no intentional doping. This evidence, along with the kink behavior seen in the JV indicates that the direct deposition of CdTe:As from an arsenic-containing source is not sufficient to achieve high hole concentrations. The moderately high JV performance therefore, is more indicative that depositing CdTe:As behind CdSeTe enabled the high J_{SC} and FF as traditional bilayer structures.

Additional CV measurements were taken on multiple other structures to explore the effect of starting with a CdSeTe:As source material as opposed to CdTe:As. The CV curves for a CdSeTe:As/CdTe/CdSeTe (Figure 29) as well as a CdSeTe:As only device (Figure 30) are shown below.

Finally, CV measurements were performed on the same CdTe:As samples which were measured with SIMS. All the samples displayed similar carrier concentrations as measured by CV. This indicates that not only does the cadmium overpressure not drastically affect arsenic incorporation into the film, but it also does not appear to have a significant effect on the rate of arsenic activation.

Dopant Activation - Having determined both the carrier concentration (by CV) and the arsenic incorporation (via SIMS) for the same CdTe:As samples, it is now possible to calculate the activation rate of the dopant. Dividing the acceptor concentration (10^{16} cm^{-3}) by the total arsenic density (10^{18} cm^{-3}) gives an activation rate of just 1%, and this value may be much smaller if the belly of the curve is used. In either case, the direct deposition of Cd(Se)Te:As material into a film results in virtually all of the arsenic incorporating not as an activated dopant, but as a defect.

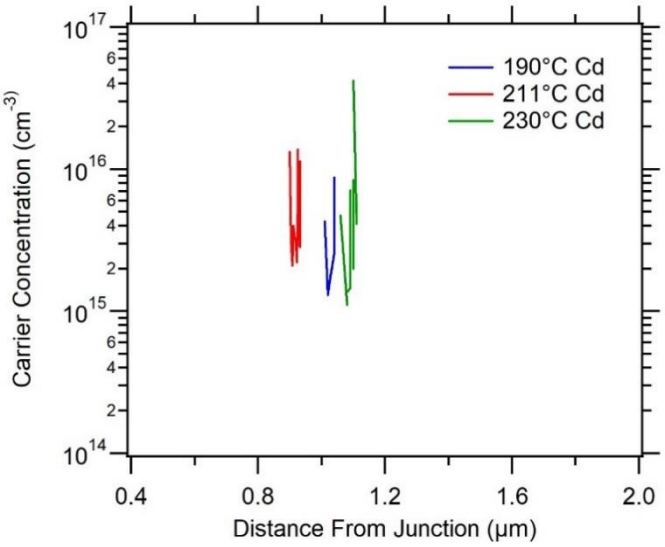
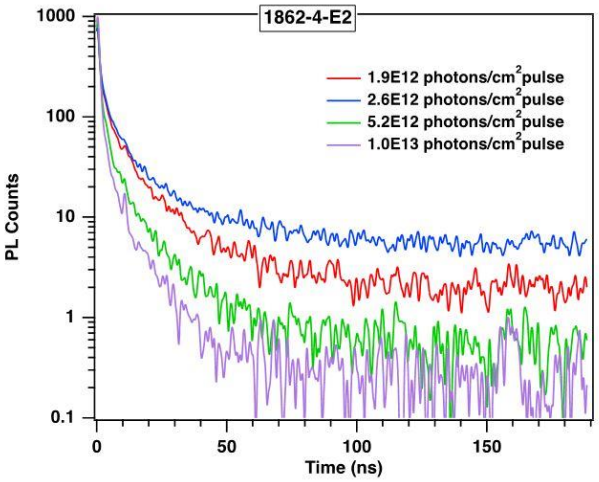


Figure 30 - CV Profiles for MZO/CdTe:As samples deposited under various cadmium overpressures (devices 1811-3,4,5)

Carrier Lifetimes - To corroborate the findings that as-deposited

material was highly defective, TRPL measurements were performed. Figure 31 shows the TRPL decays for a 2 µm CdSeTe:As sample. Because the lifetimes in CdTe are typically on the order of just few nanoseconds, it can be difficult to see the effect of adding arsenic. Therefore, CdSeTe, with its much greater lifetime was chosen to show the effect. Undoped CdSeTe films have been shown to exhibit microsecond lifetimes (Reich et al). These samples however, exhibited lifetimes of only 9–16 ns, depending on injection. This serves as another indication that the film contains high levels of defects, and that those defects are reducing the effective lifetime by providing non-radiative recombination pathways.



τ_2 **range: 16 - 9 ns**

Figure 31 - TRPL decays for a 2 µm CdSeTe:As sample (1862-4) under various injection levels showing low excess-carrier lifetime.

External Radiative Efficiency **-** ERE measurements confirmed the TRPL findings indicating high amount of non-radiative recombination. Although numerous samples were measured for ERE, they were all at or below the detection limit for the tool —with an external radiative efficiency of approximately 0.0005%. This corresponds to an implied voltage at or below 900 mV. Therefore, even though some as-deposited, non-diffused sample demonstrated decent JV behavior, their potential is extremely limited. The high defect density, although not harmful enough to prevent conversion efficiencies in the upper teens, does prevent this structure from being a viable path forward to achieve voltages greater than 900 mV.

Diffused-Arsenic Doping - The as-deposited CdTe:As or CdSeTe:As is highly defective with arsenic complexes present in the film. Therefore, diffusing arsenic into the light absorbing portion of the film from the as-deposited layer will result in a higher quality film.

Diffused-Arsenic Methodology - The results shown earlier indicate that simply using an arsenic-containing source charge during close space sublimation to fabricate films is not sufficient to achieve high levels of dopant activation and carrier concentrations. Therefore, a new structure was devised which was designed to only allow monoatomic arsenic species into a portion of the absorber. This design, referred to as the “diffused” structure, and shown in Figure 32 , was inspired by the kinetic modelling results from Krasikov and Sankin (Krasikov and Sankin 2018). They showed that interstitial arsenic, As_i, experiences a significantly smaller diffusion barrier compared to the various other As

species, complexes, and AX centers. This suggests that As_i may be the only arsenic species capable of diffusing a significant distance during processing.

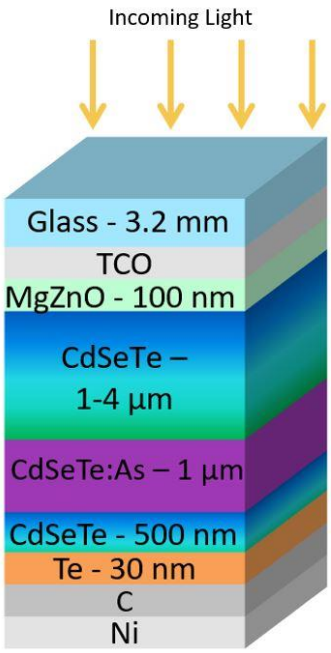


Figure 32 - Device structure used in the diffused arsenic-doping experiments, referred to in the text as the "diffused method". Not to scale.

Device Structure - In the diffused structure, a 100 nm layer of MgZnO was deposited on TEC10 glass via magnetron sputtering, followed by a 1–4 µm layer of undoped CdSeTe. Next, a 1–1.2 µm film of either CdTe:As or CdSeTe:As was deposited. During the deposition of the arsenic-containing film, cadmium overpressure was once again maintained via the co-sublimation source containing elemental cadmium. The temperature of the cadmium source was maintained at 211°C, chosen because it was the middle temperature in a range where the incorporation appeared to be insensitive to temperature variation. Finally, a thin 200 – 500 nm "cap" of undoped CdSeTe was deposited at the back, to minimize any potential loss of arsenic during the $CdCl_2$ process. The entire film stack was then subjected to an aggressive $CdCl_2$ treatment with a 480°C source temperature and a 430°C substrate heater temperature, considerably hotter than the previously optimized temperatures used for standard device structures. During the $CdCl_2$ process, interstitial arsenic is intended to diffuse from this back "reservoir" of arsenic-containing material into the front layer, resulting in two distinct regions within the film: a front "diffused" layer where only monoatomic arsenic is present, and the back layer where all of the less mobile complexes and AX centers are retained. A simple diagram of this process can be found in Figure 33 for illustrative purposes. Krasikov and Sankin's work also shows that the reaction of As_i into other arsenic species occurs on the microsecond timescale, ultimately leading to the desired As_{Te} formation over the timescale of seconds (Krasikov and Sankin 2018).

Arsenic Incorporation - To verify arsenic incorporation in the absorber using this diffused method, SIMS measurements were conducted by EAG Laboratories and the results are presented in Figure 34. To gain insight into the As diffusion profile in the front CdSeTe layer without complication from surface roughness and uneven sputter rates, the entire film was peeled from the substrate and measured from the front interface using a proprietary method. This sample had 2.5 µm of undoped CdSeTe at the front followed by 1.2 µm of CdSeTe:As. This profile shows arsenic incorporation as high as 10^{19} atoms/cm^3 at the back in the "as-deposited" reservoir region when using a source material with 10^{20}

atoms/cm^3 arsenic concentration. Interestingly, the arsenic concentration in the "as-deposited" CdTe:As shown in figure 34 only reached 10^{18} cm^{-3} when deposited from a source material with the same arsenic concentration. This may indicate that arsenic more readily incorporates into CdSeTe, with an incorporation rate of approximated 10% compared to the 1% in CdTe. The arsenic signal decreases as it approaches the front interface until it reaches the detection limit for arsenic at 5 x 10^{15} atoms/cm^3 at which point the plot becomes erratic and jagged. The unique arsenic profile seen in Figure 34 may result from the combined behaviors of the multiple arsenic species. This includes substantial amounts of immobile arsenic complexes retained in the "reservoir" at 2.5–4 µm from the front, rapid diffusion of interstitial arsenic towards the front interface, and the evolution of As_i into more stable but less mobile species, where they cease to diffuse any appreciable distance and ultimately react to form As_{Te}.

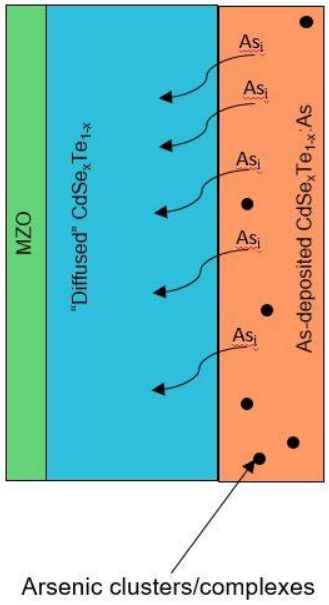


Figure 33 - Diagram of the arsenic diffusion process, where interstitial arsenic diffuses towards the front while arsenic complexes are retained in the as-deposited layer. Not to scale.

A second sample fabricated several years later and peeled from the front and measured with SIMS in the exact same way shows a similar arsenic profile shown in Figure 35 indicating that this structure can be repeatedly made.

Acceptor Concentration - As with the non-diffused arsenic doping work, it was necessary to determine the carrier concentration within the fabricated devices to ascertain the effectiveness of the arsenic doping process. Capacitance-Voltage measurements were once again performed. Additionally, Scanning Capacitance Microscopy was used to probe locations that were too deep within the film to be accurately investigated by CV.

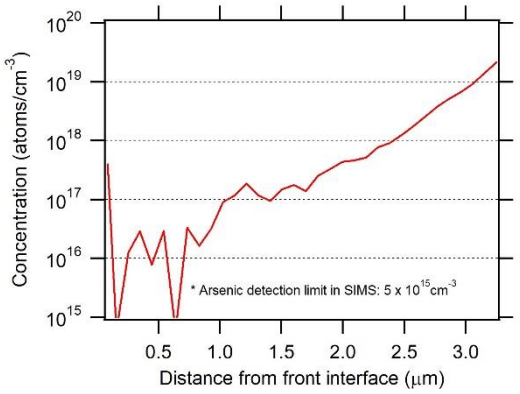


Figure 34 - SIMS showing the arsenic profile of a "diffused" sample (1968-2). Sample was peeled at NREL and SIMS were performed at EAG Laboratories.

Capacitance-Voltage – Figure 36 below shows the CV plots of numerous devices which have been fabricated using the diffused doping methodology. It shows that the device structure discussed in earlier section has repeatedly produced acceptor concentrations more than 10^{15} carriers/cm^3. The blue plot is the CV profile

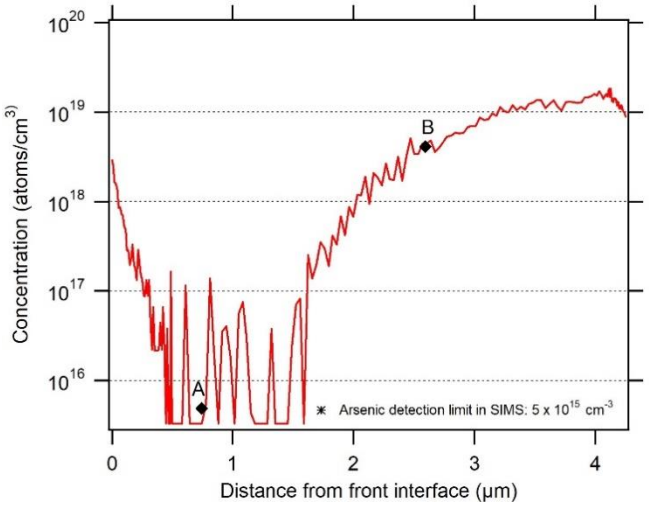


Figure 35 - SIMS showing the arsenic profile of a "diffused" sample (1546-7). SIMS were performed at EAG Laboratories. Point “A” and "B" are points of interest and compared to CV and SCM results at the same film depths

for the sample shown in Figure , the first SIMS profile for the diffused method. The black plot was observed when the front layer of undoped CdSeTe was increased from 2.5 μm to 4 μm. The green plot, showing a carrier concentration of greater than 10^{16} holes/cm^3 was achieved by performing two $CdCl_2$ treatments. The first $CdCl_2$ treatment occurred after the front layer of CdSeTe was deposited (but before the CdSeTe:As). The second treatment occurred after all absorber layers were deposited. This early $CdCl_2$ treatment would have caused recrystallization and grain growth in the front CdSeTe layer, which potentially increased the rate of arsenic diffusion. All three diffused-arsenic-doped curves can be compared to the orange curve, which is a repeat of Figure 25, the 16.8% non-diffused arsenic sample and the red curve, which is the CV profile of a baseline copper-doped device, which exhibits the low-10^{14} doping levels typical of a copper-doped CdSeTe/CdTe device (Yang, Metzger, and Wei 2017). In these discussions, all reported doping levels are taken as the carrier concentration at zero bias, indicated by a diamond on the plots.

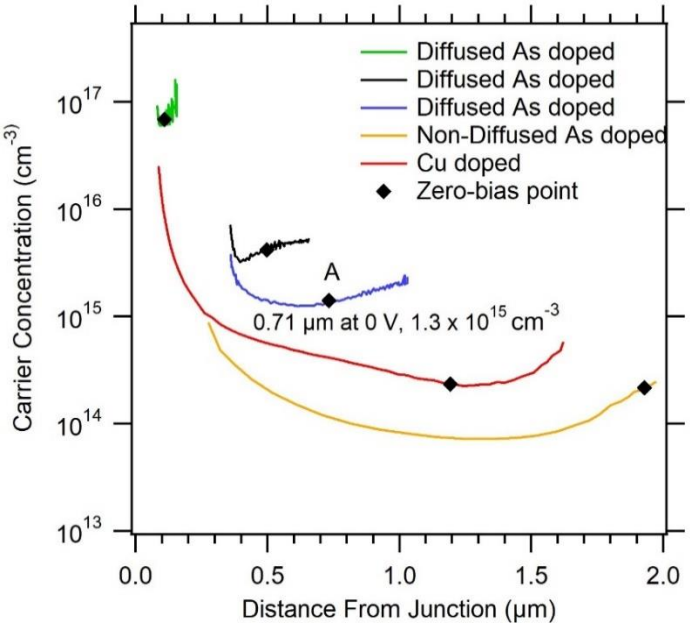


Figure 36 - CV profiles for three different diffused-arsenic devices (Blue: 1546-7, Black: 1633-4L, and Green:1894-8) compared to the profile of a non-diffused arsenic-doped sample (1379-7) and a typical baseline copper-doped sample (1634-7).

Dopant Activation -

Figure 37 displays the previously shown SIMS and CV results for the diffused-arsenic-doped sample 1546-7 for easy side-by side comparison. By dividing the carrier concentration as measured by CV at 0.7 μm from the front (1.3 x 10^{15}) by the total arsenic concentration (5 x 10^{15}) at the same depth, an activation ratio of at least

26% is obtained. For ease of comparison, these points on the different plots have been labeled as point “A”. Another location, point “B” shows a different location, approximately 2.5 µm from the front interface.

Performing the same activation calculation as before, but using the 10^{18} cm^{-3} carrier concentration given by SCM and the arsenic concentration of 3.4 x 10^{18} from SIMS at point “B” at depth of 2.5 µm, gives a doping activation ratio of 29%. Therefore, it appears that the doping profile within the front “diffused” layer of CdSeTe, which was previously undoped, is graded from approximately 10^{15} at the front to 10^{18} at the back while maintaining consistent activation rates.

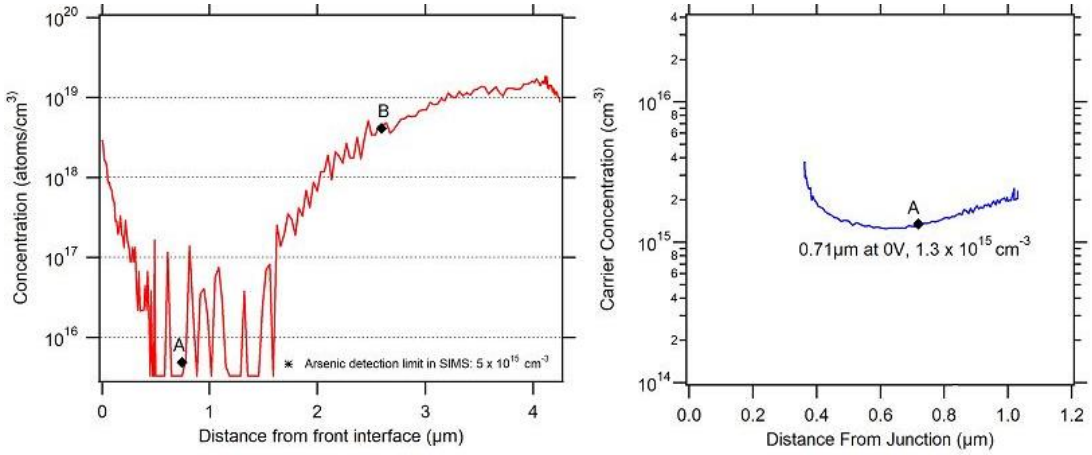


Figure 37 - Side-by-side comparison of SIMS and CV results for the same diffused-arsenic-doped sample (1546-7)

Luminescence - The evidence for high arsenic doping is further supported when considering the luminescence of these devices. Using both cathodoluminescence and steady state photoluminescence, energy peaks which correspond to arsenic sitting in a tellurium site have been identified. Figure and Figure respectively show the CL and PL spectra for arsenic-doped films. Figure shows multiple device structures, including samples with Al_2O_3, ITO, and Ag back contact/electrode layers. These additional layers do convolute the data, particularly with the addition of the low-energy peak at 1.27 eV, but the As_{Te} peak is still clearly visible in most of these structures. In this figure, only the black plot (1601-5R) is not doped with arsenic. While the CL measurements were taken at a temperature of 7 K, the PL results were obtained at room temperature. The fact that the dopant energy peak is visible at room temperature is yet another indicator that large amounts of arsenic are acting as activated dopants.

Carrier Lifetimes - As previously discussed. Kephart *et al* were able to achieve excess-carrier lifetimes more than 400 ns using a heterostructure where CdSeTe was deposited between layers of Al_2O_3. This lifetime was orders of magnitude longer than previous findings, and was an early indicator that CdTe lifetimes could be greatly improved. Figure 40 below shows the measured TRPL curve for an arsenic-doped device, with a copper-

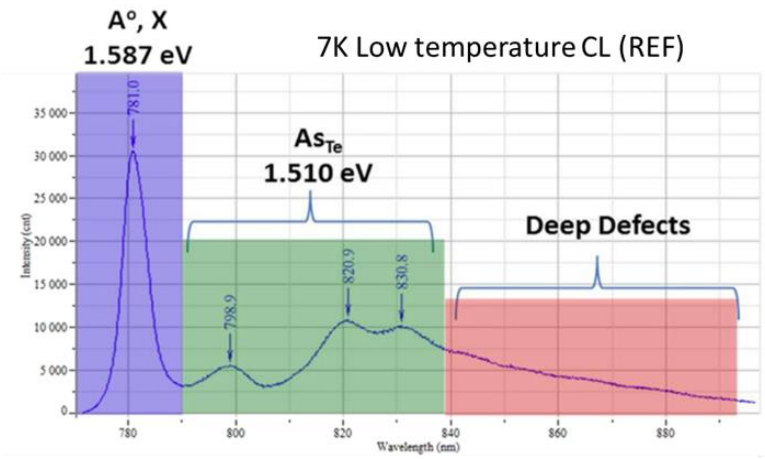


Figure 38 - Low temperature CL spectrum of an As-doped device made at NREL, measurement by NREL.

doped device included for comparison. This device, which used a CdSeTe:As layer the source of arsenic, did not have an Al_2O_3 layer, and yet had a measured lifetime exceeding 1 µs, nearly four times the lifetime of Kephart's heterostructure.

These results illustrate that diffused-arsenic doping produces devices with excess-carrier lifetimes that are orders of magnitude longer than can be obtained using any known copper-doping process. To confirm that the diffused doping method resulted in higher quality films with less non-radiative recombination, dozens of substrates split over eight experimental runs were fabricated. In each experiment, both diffused and non-diffused samples were fabricated and measured via TRPL for direct comparison. The average lifetimes of each type of sample can been seen in figure 41.

It is believed that this variation is primarily due to changes in the CdSeTe, not the arsenic doping process. The highest lifetimes measured for diffused-arsenic doping were 2.3 µs (Figure 41) whereas non-diffused lifetimes never exceeded 75 ns, approximately equal to the lowest diffused-sample lifetimes.

Interface Passivation - Lifetimes such as those shown for the diffused-arsenic doped samples in the previous section are simply not possible with very high interface recombination rates. Even if the bulk material lifetime were very good, carriers would only survive long enough to reach an interface, where they would recombine. Using TRPL where the exciting laser illuminates the back interface, it is possible to study the rear surface passivation. TRPL measurements were conducted with 640 nm laser excitation from the back of the device. 640 nm was chosen to ensure the light would be absorbed where back surface recombination dominates the response. Because the lifetimes measured from the back are quite short, and the light

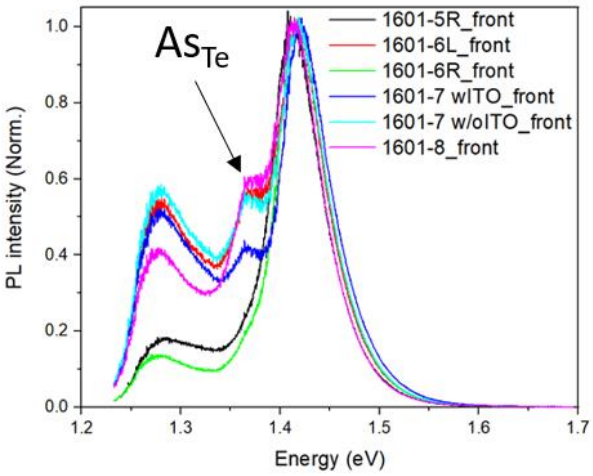


Figure 39 - Room temperature PL of various As-doped device structures (1601-5,6,7,8) manufactured at CSU's PV manufacturing lab, measurement by NREL

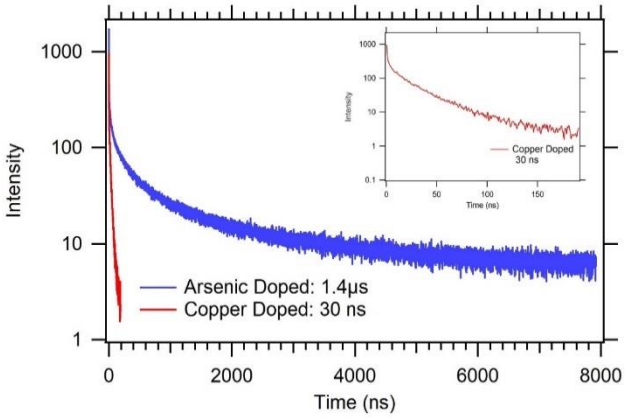


Figure 40 - A comparison of TRPL decays and fit lifetimes of copper-doped (red, 1894-7) and arsenic-doped (blue, 1633-4L) devices. The copper-doped decay curve is reproduced (inset) at a shorter timescale for better visualization.

is predominately absorbed in the area immediately adjacent to the interface, it is safe to assume that the recombination which causes the τ_1 decay is not limited by carrier diffusion. Therefore, the interface recombination velocity may be determined from the measured lifetime by Equation 12 (Ahrenkiel and Johnston 2009), where S is the recombination velocity, α is the absorption coefficient at 640 nm, and τ_1 is TRPL lifetime.

$$S_{Back} = \frac{1}{(\alpha_{640}\tau_1)}$$

Table 1 summarizes the results of measuring the back surface recombination velocity for devices containing various dopants. It clearly shows that while copper worsens the interface passivation compared to an undoped device, arsenic doping and the inclusion of CdSeTe at the back interface marginally improves it.

Yet, while this evidence that the back interface is improved by the presence of arsenic and/or selenium, the recombination velocity remains too high to reasonably allow for microsecond lifetimes. Therefore, even though the interface itself exhibits recombination velocities in the range of 10^5 cm/s, the *effective* recombination velocity is much lower. The band diagram shown below in Figure 42 is the result of DFT modelling showing upward band bending when there is a monolayer of 100% activated As_{Te} at the back of CdTe. The large amount of band bending which is induced by the graded doping towards the back of the device creates an electron reflector, which confines and repels the electrons, preventing them from ever reaching the relatively poorly passivated back interface and recombining. It is estimated, based on the exceedingly long lifetimes that the effective

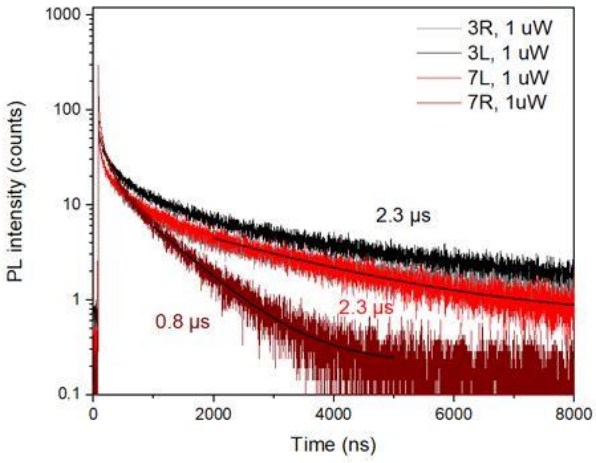


Figure 41 - TRPL decay curves showing 2.3 µs lifetime for several diffused-arsenic devices. 1698-3L,R was 4 µm CdSeTe/1 µm CdSeTe:As/500 nm CdSeTe while 1698-7L,R was 1.5 µm CdSeTe/200 nm CdSeTe:As/500 nm

recombination velocity in these arsenic-doped devices are comparable to Al_2O_3 heterostuctures, with S < 100 cm/s.

Table 1- Average excess-carrier lifetime for diffused vs non-diffused arsenic-doped sample.

Average T_2 lifetime as measured by TRPL	
Diffused-arsenic doped samples	**Non-Diffused arsenic doped samples**
807 ns	39 ns

External Radiative Efficiency – Figure 43 shows the EREs for cells with both CdSeTe and CdSeTe/CdTe absorbers for undoped, diffused-arsenic doped, and copper-doped conditions. All cells utilized MgZnO as an electron contact and evaporated Te as a hole contact layer. The CdSeTe-only absorbers were 3–4 µm thick while the CdSeTe/CdTe bilayers were 500nm CdSeTe/3µm CdTe. Inspection of these data reveals several key findings. First, for all doping conditions, CdSeTe-only films consistently exhibit significantly greater radiative efficiencies than absorbers with a CdTe layer. The passivating effect of selenium on CdTe grain boundaries was well-illustrated by Fiducia *et al.* (Fiducia et al. 2019) and these effects are apparent here where CdSeTe-only films routinely exhibit EREs an order of magnitude greater than films with a graded bilayer. Second to note is the effect of the dopant on ERE. Undoped CdSeTe exhibits remarkably high EREs, nearly 1%. The addition of diffused-arsenic doping reduces the radiative efficiency for both absorber structures, but not nearly to the extent of copper.

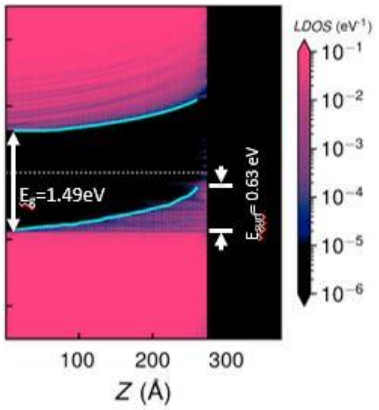


Figure 42 - Upward band bending shown in the band diagram of CdTe with a single monolayer of 100% activated As_{Te} at the back.

For copper-doped CdSeTe/CdTe, given the ERE shown in Figure 43 and assuming a $V_{OC,rad}$ value of 1150 mV, the implied voltage calculated at approximately 880 mV. This means that current generation CdSeTe/CdTe:Cu devices, with a V_{OC} of approximately 860 mV, are nearly passivation or material quality limited, and will not produce a greater voltage until the structure is changed to increase the quasi-Fermi level splitting.

Table 2 - Back interface recombination velocities using various dopants

Sample Structure	***S_{Back}*** **(cm/s)**
MZO/CdSeTe/CdTe:Cu/Te (baseline)	$1.2x10^6$
MZO/ CdSeTe /CdTe (undoped)/Te	$2.7x10^5$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Te	$1.4x10^5$

Alternatively, arsenic-doped CdSeTe samples, with greatly improved ERE values, translate to implied voltages of 900–950 mV. The band edge, reconstructed by either photoluminescence or external quantum efficiency, must be measured for each sample for which an iV_{OC} calculation is performed (Onno et al. 2022). Finally, it must be noted that these values represent a significant improvement compared to historical values for CdTe, which had previously been reported with an ERE of 10^{-4} %. Furthermore, the current CdTe efficiency record device exhibited an ERE of 0.008% and only a few photovoltaic technologies have reported ERE values of greater than one percent (GREEN 2012; Green and Ho-Baillie 2019; Yamaguchi et al. 2018) Recent studies have shown that CdSeTe, with proper processing and the addition of passivating layers, can demonstrate radiative efficiencies of several percent, resulting in iV_{OC} values that are approaching 1 V (Onno et al. 2022).

Band Tails and Reduced Theoretical Maximum Voltage - Diffused-arsenic doping shows great potential to eliminate many of the most adverse effects of copper doping. Additionally, diffused-arsenic doped films simultaneously exhibit greater acceptor concentrations, vastly improved carrier lifetimes, and higher radiative efficiencies compared to either non-diffused arsenic or copper-doped counterparts. There remain, however, obstacles to be overcome to maximize the implied voltage of arsenic-doped devices. PL and EQE measurements, necessary for the calculation of $V_{OC,rad}$ and iV_{OC}, reveal the presence of sub-bandgap features in arsenic-doped samples. These features indicate that sub-bandgap absorption occurs, likely due to defect states and bandgap fluctuations, and this absorption lowers the effective bandgap and thus $V_{OC,rad}$ from Equation 5, ultimately limiting the implied voltage which is possible for any given value of ERE. Determination of $V_{OC,rad}$ is highly sensitive to sub-bandgap absorptance since the blackbody radiation at 300K is quasi-exponential in the near infrared (Guillemoles et al. 2019; Rau et al. 2017; Wurfel 1982). One such example of these sub-bandgap features can be seen in the PL emission spectra given in Figure 44a between 900 and 1000 nm. In order to determine the $V_{OC,rad}$ for these devices, absorptance was extracted by an appropriate fitting of the measured photoluminescence spectrum using the generalized Planck Law as presented by Wurfel (Wurfel 1982) and is shown in Figure 55b. For these samples, the sub bandgap features resulted in an estimated reduction of 25 mV to $V_{OC,rad}$ for the arsenic-doped sample

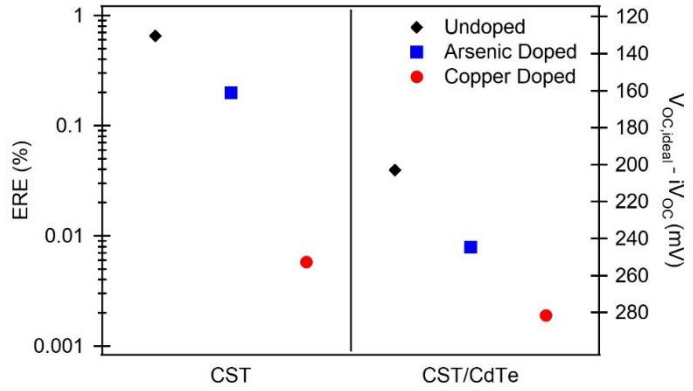


Figure 43 - ERE measurements for undoped, arsenic-doped and copper-doped CdSeTe only (left) and CdSeTe/CdTe bilayer (right) absorbers.

compared to the copper-doped sample. Similar features were reported by Moseley et al. in (Moseley et al. 2020) for VTD-grown CdSeTe:As samples. Further investigation is needed to understand the cause of and full extent of these sub-bandgap features, as well

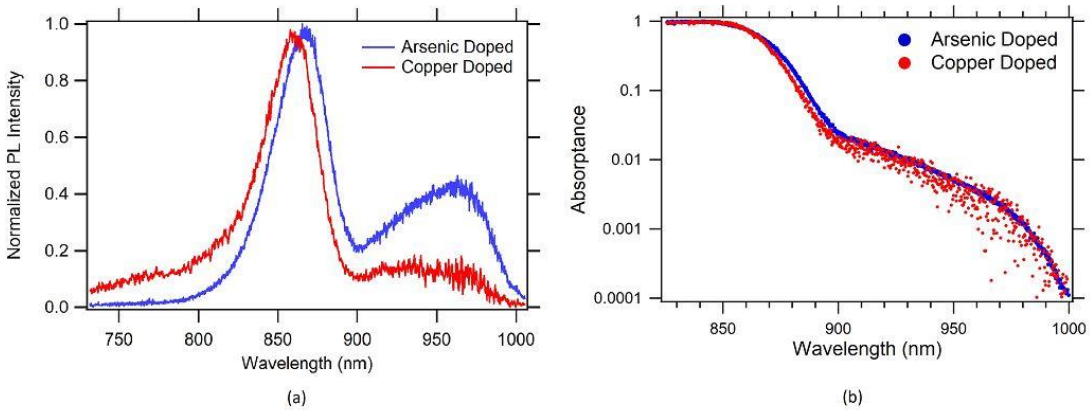


Figure 44 - (a) Photoluminescence emission spectra comparing sub bandgap features in copper (red, 1732-6L) and diffused-arsenic (blue, 1732-8L) doped samples. (b) Absorptance extracted by an appropriate fitting of the measured PL spectrum shown in Figure 44a.

as how different device structures or processing steps might mitigate them.

JV Performance - Largely since these devices, despite their numerous electro-optical improvements, have not produced a greater open circuit voltage, the 16.8% device seen in figure 26 remains the champion device for a sample deposited from an arsenic-containing source. Of the devices which exhibit high carrier lifetimes and increased doping and a high ERE, the best device to date had a photovoltaic conversion efficiency of 13%, shown in Figure 45.

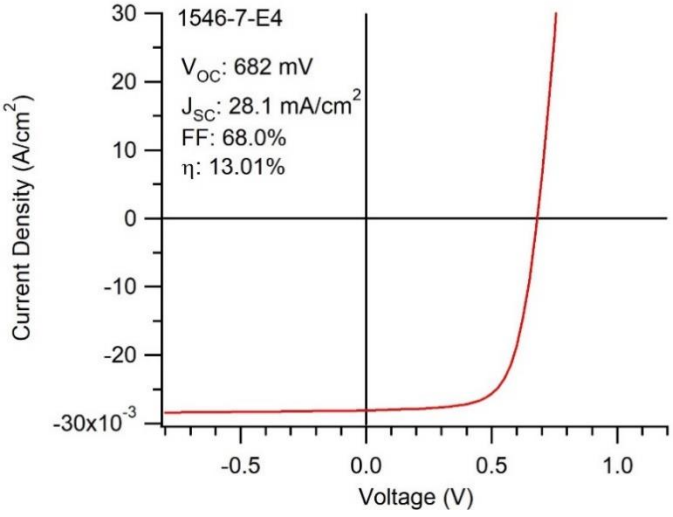


Figure 45 - JV curve showing 13.0% diffused-arsenic doped device (1546-7)

At present, it is believed that this relatively poor device performance is due to three main factors. First, the deposited CdSeTe:As layer that serves as an arsenic reservoir retains all of the dimers, tetramers and complexes. It is therefore a defective and recombination-prone region within the film. As such, the device performance is severely

hindered, despite the superior front layer because carriers generated within the front layer may still recombine within this defective region. Secondly, the doping profile may be inappropriate for high efficiency devices. It was previously shown that the doping profile appears to be graded within the front layer of CdSeTe from 10^{15} at the MZO interface to 10^{18} at the back.

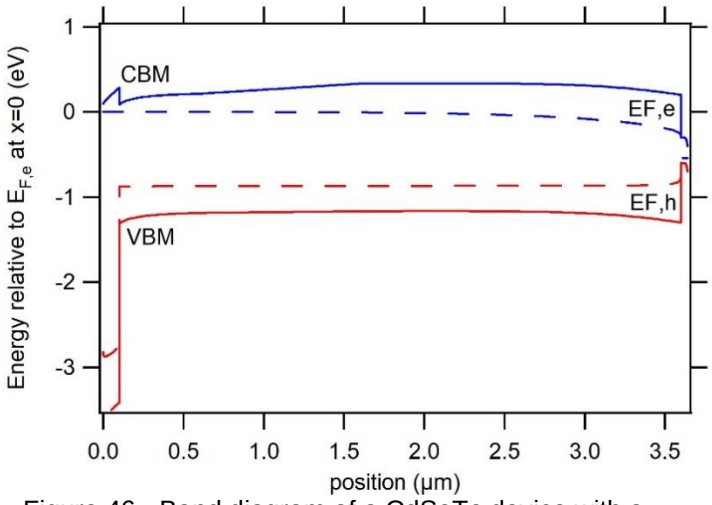


Figure 46 - Band diagram of a CdSeTe device with a theoretical hole contact with severe selectivity losses. The convergence of the quasi-Fermi levels indicates voltage loss.

This provides evidence that the diffused-arsenic doping methodology can produce samples with improved carrier concentration, excess-carrier lifetime, and radiative efficiency than can be produced with either copper doping or non-diffused arsenic doping. Indeed, on multiple occasions, individual samples simultaneously demonstrated acceptor

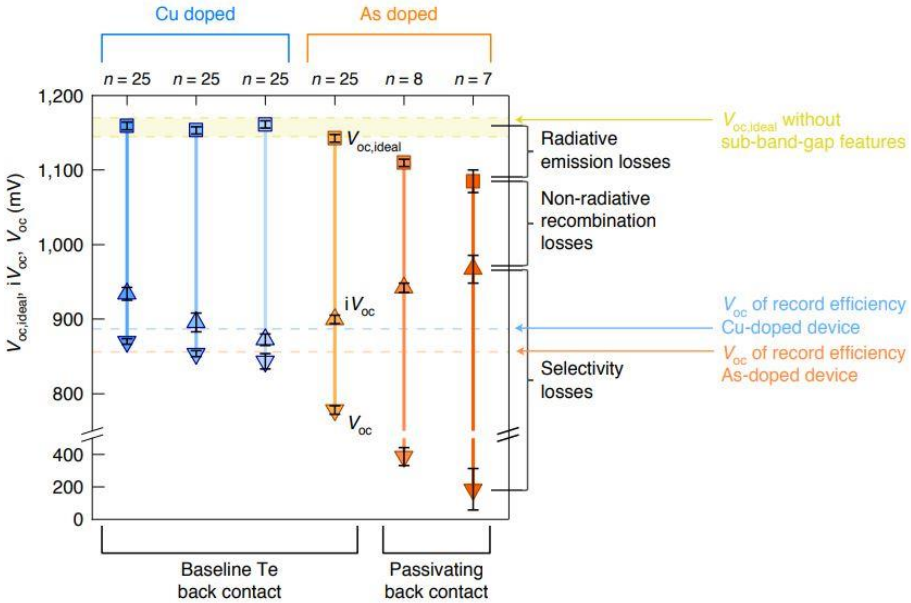


Figure 47 - Voltage loss analysis for copper and diffused-arsenic doped samples showing improved implied voltage but greater selectivity losses in arsenic-doped samples, adapted from (Onno et al. 2022).

concentrations in excess of 10^{15} cm^{-3}, microsecond lifetime, and EREs in the vicinity of 1%. **The evidence overwhelmingly supports the hypothesis that the diffused arsenic doping method produces higher quality films with far greater potential to**

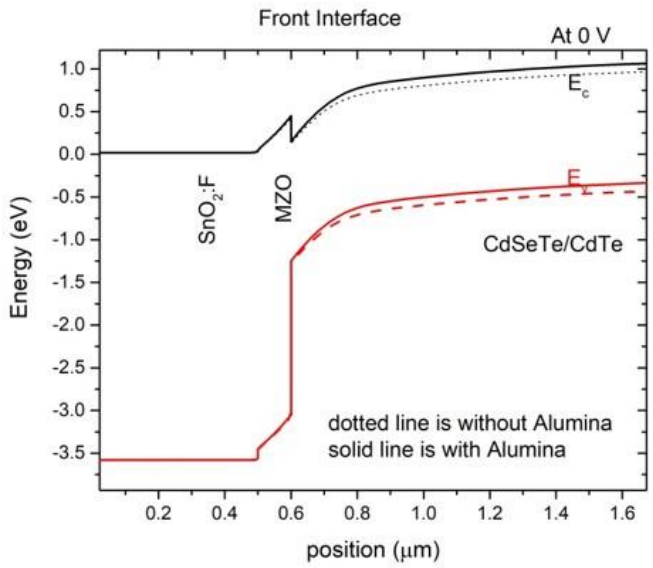


Figure 48 - MZO/CdSeTe/CdTe band alignment, showing a large valence band offset and a small conduction band "spike".

produce photovoltaic devices with improved voltage and conversion efficiency. The substantial improvement in ERE indicates that the bulk material is significantly improved with diffused arsenic doping as compared to other doping methods. However, additional steps remain that may further improve the device performance. Further passivation of the interfaces and the search for carrier selective contacts are discussed later.

Passivating Oxides and Carrier Selective Contacts - The multiple models presented in earlier all agree that interface passivation and its effect on excess-carrier lifetime strongly influences device performance. In fact, these studies indicate that as the doping levels and bulk lifetime increase, the interface becomes ever more important. Therefore, neither doping nor interfaces can effectively be studied in isolation but need to be considered on the basis that a change in one may have a large impact on the performance of the other.

Previous Passivating Oxide Work

The role which passivating oxides has played in the development of silicon devices cannot be understated. Optimizing the oxide layers has been a crucial step in engineering devices with greater than 20% conversion efficiency. The ubiquitous nature of passivating oxides in high performing silicon devices has in turn inspired a great deal of work within the CdTe community. This work has sought to reap the same performance improvements that silicon devices currently enjoy.

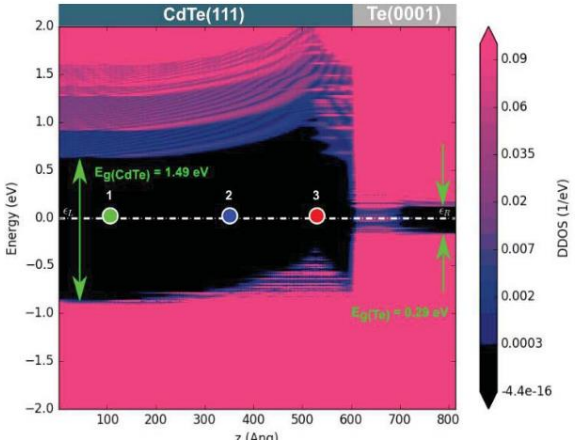


Figure 49 - Band alignment at the [111]CdTe/Te Interface, adopted from (Nicholson et al).

Electron Contact Work - $CdCl_2$:O treatment forms a layer of sulfur and tellurium oxides. The prevalence of these oxides correlated well with device performance, which the authors attributed to improved front interface passivation (Perkins et al. 2019).

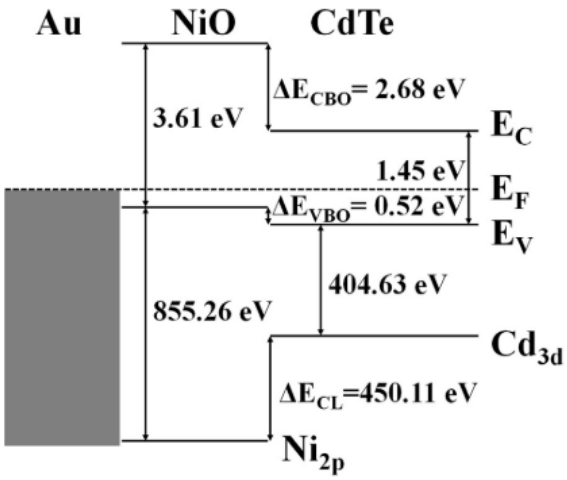


Figure 50 - Band alignment of the NiO/CdTe interface, adopted from (Di Xiao et al. 2017)

Increasing the magnesium corresponded with a conduction band spike, which in turn reduced interface recombination and produced improved open-circuit voltage (Kephart 2015). It was discovered that increasing the conduction band spike up to 0.3 eV produces an increase in voltage, but any larger offset creates a barrier to electrons which is too great to overcome via thermionic emission, manifesting as a kink in the JV curve. The 3.7 eV band gap of MZO (Minemoto et al. 2000), paired with a small conduction band offset, corresponds with the very large valence band offset between the MZO and CdTe as illustrated in Figure 48.

Hole Contact Work - As discussed earlier, it is beneficial to select contacts with appropriate work functions to ensure proper band alignment and possible band bending. For the hole contact, this requires a large conduction band offset and upward band bending going into the contact. However, due to CdTe's unusually high work function of 5.7 eV, it has proven difficult to find a viable material with an equal or greater work function. It is unsurprising, therefore that CdTe's back contact has historically been problematic, as most contacts exhibit a smaller work function, inducing downward band bending which inhibits hole extraction rather than aid it.

At Colorado State University, a tellurium back contact has typically been deposited behind the CdTe. This has historically been done based on experimental results which show that an improvement in voltage and fill factor with the inclusion of approximately 30 nm of Te (Moffett 2018). It has been hypothesized that Te mitigates the downward band bending that would otherwise be present, and recent first-principles work by Nicolson *et*

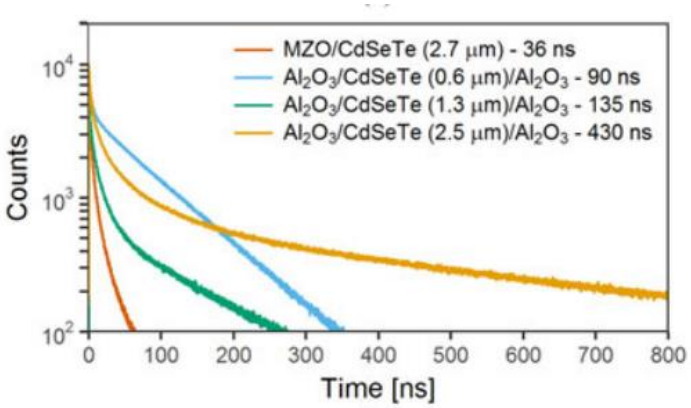


Figure 51 - TRPL lifetimes measured for various CdSeTe heterostructures, adopted from (Kephart et al. 2018)

al has shown upward band bending when Te is deposited on [111] oriented CdTe, as seen below in Figure (Nicholson et al. n.d.). Despite this band bending, the passivation of the CdTe/Te interface remains poor, with measurements indicating an interface recombination velocity of approximately 10^6 cm/s (Danielson et al. 2020).

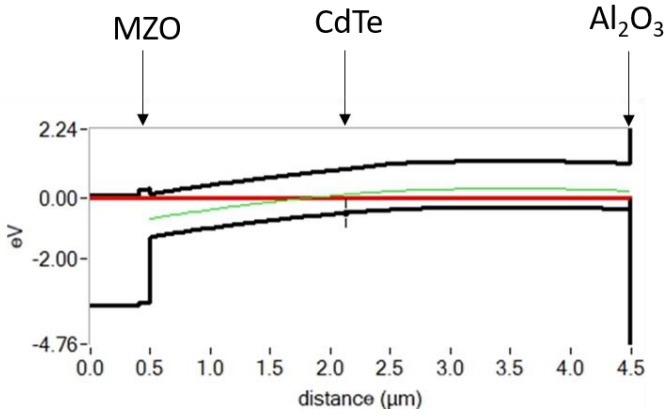


Figure 52 - Band structure with large VBO/CBO at $CdTe/Al_2O_3$ interface.

NiO has been proposed as an alternative hole contact due to its high work function and good band alignment with CdTe. Xiao *et al*, using X-ray photoelectron spectroscopy (XPS) techniques, found that when deposited by electron beam evaporation, NiO has a large conduction band offset of 2.68 eV and a relatively small valence band offset of 0.52 eV, is conducive to hole transport. Figure shows the band alignment as measured as a part of that work. Kephart *et al*'s work with aluminum oxide on CdTe has already been cited as foundational to the work present herein. Using and $Al_2O_3/CdSeTe/Al_2O_3$ heterostructure, they achieved τ_2 lifetimes of 430 ns, as seen below. While this indicates that the $CdSeTe/Al_2O_3$ interface is well passivated, the underlying mechanism for this passivation is still unknown. Alternatively, because the aluminum vacancies and oxygen interstitials appear to coincide with tetragonal Al_2O_3, it may not be present when grown on CdTe. Perkins *et al*, have proposed an alternative passivation mechanism. They found that well passivated interfaces of CdTe and Al_2O_3 corresponded with an increase in the Te^{+4} peak during XPS measurements (Perkins et al. 2018). They

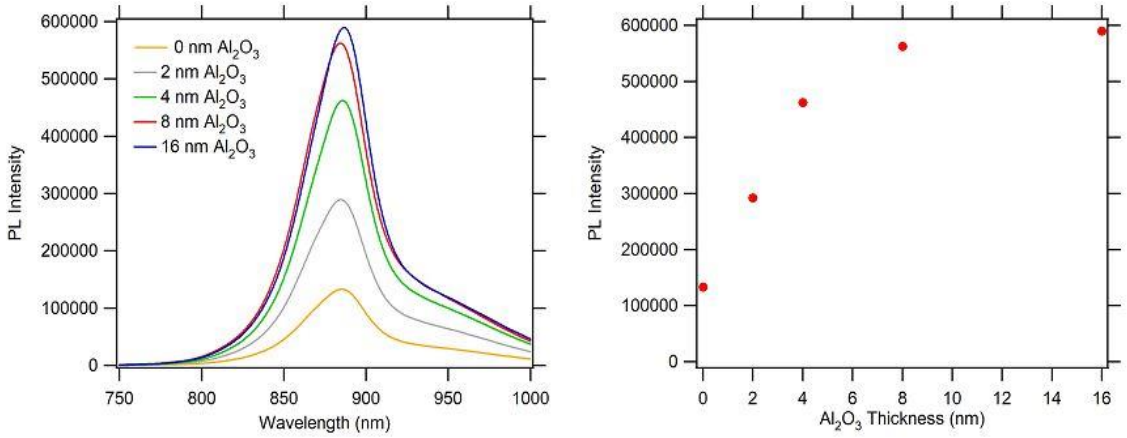


Figure 53 - (a) PL spectra of CdSeTe/CdTe devices (1537) with increasingly thick layers of aluminum oxide deposited at the back surface. (b) Plot showing the PL peak intensity for the curves shown in (a) revealing an asymptotic increase in intensity with thickness.

concluded that a tellurium oxide may be forming under the Al_2O_3 during the $CdCl_2$ treatment process, and that is providing chemical passivation at the interface.

The wide band gap of aluminum oxide (7.6 eV) ensures that very large offsets exist at both the valence and conduction bands when deposited onto CdTe (Filatova and Konashuk 2015). These large band offsets, shown below in Figure 52, prevent either electron or hole transport when the oxide layers are as thick as in Kephart's work (20–100 nm). However, if the oxide layer is made thin enough, and with sufficient band bending, carriers may pass through this barrier via quantum tunneling. Tunneling transport is the fundamental concept behind the TOPCon (tunnel oxide passivated carrier- selective contacts) structure found with silicon devices. In these structures, the absorber is completely covered in a very thin (0.5–1.8 nm) oxide layer, typically SiO_2 (Zeng et al. 2017). Although SiO_2 is most prominent in the TOPCon structure, Al_2O_3 has also shown very impressive levels of passivation (Agostinelli et al. 2006). While it is generally agreed that the majority of the carrier transport is via quantum tunneling, debate still exists as to whether microscopic pinholes in the oxide are beneficial to device performance (Feldmann et al. 2014).

Even with graded doping profiles, passivating the back surface with aluminum oxide will improve the quasi-Fermi level separation, indicated by increasing ERE.

Based on the previous work, multiple experiments were conducted where thin layers of Al_2O_3 were deposited onto CdSeTe and CdTe structures using either atomic layer deposition (performed at ASU) or magnetron sputtering of an oxide target. Resultant devices were characterized to measure the lifetimes, luminescence, and photovoltaic conversion efficiency to discern the effectiveness of aluminum oxide as a passivating and carrier selective contact for Cd(Se)Te.

Luminescence Results

To better understand the mechanics behind the passivation, Al_2O_3 films of various thicknesses were deposited. It was found that when only Al_2O_3 was deposited behind the CdTe, the PL response grew as the Al_2O_3 became thicker, as seen in Figure . Additionally, no peak-shift was noted as the aluminum oxide became thicker, which indicates that within this thickness range, the thicker oxide did not significantly affect the amount of

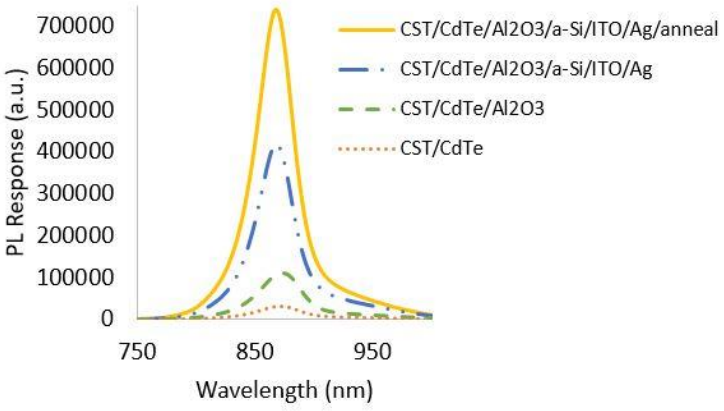


Figure 54 - Plot showing the PL response of a CdSeTe/CdTe device structure (1481) where back contact layers are sequentially added. It shows a large and consistent increase in PL with the addition of each layer or process.

selenium diffusion from the CdSeTe into the CdTe during the $CdCl_2$ treatment. Although increasing the aluminum oxide thickness shows a dramatic increase in the photoluminescence when it is very thin, the marginal gain diminishes rapidly at thicknesses greater than 4 nm. This indicates that most of the passivation mechanism occurs at the immediate interface, and is not reliant on the bulk Al_2O_3. Additionally, increasing the Al_2O_3 layer thickness likely improves the total coverage/continuity of the film (in the case of sputtered Al_2O_3) when it is very thin, but becomes less impactful as the thickness increases.

For aluminum oxide to be successfully incorporated into a device structure, and allow quantum tunneling, it must be kept very thin, likely less than 2 nm. Additionally, while the large conduction and valence band offsets seen in Figure facilitate the passivating nature of Al_2O_3, but they do nothing to aid in hole extraction. Figure shows large increases in photoluminescent response as aluminum oxide, highly p-doped amorphous silicon (a-Si:H), Indium Tin oxide (ITO), and silver are sequentially added to CdSeTe/CdTe devices. The back contact layers deposited after the aluminum oxide was chosen based on their proven performance as a hole contact in silicon devices. This shows that back-contact processing steps can further reduce the non-radiative recombination within the device. The addition of the Al_2O_3 results in an increase in PL from approximately 30k counts to more than 100k counts. This is followed by an even greater increase up to 400k counts with the addition of the a-Si:H, ITO and a silver back contact. Several phenomena are likely contributing to the interface passivation. In addition to the passivation provided by the Al_2O_3 itself, further upward band bending induced by the highly p-doped a-Si, may also repel electrons from the Al_2O_3 interface, further reducing the electron population at

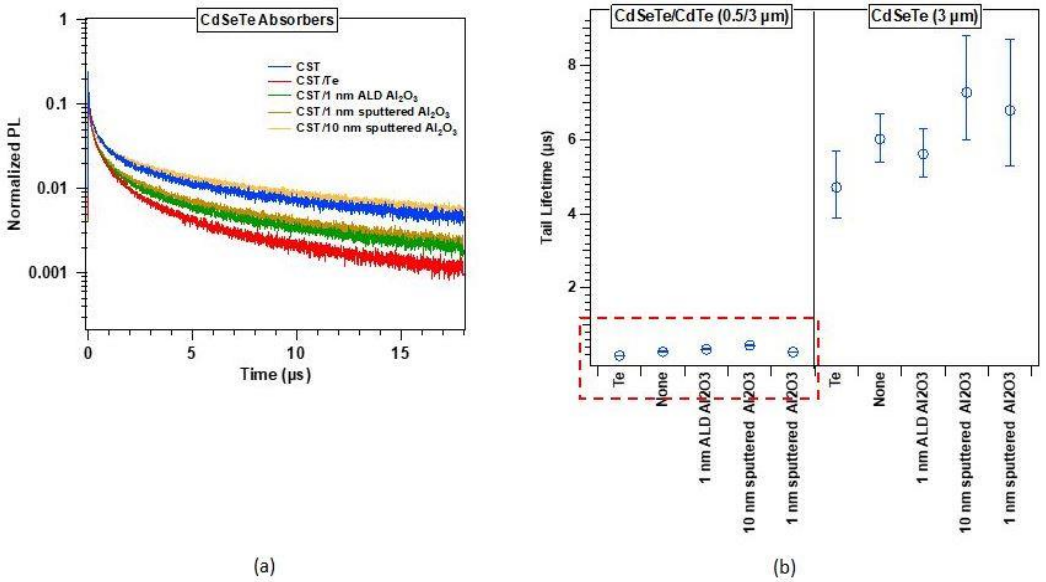


Figure 55 - (a) TRPL decays for CdSeTe films with either no back contact, a tellurium back contact, or alumina passivation layer (ALD or sputtered). (b) TRPL tail lifetimes for both CdSeTe/CdTe and CdSeTe-only absorbers with various back contacts

the back. Finally, when the device was annealed in air at 200°C for 10 minutes, the PL doubled again to more than 700k counts.

Carrier Lifetimes - CdSeTe/CdTe devices typically have measured lifetimes from 10–100 ns, CdSeTe-only devices with Al_2O_3 displayed excess-carrier lifetimes of up to 8 µs, as seen in Figure 57. **To the author's knowledge, these are the highest carrier lifetimes ever measured in polycrystalline CdSeTe or CdTe devices.** In this study, Atomic Layer Deposition (ALD)-deposited alumina was compared against sputter-deposited alumina for both differing layer thicknesses and for both CdSeTe-only and CdSeTe/CdTe absorbers. The CdTe layer exhibits a significantly shorter lifetime, and it therefore limits the overall lifetime. The gains of a well-passivated back interface do not manifest when the charge carriers must traverse a very low lifetime material. Secondly, contrary to expectations, the ALD-deposited alumina did not result in longer lifetimes compared to a sputtered oxide. Finally, lifetimes approaching 10 µs represent a fundamental paradigm shift compared to traditional CdTe devices with excess-carrier lifetimes of only a few nanoseconds. With extremely short lifetimes, the field is extremely important, as it is needed to quickly separate the carriers and sweep them to their respective contacts before they recombine.

Interface Passivation - The long carrier lifetimes measured in the previous section are due in large part to improved interface passivation at the back surface. Similar to the doping work, TRPL was measured from the back to measure the back surface recombination velocity. As Table 3 shows, there is a mild improvement in the back surface recombination velocity when aluminum oxide is deposited, compared to a baseline device with a tellurium back contact. This improvement is present even on a copper-doped sample.

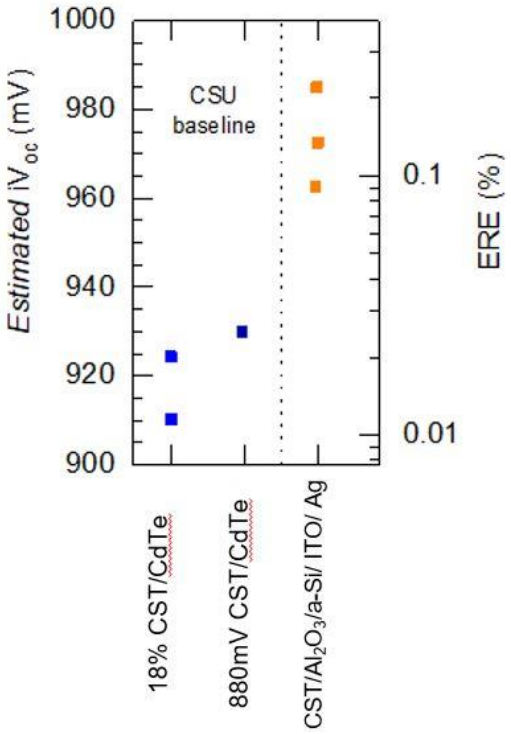


Figure 56 - ERE measurements for a passivated back contact sample, compared to the ERE of high-performing baseline structures.

External Radiative Efficiency - The improvement in interface passivation may also be seen in the ERE measurements of Figure 58. The addition of a 2 nm layer of Al_2O_3 improves the ERE by an order of magnitude. Several higher performing baseline copper-doped CdSeTe/CdTe devices with high conversion efficiencies and V_{OC}s still display ERE's of only

approximately 0.01%. The addition of Al_2O_3 by contrast increases the ERE to 0.1%. Later experiments with an optimized CdSeTe absorber boosted the ERE as high as 2.3%.

Table 3 - Back interface recombination velocities for CdSeTe/CdTe with various back contacts

Sample Structure	S_{Back} (cm/s)
MZO/CdSeTe/CdTe:Cu/Te (baseline)	$1.2x10^6$
MZO/ CdSeTe /CdTe:Cu/Al_2O_3	$8.3x10^5$
MZO/ CdSeTe/CdTe/Te (undoped)	$2.7x10^5$

Band Tails/sub bandgap features - Similar to with replacing copper doping with arsenic, the inclusion of an alumina passivating layer significantly improves the external radiative efficiency. The greater proportion of radiative recombination, in turn, increases the implied voltage of the device. However, it is necessary to inspect the band edge using EQE or PL for band tails or sub-bandgap features. These features reduce the effective bandgap of the material and therefore reduce the $V_{OC,rad}$ term in equation 5. The reduction of this term means that the implied voltage for any given ERE will be lower than in a sample without such features. Figure 59 shows the sub bandgap features for both copper and arsenic-doped samples with either a tellurium or an Al_2O_3 back contact. For both dopant cases, the passivating oxide increases the prevalence of the sub bandgap features, reducing the $V_{OC,rad}$ term by up to 75 mV depending on the severity (Onno et al. 2022). However, despite this reduction in $V_{OC,rad}$, the increased luminescence still results in an overall increase in the implied voltage compared to a non-passivated and especially a copper-doped sample.

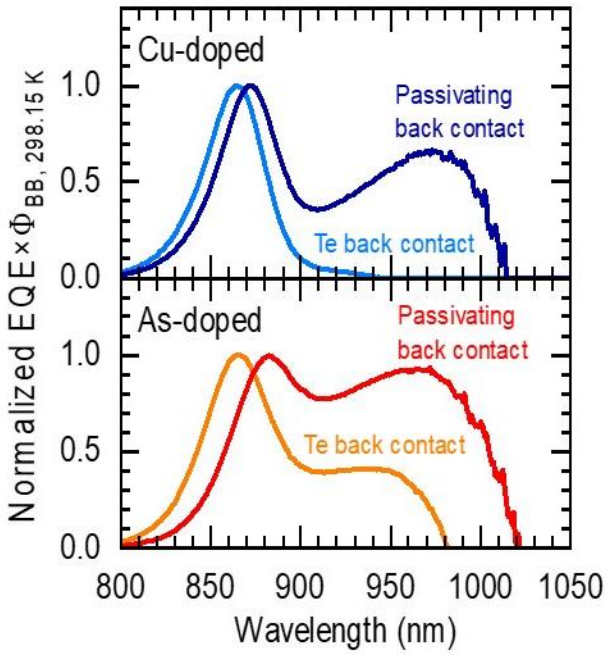


Figure 57 - Plot revealing the presence of large band tails and sub bandgap features reconstructed from EQE. The features are larger with aluminum oxide for both copper and arsenic-doped samples, adapted from (Onno et al. 2022)

Implied JV Curves - Utilizing ERE measurements taken as the light

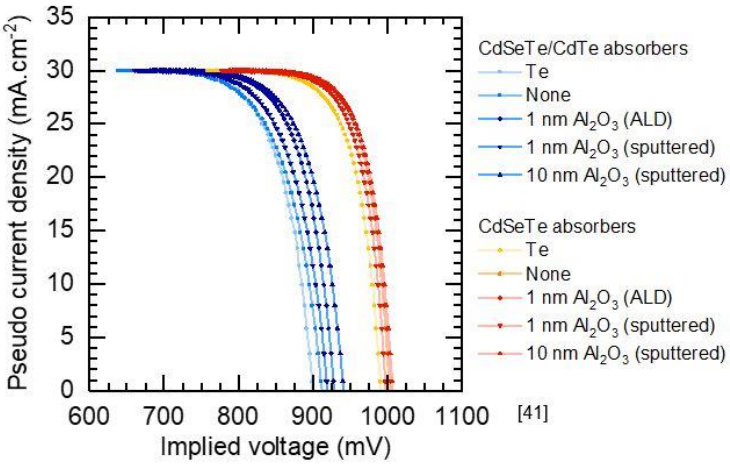


Figure 58 - Implied JV curves for CdSeTe/CdTe (Blue) and CdSeTe-only (Red/Orange) samples with various back contact structures.

injection is modulated (known as the Suns-ERE method, it is possible to construct an implied JV curve for a sample using only its photoluminescence emission. The same samples for which the TRPL lifetimes were shown were also measured using Suns-ERE. The resulting implied JV curves can be seen in Figure 60 and the implied efficiencies are shown in Figure 61. Similar to with carrier lifetimes, we see that CdTe is fundamentally limiting the potential performance of these device. CdSeTe/CdTe bilayers are limited to an implied voltage of approximately 900 mV and an implied efficiency of approximately 22–23%. By contrast, CdSeTe-only devices exhibit implied voltages of 1000 mV and implied efficiencies of 25–26%

JV Performance – Figure 62 shows the best (in terms of JV performance) Al_2O_3 back-contacted device made to date. This device contained 2 nm of Al_2O_3, 8 nm of p^+ a-Si, and approximately 70 nm of ITO. Despite the substantial increase in excess-carrier lifetime previously shown, this does not yet translate into improved open-circuit voltage. This device exhibited a V_{OC} below 780 mV, whereas a good baseline device without aluminum oxide may show as high as 860 mV. As previously mentioned, the Al_2O_3 is excellent at passivating the back interface, but by itself it does not help with hole extraction. The highly p-doped α-Si was intended to serve this purpose by inducing enough upward band bending to make a hole-selective contact. However, functioning devices such as shown here are only obtained when the $CdCl_2$ treatment follows the deposition of the Al_2O_3, a-Si, and ITO. It is currently unknown what effect the high temperatures and $CdCl_2$ treatment may have on the properties of these materials. Particularly, if the doping

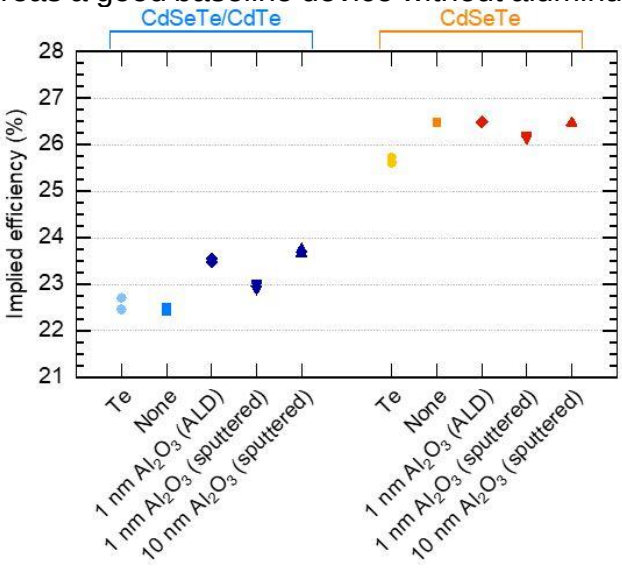


Figure 59 - Implied efficiencies for CdSeTe/CdTe (Blue) and CdSeTe-only samples (Red/Orange) with various back contact structures.

levels of the a-Si were drastically changed by the $CdCl_2$ treatment, it may no longer function as a hole contact as intended.

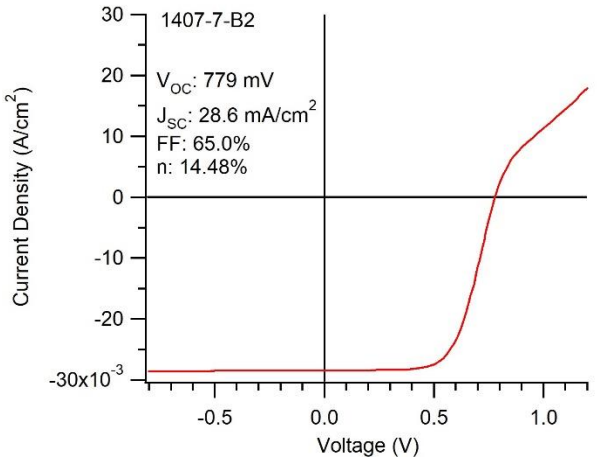


Figure 60 - Best JV performance of an Al_2O_3 back-contacted device (1407-7).

Results of Combining Al_2O_3 and Diffused-Arsenic Doping - While diffused-arsenic doping and Al_2O_3 passivation each individually improve the electro-optical properties of Cd(Se)Te devices, the combination of both results in further improvement in interface passivation and ERE while maintaining excellent lifetimes. This is consistent with the idea that improved doping densities, high bulk lifetimes, and less non-radiative interface recombination both contribute to greater quasi-Fermi level separation.

Interface Recombination -

The effects of both arsenic doping and aluminum oxide on the back surface recombination velocity have already been shown. below offers a full summary of these effects, along with data points for devices that contain both arsenic and aluminum oxide. As previously noted, the inclusion of arsenic and aluminum oxide separately each result in an improved back surface compared to a copper-doped, tellurium-contacted device.

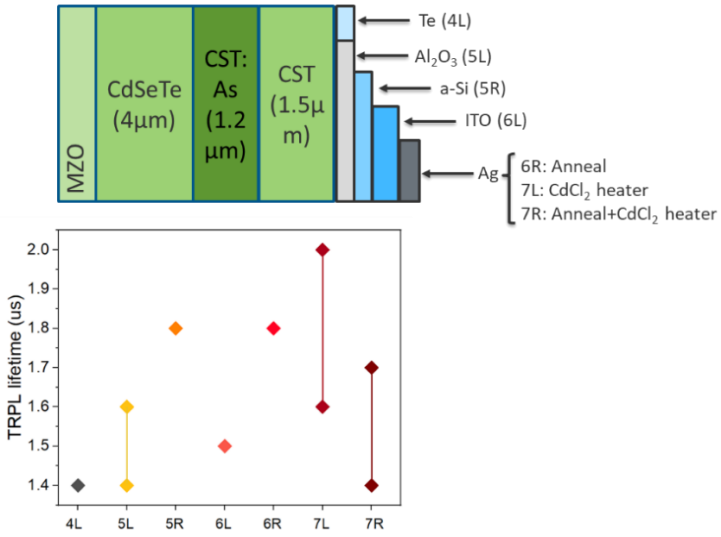


Figure 61 - Device structures and TRPL lifetime measurements for devices with diffused-arsenic doping and Al_2O_3 back contacts (1633)

When both are utilized, the back surface recombination velocity drops by nearly 2 orders of magnitude compared to the baseline device, from $1.2x10^6$ cm/s to $5.0x10^4$ cm/s.

Carrier Lifetimes - Figure 63 shows the structures and resulting TRPL lifetimes of devices fabricated during experiments which combined arsenic-doped CdSeTe absorbers with an aluminum oxide back contact layer. All of these devices demonstrated a measured τ_2 lifetime of greater than or equal to1.4 µs, reaching a maximum of 2 µs for a device with the full Al_2O_3/a-Si/ITO/Ag back contact stack. These lifetimes are slightly lower than what has been obtained with undoped CdSeTe films, which is consistent with the diffused-arsenic doping work which showed a slight reduction in carrier lifetime. Nonetheless, at more than a microsecond, these lifetimes remain among the highest ever measured for Cd(Se)Te samples.

External Radiative Efficiency - As both TRPL effective lifetime and interface recombination velocities are measures of e-h recombination rates, it comes as no surprise that improvements in both manifest as improvements to the ERE. Figure 64 and Figure 65 show the ERE measurements from two separate experimental runs utilizing both diffused-arsenic doping and Al_2O_3 passivation. The samples in Figure 64 used CdTe:As as the arsenic source and are compared to copper-doped and undoped samples. These devices all had a base CdSeTe/CdTe:As/CdSeTe structure (1601-6R). Additional devices included subsequent layers of Al_2O_3 (1601-6L), ITO (1601-7) and Ag (1601-8). 1601-4 was undoped while 1601-5 was copper doped, and 1601-10 was copper doped with a layer of Al_2O_3. It can be seen that even the undoped sample is a significant improvement over the previously reported ERE values for CdTe, largely due to the addition of selenium. However, copper-doping does not improve or reduces the radiative

Table 4 - Back surface recombination velocities for devices with As-doping and Al_2O_3 back contacts (Experimental Run 1601)

Sample Structure	S_{Back} **(cm/s)**
MZO/CdSeTe/CdTe:Cu/Te (baseline)	$1.2x10^6$
MZO/ CdSeTe /CdTe:Cu/Al_2O_3	$8.3x10^5$
MZO/ CdSeTe /CdTe/Te (undoped)	$2.7x10^5$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Te	$1.4x10^5$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3	$9.0x10^4$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3/a-Si	$8.0x10^4$
MZO/ CdSeTe /CdTe:As/ CdSeTe /Al_2O_3/a-Si/ITO	$5.0x10^4$

Table 1. Implied V_{OC} calculations for various device structures

Simplified Sample Structure	$V_{OC, ideal}$ (mV)	ERE (%)	iV_{OC} (mV)
MZO/CST/CdTe/Te	1152.9	0.03	940.7
MZO/CST/CdTe:Cu/Te (baseline)	**1152.3**	**0.01**	**900**
MZO/CST/CdTe:As/Te	1109	0.16	942.9
MZO/CST/CdTe:As/CST/Al_2O_3	1092.4	0.90	971.5
MZO/CST/CdTe:As/CST/Al_2O_3/ a-Si/ITO	1082.9	1.57	976.1
MZO/CST/CdTe:As/CST/Al_2O_3/ a-Si/ITO/Ag	1080.6	2.23	982.9
MZO/CST/CdTe:Cu/CST/Al_2O_3/ a-Si/ITO/Ag	1105.6	0.01	874.8
MZO/CST/Al_2O_3	1092	2.30	1005

efficiency. Alternatively, arsenic is shown to consistently improve ERE by nearly 2 order of magnitude, up to maximum of nearly 2% when combined with Al_2O_3.

Figure 63 shows the radiative efficiencies for devices with the same structure except the CdTe:As is replaced with CdSeTe:As. A systematic increase in the radiative efficiency is noted with the addition of each subsequent layer of Al_2O_3, a-Si, ITO, and Ag. In this plot all devices had a base structure of CdSeTe/CdSeTe:As/CdSeTe (1633-4L and 4R.) Each device after added a subsequent layer to the back contact: Al_2O_3 (1633-5L), p^+ α-Si (1633-5R), ITO (1633-6L), and Ag (1633-6R). 1633-7L and 7R were identical to the 1633-6R structure but received a $CdCl_2$ treatment with a top heater temperature ten degrees hotter than all other samples. The best ERE measured during this experiments was over 4%, not only is this higher than any other known measurement for CdTe-based devices, it is among the highest ERE values reported for any photovoltaic technology (GREEN 2012).

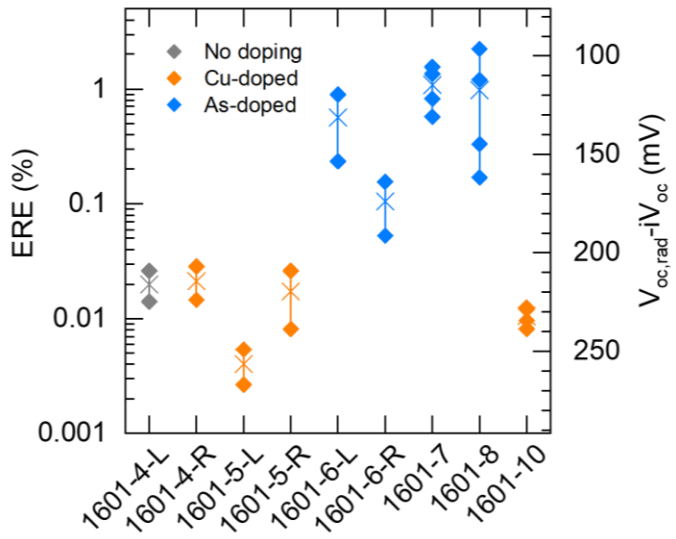


Figure 62 - External radiative efficiencies for CdSeTe/CdTe devices with various dopants.

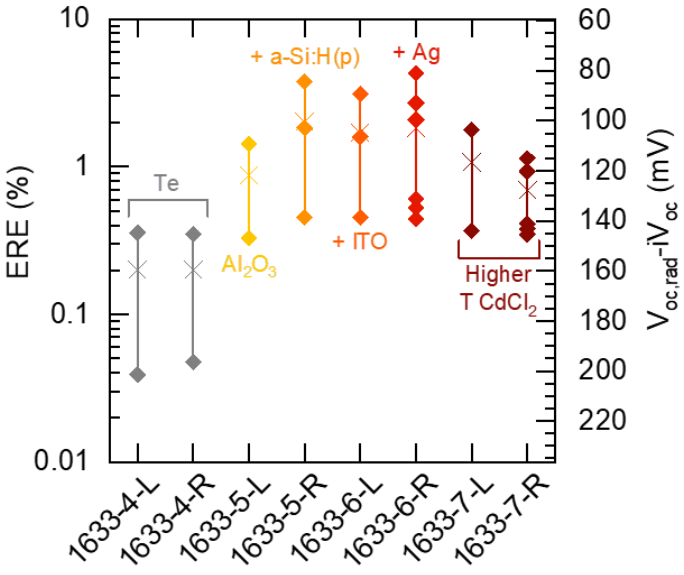


Figure 63 - External radiative efficiency for diffused CdSeTe:As devices with varying passivating back contact structures (1633).

Implied Voltage and Voltage Loss Analysis - Together, Table 1 and Figure 66 summarize numerous device structures and their resulting $iV_{OC,}$ calculated from equation 5, as well as a visualization of the various voltage losses. Replacing copper with diffused-arsenic results in several notable effects. First, there is a sizable increase in the iV_{OC} due to the greatly improved radiative efficiency. This is annotated by a green arrow pointing upward in Figure 64. This is somewhat offset by a decrease in $V_{OC,ideal}$ (synonymous with $V_{OC,rad}$ used previously). This is the effect of the increased sub-bandgap features and band tails. Ultimately, replacing copper doping with diffused-arsenic results in an improvement to the implied voltage from approximately 900 mV up to above 940 mV. The addition of Al_2O_3 as a passivating back contact layer further improves the ERE which drives up the implied

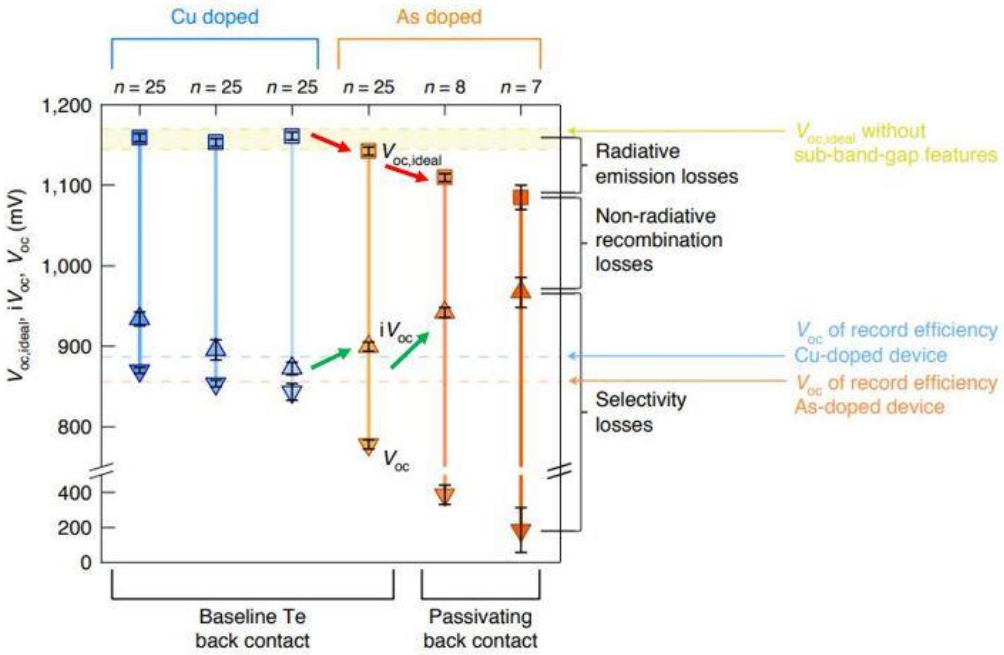


Figure 64 - Voltage loss analysis for CdSeTe samples with various dopants and back contacts, adapted from (Onno et al. 2022).

voltage while also exacerbating the sub-bandgap features and reducing the $V_{OC,rad}$. The subsequent addition of Al_2O_3, a-Si, ITO, and Ag systematically improves the iV_{OC} from

approximately 970 to 980 mV. The highest iV_{OC} measured to date for a sample with diffused-arsenic doping and a passivated back contact has an implied voltage of 982 mV. This result, just shy of the coveted 1 V mark, proves that the absorber structure is capable of producing voltages far greater than those typically seen today. The fact that these massive improvements in iV_{OC} have not been matched by an increase in actual device performance confirms that while Al_2O_3 is an excellent passivating layer, it is not an effective hole selective material. The large difference between the implied and actual voltages shown in orange in Figure 66 illustrates the criticality of finding an appropriate hole selective material.

Figure 66 is a recreation of the ERE vs voltage deficit plot shown earlier in this work. Here, several data points have been added which illustrate the progress made in improving the ERE for CdTe-based devices. It can be seen that these time-stamped data points do not follow the trend line, meaning that despite the improvement in radiative efficiency, the extracted voltage has not improved.

Results of Combining Al_2O_3 and Diffused-Arsenic Doping - While diffused-arsenic doping and Al_2O_3 passivation each individually improve the electro-optical properties of

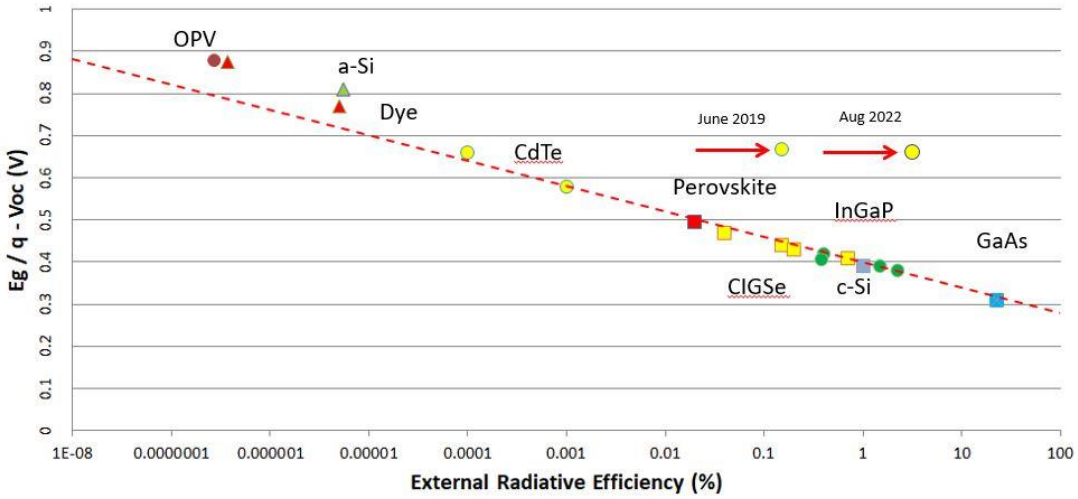


Figure 65 - Voltage deficit vs external radiative efficiencies for various photovoltaic technologies with recent CdTe progress, adopted from [27].

Cd(Se)Te devices, the combination of both results in further improvement in interface passivation and ERE while maintaining excellent lifetimes. This is consistent with the idea that improved doping densities, high bulk lifetimes, and less non-radiative interface recombination both contribute to greater quasi-Fermi level separation.

TeO_x Passivation **-** The carrier lifetime experiment displayed in Figure 68 produced a very surprising result. The control sample, with no Al_2O_3, displayed an excess-carrier lifetime of 6 µs. This was unexpected because the bare CdSeTe/air interface should have had a very high density of dangling bonds and recombination-active defects. During testing, which occurred at three separate universities/national labs, the samples were exposed to atmosphere for approximately two weeks before the TRPL measurements were performed. The results can be seen in Figure 68. Unsurprisingly, the relative intensity of the Te^{4+} peak, which is associated with oxidized tellurium (TeO_x) was greater after exposure to air. The proportion of oxidized tellurium at the surface, as determined by the ratio of peak heights, went from 0.32 to over 0.38 in as-deposited material and from 0.28 to 0.32 in $CdCl_2$-treated material. What was striking was that an increased oxidized tellurium fraction correlated with an increase in ERE, as seen in Figure 69.

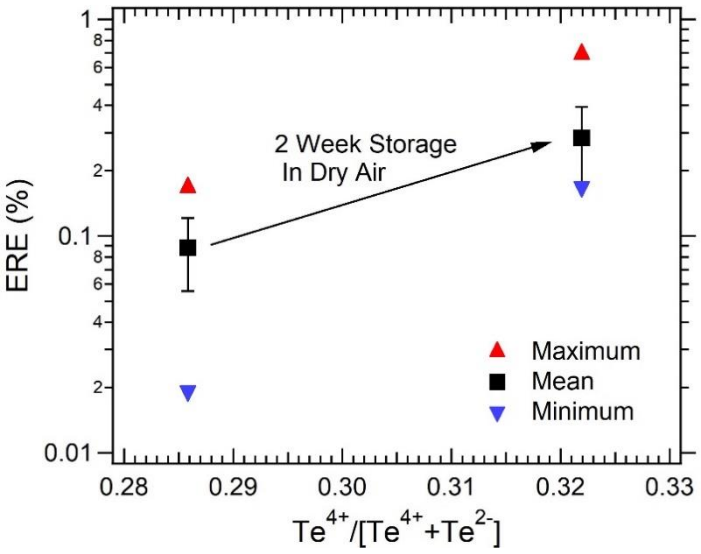


Figure 66 - Plot showing the increase in external radiative efficiency as a function of oxidized tellurium fraction.

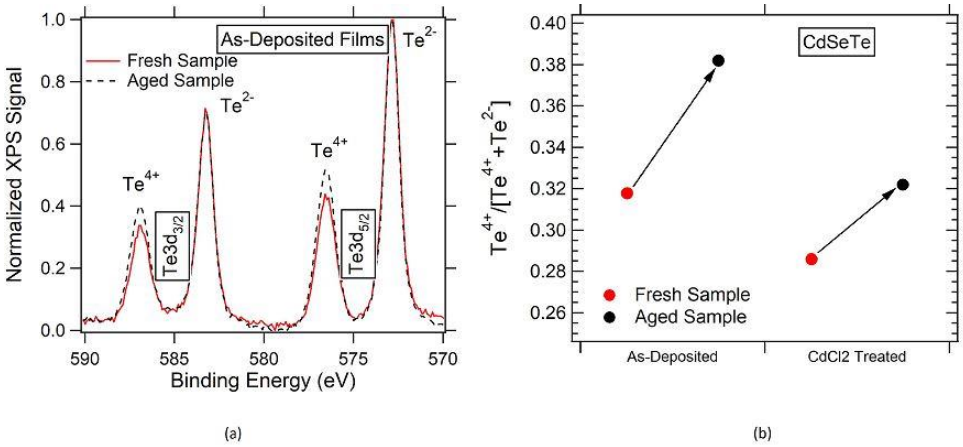


Figure 67 - (a) XPS spectra for As-deposited CdSeTe films showing that the relative Te^{4+} peak increases after two weeks exposure to air. (b) Plot showing the increase in oxidized tellurium fraction after aging for both as-deposited and $CdCl_2$-treated CdSeTe.

Extracting Current from CdSeTe-Only Devices - Although not the primary focus of this work, one conclusion which can clearly be drawn from the presented evidence is that CdSeTe has a much higher potential performance compared to CdTe or CdSeTe/CdTe bilayer absorbers. The highly luminescent and exceedingly-long lifetime CdSeTe films enable greater quasi-Fermi level splitting and therefore implied voltage than can be supported by a CdTe-containing architecture. Therefore, working towards a CdSeTe-only device structure was performed as a parallel effort to the doping and passivation work presented in the previous chapters. The intention was to incorporate the benefits of highly activated dopants and passivating oxides into absorbers with the greatest potential to maximize the total performance. Therefore, in many of the studies presented in this work, samples were fabricated where one sample contained CdTe or CdTe:As and another had a mirrored structure where the 1-4 μm CdTe was replaced with CdSeTe to maintain the same total thickness.

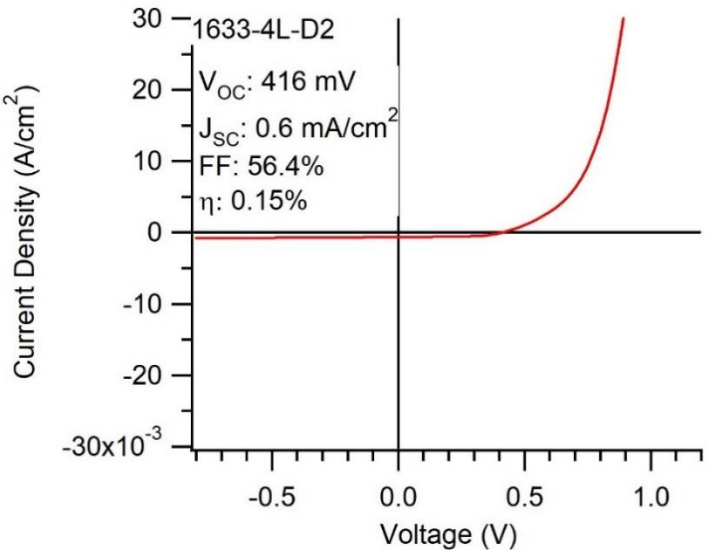


Figure 68 - Example of a zero short-circuit current device with a CdSeTe absorber (1633-4L)

Zero Current Device - Recall that the introduction of CdSeTe into previously CdTe-only devices resulting in a large improvement in J_{SC} due to the lower bandgap. The bandgap of CdSeTe varies depending on the selenium composition. From a bandgap of 1.49 eV as CdTe, the bandgap shrinks to a minimum of 1.37 eV at approximately 40% CdSe, then grows with increasing selenium as the bandgap approaches that of pure CdSe at 1.7 eV, described as “band bowing” (Muthukumarasamy et al. 2009; Swanson, Sites, and Sampath 2017). Because of this history, CdSeTe has typically been associated with higher currents, up to the maximum of 32 mA/cm^2 under AM1.5 illumination. Surprisingly, these CdSeTe-only devices would often produce zero current. The JV curve of an example zero-current device is provided in Figure 70.

It is possible that the CdSeTe, as deposited, is n-type due to a large number of V_{Te} caused by the high vapor pressure and low sticking coefficient of selenium, rather than the previously supposed p-type. The conductivity of a material to a particular carrier is proportional to the product of the mobility and the carrier concentration (Neamen 2003). Therefore, an n-type material will inherently have a lower conductivity to holes. N-type CdSeTe is not particularly problematic in the traditional CdSeTe/CdTe device structure.

In this structure, the CdSeTe layer is kept thin, typically less than 1 µm, so the holes do not have to travel far before reaching the p-type CdTe. Additionally, the diffusion of selenium between the CdSeTe and CdTe layers likely removes much of the V_{Te}. Finally, even if n-type CdSeTe is located at the front, it would display increased conductivity to the electrons which are moving toward the front interface. N-type CdSeTe is however highly problematic in a CdSeTe-only structure.

Alternatively, using electron backscatter diffraction, First Solar has noted that prior to $CdCl_2$ treatment, CdSeTe films contained large amounts of large bandgap wurtzite crystalline phase. Even small amounts of wurtzite phase resulted in decreased performance (Hayes 2016).

The intermittent loss of current in arsenic-doped devices is primarily due to three causes. Eliminating the following causes will result in devices with >25mA/cm^2 J_{SC}:

I) A buried junction caused by a layer of n-type CdSeTe.

II) Increasing selenium concentration causing the formation of photo-inactive wurtzite phase.

III) Increasing selenium concentration causing microstructural changes during film growth. These changes affect how $CdCl_2$ interacts with the film. $CdCl_2$ accumulation at the grain boundaries and interfaces confine charge carriers and reduce current.

Determining Carrier Type - Several characterization methods were employed to probe the doped nature of CdSeTe. The hot probe method is a simple method of determining the majority carrier type. Two electrical probes of a multimeter are put in contact with the semiconductor. The positive terminal is heated significantly above the temperature of the negative terminal. The thermal energy of the hot probe causes diffusion of the majority carrier away from the probe, inducing a voltage across the terminals. The sign of the voltage indicates the majority carrier type, a positive voltage indicates an n-type semiconductor while a negative voltage indicates p-type (Axelevitch and Golan 2013).

The Hall Effect measurement relies on the Lorentz force to determine the carrier type in a semiconductor (Hall Effect Measurements n.d.).

Scanning Kelvin Probe Microscopy (SKPM) is a particular variation of atomic force microscopy. This can be used to determine the type of carrier within the semiconductor (Al-Jassim n.d.).

Hall Effect and Hot Probe Measurements - Neither the Hall Effect nor the hot probe measurements gave conclusive results. In the case of Hall measurements, the Hall voltage was below the detection limit which not only made it impossible to determine whether the CdSeTe was n or p-type, but also indicated that regardless of the type, the carrier concentration was likely quite low. This is exacerbated if the material also has a low mobility. Hot probe measurements experienced a similar issue. An extremely low voltage was measured, and the sign of the voltage would change between subsequent measurements, which again likely indicates a film which is close to intrinsic.

Scanning Kelvin-Probe Microscopy Measurements – Figure 71 shows the results of the SKPM measurements. The top profile shows the topography of the film as determined by normal AFM measurement. The subsequent plots show the potential, potential difference, and ultimately the calculated electric field, respectively. The electric field, being slightly negative and relatively constant through the film depth indicate that undoped CdSeTe is slightly n-type. It should be noted that when considering hole conductivity, the difference between an intrinsic material and a slightly n-type material is not particularly impactful. Both materials are characterized by a low hole concentration which will be set by excess carriers within the interaction volume during illumination. Particularly if the hole mobility is also low, the semiconductor will have poor hole conductivity.

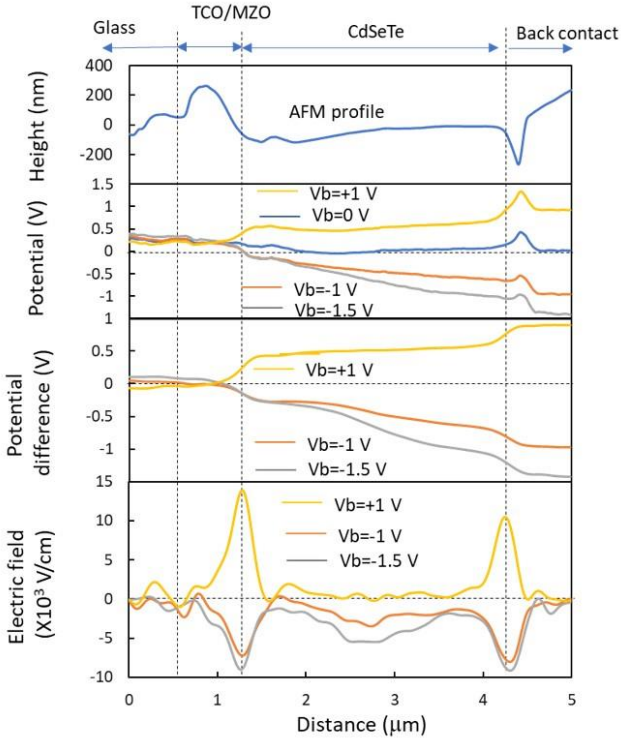


Figure 69 - Scanning Kelvin probe microscopy measurement of a CdSeTe-only device (1809-8L) indicating that the CdSeTe is slightly n-type, SKPM measurements performed at NREL.

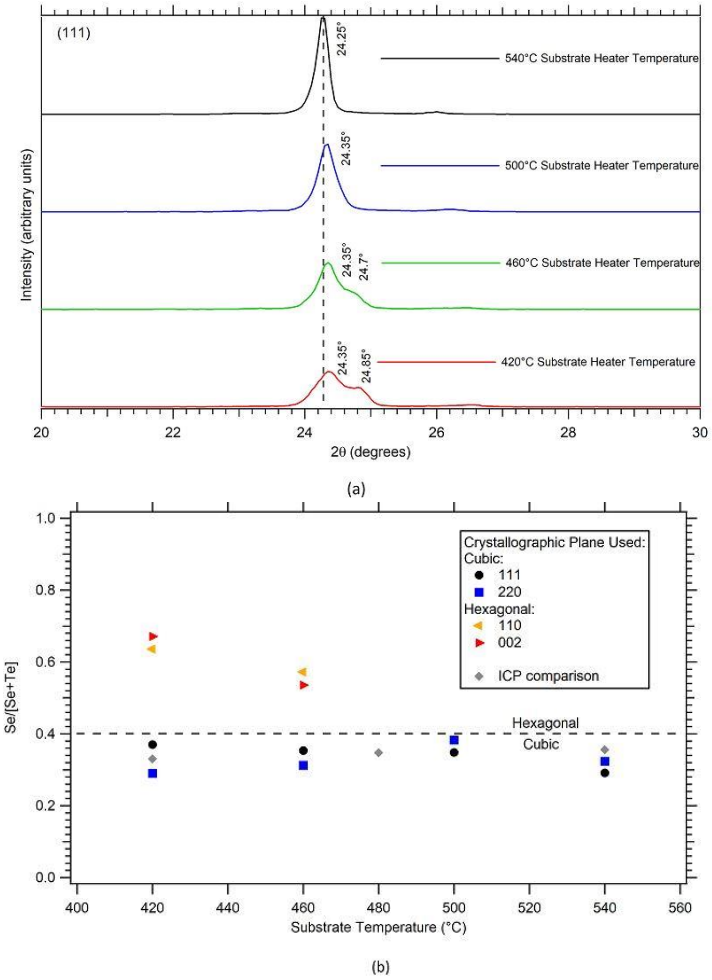


Figure 70 - XRD measurements of as-deposited $CdSe_{0.4}Te_{0.6}$ shows the reduction of the hexagonal peak and strengthening cubic peak as substrate temperature increases. The vertical dashed corresponds with the 540°C peak to aid in visualizing the peak shift. (b) A comparison of the selenium composition of the cubic and hexagonal phases within $CdSe_{0.4}Te_{0.6}$, as determined by a fit of the lattice parameters, adapted from (Danielson, A., Reich, C., Drayton, J., Bothwell, A., Shimpi, T., Sites, J., Sampath 2022).

Wurtzite Phase CdSeTe - In addition to the low hole conductivity caused by the apparent n-type or intrinsic nature of CdSeTe, the presence of wurtzite phase material may also contribute to current loss. CdSeTe forms cubic crystals until approximately 50% CdSe, at which point the hexagonal-phase wurtzite becomes energetically favorable. As previously mentioned, the bandgap also increases beyond 40% selenium up to a maximum of 1.7 eV for pure CdSe. Even if a film predominantly consists of cubic phase CdSeTe, even small amounts of a high bandgap material interspersed throughout it will likely serve as a barrier to carriers. While both carriers may be affected by this, the hole barrier will be more apparent because e-h generation occurs so much closer to the electron contact in CSU devices.

To study the formation of hexagonal phase CdSeTe, films were deposited where the substrate temperature during deposition was varied. The substrate heater was varied from 420°C, which was the historic temperature used for CSU CdSeTe/CdTe baseline structures up to 540°C. The films were then analyzed using Glancing Angle X-ray Diffraction (GAXRD), the results of which are shown in Figure 72a. In this figure, each fit peak location is annotated above the curve, and a vertical dashed black line is centered on the 540°C peak location to highlight the peak shift between samples.

It is apparent from the XRD spectra that the depositing film forms two sets of peaks at lower substrate temperatures corresponding to the cubic (111) and hexagonal (002)

phases, but a single cubic peak at higher substrate temperatures. Using XRD cards of the CdTe-CdSe solid solution the the lattice parameter a_0 for the cubic phase and the lattice parameters a and c for the hexagonal phases were fit.(Ben-Dor, L. Yellin, N. Shaham 1984; Litwin 1964; Shevchenko et al. 1974; Vitrikhovskii, N. Mizetskaya, I. Oliinyk 1971). Based on these fits and determination of the lattice constants using the cubic (111) and (220) planes and the hexagonal (002) and (110) peaks, composition for the different phases was calculated and compared to the selenium composition as determined by Inductively-Coupled Plasma Mass Spectrometry (ICP-MS). The comparison is shown in Figure 72b. First, it is apparent that the hexagonal phase has a selenium composition between x = 0.5 and x = 0.7, decreasing with the increased substrate heater temperature but always drastically greater than that of the cubic phase material. Additionally, it is clear that the volume fraction of these hexagonal phases is small, since the ICP-MS data agree with the compositions determined by the cubic phase, approximately x = 0.3 to 0.38. At temperatures of 500°C and greater, only the cubic phase is seen. The increased substrate temperature also resulted in large equiaxed grains and only a small decrease in the deposition rate.

Microstructural Changes and $CdCl_2$ Accumulation - The samples prepared for and presented in this work were fabricated using a CdSeTe source charge that was $CdSe_{0.4}Te_{0.6}$, meaning 40% CdSe mixed with 60% CdTe. This results in a 20 atomic percent selenium mixture. Figure 73 compares two EDS line scans performed on films that were fabricated from CdSeTe source charge that was initially at 20 atomic percent selenium.

Previous EDS measurements have shown that the selenium concentration in growing films is usually lower than that of the source charge, as not all the sublimated selenium incorporates into the film. Typically for a 20 atomic percent source charge, films show between 10 and 12 at% selenium. This is very similar to the first linescan shown in Figure 73. However, the second line scan shows that the selenium

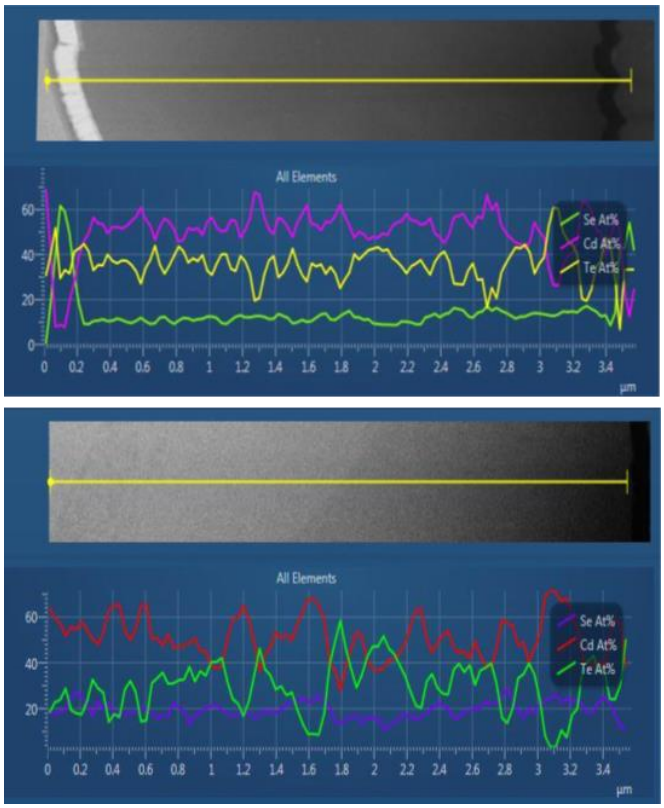


Figure 71 - EDS line scans comparing two devices, Sample 1546-7 (Top) and Sample 1633-4 (Bottom) deposited with the same source charge material composition.

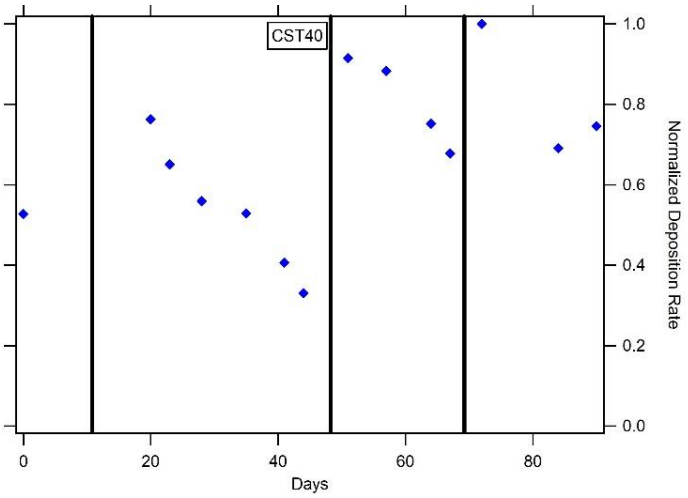


Figure 72 - The normalized deposition rate of CdSeTe over several months showing a drastic decrease as the source material is used. The vertical black lines represent when the source material was replaced with fresh material. Adapted from (Danielson, A., Reich, C., Drayton, J., Bothwell, A., Shimpi, T., Sites, J., Sampath 2022)

concentration is double the typical value at 20 atomic percent. This finding contributes to the growing body of evidence that the CdSeTe source material changes over time and therefore films fabricated under the same conditions at different times may not necessarily exhibit the same properties (Danielson, A., Reich, C., Drayton, J., Bothwell, A., Shimpi, T., Sites, J., Sampath 2022). As the source is heated, the constituent materials sublimate at different rates due to their differing partial vapor pressures. Over time, it is hypothesized that the CdTe disproportionately leaves the source material, leaving it selenium rich. This encourages the growth of wurtzite phase crystals, and drastically affects the deposition rate, as can be seen in Figure 74.

In addition to, and possibly because of the changes in selenium concentration, it has been noted that the film microstructure can vary greatly, even when the same materials and processing conditions are used. Figure 75 and Figure 76 are TEM images showing the grain structure of the same films for which the earlier EDS data was shown. The first TEM image shows a dense film with large grains. Contrastingly, the second image, which was intended to be a repeat of the first's structure, shows multiple voids and stacking faults. The thicknesses of these films were also considerably different, despite the same deposition time.

Finally, as the film density and prevalence of voids change within the film, the interaction between the $CdCl_2$ and the film changes too. $CdCl_2$ treatment is a necessary step in the fabrication of CdTe based devices, passivating defects and facilitating grain growth. But too much $CdCl_2$ can harm the device, particularly if large amounts of $CdCl_2$ reside at the interfaces. $CdCl_2$ is a high bandgap material and may block charge transport. Just such a device is shown in Figure 77, where the "light element grains" are $CdCl_2$ accumulation at the front interface.

If the $CdCl_2$ encounters a less dense film, it is likely to migrate towards the front interface more quickly. Like the previous discussions, the result is that the same $CdCl_2$ treatment may be optimal for one film, but the same treatment may drive too much $CdCl_2$ to the front interface in another. Therefore, the $CdCl_2$ optimization cannot be performed independently, robust control of film quality is a prerequisite.

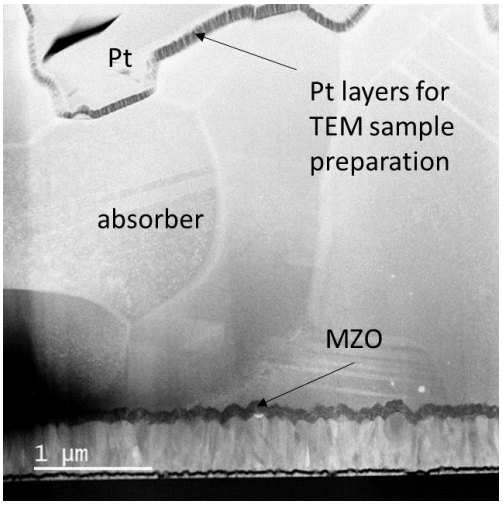


Figure 73 - TEM image showing large grained microstructure in an arsenic-doped device, Sample 1546-7.

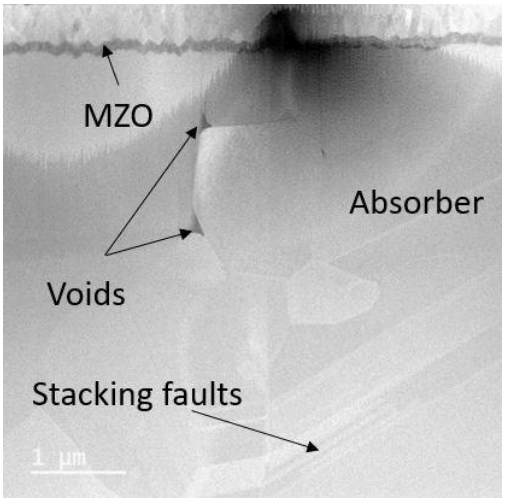


Figure 74 - TEM image showing an arsenic-doped film from sample 1633-4 with voids and stacking faults.

Recovering Current in CdSeTe-only devices - At present, numerous CdSeTe-only devices have been fabricated, each employing a unique set of strategies, and all producing a current density of at least 25 mA/cm^2.

Figure 78 shows the JV plot for a CdSeTe-only device with a conversion efficiency of 7.8% and J_{SC} of 25 mA/cm^2. This result was obtained by thinning the total CdSeTe layer down to 1 µm and then adding sputtered ZnTe:Cu as a hole contact. Accounting for low hole conductivity, the thin absorber ensures that e-h generation occurs close to the hole contact. The thin absorber has the added benefit of maximizing the excess carrier concentration and thus qFLS (assuming the interfaces are well passivated.) The CdSeTe was deposited at an elevated substrate heater temperature of 480°C to ensure a dense film consisting of large equiaxed grains and no wurtzite phase. ZnTe:Cu hopeful candidate as a hole contact due to its band alignment and purported ability to be highly p-doped, but has not yet been optimized. The low V_{OC} seen in this device is believed to be due to the poor interface passivation between the CdSeTe and the ZnTe:Cu. Despite this, the copper-doping may also assist in increasing the hole conductivity in the ZnTe and into the CdSeTe.

In another experiment (samples 1999-1,3), 2.5 µm thick CdSeTe films were fabricated. Some samples received a CuCl-doping treatment while others did not. Additionally, some samples were etched in a solution consisting of 20 g of citric acid dissolved in 100 mL of hydrogen peroxide to see if removing a portion of the absorber thickness affected current collection. Table below summarizes the J_{SC} results. The sample without a copper treatment or etch exhibited low current density at just 7 mA/cm^2.

The final experiment fabricated a CdSeTe film, reported at 820 nm thick and deposited at 420°C substrate heater temperature. After film deposition, the sample received a CuCl treatment and an 1800-second anneal over a Cd_3As_2 source maintained at 360°C while the substrate heater was set to 500°C. Figure 78 shows the JV plot for this device

compared to an identical sample which did not receive the Cd_3As_2 anneal. This plot reveals that while the non-annealed sample had a J_{SC} of approximately 12 mA/cm^2, the Cd_3As_2-annealed sample demonstrated a J_{SC} greater than 28 mA/cm^2. Previous experiments with Cd_3As_2, which are beyond the scope of this work, have shown that Cd_3As_2 may hold some promise as an alternative method for arsenic doping CdTe-based materials. Thus far, Cd_3As_2 has not been able to produce samples with the high dopant activation or radiative efficiency of the diffused-arsenic method. There has however, been some conflicting evidence that suggests that it may improve the acceptor concentration within the absorber. Regardless, the effect of the Cd_3As_2 anneal on the current collection in CdSeTe-only devices was substantial.

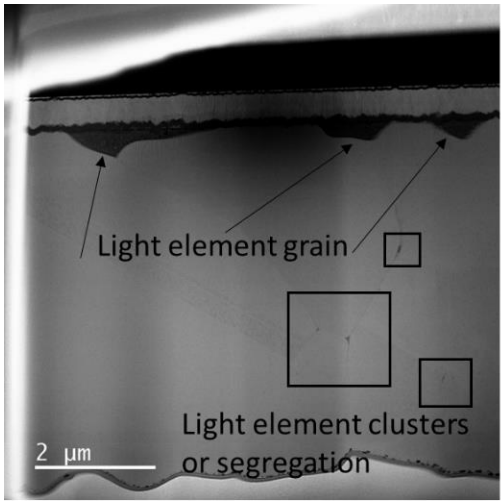


Figure 75 - TEM image showing the segregation of chlorine in voids and at the interface in sample 1633-4.

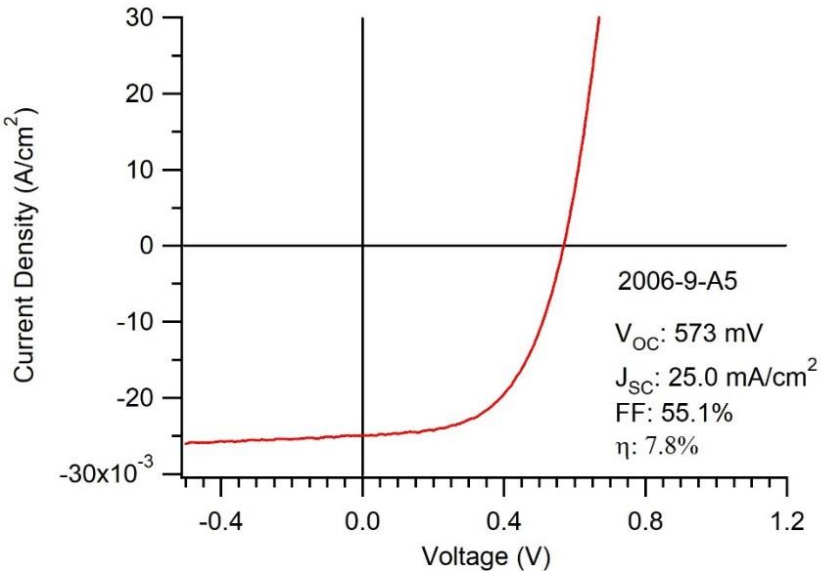


Figure 76 - JV plot of a CdSeTe/ZnTe device exhibiting 25 mA/cm^2 current density.

Table 5 - Current collection for CdSeTe samples with Cu-doping and an acid etch, experiment performed by Tushar Shimpi

Acid Etch	CuCl Treatment	J_{SC} (mA/cm^2)
No	No	7
No	Yes	26
Yes	No	5
Yes	Yes	28

SIGNIFICANT ACCOMPLISHMENTS AND CONCLUSIONS: Although the multiple methods for testing the carrier type in CdSeTe have different sensitivities and detection thresholds, they consistently and conclusively report very low acceptor concentrations. It is not certain if this is due to an absorber which is nearly intrinsic or lightly n-type doped, but at these levels, the difference is largely semantic rather than practical. The constant result is that the very low hole concentrations found in these films contribute to low hole conductivity, particularly if the hole mobility is also low, which may be impacted by the presence of wurtzite crystallites in the film.

In addition to the general low hole conductivity throughout the film, the presence of high bandgap wurtzite material may also create localized, sudden, and large energetic barriers which impede or even confine carriers. XRD measurements conclusively show that wurtzite is present in CdSeTe when deposited using the conditions which have historically been used. Based on this evidence, the standard substrate temperatures used for CdSeTe deposition by numerous researchers have been increased to a minimum of 480°C to prevent hexagonal phase formation. Of the potential issues impeding current collection, this was the most easily remedied, as the increased substrate temperature had only a small impact of the deposition time and resulted in a higher quality film.

The densification of the film that accompanied the increase in substrate temperature has reduced the prevalence of voids which has likely reduced $CdCl_2$ accumulation. Nonetheless, there exists widespread evidence that the CdSeTe source charge changes over time as it is used. The compositions of devices made from this source charge, therefore, are not constant either. These changes do result in differing structures, making it difficult to optimize $CdCl_2$ passivation without overdoing it until they can be made consistently the same.

Bearing in mind these potential sources of current loss, three separate strategies which have successfully recovered a current of at least 25mA/cm2 have been presented. The fact that each was able to recover current while being designed to mitigate one or more differing obstacles indicates that multiple issues contribute to current loss as opposed to a sole cause. There is however, one striking similitude between each of the three strategies to recover current: They each address the problem of low hole conductivity, albeit in different ways. Sample 2006-9 recovered current by thinning the total absorber thickness and by incorporating an increased substrate temperature to eliminate hexagonal phase material. Samples from experimental run 1999 also thinned the absorber thickness via etching, but recovered most of the current by using CuCl to dope the CdSeTe. Finally, sample 2018-5R thinned the absorber and utilized both copper and Cd_3As_2 to dope the film p-type. **Careful control over the device structure recovers full short-circuit current values. Additionally, of all the potential sources of current loss, the low hole conductivity, predominately driven by the low hole density in n-type CdSeTe is the primary factor limiting current collection from CdSeTe-only devices.**

The work presented in this report has been focused on utilizing arsenic doping and passivating oxides to reduce the voltage deficit in CdTe-based solar cells. Throughout this work, I have endeavored to show that copper, although historically used to dope CdTe, is a major limitation to future development. As a deep acceptor with low activation and self-compensation as well as a tendency to migrate, copper results in devices with low excess-carrier lifetimes, low luminescence, and consequently smaller implied voltages.

By contrast, arsenic doping has been shown to be a viable method for drastically improving the electro-optical properties of the absorber. Arsenic has resulting in films with higher measured carrier concentrations, longer lifetimes, lower interface recombination rates, higher radiative efficiencies, better implied voltages…often simultaneously and in the same sample. However, the arsenic doping method substantially alters the efficacy of the process. Fabricating films directly from an arsenic-containing source material without additional processing results in only moderate arsenic incorporation. This method has been shown to be able to incorporate up to 10^{18} cm^{-3} arsenic in CdTe and up to 10^{19} cm^{-3} in CdSeTe. Furthermore, the incorporation rate is insensitive to the cadmium overpressure that is present during deposition. The arsenic that does incorporate into the film does so as dimers, tetramers, and clusters as opposed to the desired monoatomic arsenic. The doping activation rate is therefore low and the devices exhibit low acceptor concentrations at or below 10^{14} cm^{-3} and lifetimes on the order of nanoseconds. To obtain the superior properties necessary for improved performance, further processing of arsenic containing films is needed.

These superior properties are obtained through the diffused-arsenic method. In this method, the arsenic-containing layer is deposited behind a layer of undoped CdSeTe. An aggressive $CdCl_2$ treatment, performed at an elevated temperature, encourages diffusion of arsenic from the initial layer into the previously-undoped CdSeTe. Kinetic simulations suggest that the only species of arsenic which is capable of diffusing any appreciable distance is interstitial arsenic, which quickly moves through a series of reactions culminating in As_{Te}, a shallow p-type dopant in Cd(Se)Te, resulting in activation rates of at least 26% and a graded doping profile. Using this method, microsecond lifetime and carrier concentrations greater than 10^{16} cm^{-3} have been

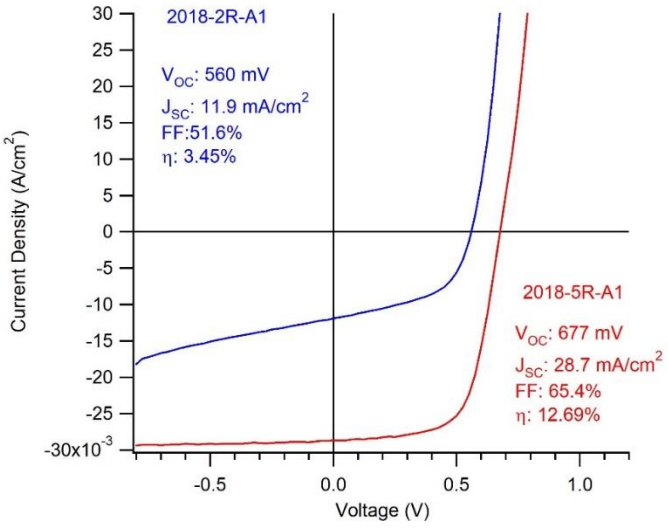


Figure 77 - JV plots of CdSeTe-only devices showing the effects of a 1800s Cd_3As_2 anneal (Red) compared to no anneal (Blue).

measured using CV. Resultantly, the implied voltages of diffused-arsenic samples are approximately 40 mV greater than have ever been measured for a copper-doped device.

Aluminum oxide has previously been shown to be effective at passivating silicon TOPCon solar cells, as well as CdSeTe in double heterostructures. In this work, Al_2O_3 was incorporated into function devices by adding a thin layer, typically 2 nm, at the back interface to provide interface passivation. Due to its large bandgap, Al_2O_3 has large offsets in both the conduction and valence bands when paired with Cd(Se)Te and therefore creates a large energetic barrier to both electrons and holes. While it is desirable that the electrons be repelled, this necessitates additional layers to ensure that holes can traverse this barrier and be extracted. To that end, p-type amorphous silicon, ITO, and a silver electrode were deposited behind the Al_2O_3 to induce upward band bending and encourage tunneling transport of holes through the Al_2O_3. When alumina was deposited behind CdSeTe, it resulted in a TRPL-measured lifetime of 8 µs, the longest lifetimes ever measured for polycrystalline CdTe-based materials. These lifetimes, along with improved interface recombination, again resulted in improved radiative efficiencies. Combining the diffused-arsenic method with aluminum oxide passivation further reduced the interface recombination velocity, contributing to ERE values as high as 4% and implied open-circuit voltages approaching 1 V.

Table 6 - Summary of Key Findings

ARSENIC DOPING	**ALUMINA PASSIVATION**
Arsenic incorporation of 10^{18} cm^{-3} in CdTe	Increased photoluminescence
Arsenic incorporation of 10^{19} cm^{-3} in	**Carrier lifetime of up to 8 µs observed**
Arsenic clusters observed in source	Al_2O_3 creates a large barrier to hole
Poor dopant activation and lifetimes in as-deposited films	**Combining As-doping and Al_2O_3 results in ERE of up to 4%**
DIFFUSED-ARSENIC DOPING	**IMPLIED VOLTAGE**
Diffusion of As_i necessary for high dopant activation	CdSeTe/CdTe bilayer reduces ERE/iV_{OC}
Doping density of 10^{15}–10^{16} cm^{-3}	Copper doping drastically reduces
Doping Activation > 25%	**iV_{OC} = 1 V achieved**
Graded doping profile	**Implied efficiency = 25%**
Reduced interface recombination velocity	**RECOVERING CURRENT IN CdSeTe**
Carrier lifetime > 1 µs	n-type CdSeTe, Wurtzite phase crystals & $CdCl_2$ accumulation observed
ERE > 2 %	**28 mA/cm^2 may be recovered**
High doping/long lifetime/high ERE in the same devices	Thinner absorber, improved CdSeTe crystallinity, and p-type doping improve hole conductivity

Despite these substantial improvements, the devices presented in this work did not demonstrate an improved open-circuit voltage. Both structures exhibit extremely poor carrier selectivity at the hole contact. While the absorber can produce a substantial internal voltage, that voltage is lost across the contacts due to the poor alignment of the hole contact conduction band and an inadequate ratio of hole/electron conductivities. Therefore the search for an appropriate hole contact for Cd(Se)Te should be considered a critical step in the future development of this technology.

CdSeTe has shown greater potential than CdTe as a material capable of producing the internal voltages necessary to exceed current voltage records. The benefits of diffused-arsenic doping and aluminum oxide passivation are maximized when paired with CdSeTe. Therefore, it is likely that future devices will consist of an entirely CdSeTe absorber layer. To aid in this endeavor, the cause of CdSeTe-only devices which produced no current needed to be studied and addressed. While several contributing factors were identified, the low hole conductivity, due to low hole density in intrinsic or slightly n-type CdSeTe appears to be limiting current collection.

Employing these methods, this contribution has shown that CdSeTe-only absorbers with well passivated interfaces and carrier selective contacts have the potential to produce devices with a photovoltaic conversion efficiency of at least 25%. Table below summarizes the key findings presented in this work. These advancements will place CdTe in good stead when competing in global energy markets as a cheap, reliable, and highly efficient photovoltaic technology. More importantly, highly optimized photovoltaics offer humanity additional tools to combat climate change while providing clean and renewable energy.

BUDGET AND SCHEDULE:

Project Start Date – 1/1/2019
Project End Date – 6/30/2022

Total Federal Funds Authorized - $750,000.00
Total Federal Funds Utilized - $749,909.61
Total Recipient Share Required - $187,500.00
Total Recipient Share Utilized - $190,439.67

No Changes to project budget or schedule were made.

PATH FORWARD: Despite the progress demonstrated in this work, a significant effort remains before the full implied voltage shown here can be extracted as an external voltage. Four main efforts have been identified and are briefly described below.

Optimizing CdSeTe-only devices - As previously discussed, the high lifetime of CdSeTe makes it a much more promising material for use in high efficiency solar cells compared to CdTe. Chapter 8 discussed several of the difficulties that were encountered when transitioning from a CdSeTe/CdTe bilayer absorber to CdSeTe-only, but there are other

issues which still need to be addressed. First, the most widespread commercial method for depositing CdSeTe today is to deposit a thin layer of CdSe followed by CdTe and using the $CdCl_2$ process to create CdSeTe. This is an excellent method for creating an absorber with a graded bandgap due to selenium diffusion. This method, however, may not be appropriate for creating an absorber where the full thickness has a consistent selenium content. Additionally, it was alluded toearlier, but CdSeTe film growth and the resulting grain structure has been found to be highly sensitive to certain deposition conditions, particularly the substrate temperature during fabrication. Figure 80 reveals the radical change in CdSeTe grain structure as the substrate heater temperature is increased from 420°C to 540°C, as seen using SEM imaging. The grain boundaries in CdTe have been previously identified as recombination-active areas (Moseley et al. 2015), and minimizing grain boundaries by increasing grain size corresponded with an increase in device performance (Major et al. 2010). It remains to be seen whether there is a similar benefit to increasing the CdSeTe grain size, particularly given the highly passivating nature of selenium in CdTe. Particularly if the total absorber thickness is thinned down to between one and two micrometers, grains which run the full depth between the two contacts should be possible. The cross-sectional SEM image shown in Figure 81 gives an example of a CdSeTe film where dense, multi-micrometer-sized grains have been obtained, although they are not full depth in the shown sample.

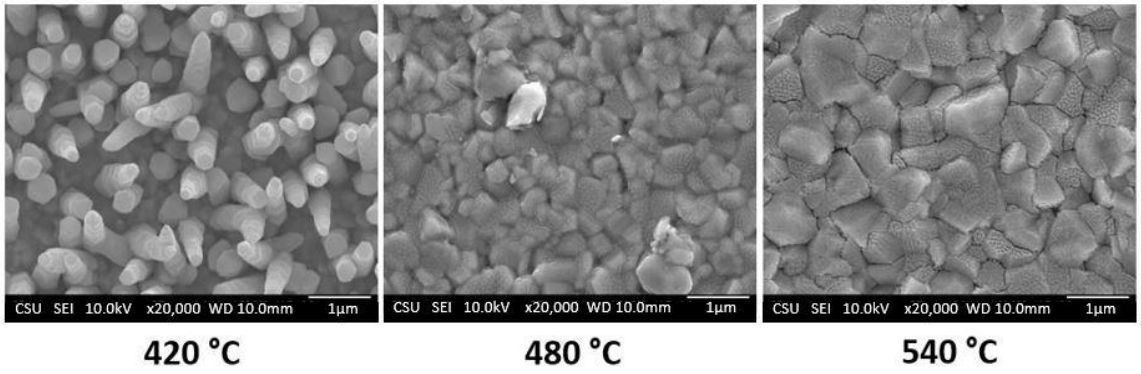


Figure 78 - SEM images of as-deposited CdSeTe, showing extreme columnar growth occurring at lower substrate temperatures and larger, equiaxed grains at higher temperatures.

Explore undoped CdSeTe devices to maximize implied voltage - It is clear that the diffused-arsenic-doping method results in carrier lifetimes which are orders of magnitude greater than what has been achieved using copper doping. Nonetheless, there is still a small decrease in TRPL-measured lifetime for arsenic-doped samples compared to undoped CdSeTe. This is to be expected, as anything less than 100% dopant activation means that there is some arsenic within the absorber which is simply acting like a defect, likely creating a site for non-radiative recombination. In fact, even with perfect activation, as the concentration of electrons and holes increase, the radiative-limited lifetime will decrease due to the nature of recombination being dependent upon electrons and holes

finding one another (Peter Wurfel and Uli Wurfel 2016). For this reason, an undoped absorber may be capable of supporting greater-quasi Fermi level separation than its doped counterpart. This is the basis of the p-i-n solar cell structure. An undoped CdSeTe absorber, with sufficiently long lifetime would ensure that each charge carrier could reach its respective contact. Carrier selectivity could then be derived from the band alignment of the two contacts, without having to modify the absorber layer, which could improve the overall absorber quality and simplify the manufacturing process.

Utilize Arsenic doping to improve hole conductivity - As illustrated, there may be issues springing from using an entirely undoped, nearly intrinsic layer of CdSeTe as the absorber. A low hole concentration was determined to be a key factor contributing to CdSeTe-only devices which produced zero current. As carrier conductivity is the product of the carrier mobility and carrier density, poorly doped films will naturally exhibit lower conductivity. Worse, if the material naturally has a low carrier mobility, as is suspected of CdSeTe for holes, then these factors combine to create a conductivity that is prohibitively low for charge transport through the absorber and into an external circuit. Therefore, it may be that an entirely undoped CdSeTe absorber is not feasible. If this is the case, arsenic doping may yet be necessary. In this case, the arsenic doping may not be used to achieve a bulk doping level in excess of 10^{16} cm^{-3} as shown in this work, but rather just the minimum doping required to achieve proper levels of hole conductivity while maintaining very high levels of arsenic activation. Possibly the diffused-arsenic method could be used, if an effective method of removing the “reservoir” material is found, or alternatively a new material which can easily be applied to and removed from the back surface of the CdSeTe, like how aluminum paste is utilized in Back-Surface Field (BSF) silicon solar cells or spin-on dopants. SCM measurements will be a valuable tool when measuring carrier concentrations, particularly towards the back of devices, where CV measurements cannot probe.

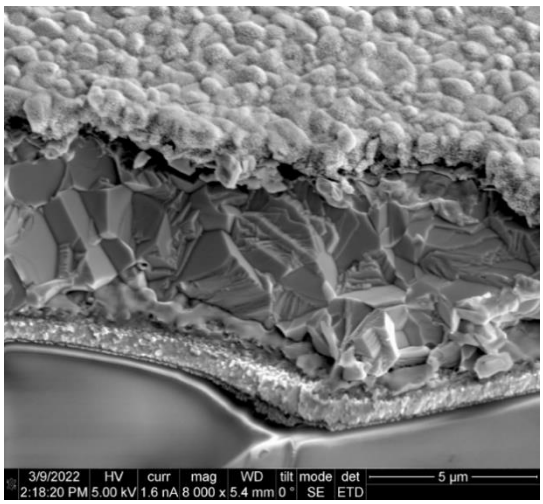


Figure 79 - Cross-sectional SEM image showing large dense grains of CdSeTe and a top layer of Al_2O_3.

Find an effective hole contact for Cd(Se)Te - The final proposal for future work is hardly a new one. For several decades researchers have struggled with finding an appropriate hole contact. Cd(Se)Te’s large work function makes it difficult to find a partner material which has an appropriately large valence band energy and a large conduction band offset with Cd(Se)Te. Nevertheless, this is perhaps the most critical task needed to enable next generation CdTe-based solar technology. This work has shown that multiple CdSeTe architectures, each utilizing a different combination of diffused-arsenic, aluminum oxide passivation, and large-grained, dense CdSeTe absorbers have already produced implied voltages ranging from 970–1000 mV. This signifies that selectivity losses caused by

imperfect contacts is preventing this technology from producing 1 V cells today. Copper-doped samples exhibit low selectivity losses, which indicates that the MgZnO electron contact is not the source of most of the selectivity losses in the current structure. Therefore, improvements to the hole contact are almost certain to produce large gains in external voltage. Possible candidate materials include both intrinsic ZnTe and ZnTe:Cu, platinum, TiO_x, MgO and MXenes, as well as a number of organic-based hole transport layers such as Poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA.) Finally, it may be possible to incorporate perovskite layers which have shown excellent hole selectivity in other technologies, although the sensitive nature of these materials may make it difficult to incorporate into existing processes. Regardless of which material ultimately proves to be the best, a well-passivated back interface between CdSeTe and an optimized hole-selective contact with proper band alignment will minimize voltage loss across the contact, maximize the external voltage, and push the device performance beyond what has thus far been possible.

INVENTIONS, PATENTS, PUBLICATIONS, AND OTHER RESULTS -

Peer Reviewed Journal Publications -

Danielson, A., Reich, C., Munshi, A., Pandey, R., Sites, J., & W. Sampath "Electroptical characterization of arsenic-doped CdSeTe and CdTe solar cell absorbers doped *in-situ* during close space sublimation". Thin Solid Films. *Under Review*.

Danielson, A., Reich, C., Bothwell, A., Drayton, Shimpi, T., Sites, J., & W. Sampath "A comprehensive material study of CdSeTe films deposited with differing selenium compositions*". Under Review*.

Reich, C., Danielson, A., Onno, A., Mahaffey, M., Weigand, W., Holman, Z., & W. Sampath "High efficiency undoped CdSeTe solar cells enabled by long lifetimes". *In preparation.*

Xiao, C., Jiang, C-S., Nardone, M., Albin, D., Danielson, A., Munshi, A., Shimpi, T., Sampath, W., Jones, S., Al-Jassim, M., Teeter, G., Haegel, N., & H. Moutinho "Microscopy Visualization of Carrier Transport in CdSeTe/CdTe Solar Cells," ACS Applied Materials & Interfaces. Accepted. (2022)

Onno, A., Reich, C., Li, S., Danielson, A., Weigand, W., Bothwell, A., Grover, S., Bailey, J., Xiong, G., Kuciauskas, D., Sampath, W., & Z. C. Holman "Understanding what limits the voltage of polycrystalline CdSeTe solar cells," *Nature Energy*. (2022) https://doi.org/10.1038/s41560-022-00985-z

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