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APPLICATION OF CHEMICAL-MECHANICAL POLISHING TO PLANARIZATION OF SURFACE-MICROMACHINED DEVICES

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ABSTRACT

Chemical-Mechanical Polishing (CMP) has emerged as an enabling technology for the manufacturing of multi-level metal interconnects used in high-density Integrated Circuits (IC). In this work we present the extension of CMP from sub-micron IC manufacturing to the fabrication of complex surface-micromachined Micro-ElectroMechanical Systems (MEMS). This planarization technique alleviates processing problems associated with fabrication of multi-level polysilicon structures, eliminates design constraints linked with non-planar topography, and provides an avenue for integrating different process technologies. We discuss the CMP process and present examples of the use of CMP in fabricating MEMS devices such as microengines, pressure sensors, and proof masses for accelerometers along with its use for monolithically integrating MEMS devices with microelectronics.

INTRODUCTION

Local and global planarization techniques have become key manufacturing technologies for the fabrication of high-density Integrated Circuits (IC). Several methods such as BPSG reflow [1], spin-on-glass [2], and plasma etch [3] have been historically used to accomplish planarization in the IC industry. As increased metal interconnect levels are used and as photolithography requirements are tightened for sub-micron IC fabrication, Chemical-Mechanical Polishing (CMP) has emerged as an enabling technology for fabrication of these structures [4]. CMP processes produce both global and local planarization through relatively simple and quick processing.

In micromachining, the use of polysilicon and silicon dioxide as a structural and sacrificial material, respectively, has been widely employed since its introduction [5]. As these relatively thick (~2 μm) layers of polysilicon and oxide are deposited and etched, considerable surface topography arises which imposes limitations in deposition, patterning, and etching of subsequent layers. It is desirable to planarize specific layers in order to eliminate processing difficulties associated with photoresist step coverage, depth-of-focus of photolithography equipment, and stringer generation during dry etch. Presently, these problems are addressed through careful design of structures, special photoresist processes, and the use of extra mask levels.

In the area of Micro-ElectroMechanical Systems (MEMS), fabrication issues associated with non-planar devices and techniques for overcoming topography problems are just beginning to appear. Researchers at U. Wisconsin have demonstrated locally-planarized surface-micromachined pressure sensors produced in a double LOCOS process [6]; while the use of plasma planarization has recently been demonstrated on MEMS devices by researchers at Delft [7]. Although these planarization techniques have yielded improvement in the manufacturability of MEMS devices through local planarization, CMP provides a higher quality of both local and global planarization in a manufacturing environment. Recently, researchers at Case Western have used CMP to improve the optical quality of mirrored surfaces produced on polysilicon surface-micromachined devices [8] by reducing the roughness of the polysilicon.

Additionally, present non-planar multi-level, surface-micromachining technologies place constraints on designs for upper polysilicon levels to prevent their interference with previously deposited layers. The planarization of sacrificial oxide layers prior to deposition of subsequent, conformal polysilicon layers removes these design constraints and enables the fabrication of new classes of devices. Examples of these new devices are flow channels that contain other micromachined structures within the flow channel and planar covers with applications in packaging of devices. CMP planarization provides an avenue to integrate separate process technologies such as microelectronics and micromechanics or surface micromachining and high-aspect-ratio micromachining. The planarization offered by CMP will also enable the fabrication of devices with four or more structural levels of polysilicon.

CHEMICAL-MECHANICAL POLISHING

Figure 1 illustrates the CMP process in which an oxide surface is planarized by rotating a wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry. The theory of oxide polishing is not well understood; however, it is generally accepted that the alkaline chemistry hydrolyzes the oxide surface and sub-surface thus weakening the SiO_2 bond structure [9]. The mechanical energy imparted to the abrasive slurry particle through pressure and rotation causes high features to erode at a faster rate than low features, thereby planarizing the surface over time. For the particular results shown here, a colloidal-fumed silica slurry (Cabot SS-12) and a polyurethane pad (Rodel IC1000/Suba IV) are used.

One of the main differences between planarizing inter-level dielectric materials used in ULSI interconnect technology and sacrificial oxide material used in MEMS technology is the large step heights (2-4 μm vs. 0.8 μm) associated with MEMS. These large step heights present a challenge to any planarization strategy. Figures 2 and 3 show the surface topography of single level polysilicon structure prior to CMP (2) and after the CMP process (3). As can be seen from the figure, CMP does an excellent job of removing the ~ 2 μm step height and planarizing the surface.

MEMS APPLICATIONS OF CMP

Improved Manufacturability of MEMS with Large Topography

The deposition and subsequent patterning of thin films conformally deposited over large surface topographies poses significant manufacturing challenges. These challenges include problems with photoresist coverage near large step heights, stringer generation at these steps during dry etch, and photoresist removal. An example of a stringer after release from the edge of a surface-micromachined gear is shown in Figure 4. Planar structures inherently alleviate these problems caused by step heights without the need for additional processing or careful design.

Multi-Level Structures

Multiple levels of structural polysilicon enable fabrication of increasingly complex MEMS devices such as microengines [**10**] capable of driving sets of gears. Simple flexure structures such as comb drives [**11**] can be built in a single level of structural polysilicon while a second level enables the production of gears with pin joints. A third level enables linkages between spinning gears, but introduces severe topography problems that must be solved with a combination of careful process and device design. Figure 5 shows the hub and linkage arm of an electrostatic microengine fabricated in a non-planar technology. Intrusion of upper polysilicon levels into gaps left between lower polysilicon levels complicates design and limits layout flexibility in addition to causing undesirable areas of stress concentration. These intrusions are clearly seen in Figure 5, but are completely eliminated in the structure fabricated with CMP shown in Figure 6. Additional levels of polysilicon promise even more complex structures, but the extreme topography of these multi-level structures (four or more active layers) has prohibited their fabrication. A micromachining technology that includes planarization steps such as CMP will enable device fabrication with these additional levels.

CMP also enables the fabrication of structures with flat covers fabricated in upper polysilicon levels that overlap structures fabricated in lower polysilicon levels. Figure 7 shows a fluid pump with a constant cross-section flow channel containing a pumping shaft. Close vertical dimensions between the polysilicon pumping shaft and its cover must be maintained without intrusion of the cover into the pump mechanism. The fabrication of this structure without planarization would have been nearly impossible. These types of covers made from polysilicon or silicon nitride deposited over refilled and planarized regions may also be used for packaging of MEMS.

Pressure Sensors

A planar pressure sensor technology [**12**] has been developed based upon a silicon nitride layer as the diaphragm material. A trench is etched ~2 μm deep in the surface of a silicon wafer. This trench is refilled with a sacrificial oxide and planarized with CMP. A silicon nitride diaphragm layer is then deposited. The sacrificial oxide underneath this diaphragm layer is removed using HF leaving a cavity beneath the diaphragm. An additional silicon nitride layer is used to seal the cavity in near-vacuum conditions (approx. 200 mTorr). Polysilicon piezoresistors are deposited on the diaphragm to sense the diaphragm strain that results from changes in ambient pressure. A completed, 100-μm-diameter planar pressure sensor is shown in Figure 8. This sensor shows marked improvement in planarity when contrasted against a similar, non-planar sensor shown in Figure 9.

In the non-planar sensor manufactured without CMP the reference pressure cavity is formed above the silicon surface producing large step heights. These steps cause processing difficulties with photoresist coverage and removal, dry etch selectivity to photoresist where the photoresist thins over steps, and metal step coverage. These challenges to manufacturing were eliminated in the CMP-planarized sensor. In the future, the use of an embedded cavity will enable the monolithic integration of this sensor technology with CMOS in a modified version of the integration process described later in this paper and will also enable the use of deeper vacuum cavities to extend the sensing range of the devices.

High-Aspect Ratio Micromachining

In addition to its uses for planarization of surface-micromachined devices, CMP plays a key role in the fabrication of high-aspect ratio micromolded polysilicon and tungsten devices. In the technology presented here[**13**], deep, narrow trenches lined with oxide are filled with thin films (~2-5 μm) of either polysilicon as shown in Figure 10 or tungsten as shown in Figure 11 and planarized with CMP. These structures can then be integrated with surface micromachined polysilicon structures to form large high-aspect-ratio proof masses with compliant surface-micromachined springs as shown in Figure 12.

Integration of MEMS with Microelectronics

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MEMS with driving, controlling, and signal processing electronics [**14**]. The monolithic integration of micromachines and microelectronics enables the development of wide new classes of small, smart, products with maximum levels of system performance. A new integration scheme [**15**] overcomes the limitations of traditional integration schemes and enables, for the first time, the integration of micromachines of arbitrary complexity with high performance, state-of-the-art CMOS. Functionality yields in excess of 70% have been achieved with this technology. Examples of devices built in this technology are shown in Figures 13 and 14.

We have developed this embedded MEMS approach to enhance the manufacturability, design flexibility, and performance of microelectronic/micromechanical devices. This process places the micromechanical devices in a shallow (~6-12 μm)trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topography of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures.

Figure 15 is a schematic cross-section of the integrated technology. Alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench is etched in (100) silicon wafers using an anisotropic etchant that preferentially etches the (100) crystal plane

and produces a trench with sidewalls having a slope of 54.7° relative to the surface. This slope aids in the subsequent photo patterning within the wells.

The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench. This approach is used to optimize level-to-level registration and resolution of features within the trench. Feature sizes with critical dimensions as small as 0.8 μm were successfully defined within the trench.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the planarized trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires an additional step to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures. Photoresist is used as a protection layer over the exposed bond pads during the release process.

This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. A planarized wafer with the embedded MEMS can serve as starting material for a conventional microelectronics foundry service since the technology does not require significant modifications of standard microelectronic fabrication processes.

CONCLUSION

Just as planarization techniques are now important in multi-level-metal IC processes, planar processing is emerging as a crucial step in fabrication of complex MEMS such as devices with multiple structural levels, enclosures, embedded reference pressure cavities, or integrated microelectronics. In this paper, CMP has been demonstrated as a valuable processing technique to add to the toolbox of today's sophisticated micromachinist.

ACKNOWLEDGMENTS

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REFERENCES

1. S. Robles, K. Russell, M. Galiano, V. Kithcart, V. Sira, and B. C. Nguyen, "Benefits of Sub-Atmospheric CVD BPSG Over the Conventional Pressure Process", *Proc. VLSI Interconnect Conference*, p. 122, (1995).

2. L. Chen, "Aspect-Ratio-Independent-Coating (ARIC) SOG Process for the Double Metal 16M DRAM Planarization", *Proc. VLSI Interconnect Conference*, p. 274 (1995).

3. A. Nagy, J. Helbert, "Planarized Inorganic Interlevel Dielectric for Multilevel Metallization", *Solid State Technology*, p. 53, Jan. (1991).

4. W. Patrick, W. Guthrie, C. Standley, and P. Schiable, "Application of Chemical Mechanical Polishing to the Fabrication of VLSI Circuit Interconnections," *Journal of the Electrochemical Society, 138*, pp. 1778-1784 (1991).

5. R. Howe and R. Muller, "Polycrystalline Silicon Micromechanical Beams," *Journal of the Electrochemical Society, 103*, pp. 1420-1423 (1983).

6. H. Guckel and D. Burns, "Planar Processed Polysilicon Sealed Cavities for Pressure Transducer Arrays," *IEDM*, pp. 223-225 (1984).

7. Y. Li, P. French, and R. Wolffenbuttel, "Plasma Planarization for Sensor Applications," *IEEE JMEMS, 4*, pp. 119-131, (1995).

8. A. Yasseen, S. Smith, M. Mehregany, F. Merat, "Diffraction Grating Scanners Using Polysilicon Micromotors," *Proc. IEEE MEMS '95*, pp. 175-180 (1995).

9. L. Cook, "Chemical Processes in Glass Polishing," *J. Non-Cryst. Solids, 120*, pp. 152-171, (1990).

10. E. Garcia and J. Sniegowski, "Surface Micromachined Microengine," *Sensors and Actuators A, 48*, pp. 203-214 (1995).

11. W. Tang, T-C. Nguyen, and R. Howe, "Laterally Driven Polysilicon Resonant Microstructures," *Sensors and Actuators, 20*, pp. 25-32 (1989).

12. W. Eaton and J. Smith, "Surface-Micromachined Planar Pressure Sensor with a Sub-Surface, Embedded Reference Pressure Cavity," submitted to SPIE Micromachining and Microfabrication (1996).

13. J. Fleming and C. Barron, "Novel Silicon Fabrication Process for High-Aspect-Ratio Micromachined Parts," *Proc. SPIE Micromachining and Microfabrication '95, 2639*, p. 185 (1995).

14. R. Howe, "Polysilicon Integrated Microsystems: Technologies and Applications," *Proc. Transducers* '95, pp. 43-46 (1995).

15. J. Smith, S. Montague, J. Sniegowski, J. Murray, and P. McWhorter, "Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS", *Proc. IEDM ' 95*, pp. 609-612 (1995).

FIGURES

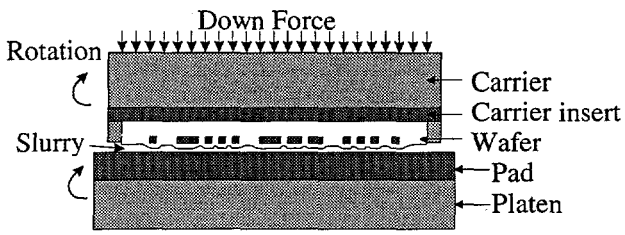

Figure 1. Schematic representation of CMP process in which an oxide surface is planarized by rotating the wafer under pressure against a polishing pad in the presence of a silica-based alkaline slurry.

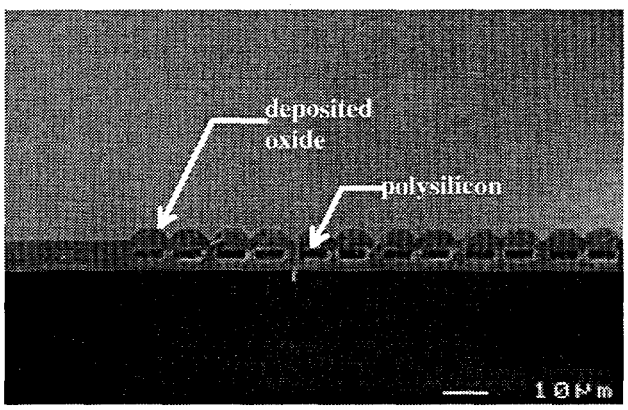

Figure 2. Cross section of a partially-fabricated micromachine showing the uneven topography before CMP planarization.

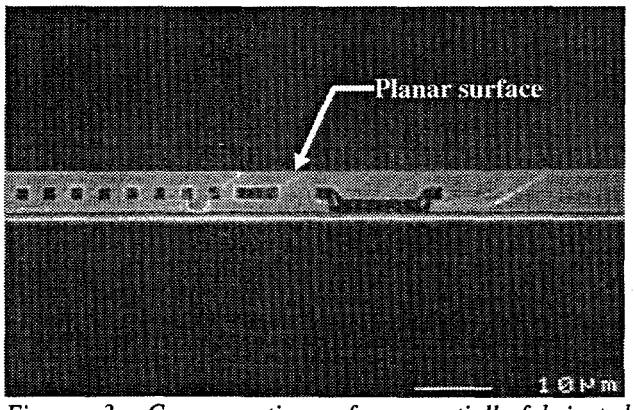

Figure 3. Cross section of a partially-fabricated micromachine after CMP planarization. Note the planar oxide surface.

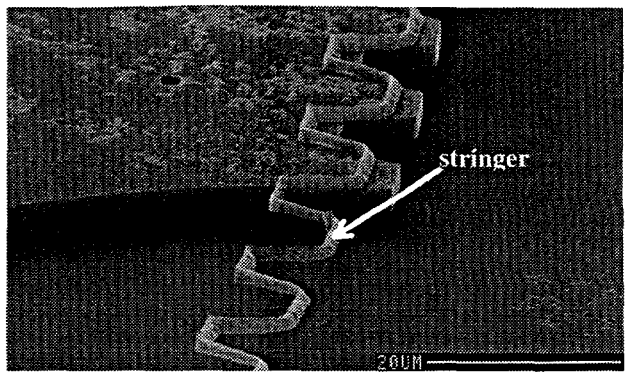

Figure 4. Polysilicon stringer next to a gear edge. The stringer was formed during a later polysilicon deposition and patterning.

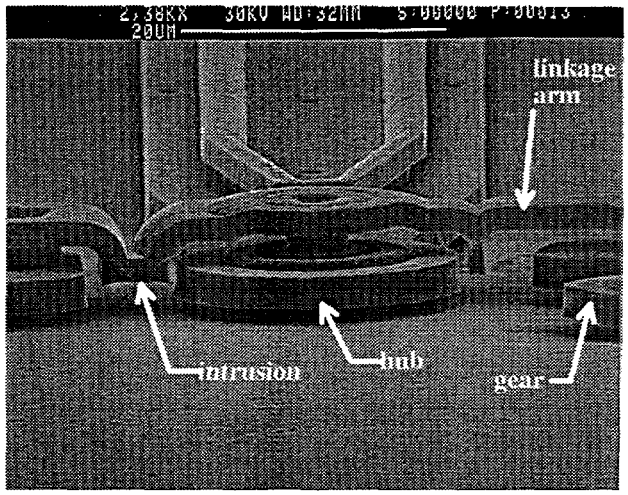

Figure 5. Hub and linkage arm of a microengine produced in a conventional, non-planar micromachining process.

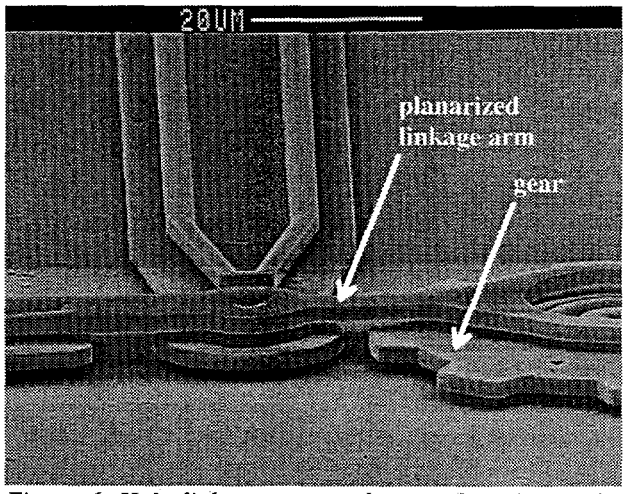

Figure 6. Hub, linkage arm, and gear of a microengine manufactured in a process utilizing CMP planarization.

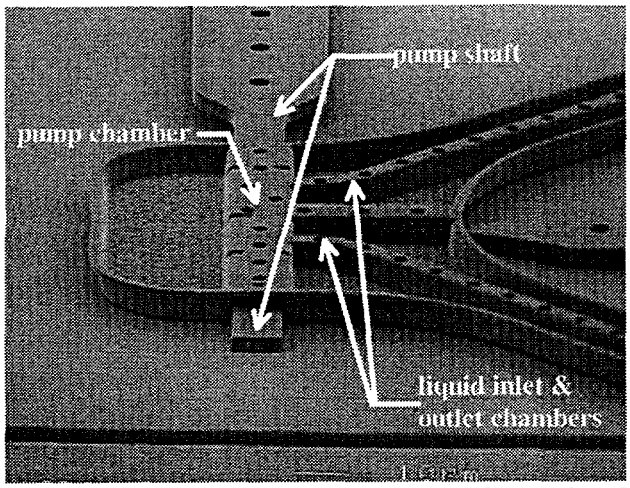

Figure 7. Micromechanical fluid pump fabricated with CMP. The planar top surface of the pump chamber indicates there is no protrusion of the top polysilicon into the enclosed pump mechanism.

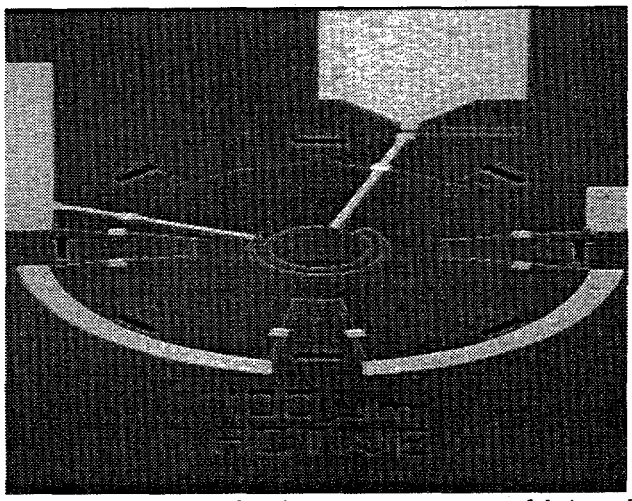

Figure 8. Top view of a planar pressure sensor fabricated in a process that includes CMP. The reference cavity is embedded below the substrate surface, eliminating step coverage problems.

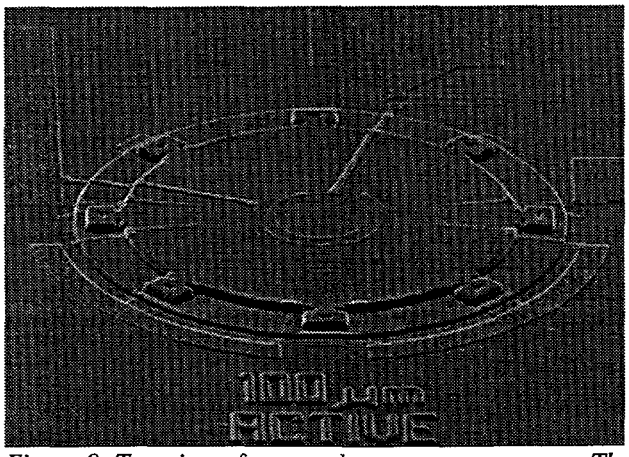

Figure 9. Top view of a non-planar pressure sensor. The circular diaphragm covers a 2μm-high reference vacuum cavity, and is the source of step coverage problems.

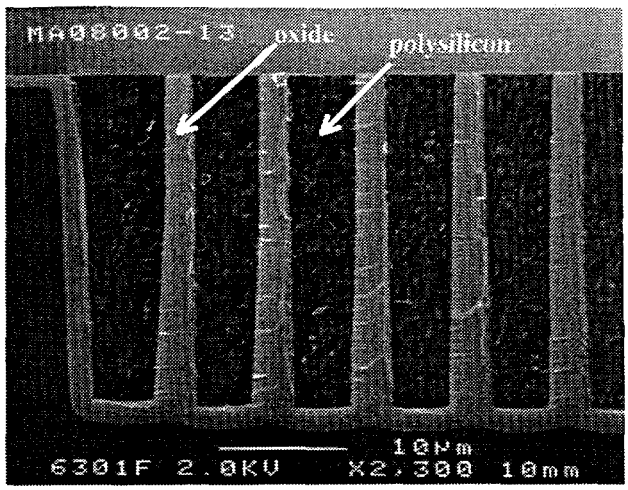

Figure 10. Cross-section of a high-aspect-ratio polysilicon accelerometer proof mass with CMP-planarized top surface.

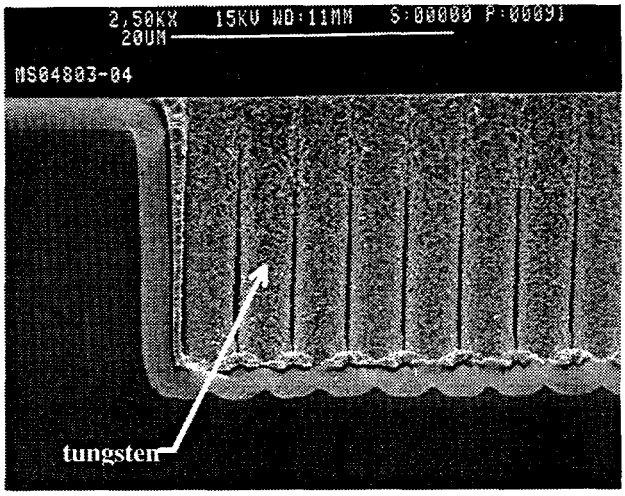

Figure 11. Cross-section of a high-aspect-ratio tungsten accelerometer proof mass with CMP-planarized top surface.

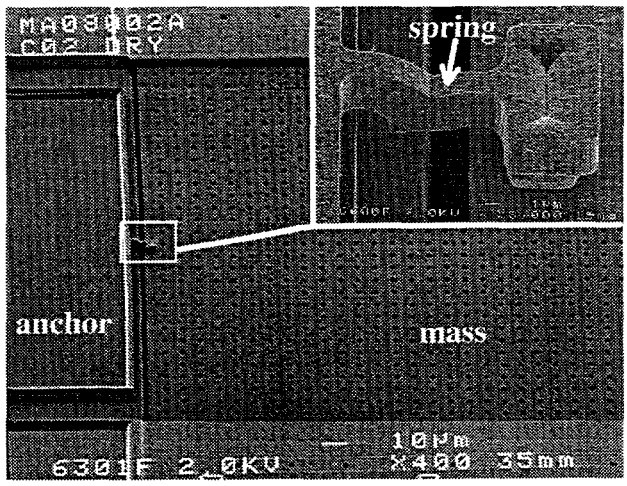

Figure 12. High-aspect-ratio polysilicon accelerometer mass integrated with a surface-micromachined spring

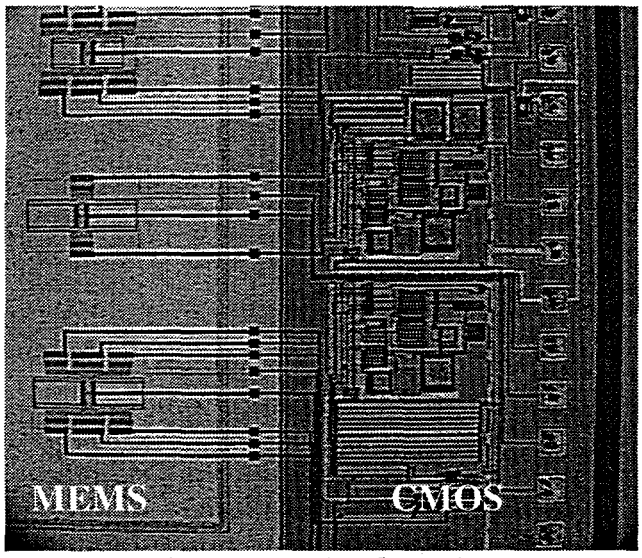

Figure 13. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics.

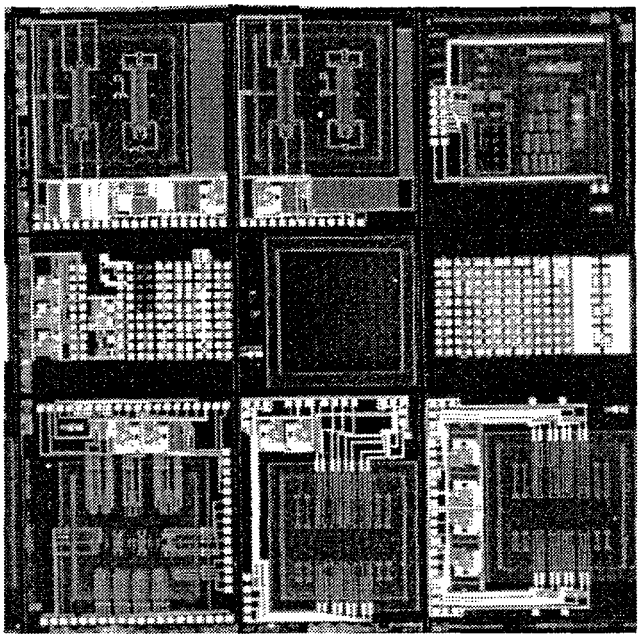

Figure 14. Photograph of the completed integrated MEMS/CMOS die illustrating the layout of the various sensors, resonators, test structures, and electronics.

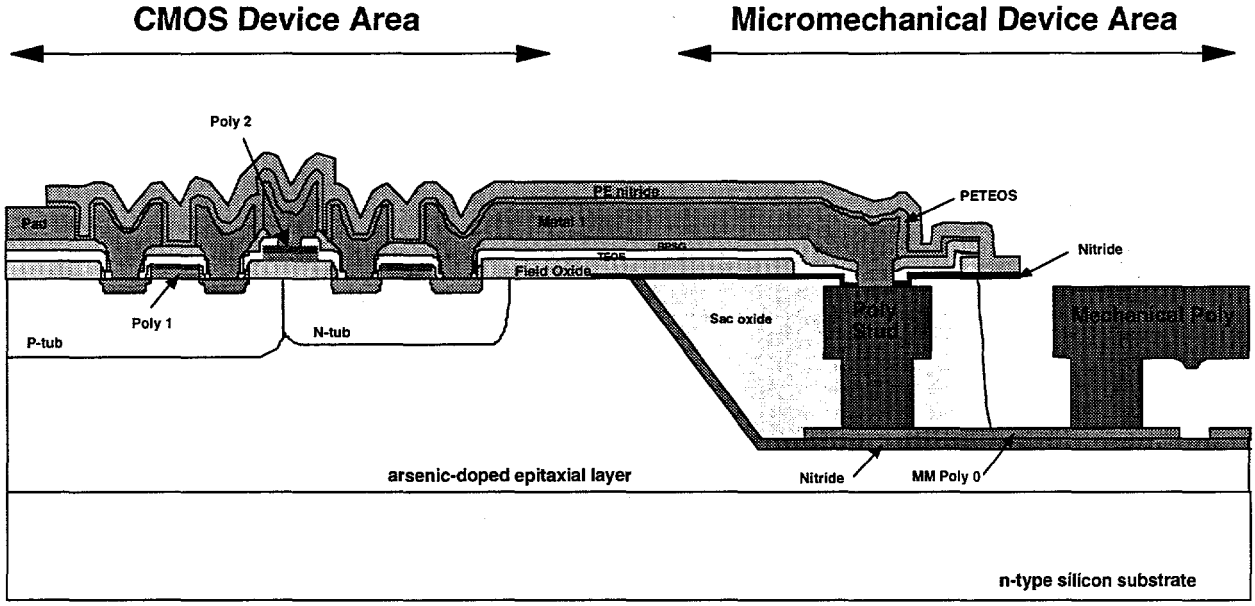

Figure 15. Cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

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