SAND2024-01010J

The Effects of Threshold Voltage and Number of Fins per Transistor on the TID Response of GF 12LP Technology

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***Abstract*— This abstract presents a comprehensive analysis of total ionizing dose (TID) response in GlobalFoundries' 12LP 12nm bulk FinFET technology using 10keV X-rays. Devices with higher threshold voltages (VTs) demonstrated lower increases in off-state leakage current ($I_{DS,OFF}$) post-irradiation, highlighting the mitigating role of high VT in TID response. Our data shows that transistors with fewer fins exhibit superior TID resistance, implying lower susceptibility to radiation effects. Our study also probed two bias conditions, "Gate-On" and "Pass-Gate," with the former displaying more severe TID degradation. Interestingly, p-type devices displayed negligible degradation, underscoring their inherent resilience to TID effects. Additionally, medium thick n-type devices echoed the fin-count-dependent TID response observed in other transistor types, further strengthening our findings. These results underscore the importance of strategic transistor selection and design for enhancing the TID resilience of future CMOS FinFET architectures, particularly critical in radiation-intense environments.**

***Index Terms*—FinFET, total ionizing dose, number of fins per transistors, threshold voltage, leakage current**

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I. Introduction

Fin-based field effect transistor (FinFET) complementary metal-oxide semiconductor (CMOS) technologies offer significant performance and density advantages over older planar CMOS technologies [1]. The GlobalFoundries (GF) 12LP 12nm bulk FinFET technology examined in this paper features four threshold voltages, namely Super-Low Threshold Voltage (SLVT), Low Threshold Voltage (LVT), Regular Threshold Voltage (RVT), and High Threshold Voltage (HVT), which allow for different power/performance tradeoffs. This makes the 12LP technology versatile and adaptable to various application requirements [2].

This paper presents total ionizing dose (TID) data and analyses on the GF 12LP technology. Data sets have been gathered previously across some 12LP transistor variants. In 2017, King et al. reported changes in TID-induced off-state leakage currents for both high-VT and low-VT transistors, suggesting potential differences in fin body doping between these two types of transistors [3]. Subsequent research by Arizona State University (ASU), showed similar trends in TID degradation, particularly a TID layout dependence increases in off-state leakage currents. ASU's work also found through simulation the effect of sub-fin doping level on the TID increase in leakage current [4], [5]. Furthermore, on-chip TID tests performed by Aerospace Co. revealed significant degradation in transistor off-state (sub-threshold) operation around 500 krad(SiO_2) [6]. However, despite these findings, the previous transistor-level studies on this technology only reported TID data on RVT and LVT transistors.

The number of fins per transistors on the TID response in bulk FinFETs has been addressed in earlier studies [7], where one study showed that n-type transistors with fewer fins experience the highest increase in off-state leakage currents [8], while another study presented no TID degradation dependence on the number of fins per transistors in n-type transistors, even at ultrahigh doses [9]. These studies were conducted on different technology nodes which highlight the importance of TID susceptibility to manufacturing processing techniques and transistor geometries [10]. Detailed analysis has not yet been presented on the effects of fin number on the TID response of GF 12LP technology.

In this study, we present a comprehensive analysis of the TID response of 12LP transistors of various types. Our research investigates the TID sensitivity of transistors with respect to two key parameters: 1) the process threshold voltage (VT) options available, and 2) the number of fins per transistor (n_{Fins}). The insights gained from this in-depth examination of the transistor-level TID behaviors will serve as valuable guidance for future design efforts aimed at enhancing the hardness of CMOS FinFET technologies.

II. Experimental Details

In this work, we tested wafers that contain a wide variety of transistor geometries for every threshold voltage in the technology. We irradiated these transistors at the wafer-level across many sites with an ARACOR 10 keV X-ray source, using a probe station with a custom 1×25 pin probe card. A small collimator was used to focus the X-ray beam and prevent dose exposure on adjacent structures. The collimator slit opening was large enough to allow uniform exposure to all transistors being irradiated. Only one test structure per die was tested, ensuring zero radiation dose on subsequent transistors tested. Two in-situ irradiation bias conditions were used during irradiations: 1) the gate terminal and substrate were grounded with constant voltage equal to the nominal supply voltage applied to the drain and source terminals (V_D = V_S = 0.8 V), called "Pass-Gate" bias herein, and 2) with constant gate voltage equal to the nominal supply voltage (V_G = 0.8 V) while the drain, source, and substrate are grounded, called "Gate-On" bias herein,. Measurements were made before and after total dose steps of 100, 200, 500, 1000, and 2000 krad(SiO_2). A Keysight B1500A semiconductor analyzer and B2200A switch matrix unit were used to apply the irradiation bias and measure the transistors' current-voltage (I-V) characteristics both pre- and post-irradiation.

We first report the experimental results on individual n-type transistors from the GF 12LP technology, which we will henceforth refer to as 'Single-Transistor Structures', covering all four threshold voltage variants available in the core. Furthermore, we report the TID behavior dependence on the number of fins per transistor. Specifically, we tested Single-Transistor Structures with n_{Fins}= 1, 2, 3, 4, 12, 20, and 40. All the devices tested had the minimum gate length allowed by design rules. Minimum gate lengths, commonly used for digital designs, typically result in a poorer TID response, especially in off-state leakage currents, compared to longer gate lengths in bulk FinFETs, as previously reported by Chatterjee *et al*. [8], [11]. It is worth noting that the HVT transistors have a slightly different minimum gate length than the SLVT, LVT, and RVT transistors.

We also performed tests on devices arranged in different array configurations, with transistors connected in parallel, and each transistor containing a fixed number of fins. Going forward, these will be designated as 'Parallel Array Structures.' The total number of fins per array (n_{Fins_Total}) was determined by multiplying the number of fins per transistor (n_{Fins}) with the number of identical transistors connected in parallel ($n_{FinFETs}$). Notably, all Parallel Array Structures included a total of 40 fins per device.

P-type FinFET Parallel Array Structures were tested for all VT variants in array configurations with 4 fins per transistor, along with RVT Parallel Array Structures possessing 1 fin and 40 fins per transistor. The TID responses of p-type FinFETs are not shown here as they exhibited no degradation even when exposed up to 2000 krad(SiO_2). Similar results were presented by Neuendank et al., where no TID effects (up to 1000 krad(SiO_2)), were observed in PMOS devices [5].

Ten samples of each VT variant with varying numbers of fins for Single-Transistor Structures were tested across ten die

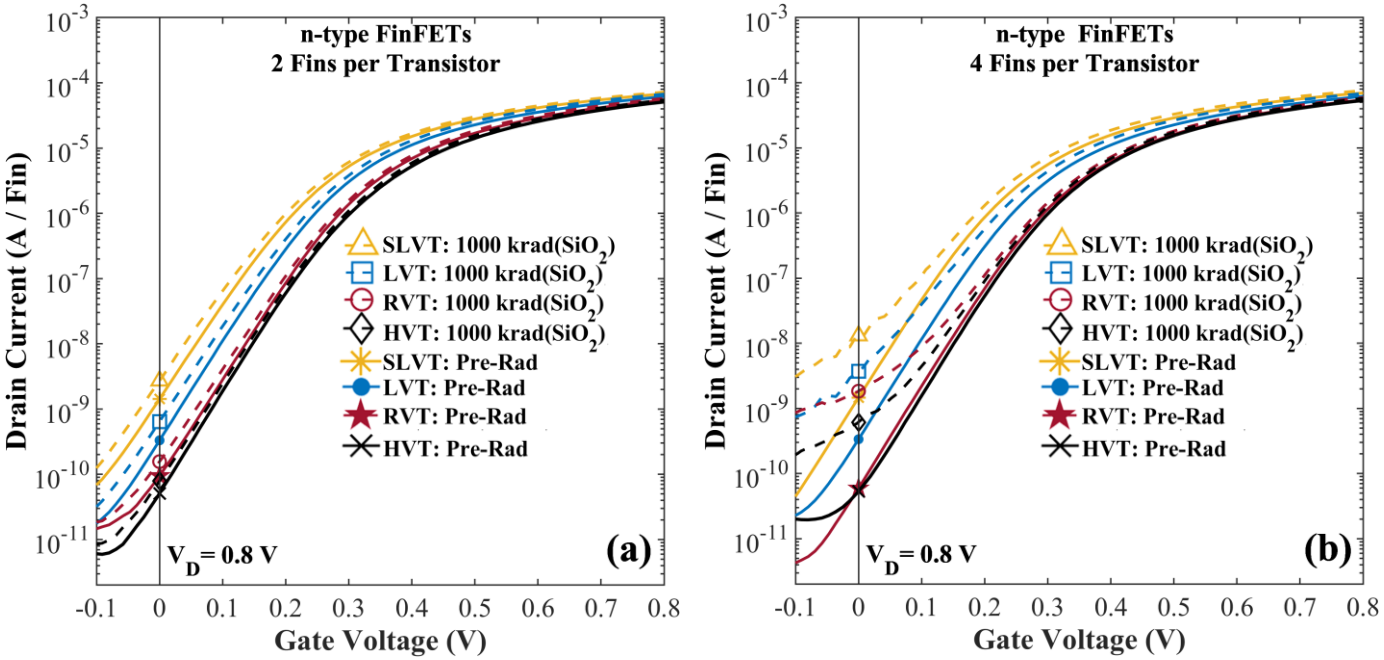

Fig. 1 I_{DS}-V_{GS} (V_{DS} = 0.8 V) characteristics for pre-rad and post- 1000 krad(SiO_2) of n-type Single- Transistor Structures with 2 (a) and 4 (b) fins per transistor with SLVT, LVT, RVT, and HVT threshold voltages. Currents are divided by the number of parallel fins to show per-fin currents.

locations on one wafer. Additionally, Parallel Array Structures were examined across ten die locations on another wafer.

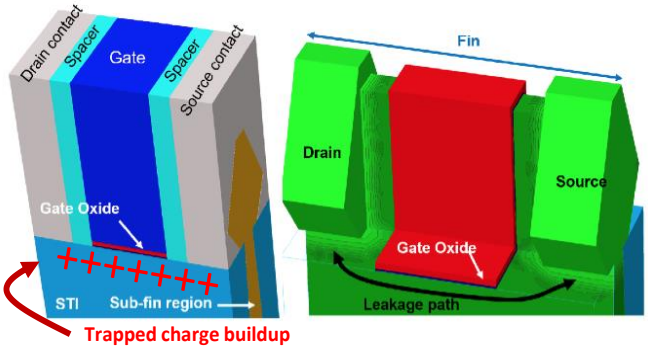

Fig. 2 Representative illustration of n-channel FinFET showing location in STI of net positive charge buildup and radiation-induced leakage path [2].

In our analysis, we observed that the "Gate-On" bias condition resulted in the worst TID degradation, consistent with previous works in this technology [3], [4]. Hence, the primary focus of our study will be on analyzing the TID results under this bias condition in both Single-Transistor Structures and Parallel Array Structures. The results for the less damaging "Pass-Gate" bias condition will be briefly presented for comparison. It is important to note that the error bars in our data represent the minimum and maximum values obtained from the ten samples tested for each transistor structure type, showing the full range of the data in its entirety.

III. Experimental Results

A. Threshold Voltage Variant TID Response

Fig. 1 plots the representative I_{DS}-V_{GS} electrical characteristics of n-type Single- Transistor Structures with 2 (Fig. 1(a)) and 4 (Fig. 1(b)) fins per transistor (n_{Fins} = 2, 4), which are commonly used in digital designs. The drain currents are divided by the number of parallel fins in the same transistor to show the per-fin currents, allowing for direct comparison of data across all figures in this paper. The solid lines present the characteristics before irradiation in the Gate-On condition, while the dotted lines present the characteristics after 1000 krad(SiO_2) irradiations.

Fig. 1 reveals the dependence of TID behavior on the VT type. The results show that the RVT (Regular Voltage Threshold) and HVT (High Voltage Threshold) transistors exhibit lower leakage currents, i.e., $I_{DS,OFF}$, both before and after irradiation when compared to the LVT (Low Voltage Threshold) and SLVT (Super Low Voltage Threshold) transistor variants. $I_{DS,OFF}$ is the drain current when the gate voltage (V_G) and source voltage (V_S) are both set to zero, while the drain voltage (V_D) is fixed to the nominal supply voltage (0.8 V). Previous studies have identified increased $I_{DS,OFF}$ after exposure as parasitic leakage current through a radiation-induced inversion layer in the sub-fin region, which runs in parallel to the as-designed n-type FinFET [3], [4]. This inversion in the sub-fin region has been attributed to net positive oxide charge buildup (N_{OT}) in the shallow trench isolation (STI) oxide structure adjacent to the silicon sub-fin [12], as illustrated in Fig. 2.

Fig. 1 shows that after 1000 krad(SiO_2), $I_{DS,OFF}$ has increased by ~2X (2 Fin HVT) to more than ~16X (all 4 Fin VT variants) compared to the pre-radiation current. Any increase in current with irradiation indicates that the parasitic leakage path through the inverted sub-fin becomes a measurable if not the dominant pathway for current from drain to source in the off-state. This parasitic current can have a significantly deleterious impact on the static power dissipation of very large-scale integration (VLSI) circuits manufactured in the technology.

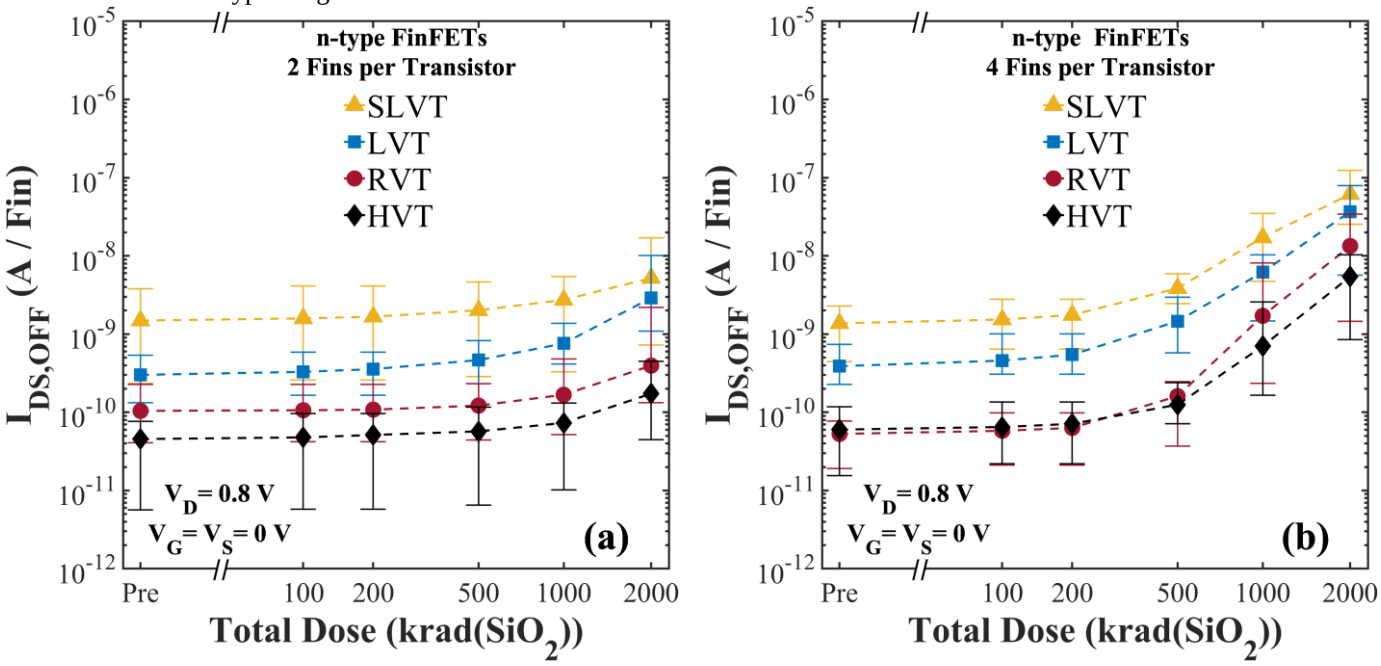

Fig. 3 Average off-state drain-source leakage ($I_{DS,OFF}$) current at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) of n-type Single- Transistor Structures with a) 2 and b) 4 fins per transistor with SLVT, LVT, RVT, and HVT threshold voltages. Error bars represent the minimum and maximum values across the ten samples tested.

Fig. 3 presents the average, minimum, and maximum values of $I_{DS,OFF}$ at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) for the ten die samples, each with the four VTs irradiated in the "Gate-On" bias condition of n-type Single-Transistor Structures with 2 (Fig. 3(a)) and 4 (Fig. 3(b)) fins per transistor. Notably, there is a substantial variability in $I_{DS,OFF}$ for each dose level, evidenced by the differences between the minimum and maximum values observed across the tested transistors.

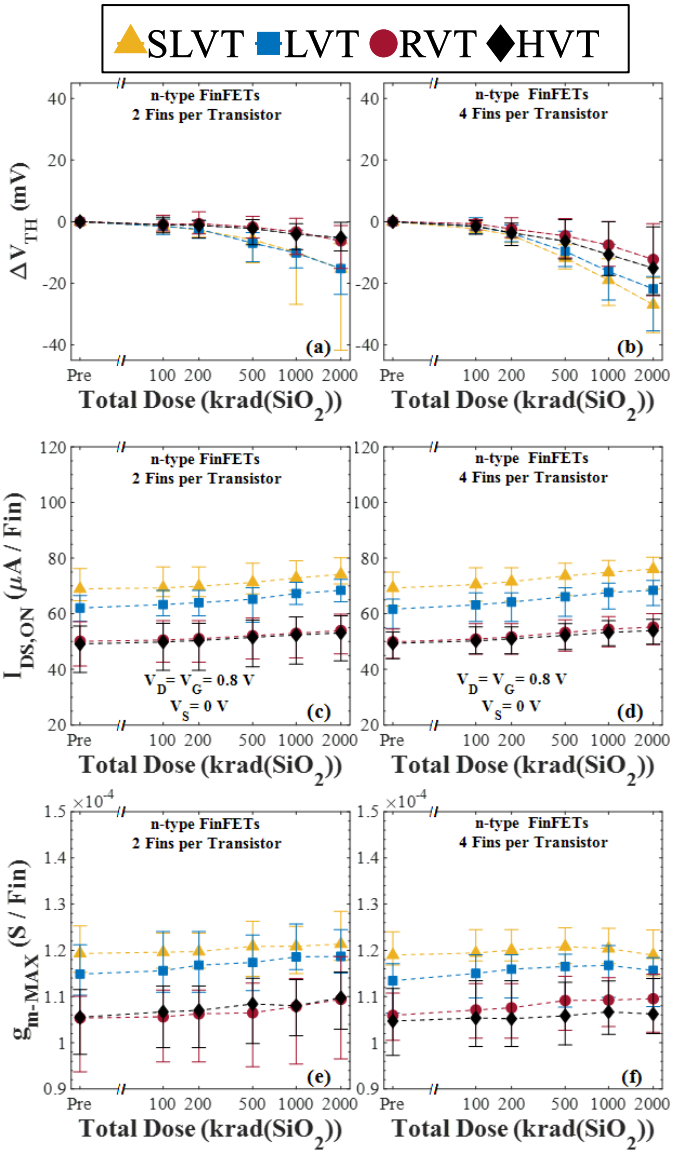

Fig. 4 Average changes in threshold voltage (ΔVth) (a)(b), absolute drive currents per fin (c)(d), and max transconductance (e)(f) at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) of n-type Single- Transistor Structures with 2 and 4 fins per transistor with SLVT, LVT, RVT, and HVT threshold voltages. Error bars represent the minimum and maximum values across the ten samples tested.

Despite this considerable variability, the data suggest that the relative order of pre-radiation leakage currents across these four VTs is maintained as the parasitic leakage currents increases due to TID. In addition, the changes in threshold voltage (ΔVth ~20-50mV), drive current ($\Delta I_{DS,ON}$ ~5-14%), and maximum transconductance ($\Delta gm,max$ ~ 2-6%) across all VTs in the 2 and 4 fin variants, are shown in Fig 4(a)-(f). This observation holds true across all fin variants (not shown) and presents similar TID trends as described in the work of King et al [3].Therefore, the rest of this paper will concentrate on presenting and analyzing the off-state leakage currents with Total Ionizing Dose (TID).

From the trends observed in Fig. 1 and 3, it is evident that the VT effect on the TID response is consistent for both 2-fin and 4-fin per transistor devices. Nevertheless, the number of fins per transistor also significantly influences the TID performance of the device, as shown by the higher magnitude change in $I_{DS,OFF}$ of the 4-fin transistors. A more in-depth exploration of this fin per transistor impact will be covered in our subsequent discussion of experimental data.

Threshold voltages in FinFETs, and in conventional planar CMOS technologies, can be controlled by several factors including the gate work function or body doping. Lower threshold voltage devices (e.g., SLVT and LVT) may undergo processing steps that result in smaller gate work functions or lower fin and potentially sub-fin doping densities compared to higher VT transistors (e.g., RVT and HVT). In processes where VT is modified by doping, a lower density of dopants in the sub-fin can increase the likelihood of sub-fin inversion after TID exposure and lead to higher off-state leakage current ($I_{DS,OFF}$) [3], [4], [12], [13], [14], [15]. This will be discussed in the following section.

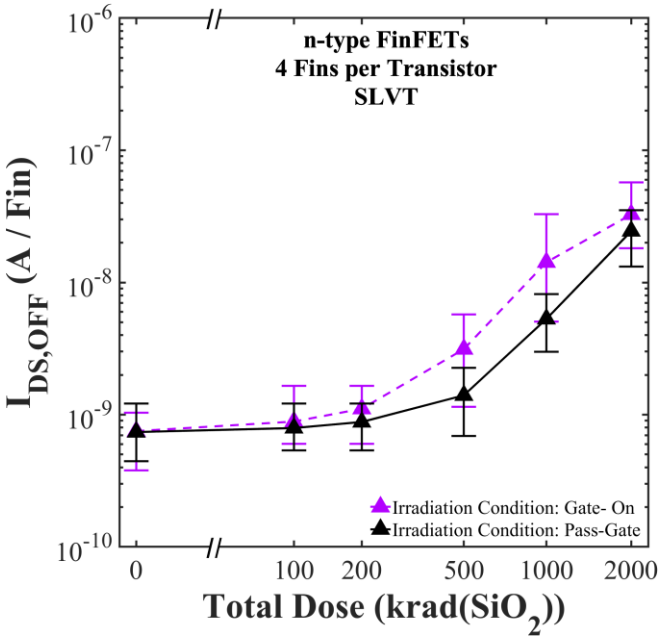

Fig. 5 Average off-state drain-source leakage ($I_{DS, OFF}$) current at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) of n-type Parallel Array Structure with 4 fins per transistor (n_{Fins}=4) with SLVT threshold voltage irradiated in the Gate On (purple) and Pass- Gate (black) condition. Error bars represent the minimum and maximum values across the ten samples tested.

The off-state leakage current in FinFETs during irradiation is known to be influenced by the bias condition [3], [16]. Our work showed that the applied bias during irradiation had a minor influence on the increase in $I_{DS,OFF}$, as indicated by the overlap of error bars showed in Figure 5. However, on average, the "Gate-On" bias condition (purple dotted line) exhibits a

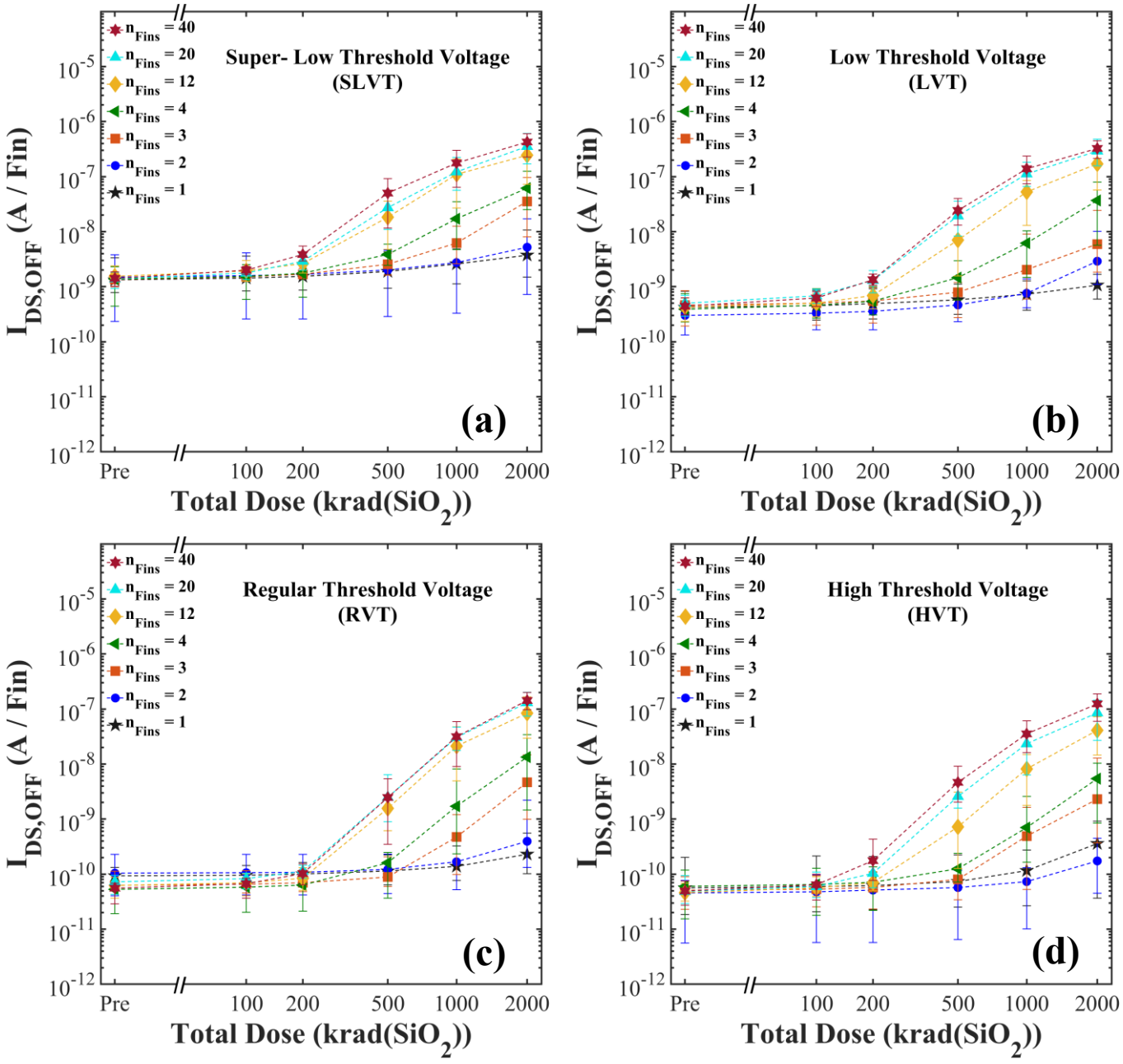

Fig. 6 Average off-state drain-source leakage ($I_{DS,\ OFF}$) current at 0, 100, 200, 500, 1000, and 2000 krad(SiO_2) of n-type transistors with 1, 2, 3, 4, 12, 20, and 40 fins per transistor for a) SLVT, b) LVT, c) RVT and d) HVT. Error bars represent the minimum and maximum values across the ten samples tested.

higher $I_{DS,OFF}$ current compared to the "Pass-Gate" condition (black solid line) in the SLVT n-type Parallel Array Structure with four fins per transistor. The precise cause is yet to be determined; however, the observed variations might be attributed to disparities in electric field distributions, potentially arising from transistor geometry or inherent aspects of the manufacturing process.

B. Fins per Transistor TID Response

Fig. 6 plots average, minimum, and maximum values in $I_{DS,OFF}$ across ten samples at different total dose levels (0,100, 200, 500, 1000, and 2000 krad(SiO_2)). These measurements were performed on n-type Single- Transistor Structures irradiated in the "Gate-On" bias condition, with varying numbers of fins per transistor (n_{Fins}) for a) SLVT, b) LVT, c) RVT, and d) HVT. Note that the standard cell libraries used to synthesize digital circuits typically use very few fins in each transistor to maximize density. However, Fig. 6 shows up to 40 fins per transistor to explore the mechanism of how fin count affects the TID behavior, and because large-fin-count transistors are sometimes used in analog designs. The results clearly indicate that the off-state leakage current ($I_{DS,OFF}$) increases with higher total dose and as the number of fins per transistor (n_{Fins}) increases. These results lead us to believe the oxide trapping in the sub-fin regions is different in the oxides in high fin count transistors than in those of the small fin count transistors. Notably, these trends hold true across all threshold voltage (VT) variants and transistor array structures tested. The FinFETs with 1 and 2 fins per transistor (n_{Fins}=1, 2) show the

least susceptibility to dose effects, followed by those with 3 and 4 fins per transistor (n_{Fins}=3, 4). Conversely, the FinFETs with 12, 20, and 40 fins per transistor (n_{Fins}=12, 20, 40) exhibit the largest increases in leakage current. Additionally, medium thick gate oxide Parallel Structures with 4, 10, and 40 fins per transistor displayed the same total number of fins, where the 40 fins per transistor structure displayed the largest increase in off-state leakage.

IV. Discussion

A. Threshold Voltage Variant TID Mechanisms

The current characteristics shown in Figs. 1 and 3 point to a strong dependence on the threshold voltage type for the TID response at and above 500 krad(SiO_2). Recall that it is assumed that the increase in $I_{DS,OFF}$ is current flowing in parallel with the as-designed sub-threshold current. As such, a change in $I_{DS,OFF}$ above its pre-irradiated level is primarily a measure of parasitic leakage current through the inverted sub-fin. Thus, the data in Fig. 4 would indicate that the SLVT and LVT variants not only have a higher sub-threshold current prior to irradiation (owing to the lower threshold voltage) but also a larger sub-fin leakage current after exposure.

As discussed in the previous section, threshold voltages in MOSFETs can be altered by various processing methods, including by changing the work function on the gate or by adjusting the doping profile of the fin. If the VT is changed in 12LP by adjusting doping, this could serve as a potential explanation for why TID depends on VT. In a paper by Wallace *et. al*., simulations were conducted to examine the radiation dependance on the doping profile of the sub-fin, just below the fin (or body) [4]. Their results showed that there was large TID response sensitivity in devices with more lightly doped sub-fins. If the GF 12LP technology controls the threshold voltage via doping, it may be the case that an unintentional lower body doping in the fin for the SLVT and LVT devices may decrease the doping of the upper part of the sub-fin region, without affecting the device performance. This would make the RVT and HVT FinFETs less susceptible than SLVT and LVT variants to N_{OT} buildup in the STI, i.e., the sub-fin would be more easily inverted in the SLVT and LVT devices. The experimental data seem to be consistent with this hypothesis.

Furthermore, the data indicates that as you increase the transistor's VT, the TID sensitivity to the number of fins, also increases. This could further point to the unintentional lower body doping of the fin structure on leakage current due to its impact on the electric field distribution or carrier concentration in the channel.

B. Fins per Transistor TID Mechanisms

The data presented in Fig. 6 shows the TID response characteristics are also strongly influenced by the number of fins per transistor. Evident in these plots is an increase in TID susceptibility as the number of fins per transistor increases. Fig. 7(a) shows the off-state leakage current at 1000 krad(SiO_2) for the SLVT device as a function of fins per transistor (purple triangle symbols). Also on the figure are the results of a mathematical model (solid black line) that follows the experimentally observed trends. Fig. 7(b) shows the data and model fits after a 2000 krad(SiO_2) dose.

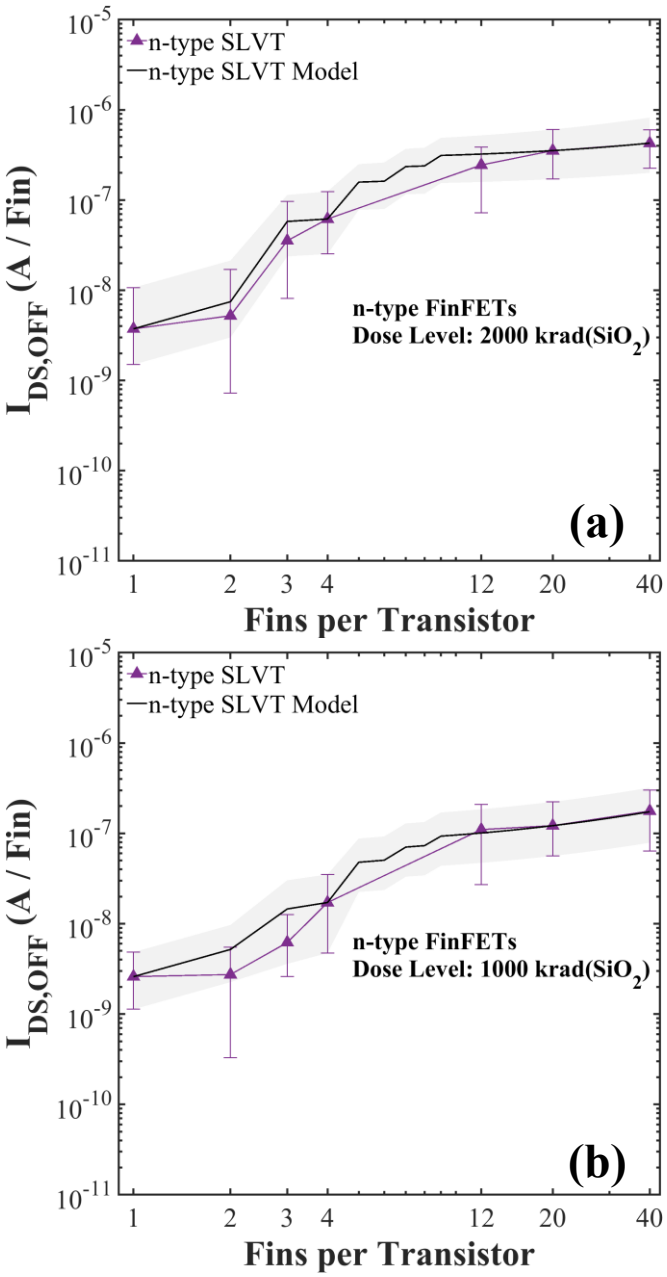

Fig. 7 Average off-state drain-source leakage ($I_{DS,OFF}$) vs. fin number. Symbols show data and solid line is the model fits after a) 1000 krad(SiO_2) and b) after 2000 krad(SiO_2). Shaded regions represent the min and max values calculated from equation 1.

The model provides a possible explanation for how fin count affects the TID response. It is based on assumptions regarding stress effects including densification in the STI, which have been shown to be related to the number of parallel fins in a FinFET device [17]. Variability in STI stress across a multi-fin transistor may lead to different trapping precursor densities or local electrical fields, which may cause variations in trapped charge build-up [18], [19]. Additionally, it has been shown that stress can cause splitting of the conduction bands, which can

potentially lower the effective field making it easier to create an inversion layer [20]. To explore this effect, a mathematical model was created as a possible proof of concept to account for the potential strain-induced variability.

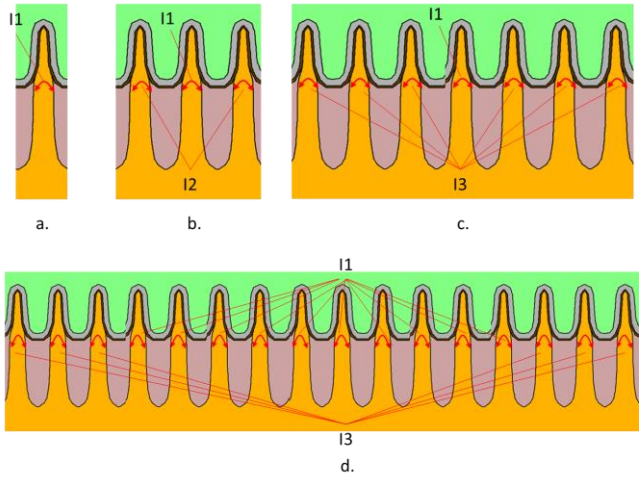

Fig. 8. Fin cross-sections of FinFET transistors with various parallel fins illustrating locations specifics leakage currents.

For this model, 1 and 2 fin transistor STIs are considered to have only slight degradation causing only a small parasitic current, I_1 (illustrated for one-fin cross-section in Fig. 7(a). For transistors with 3 or 4 parallel fins, the two outer fins are assumed to exhibit more parasitic current, I_2, than the one or two interior fins which continue for exhibit a low parasitic current, I_1, (illustrated for three-fin cross-section in Fig. 8(b)).

Here we are assuming that outer fins experience more stress, which is consistent with studies that have even shown the stresses causing bending of the outermost fins [21]. For transistors with 5-8 fins, the outer fins, (up to three on each side) show even more parasitic current, I_3, while the one (for odd Fin count) or two (for even count) inner-most fins still exhibit the low current, I_1 (illustrated for seven-fin cross-section in Fig. 8(c)). For transistors with 9 or more fins, the large currents, I_3, are assumed to stay fixed to the six outer most fins while any inner fins beyond the six show only the small leakage current, I_1 (illustrated for sixteen-fin cross-section in Fig. 8(d). The current values used for the model were extracted from the data and used to create a piecewise representation of each fin configuration. I1 uses the current from a 1 fin device, while I2 and I3 are extracted from outermost fin current on the 4 and 20 fin devices respectively. A fin number dependent set of equations for the total leakage current model is given in Eq. (1).

$$I_{total} = \begin{cases} nI_1 for\ n \le 2 \\ 2I_2 + (n-2)I_1\ for\ 2 < n \le 4 \\ I_1 + (n-1)I_3\ for\ n = 5,\ 7 \\ 2I_1 + (n-2)I_3\ for\ n = 6,\ 8 \\ 8I_3 + (n-8)I_1\ for\ n \ge 9 \end{cases} \quad (1)$$

Where $I_1 < I_2 < I_3$

Considering our data, an insightful strategy can be proposed for applications that necessitate large fin counts, such as specific analog and I/O transistors. Instead of using a single transistor with a high number of fins, hardening against TID can be significantly enhanced by employing numerous transistors in parallel, each with a reduced fin count.

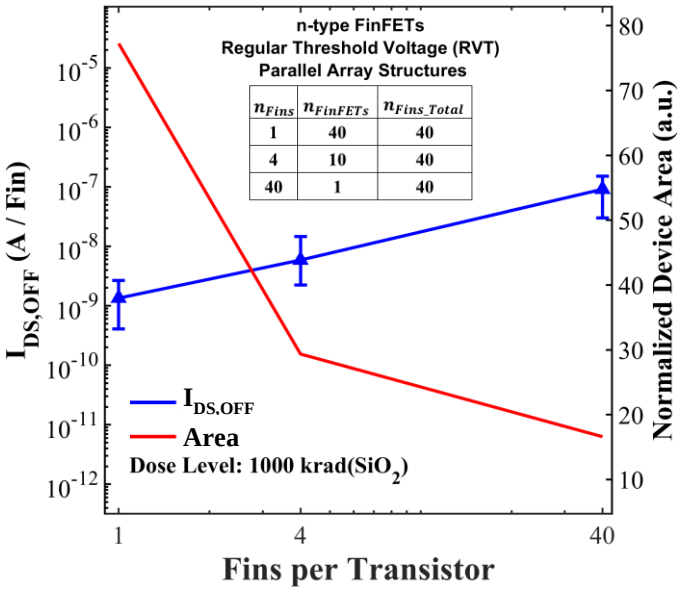

Fig. 9 Average off-state drain-source leakage ($I_{DS,OFF}$) (left axis- blue line) at 1000 krad(SiO_2) and the normalized Parallel Array Structure area (right axis- red line) for n-type RVT Parallel Array Structures with 1, 4, and 40 fins per transistor (n_{Fins} = 1,4,& 40). Error bars represent the min and max values across ten samples.

Fig. 9 presents $I_{DS,OFF}$ (blue line) at 1000 krad(SiO_2) for n-type RVT Parallel Array Structures with 1, 4, and 40 fins per transistor (n_{Fins} = 1,4,& 40) connected in parallel ($n_{FinFETs}$ = 40, 10, 1), all with a total of 40 fins (n_{Fins_Total}). As seen from the figure, this approach substantially improves the TID response where those arrays with lower fins per transistors experience less increase in $I_{DS,OFF}$. Although it incurs an increase in area usage (red line), the trade-off is a commendable enhancement in radiation resistance in the off-state current of the transistors. Therefore, strategic design choices can effectively mitigate radiation-induced degradation.

V. Conclusion

Transistor-level TID test results were presented on GF 12LP 12nm bulk FinFET technology. Our results indicated that there was higher TID degradation when the "Gate-On" irradiation bias condition was applied than when the “Pass-Gate” bias was applied. Additionally, p-type devices displayed higher tolerance to TID degradation.

The results clearly show that the TID response is best when using fewer fins per transistor. Medium thickness gate oxide n-type devices also showed a TID response dependent on the number of fins per transistor. Furthermore, our investigation has indicated that transistors with lower VTs experience a larger increase in absolute off-state leakage currents with TID than their higher VTs counterparts. The higher VT transistors experienced larger TID-induced relative increases in off-state

leakage current (i.e., post- rad current divided by pre- rad current) than the lower VT transistors. This distinction becomes particularly pertinent when optimizing for low- power or high-performance applications. Finally, hypotheses were also presented that can explain these two observed trends. These trends may differ for FinFET technologies other than GF 12LP.

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