Final Technical Report (FTR)

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d. Recipient Organization	University of Washington
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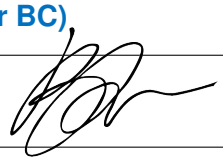

1/18/2024

Signature of Certifying Official *Date*

By signing this report, I certify to the best of my knowledge and belief that the report is true, complete, and accurate. I am aware that any false, fictitious, or fraudulent information, misrepresentations, half-truths, or the omission of any material fact, may subject me to criminal, civil or administrative penalties for fraud, false statements, false claims or otherwise. (U.S. Code Title 18, Section 1001, Section 287 and Title 31, Sections 3729-3730). I further understand and agree that the information contained in this report are material to Federal agency's funding decisions and I have any ongoing responsibility to promptly update the report within the time frames stated in the terms and conditions of the above referenced Award, to ensure that my responses remain accurate and complete.

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3. Executive Summary: The proposed technology combines advances in wide-bandgap power electronics with breakthroughs in distributed and decentralized control to produce ultra-low-cost medium-voltage transformerless PV inverters that are composed of stackable lightweight blocks. Taken together, the proposed circuit designs and accompanying control strategies will yield integrated control+circuit (C2) blocks, each comprising a converter and local controller, that can be assembled in a modular fashion to obtain distributed conversion interfaces for next-generation commercial and utility-scale PV systems. We will utilize SiC devices to obtain C2 blocks that can individually operate at a voltage and power in excess of 1 kV and 100 kW, respectively, such that ensembles of series-connected blocks perform direct dc to three-phase ac conversion at medium voltages (e.g., 12 kV–35 kV) and at multi-MW power levels.

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5. Background: Today, utility-scale PV inverters are predominantly built with conventional single-stage converter topologies that interface with an externally installed low-voltage to medium-voltage line-frequency transformer. Given the non-trivial costs and maintenance associated with centralized transformers, several leading manufacturers are exploring the development of transformerless inverters that produce medium voltage ac (MVAC) directly. Towards this end, multilevel inverters have emerged as a viable means of transferring energy at elevated voltages as the large number of series-connected devices allows for increased operational voltages. However, existing multilevel inverter topologies require bulky passive components that add costs and centralized controllers that impede scalability. Presently, multilevel inverters have a negligible role in the PV market.

As inverter costs continue their downward trajectory, one of the main bottlenecks to further cost reductions is BOS costs. In fact, recent PV market analysis has demonstrated that BOS costs are playing an increasingly dominant role in overall system costs and now exceed inverter costs. For instance, centralized inverters have significant dc-side wiring costs and string-level three-phase inverters have substantial ac-side wiring requirements due to the high number of parallel units. Accordingly, a converter that has streamlined dc and ac wiring requirements would considerably reduce overall system cost.

One of the most well-established technologies for medium- and high-voltage power electronics ac systems is the MMC. Hence, we will consider it as an important frame of reference. There are

some distinct properties of the MMC that have hindered their use in transformerless PV inverters. For instance, one prerequisite of the MMC is that the dc input voltage must exceed the peak ac-side medium voltage for the system to be operational. If used in a PV application this implies that either medium voltage dc must be provided by the PV array directly or an additional boost converter stage is needed. Both approaches are undesirable since a medium voltage PV string would be infeasible for many reasons, such as costly dc-side protection and PV module voltage isolation, while an additional boost converter would add costs and reduce efficiency. In contrast, our proposed design straightforwardly accommodates standard PV string voltages used in industry today.

Another disadvantage of the MMC is its necessity for large and costly capacitor banks. This stems from its physical structure where each phase leg is composed of a distinct converter stack that must process single-phase power. Irrespective of whether each converter in the MMC stack is composed of half-bridges, full-bridges, diode clamped elements, or flying capacitors, the fundamental fact remains that each collection of converters in each phase-leg must process pulsating single-phase power. This necessitates significant capacitance within each modular converter in addition to centralized controllers that manage system capacitor voltages. Not only does the centralized MMC controller prevent system scalability, but it also acts as a single point of failure.

6. Project Objectives: At the core of the proposed system lies a novel dc to three-phase ac conversion block whose innovative controls and circuit design significantly reduces cost and weight while increasing efficiency. To obtain a modular architecture that maximizes resiliency and simplifies installation, we apply the latest advances in controls to obtain autonomously controlled C2 blocks that are stacked in series with minimal external wiring and can be bypassed during faults without interrupting system-wide power delivery. Using a cost-analysis-driven design that unambiguously links monetary costs with physical design variables, we will determine the optimal number of stacked C2 blocks, their parameters, and underlying components to achieve the lowest LCOE.

The proposed technology combines advances in wide-bandgap power electronics with breakthroughs in distributed and decentralized control to produce ultra-low-cost medium-voltage transformerless PV inverters that are composed of stackable lightweight blocks. Taken together, the proposed circuit designs and accompanying control strategies will yield integrated circuit+control (C2) blocks, each comprising a converter and local controller, that can be assembled in a modular fashion to obtain distributed conversion interfaces for next-generation commercial and utility-scale PV systems. We will utilize SiC devices to obtain C2 blocks that can individually operate at a voltage and power in excess of 1 kV and 100 kW, respectively, such that ensembles of series-connected blocks perform direct dc to three-phase ac conversion at medium voltages (e.g., 12 kV–35 kV) and at multi-MW power levels.

7. Project Results and Discussion: Provide a high-level, quantitative comparison of anticipated project outcomes against realized results with clearly stated quality metrics to assess the confidence of the results. A clear sense of progress against award milestones, both throughout and at award end, should be conveyed. State the project tasks and go/no-go milestones/deliverables and metrics and compare them to what was actually achieved. This section's structure should be based on the SOPO, making comparisons at the task level with the subtasks providing support for claimed progress. Milestone rows should be copied verbatim to appropriate points in the technical discussion. Enough detail and/or references to supporting documentation must be provided to make it clear that milestones were successfully accomplished. If milestones were not met, discuss any extenuating circumstances and difficulties encountered. The methodologies (e.g., modeling

approaches, experimental methods) utilized to obtain the results should also be included. Relevant figures and data tables should be included and discussed in enough detail to demonstrate the technical progress made on the award.

1 Summary of Project Milestones

All Task 1 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M1.1	Updated cost data for cost optimization model.	Set of data containing up to date costs for relevant system components.	The team has successfully obtained cost data for the key system components.	Existence of updated cost data	Y	Pages 35-37 of BP1 Q3 report.
M1.2	Cost and efficiency models	The efficiency and cost of a system containing C2 blocks is expressed as a function of converter-level parameters and ratings such as voltage rating, current rating, magnetics characteristics, and device properties.	The efficiency and cost models have been completed. Existing results include all semiconductor and magnetics losses.	Project team review and written summary of review discussion	Y	Pages 38-40 of BP1 Q3 report, Pages 15-20 of BP1 Q2 Report & pages 3-6 of BP1 Q1 Report
M1.3	A comprehensive LCOE-improvement model and corresponding design optimization problem.	A LCOE improvement model which incorporates inverter capital costs, BOS costs, and efficiency is formulated and translated into a design optimization problem.	The optimization problem has been formulated. This design optimization problem has been solved with a few types of solvers and the performance of the solvers has been compared.	Design problem presented to DOE and demonstrated with numerical examples.	Y	Pages 4-7 of BP1 Q4 Report, Pages 41-44 of BP1 Q3 Report, Pages 15-20 of BP1 Q2 Report.

All Task 2 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M2.1	A simulation of five or more cascaded C2 blocks with fully functional MPPT, dc-link, and power sharing controls.	A simulation showing that all dc-link voltages stay within 10% of the setpoint, the PV maximum power point is tracked within 10%, and power is shared on the ac side in proportion to the PV maximum power for each C2 block.	A detailed switch-cycle averaged simulation was assembled and the overall system performance was validated. All performance targets were satisfied.	Quantitative simulation results from a performance evaluation script within MATLAB/ Simulink.	Y	Page 7 of BP1 Q3 report.
M2.2	A simulation showing five or more interleaved C2 blocks with communication-free interleaving controllers.	A simulation showing that the generation of a low-distortion $2N + 1$ level ac waveform without communication.	An improved version of the controller was developed and tested in HIL. Simulations and experiments demonstrated feasibility of the proposed controller.	Quantitative simulation results from a performance evaluation script within MATLAB/Simulink.	Y	Page 9 of BP1 Q3 report, Pages 9-12 of BP1 Q2 report & Pages 9-11 of BP1 Q1 report.
M2.3	A hardware validation of decentralized dc-link controllers.	Measurements on five or more low-voltage C2 block which shows that the dc-link voltages stay within 10% of the setpoint.	The low-voltage hardware was built and debugged. Each of the 5 C2 blocks was tested and dc-link voltages were maintained within 10% of the setpoint.	Electrical measurements.	Y	Pages, 9-13 of BP1 Q4 Report, Page 12 of BP1 Q3 report, Pages 11-14 of BP1 Q2 report, Pages 12-16 of BP1 Q1 report.

All Task 3 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M3.1	A candidate magnetics design which accommodates rated power transfer.	Detailed simulations and analysis demonstrate that the QAB magnetics can deliver 15kW from the dc input to the three-phase ac outputs.	A magnetics design was finalized and detailed models show it can transfer rated power at high efficiency.	Quantitative simulation results and accompanying analysis/models.	Y	Pages 14-19 of BP1 Q3 report, Pages 3-6 of BP1 Q2 report.
M3.2	A high-level HV-PCB layout which ensures voltage isolation of at least 30 kV.	A diagram which prescribes the physical placement of the primary circuit and three secondary circuits associated with the QAB and an accompanying finite-element model which shows electric fields below the arcing threshold for HV-PCBs.	A first version of the high-level prototype design was created. This initial design specifies the hardware architecture, sensors, control boards, magnetics placement, communications, and interconnects. A finite element model of the HV-PCB planar magnetics board also demonstrates isolation of at least 30 kV.	A diagram and simulation results from an electromagnetic finite-element simulation package.	Y	Pages 21-22 of BP1 Q3 report, pages 6-7 or BP1 Q2 report.
M3.3	A candidate converter circuit design with at least 98.5% CEC efficiency.	Analysis and simulation of candidate 15kW power stage design demonstrates at least 98.5% CEC efficiency.	Simulations of candidate designs demonstrate that an efficiency of at least 98.5% efficiency is feasible. Detailed loss analysis supports this conclusion.	Quantitative simulation results from a performance evaluation script.	Y	Pages 16-18 of BP1 Q4 Report, Page 33 of BP1 Q3 report.

All Task 4 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M4.1	Cost data that is updated in BP2 and used for design optimization	Set of data containing up to date BP2 costs for relevant system components	Updated cost data has been imported into the optimization code.	Existence of updated cost data	Y	BP2 Q3 report pages 3-4
M4.2	A comprehensive optimization-driven design framework which incorporates market cost data	Existence of a design framework and accompanying output data produced by the design routine	A fully-functional optimization routine has been created.	Design optimization models are presented to DOE	Y	BP2 Q3 report pages 4-6
M4.3	Design optimization results for a utility-scale system and LCOE reduction estimates in comparison to centralized inverters (and three-phase string inverters) with line frequency transformers	A utililty-scale candidate design which shows LCOE reductions in comparison to centralized inverters (and three-phase string inverters) with line frequency transformers	Preliminary results including potential improvements in electric BOS and system rating as free variable indicate a roughly 5.5% LCOE improvement.	Numerical data produced by design/cost optimization and cost sensitivity analysis	Y	BP2 Q3 report pages 6-10. BP2 Q4 report pages 6-7

All Task 5 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M5.1	Experimental results from five or more cascaded low-voltage C2 blocks with the proposed dc-link, MPPT, and power sharing controls	Measurements on all low-voltage C2 blocks show that the PV maximum power point is tracked within 5%, the dc-link voltages stay within $\pm$10% of the setpoint, and ac-side power sharing is achieved	Convergence to MPPT was within 5% and dc link voltages were regulated within 10%.	Electrical measurements	Y	BP2 Q1 report pages 5-6, BP2 Q4 pages 8-12.
M5.2	A system of five or more C2 blocks with decentralized interleaving controls	Measurements showing that the system of five or more cascaded low-voltage C2 blocks reaches the interleaved state without communication	A system of 5 cascaded C2 blocks achieved decentralized interleaving in hardware.	Electrical measurements	Y	BP2 Q3 report pages 12-13, BP2 Q4 report page 15.

All Task 6 Milestones were completed. Note that it was agreed that M6.2 could be completed via simulation due to limitations on existing off-the-shelf magnetics components which impeded hardware efficiency.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M6.1	Fabricated planar magnetics components which meet leakage inductance specs for required power transfer	Measurements show that the target leakage inductances are obtained and the required power transfer is feasible	Measurements have been carried out on planar transformer and inductor prototypes for 7.5 kW of power transfer.	Electrical measurements	Y	BP2 Q3 report pages 15-17.
M6.2	A 7.5 kW C2 block with at least 98.5% CEC efficiency	Electrical measurements show that 98.5% CEC efficiency can be met or exceeded. (Agreed to meet this in simulation.)	Models and simulations (which have been validated against measurements) show that a $>$98.5% CEC effiency is feasible.	Electrical measurements	Y	BP2 Q3 report pages 18-24, BP3 Q1 report pages 3-6, BP3 Q2 report pages 5-7, BP3 Q5 report pages 3-5.
M6.3	A 7.5 kW C2 block which can withstand 13kV of voltage isolation	The absence of arcing or faults when 13kV is subjected across the magnetic isolation barrier within a C2 block	$>$18 kV of isolation was measured.	Electrical measurements	Y	BP2 Q1 report page 15.
M6.4	A simulation with 10 or more cascaded 7.5 kW C2 blocks	Simulations which match planned 13.2 kV experiments and show that all dc-link voltages stay within 10% of the setpoint and ac-side power sharing is achieved.	Simulations show ac-side power sharing and dc link voltages regulated within 1% of reference value.	Electrical measurements	Y	BP2 Q2 report page 16
M6.5	An experiment with 3 or more cascaded 7.5 kW C2 blocks	Measurements showing that the cascaded system can maintain dc-link voltages within 10% of the setpoint and ac-side power sharing is achieved while grid-connected.	Experiment successfully completed on three module setup.	Electrical measurements	Y	BP2 Q3 report pages 25, BP2 Q4 report pages 17-18, BP3 Q1 report pages 3-6, BP3 Q2 report pages 4, BP3 Q3 pages 4-7, Final Report page 32.

All Task 7 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M7.1	A written summary of IAB feedback obtained over BP2	Existence of documentation with IAB feedback	Feedback was consolidated into a written document.	Report	Y	Report will be sent to DOE

All Task 8 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M8.1	Measurements from low-voltage testbed showing operation during realistic system disturbances	Uninterrupted power delivery during the following scenarios: 1) a unbalanced voltage sag of 5% on one ac grid phase, and 2) dc-side MPPT mismatches within 10% of a nominal value	Controllers were experimentally shown to accommodate low-voltage faults above 5% and large dc-side power mismatches above 10% with uninterrupted operation.	Electrical measurements	Y	BP3 Q2 report pages 9-10, BP3 Q4 report pages 4-9, BP3 Q5 report pages 6-11.
M8.2	LCOE framework which includes conductor costs, uninterrupted operation, and maintenance.	A mathematical model and numerical study will be used to demonstrate a greater than 3% LCOE reduction.	With the final LCOE-oriented design optimization method, the team presented the potential LCOE improvement of 5.5 % with the new power electronics architecture.	Numerical modeling	Y	BP3 Q3 report pages 8-12

Nearly all Task 9 Milestones were completed. We were unable to run the experiment at full voltage due to noise corrupting the centralized controller synchronization signal. This indicates that the decentralized methods we developed are indeed important and used in future projects/experiments. The existing results were limited to three series-connected converter blocks across a resistive load.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M9.1	A controllable grid interface configured to produce 13.2 kV and with appropriate instrumentation for data collection.	Electrical diagrams, design documentation, and photos showing completed experimental setup.	Testing plans at NREL were completed with necessary devices identified including meters and switches.	Diagrams, design documentation, and photos	Y	BP3 Q1 report page 15, BP3 Q2 report pages 12-13, BP3 Q3 report pages 14-15.
M9.2	A system of seven or more C2 blocks across a 7.2 kV grid.	Electrical measurements showing full-rated power delivery (within 5% of 7.5 kW) when connected to a 7.2 kV CGI.	The multi-converter racks were built and operated with three-units across a resistive load at reduced power.	Experimental measurements	N, Partial	BP3 Q1 report page 16, BP3 Q4 report pages 10-13, BP3 Q5 report page 13, Final Report page 33.
M9.3	A system of fourteen or more C2 blocks across a 13.2 kV grid.	Electrical measurements showing full-rated power delivery (within 5% of 7.5 kW) when connected to a 13.2 kV CGI.	The overall experiment was built but ran out of time to conduct experiment at full voltage.	Experimental measurements	N	BP3 Q4 report pages 10-13.

All Task 10 Milestones were completed.

	Metric Definition	Success Value	Measured Value	Assessment Tool	Goal Met (Y/N)	Supporting Data (pg. #)
M10.1	Final project results and industry feedback regarding market adoption.	Conclusion of meetings with industry contacts.	The team gathered industry feedback at the midpoint of the project and that report was submitted. Industry feedback is contained within that report.	Results evaluated in quarterly report and review.	Y	See M7.1 report
M10.2	Final project report.	A final project report that includes technical results, lessons learned, and feedback obtained from industry stakeholders.	The final report has been completed and submitted.	Final project report.	Y	This report.

2 Design of a three-phase DC-AC converter module: Architecture

Recently, modular converter typologies have gained attention as effective interfaces between low voltage (LV) dc/ac systems and the medium voltage (MV) ac grid. These architectures have been applied in a diverse set of use cases from electric vehicle (EV) charging to photovoltaic (PV) power

systems.

The proposed stackable, modular architecture is shown in Figure. 1 (a), where each module is comprised of a single dc port and three isolated single-phase ac ports. Each port can be used independently or configured to stack in series or parallel depending on the application requirements. Figure. 1 (a) provides an example configuration where each dc port is tied to independent LV sources like PV strings, while the ac ports are combined in series to facilitate connection with the MV three-phase grid. The architecture takes advantage of balanced three phase power to eliminate pulsating power at twice the line frequency at the dc port, effectively reducing energy storage requirements. The topology of each module is shown in Figure. 1 (b) and is comprised of a single quadruple active bridge (QAB) creating three isolated dc link voltages, each followed by a single-phase dc-ac inverter bridge. The QAB is operated as a fixed ratio converter known as a dc transformer (DCX) and provides galvanic isolation between the primary and each of the individual ac phases through solid state transformers (SST) that will be discussed in Section 3. This provided isolation allows for flexible stacking of each module's ac ports.

Each QAB phase A, B, and C provide time-varying power $p_A(t)$, $p_B(t)$, and $p_C(t)$ respectively, containing both a dc and a twice-line-frequency ac component. The three phase currents sum together on the primary side, resulting in dc power transfer from the input. This balanced three-phase power transfer allows for significant reduction in the sizes of passive components, specifically the dc-link capacitance.

This provides a significant advantage as compared to single-phase systems that require bulky dc-link capacitors capable of filtering the twice-line-frequency ac component. The three-phase power transfer eliminates this requirement, meaning the capacitors only need to be sized to filter switching ripple of the secondary-bridge and inverter bridge currents.

2.0.1 Design requirements for the three-phase DC-AC converter module

The overall system requirements are highlighted below:

1. System is capable of interfacing with a $13.2\,\mathrm{kV}$ ac grid and PV arrays rated for $1\,\mathrm{kV}$ dc.
2. System is comprised of 14 modules with ac output ports connected in series.

These system requirements educated the design choices made for each module. The design specifications for the module are highlighted below:

1. One module can supply $7.5\,\mathrm{kW}$ total output power, where $2.5\,\mathrm{kW}$ is delivered to each phase
2. Capable of $1\,\mathrm{kV}$ dc voltage operation
3. $1.7\,\mathrm{kV}$ silicon carbide devices from Wolfspeed Cree are used
4. Distributed control strategy, the primary and each secondary have their own dedicated microcontroller
5. Medium voltage isolation between the primary and each secondary is provided with planar magnetics, see Section 3.

2.0.2 Design of the three-phase DC-AC converter module

Taking the design constraints into consideration, a switching frequency of $200\,\text{kHz}$ and an optimal phase shift of 30° is selected for the QAB and a switching frequency of $10\,\text{kHz}$ is selected for each inverter. Steady state analysis can then be performed for each converter to determine component selection for filter inductance of the QAB and inverter as well as dc-link capacitance. The QAB component value selections are:

1. $66\,\mu$H series inductance
2. $385\,\mu$H magnetizing inductance
3. $64\,\mu$F dc-link capacitance at output of each QAB

The inverter component value selections are:

1. $320\,\mu$H filter inductance

3 High voltage planar magnetics and medium voltage transformer

Medium voltage transformers are gaining extreme popularity in power electronics applications, such as solid-state transformers (SST). Such SSTs eliminate intermediate conversion stages and improve efficiency. Planar transformers with printed circuit boards (PCBs) are commonly used in various applications. However, no literature or current state-of-the-art has ever explored a planar transformer to achieve high-frequency MV isolation in 10's of KV. A challenge is that standard PCB dielectrics like FR4 cannot offer adequate isolation between layers, and in fact require impractical distances between the layers, which may not be feasible to design. This challenge comes from the fact that interleaving the primary and secondary layers is very much necessary to reduce AC winding losses in high-frequency transformers. To overcome such challenges, a novel PCB technology and a design approach for high-frequency MV planar transformers is illustrated below:

As described in Section 2, multiple of these dc-ac modules are connected in series to interface the PV string modules to an MV ac grid without the need for bulk line frequency transformers, as shown in the Figure. 1 (a). Figure. 1 (b) is the same as the module shown in Section 2. From Figure. 1 (b), it can be seen that the ac line voltage appears across the primary and secondary of the high-frequency transformers, which must therefore meet MV isolation requirements. The planar transformer is designed for the QAB stages in the stacked architecture of Figure. 1.

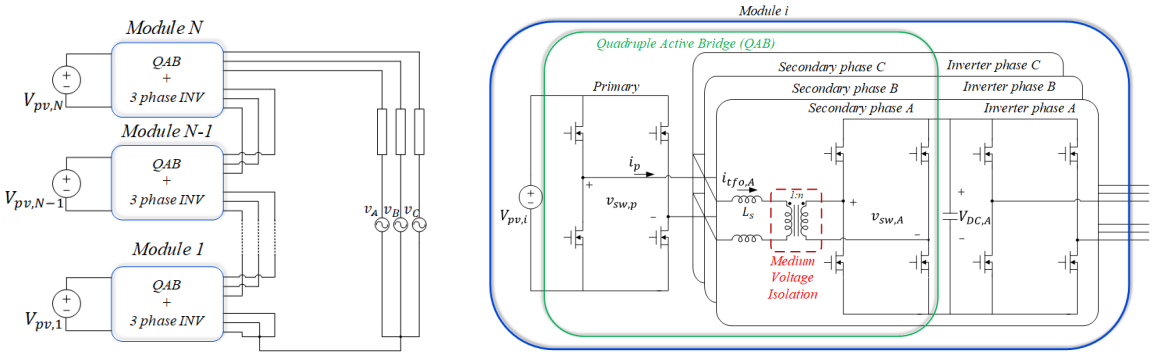


Figure 1: (a) Stackable architecture for PV string to medium voltage ac conversion, (b) Module schematic. In a target system, the nominal operating conditions are 1 kV dc string voltage, and 13.2 kV MVAC grid voltage.

3.0.1 Design requirements for the MV planar transformer

The design specifications for the planar transformer are highlighted as below:

1. $1\,\mathrm{kV}$ DC input and three-phase AC output voltages per module
2. Each MV transformer per module is rated for an output power of $2.5\,\mathrm{kW}$
3. The switching frequency is around $200\,\mathrm{kHz}$

3.0.2 Isolation requirements for MV transformer design

While interleaving the primary and secondary windings, the dielectric between the adjacent layers must have a sufficiently high breakdown voltage. Second, the vias interconnecting primary or secondary layers must be spaced sufficiently far from the windings since the vias and the windings act as two adjacent conductors with high potential difference between them. Third, the fringing electric fields at the edge of the PCB winding may result in voltage breakdown and arcing to the ferrite core or to an adjacent layer. With a breakdown voltage rating of $7\,\mathrm{kV/mil}$ (276 kV/mm), polyimide (Panasonic Felios RF775) is an attractive and low-cost dielectric option. Having a dielectric with 5 mil (0.13 mm) of RF775 enables potential difference of $\approx 35\,\mathrm{kV}$ between two adjacent PCB layers. In contrast, using standard FR4 material as dielectric (breakdown voltage $500\mathrm{V/mil}$) would require a 70 mil (1.8 mm) thick dielectric in order to withstand the same voltage of $35\,\mathrm{kV}$, leading to an impractical PCB design.

The location of the vias interconnecting the primary and secondary windings must be placed far away from the windings. Further, it is a better and safer option to move the windings away from the core in order to avoid breakdown and arcing to the ferrite core due to high fringing fields.

3.0.3 Design of a planar transformer

While preserving the constraints due to MV isolation requirements discussed in the previous section, the core geometry and the PCB windings can be selected to minimize the loss of the transformer under application-specific operating conditions. As indicated above, the specifications on the DC bus voltages are around $1\,\mathrm{kV}$, while the average power processed by each module is about $7.5\,\mathrm{kW}$.

Assuming quasi-steady-state operation at each point along the line cycle, the core loss is estimated following the iGSE method, and the ac winding losses are computed using Dowell's equations for up to the 11^{th} harmonic of the transformer currents. Finally, the overall loss is obtained by averaging the losses over a line cycle. The process is repeated for various core sizes and winding arrangements to arrive at a design where the total average loss is minimized subject to meeting the isolation constraints.

The final design summary of the transformer is as follows:

- No. of turns in primary and secondary: 30
- No. of turns per layer: 5
- Total no. of layers: 12
- Core size and material: EILP 102 with N87 material
- Copper thickness: 4oz

The design parameters are obtained following an optimization procedure that minimizes the overall loss at 75% of maximum power. Hipot testing was done at NREL to validate the MV isolation.

A MV transformer is built with 5 mils of Panasonic Felios RF 775 as the dielectric, according to the specifications described earlier in the section. The isolation capability is tested using the setup described in Section 3.0.4. A complete fabricated planar MV transformer is shown in Fig. 2 (a) with the PCB winding top view and assembly. Further, a circuit diagram of the guarded hipot test setup used to verify the isolation capability of the MV transformer is also shown in Fig. 2 (b)

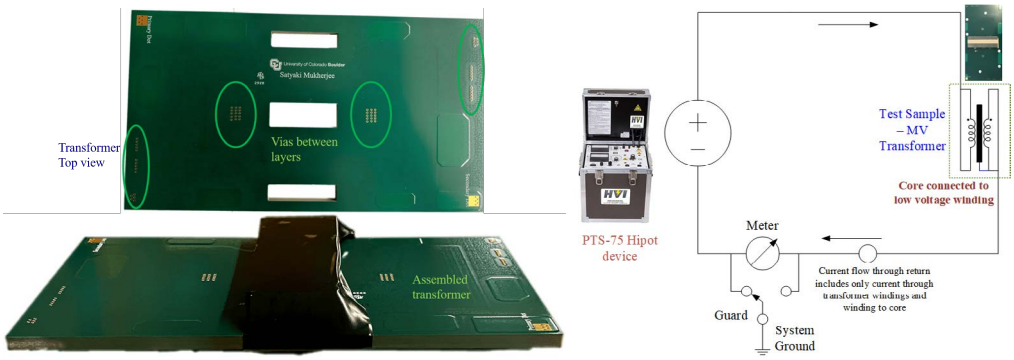


Figure 2: MV transformer and hipot test setup: (a) Fabricated planar MV transformer: PCB winding top view and assembly, and (b) circuit diagram of the guarded hipot test setup used to verify the isolation capability of the MV transformer.

3.0.4 MV Isolation testing

Figure 3: Hipot test setup and result data: (a) Photograph of the hipot testing setup with the device under test and connections from the PTS-75 hipot tester marked, (b) thermal image of the MV transformer with $26\,\text{kV}$ applied between it's primary and secondary terminals with grounded core segments, and (c) measurements of insulation impedances reported using the hipot tester across a wide range of applied voltages. Operating conditions : Ambient temperature : $21.9°C$, Relative humidity : 10.10%, elevation from sea level : $5,675\,\text{ft}$.

Fig. 2(a) shows a fully assembled transformer with the dielectric between two copper layers capable of withstanding $\approx 35\,\text{kV}$ using a sheet of 5 mil polyimide (Felios RF775). A high-voltage test setup using PTS-75 hipot tester is utilized to test the isolation capability of the MV transformer at the Energy Systems Integration Facility of the National Renewable Energy Laboratory at an elevation of $5,675\,\text{ft}$. from the sea level. Using the hipot tester, medium voltage is applied between the primary and the secondary windings of the prototype transformer. The core of the transformer is connected to the low-voltage side, which is referred to as the system ground. In accordance

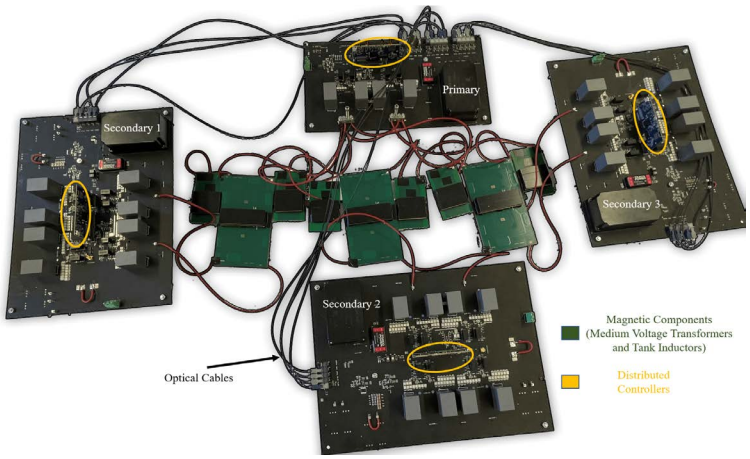


Figure 4: Photograph of the dc-to-ac module comprising one primary and three secondary full bridges, three MV transformers, and six power-transfer series inductors. Distributed controllers are marked on each of the primary and secondary boards.

with the hipot tester recommended procedure, a guarded return connection was used to accurately measure the leakage current between the transformer windings as well as between the high voltage windings and the grounded ferrite core. The connection diagram of the hipot test setup is shown in Fig. 2(b).

The insulation impedance is measured using the applied voltage and the hipot built-in high precision current meter. Fig. 3(a) shows a photograph of the MV transformer undergoing the hipot test procedure with all the connections labeled appropriately.

Fig. 3(b) shows a thermal image of the transformer under hipot testing, with $26\,\text{kV}$ applied between the primary and the secondary terminals demonstrating operation unaffected by the applied voltage. In Fig. 3(c), the insulation impedance measured using the PTS-75 hipot tester is plotted against a wide range of applied voltages. The device under test, i.e. the prototype transformer, is capable of maintaining $> 50\,G\Omega$ impedance up to $26\,\text{kV}$ across the transformer terminals, indicating no breakdown. Testing up to $26\,\text{kV}$ allows for almost 140% margin on the isolation requirement given by the peak line-to-neutral voltage of $10.8\,\text{kV}$ at the nominal system operating point in the $13.2\,\text{kV}$ line-to-line MV ac (MVAC) grid, thus meeting the ANSI NETA ATS 2017 standard for isolation requirements. The insulation on the MV transformer was found to be most prone to the breakdown between the high-voltage winding and the grounded core. A separate experiment with only the planar PCB excluding grounded ferrite core segments demonstrated $152\,G\Omega$ insulation impedance at $26\,\text{kV}$ applied across the windings.

3.0.5 Prototype Module with the High-Frequency MV Planar Transformer

Fig. 4 shows a completely assembled module utilizing three MV transformers of Fig. 2(a). A primary board with a full bridge inverter of the QAB stage and three secondary boards each consisting of a full bridge rectifier for the QAB stage and a low-frequency full bridge inverter, all utilizing $1700\,\text{V}$ SiC devices with distributed controllers are shown in Fig. 4.

Fig. 5(a) demonstrates switch-node voltages with zero voltage switching of the high-frequency SiC MOSFETs. High-frequency primary and secondary current waveforms of all three DAB mod-

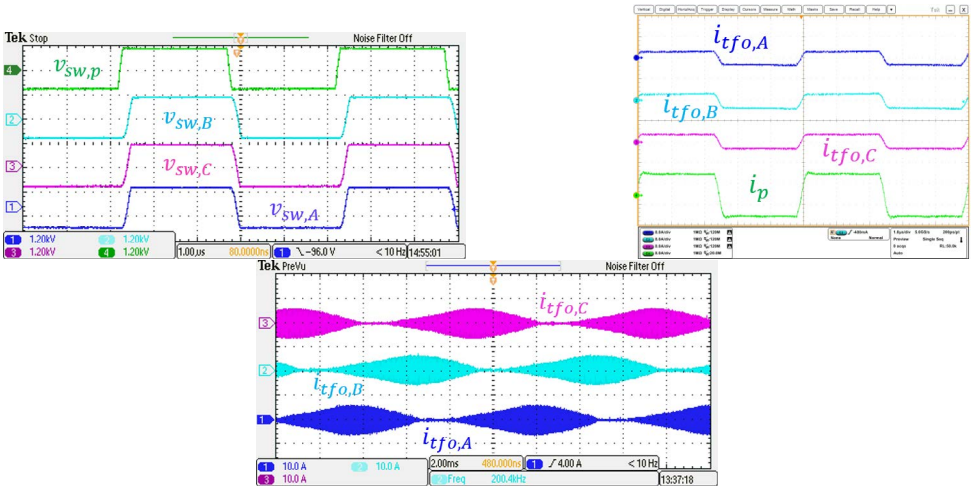


Figure 5: (a) Switch-node voltage waveforms in the dc-to-ac module illustrating generation of three isolated dc bus voltages from the primary input dc voltage of 1000 V, (b) zoomed-in high-frequency flat-top current waveforms processed by the MV transformers, and (c) secondary currents of the three module transformers with twice line-frequency components illustrating three-phase operation of the module delivering a total of 7.5 kW.

ules in the QAB stage are shown in Fig. 5(b), utilizing the MV transformer at $V_{pv,i} = V_{DC,link} = 1000$ V, $L_s = 60\mu$ H and processing 7.5 kW power with 97% overall efficiency. Additionally, Fig. 5(c) shows pulsating currents processed by the three MV transformers over the line cycle for dc-to-3 phase ac operation of the module. Predicted transformer loss of approximately 55 W per transformer, with 7.5 kW three phase power processed by the converter module, is consistent with the experimental results. Out of a total loss of 55 W, 15 W is the core loss and 40 W is the conduction loss. The conduction losses are largely attributed to two factors: 1) presence of an airgap, in order to ensure zero voltage switching of the secondary SiC MOSFETs, which degrades interleaving of the high-frequency windings and results in a higher current density in the top winding layer, and 2) to maintain proper isolation, the length of the transformer windings are increased resulting in a larger dc resistance. The transformer losses are related to the choice of the planar core (EILP 102), which is the largest standard planar core available. If a larger core was available, a design with fewer turns would result in a more efficient planar MV transformer.

4 Soft switching in a QAB converter

The most important feature of this topology of a QAB converter is that it is of utmost importance to achieve zero voltage switching over the entire line cycle. In order to guarantee ZVS operation over the entire line cycle, it is enough to show that ZVS can be achieved at zero power instant. The tank inductance does not have enough energy stored in it in order to ensure ZVS at zero power intervals. Thus, we rely on the circulating currents induced due to the magnetizing inductance of the transformer. However, these circulating currently greatly reduce the switching loss at the expense of increased conduction losses. As an alternative, a larger series inductance could be used, but this approach would result in reduced efficiency at full load.

Over a line cycle, the power processed by each secondary is determined by the corresponding

phase shift between the secondary and the primary full bridge:

$$\begin{aligned}\varphi_A(t) &= \varphi_m \sin^2(\omega_0 t)\\ \varphi_B(t) &= \varphi_m \sin^2\left(\omega_0 t + \frac{2\pi}{3}\right)\\ \varphi_C(t) &= \varphi_m \sin^2\left(\omega_0 t - \frac{2\pi}{3}\right),\end{aligned} \tag{1}$$

where φ_m is the maximum phase shift, and ω_0 is the angular line frequency.

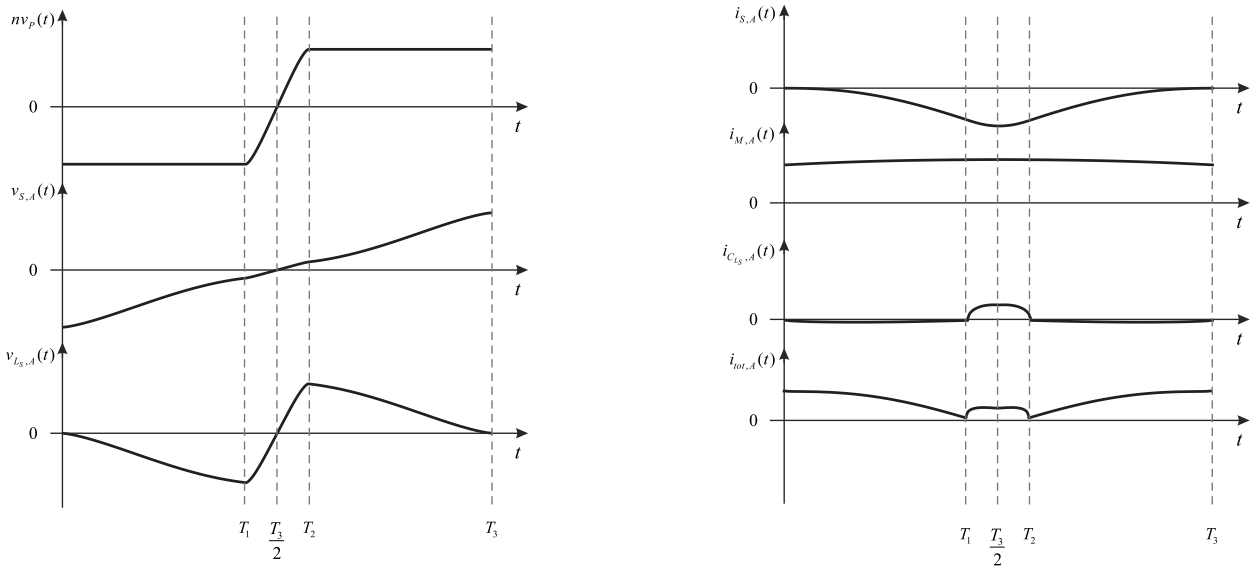


Figure 6: Model-based waveforms of the ZVS transition at the zero power transfer instant for Phase A. Referring to Fig. 7, $T_3 = t_{ds}$ and $T_2 - T_1 = t_{dp}$.

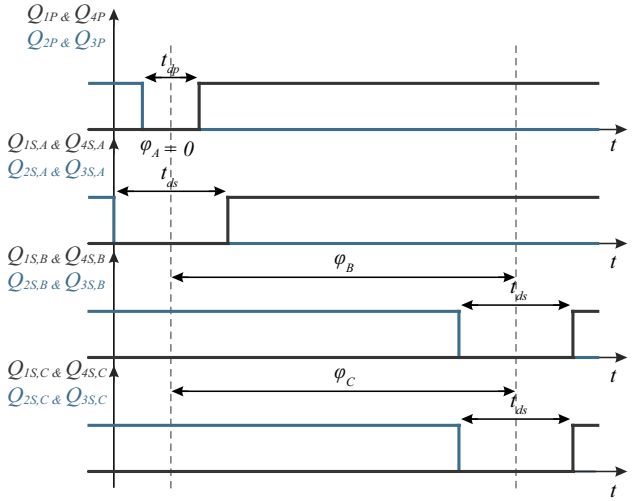


Figure 7: QAB switch control signals at the time when the secondary Phase A processes zero power.

Consider the time instant when the power processed by phase A is zero, while phases B and C contribute non-zero instantaneous power levels to maintain constant overall power in the three-phase module. The corresponding switch control signals are shown in Fig. 7. The phase shift φ_A

Table 1: Time instants of the switching sequence during ZVS transition

T_1	$0.5(t_{ds}-t_{dp})$
T_2	$0.5(t_{ds}+t_{dp})$
T_3	t_{ds}

Table 2: Time intervals of the switching sequence during ZVS transition

Interval I	$0 \le t < T_1$
Interval II	$T_1 \le t < T_2$
Interval III	$T_2 \le t < T_3$

between the primary bridge and the phase A secondary bridge is zero, so that the corresponding control pulses are centered around the same instant. Theoretical, model-based waveforms during the rise-time transition of the secondary switching node are shown in Fig. 6. Definitions of the time instants and the time intervals during the transition are given in Tables 1 and 2, while the corresponding equivalent circuit models for the switching sequence consisting of Intervals I, II and III are shown in Fig. 8.

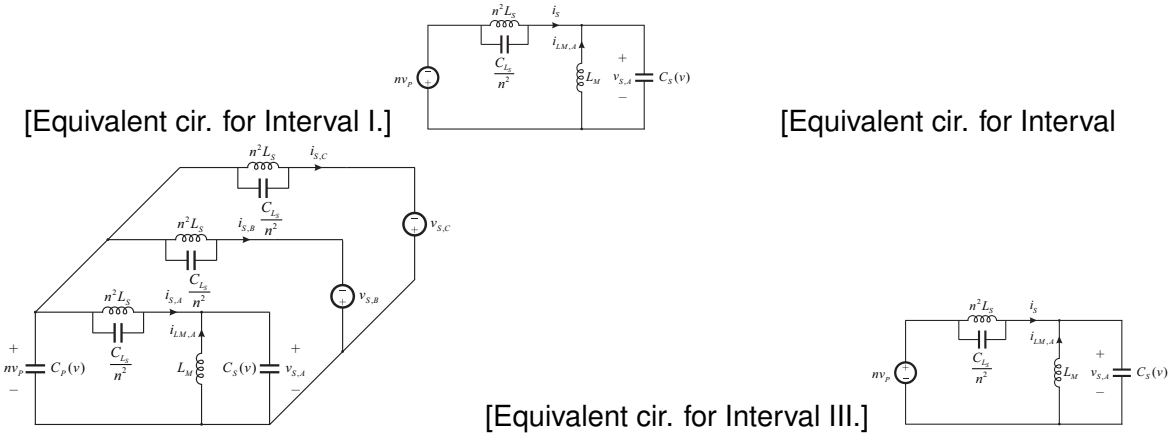


Figure 8: Equivalent circuits during ZVS transition at the zero power transfer instant for one of the phases.

At the beginning of time Interval I (Fig. 8(a)), the secondary side switches $Q_{2S,A}$ and $Q_{3S,A}$ are turned off. The magnetizing inductance current $i_{M,A}$ starts charging voltage dependent switching-node capacitance $C_S(v)$ of the phase A secondary bridge, and the switching node voltage $v_{S,A}$ starts increasing. As $v_{S,A}$ increases, a negative voltage is applied across the series inductance, and the current $i_{S,A}$ starts decreasing.

The primary-side switches Q_{2P} and Q_{3P} turn off at the beginning of Interval II. The equivalent circuit in Interval II is shown in Fig. 8(b). During this interval, phases B and C are charging the switching-node capacitance $C_P(v)$ on the primary side. It is assumed that the QAB is closed-loop controlled to operate as a DCX, so that $v_{S,B}$ and $v_{S,C}$ can be considered constant voltage sources. The rise time of the primary side switching node v_P is faster than $v_{S,A}$, because the sum of the currents $i_{S,B}$ and $i_{S,C}$ is much higher than the peak of the magnetizing current. This implies that $\frac{dv}{dt}$ across the series inductance parasitic capacitance C_{L_S} is approximately constant, therefore the constant current through C_{L_S} charges $v_{S,A}$ linearly.

At the mid-point of Interval II, nv_P becomes higher than $v_{S,A}$, and the slope of $i_{S,A}$ changes polarity. Interval II ends, completing the ZVS transition of v_P, at the end of the primary-side dead time t_{dp}.

Interval III starts with turning on switches Q_{1P} and Q_{4P} of the primary full bridge. The corre-

sponding equivalent circuit is shown in Fig. 8(c). During this interval, current $i_{S,A}$ is increasing until $v_{S,A}$ reaches the end of the ZVS transition. At that instant, $Q_{1S,A}$ and $Q_{4S,A}$ are turned on, which ends Interval III and the secondary phase A dead time t_{ds}.

It should be noted that the total current that charges the switching node capacitance,

$$i_{tot,A} = i_{S,A} + i_{M,A} + i_{C_{L_S},A} \tag{2}$$

reaches a minimum at the beginning of the Interval II. If this current became negative, it would start discharging the secondary side switching-node capacitance $C_S(v)$, which means that it would not be possible to complete the ZVS switching sequence as described above. Fig. 6 shows theoretical waveforms for the case when the minimum of $i_{tot,A}$ is zero. This represents the optimal design, in the sense of achieving ZVS operation while minimizing the peak of the magnetizing inductance current, and therefore minimizing the conduction losses introduced by the circulating current. Proper sizing of the magnetizing inductance and appropriate selection of primary and secondary dead-times is critical for an optimal design

Thus, an optimal design procedure gives the following values:

- Primary side dead-time: $110\,\text{ns}$
- Secondary side dead-time: $740\,\text{ns}$
- Magnetizing inductance: $385\,\text{uH}$

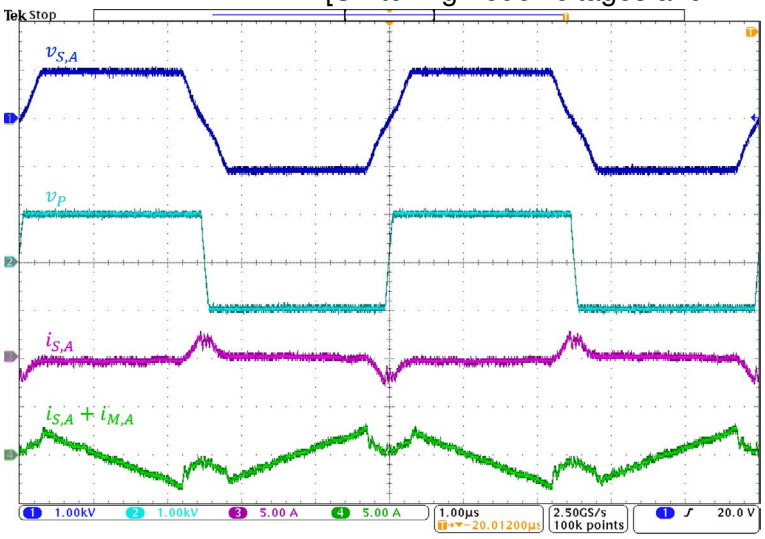
The above parameters ensure ZVS over the entire line cycle. Fig. 9(a) shows ZVS operation at the zero power crossing of phase A, while Fig. 9(b) confirms that the measured waveforms closely match the theoretical waveforms shown in Fig. 6. It should be noted that the planar implementation of the mangetic components have pronounced parasitics, which result in increased high-frequency parasitic oscillations.

5 AC-side controllers for decentralized power sharing and interleaving

In this work, we formulated a model of the stacked converter system equipped with the Andronov-Hopf Oscillators (AHO) to control active and reactive power delivery on the ac side of the system. The aim was to obtain a decentralized structure that bypassed the need for a centralized controller which may act as a single point of failure and hinder scalability. In prior reports, we determined the parameters of the AHO controller that will result in stable operation of the system. Here, the experimental results that validate the performance of the proposed AHO-based controller for cascaded dc-ac inverters is presented. The laboratory-scale experimental hardware platform consisting of 5 cascaded three-phase inverters as shown in Fig. 10. On the ac-side the inverter stack is interfaced to an R-L load through an inductive line filter. The most noteworthy feature of this control method is that there is no communication links among the stacked inverters.

Experimental validation of the proposed AHO-based cascaded inverter control method is demonstrated in Figs. 11–14(b). Figure 11(a) shows steady-state operation of the system with equal nominal RMS voltage set-points at $V_{\text{nom}} = 40\,\text{V}$, for all the 5 units. In this case, the overall stack voltage is 200 V_{rms} and every unit delivers 420 W of active power to the load. A zoomed-in view of the inverter phase voltages is shown in Fig. 11(b) (bottom), which verifies the fact that the inverter output voltages have zero relative angle difference at steady state ($\delta_{j1,\text{eq}} = 0$, $j = 1, \cdots, 5$), owing to uniform voltage and power set-points along the stack. Figure 11(b) (top) shows the fundamental 60 Hz component in individual inverter output voltages that verify uniform voltage sharing.

[Switching-node voltages and currents]



[Waveforms during ZVS transition.]

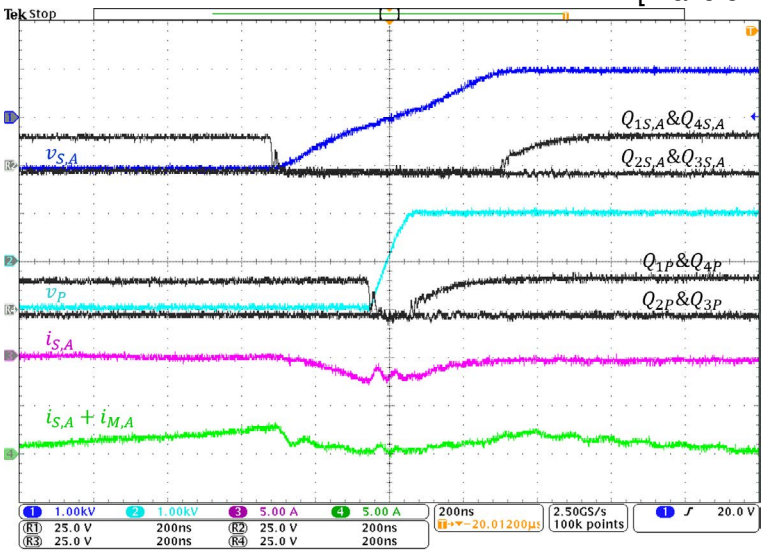


Figure 9: Waveforms illustrating zero voltage switching at the zero power instant for phase A.

Figs. 12 and 13 demonstrate non-uniform power sharing in the cascaded system. Figure 12(a) shows the system steady state operation with unequal nominal voltage set-points as, $V_{\text{nom1}} = 50$ V, $V_{\text{nom2}} = 45$ V, $V_{\text{nom3}} = 40$ V, $V_{\text{nom4}} = 35$ V, $V_{\text{nom5}} = 30$ V. In this case, the inverters share the total load power according to their power ratings. Even if the inverters generate unequal voltages, their relative angle differences are still same as can be seen in Fig. 12(b) (bottom). Figure 12(b) (top) shows the fundamental 60 Hz component in the inverter voltages which are unequal and vary according to the nominal voltage set-point of the inverter. Fig. 13 shows another case of non-uniform power sharing where 3 inverters are of equal power rating while the other two have different ratings. These results illustrate how series-connected converters can share adjustable power and voltages without explicit communication channels.

Next, Fig. 14(a) demonstrates the communication-free synchronization of the inverters from randomized initial voltages to the desired nominal voltage $V_{\text{nom}} = 40\,\text{V}$. The time required for the

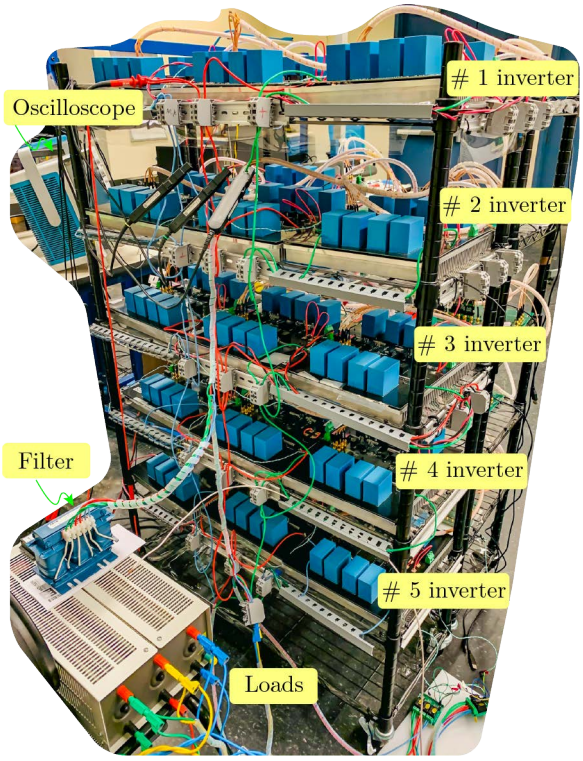
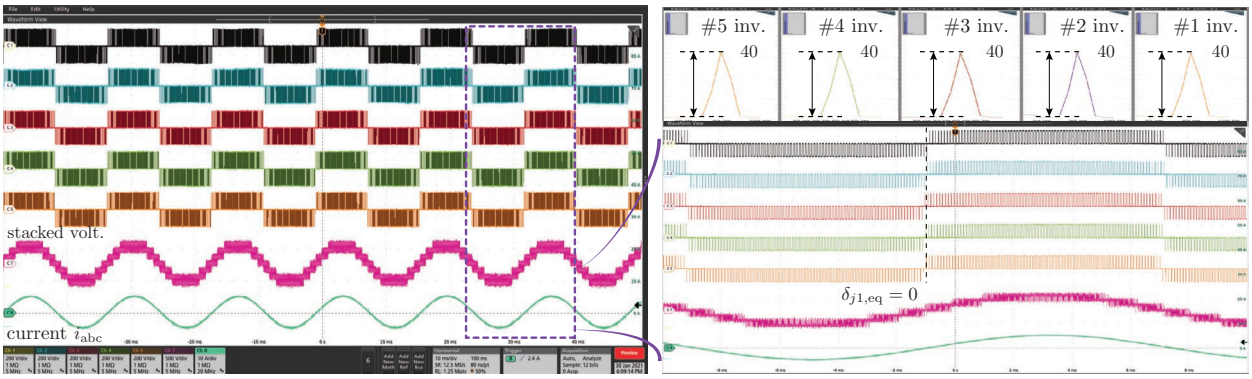


Figure 10: Developed experimental platform: 5 cascaded inverters supplying common loads.



(a) inverter voltages, stacked voltage and current (b) one-cycle zoom in

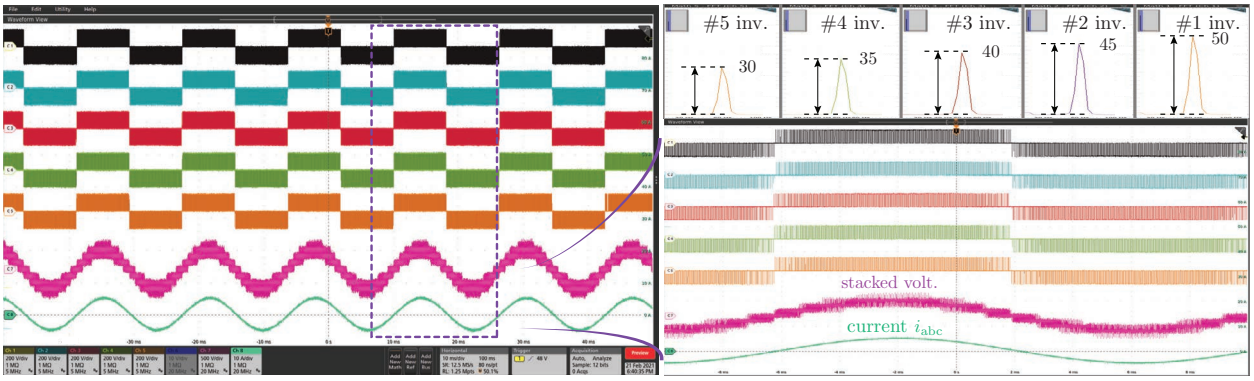
Figure 11: Uniform load sharing: $V_{\mathrm{nom1}} = 40$ V, $V_{\mathrm{nom2}} = 40$ V, $V_{\mathrm{nom3}} = 40$ V, $V_{\mathrm{nom4}} = 40$ V, $V_{\mathrm{nom5}} = 40$ V.

inverter voltages to synchronize with one another is around $200\,\mathrm{ms}$.

In Fig. 14(b) the dynamic response of the stack of inverters to a load-step change is shown. In this case, the load is stepped up by 33% and the inverters step up their power output while regulating their output voltages within the specified 2% offset range. Also, as can be seen, the response time of the inverters to this load step change is less than 1 ac cycle.

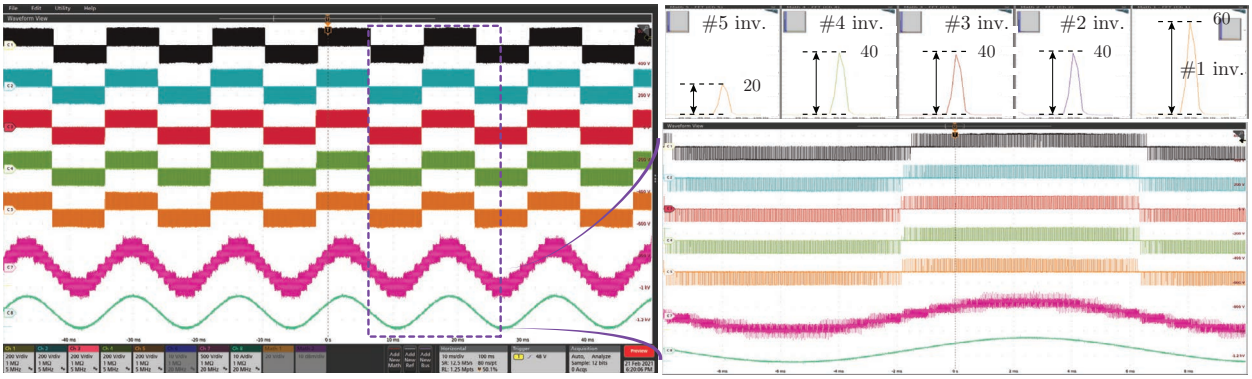
6 Control Design of Cascaded Converters

Practical implementation of the quadruple-active bridge converter module in PV systems requires a variety of controllers that collectively achieve maximum power point tracking, dc-link regulation, and ac-side power control. Design of such multi-loop systems is generally quite challenging due



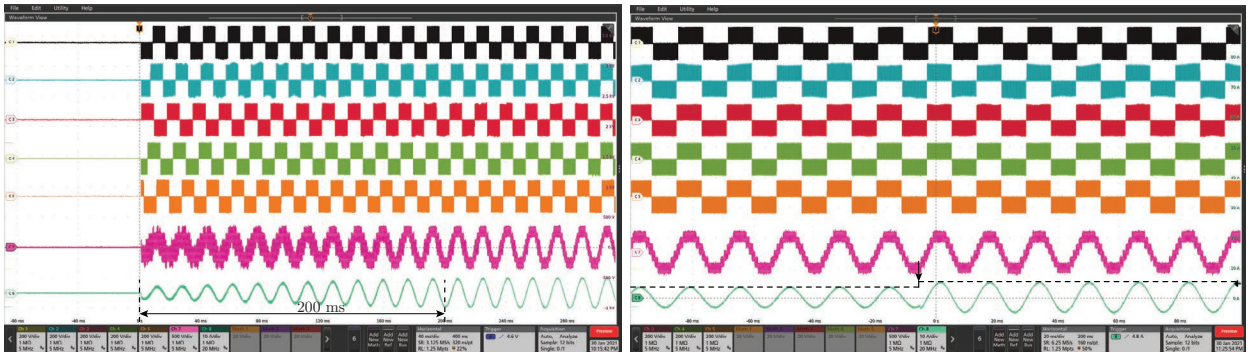
(a) inverter voltages, stacked voltage and current (b) one-cycle zoom in

Figure 12: Non-uniform load sharing. Case-1: $V_{\text{nom1}} = 50$ V, $V_{\text{nom2}} = 45$ V, $V_{\text{nom3}} = 40$ V, $V_{\text{nom4}} = 35$ V, $V_{\text{nom5}} = 30$ V.



(a) inverter voltages, stacked voltage and current (b) one-cycle zoom in

Figure 13: Non-uniform load sharing. Case-2: $V_{\text{nom1}} = 60$ V, $V_{\text{nom2}} = 40$ V, $V_{\text{nom3}} = 40$ V, $V_{\text{nom4}} = 40$ V, $V_{\text{nom5}} = 20$ V.



(a) (b)

Figure 14: Transient performance : (a) Start up transient and (b) Load step change 30%.

to the potential for destabilizing interactions among loops. We propose a design approach where singular perturbation theory is used to decompose the timescales at which each control loop operates and provides a systematic framework for parametric selection. Our approach also ensures system stability of multiple modules with identical controls connected in series across a grid. Next, we discuss the various control subsystems.

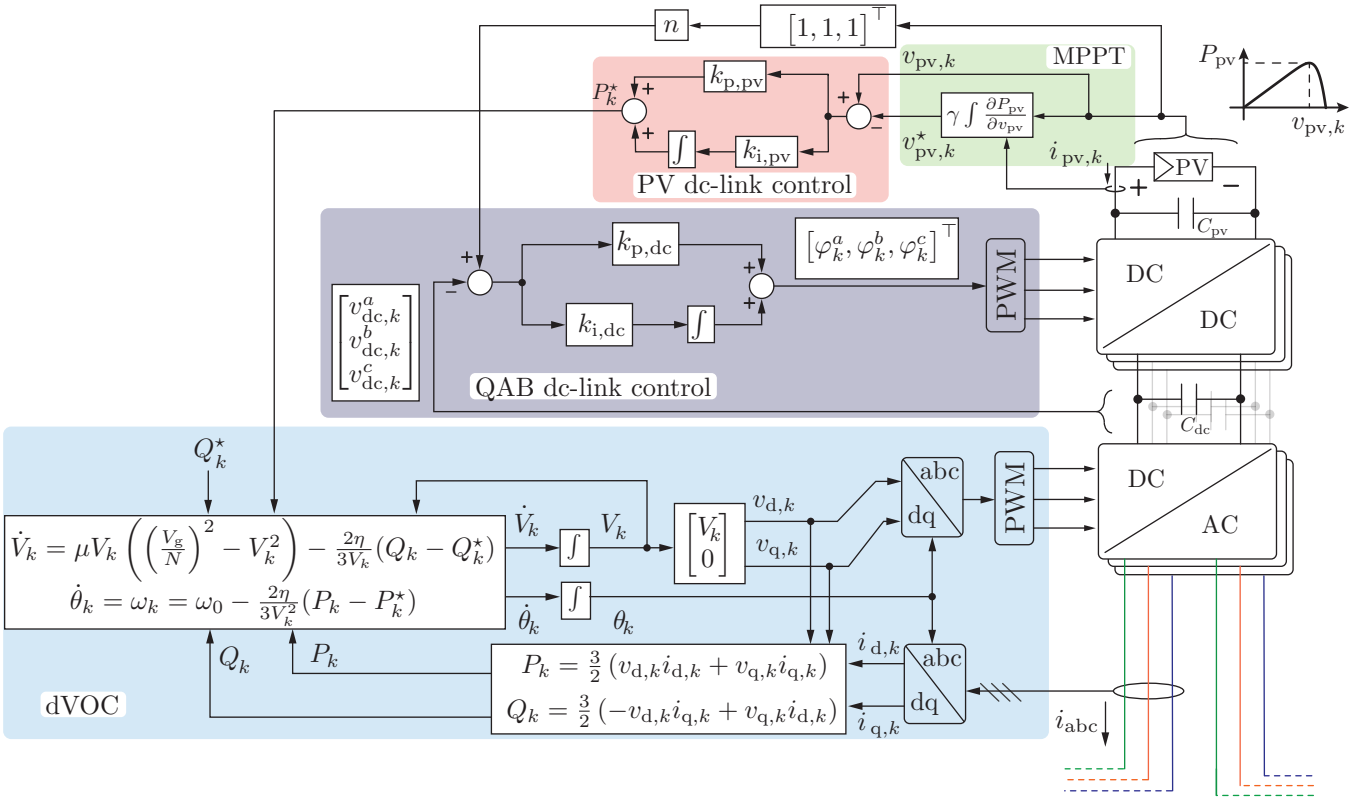


Figure 15: The control architecture of the k-th converter module contains the following interconnected control loops: MPPT, PV dc-link control, floating dc-link controls, and dVOC-based ac-side control. The quadruple active bridge converter is compactly depicted with three dc-dc blocks, and the dc-ac H-bridge inverters interface to adjacent units in the system.

QAB with Floating Dc Links: The primary side bridge is common to each of the three floating secondary bridges. All four bridges are modulated to produce an ac voltage waveform with 50% duty ratio, and the primary-side bridge acts as an angular reference to the remaining three others. Accordingly, the phase shifts of the secondary bridge waveforms relative to the primary side will act as our control signal for dc link voltage regulation. We denote the phase shift of the secondary DAB bridge associated with the j-th ac phase within the k-th module as φ_k^j, where $j \in \{a,b,c\}$. The voltage across each of the floating dc links evolves as

$$C_{\mathrm{dc}} \frac{dv_{\mathrm{dc},k}^j}{dt} = \frac{v_{\mathrm{pv},k}}{nL\omega_{\mathrm{sw}}} \varphi_k^j \left(1 - \frac{\varphi_k^j}{\pi}\right) - \frac{P_k^j}{v_{\mathrm{dc},k}^j}, \tag{3}$$

where ω_{sw} is the DAB switching frequency in rad/s, φ_k^j is the phase shift of each secondary bridge with respect to the primary, and $v_{\mathrm{pv},k}$ is the dc voltage across the PV input. P_k^j denotes the power transferred from the primary to the j-th secondary.

A proportional-integral (PI) controller ensures DCX operation such that the dc voltage across C_{dc} tracks nv_{pv}. This gives the following control law:

$$\varphi_k^j = k_{\mathrm{p,dc}}(nv_{\mathrm{pv},k} - v_{\mathrm{dc},k}^j) + C_{\mathrm{dc}} k_{\mathrm{i,dc}} \int (nv_{\mathrm{pv},k} - v_{\mathrm{dc},k}^j) \mathrm{d}t \tag{4}$$

This controller is replicated across the three dc links where $j \in \{a,b,c\}$. The proportional and integral gains are denoted as $k_{\mathrm{p,dc}}$ and $k_{\mathrm{i,dc}}$, respectively.

Within a given module, we assume the floating dc-link voltage for each phase, $v^j_{\mathrm{dc},k}$, is approximately equal to its steady state value, $v^0_{\mathrm{dc,k}}$. Furthermore, each DAB is assumed to operate with small phase shifts such that $(\varphi^j_k)^2$ is negligibly small. Taken together, these modeling constructs allow us to convert the dynamics in (3) into the simplified model given by

$$C_{\mathrm{dc}}\frac{dv^j_{\mathrm{dc},k}}{dt} = \frac{v_{\mathrm{pv},k}}{nL\omega_{\mathrm{sw}}}\varphi^j_k - \frac{P^j_k}{v^0_{\mathrm{dc}_k}}. \Rightarrow C_{\mathrm{dc}}\frac{dv_{\mathrm{dc},k}}{dt} = \frac{v_{\mathrm{pv},k}}{nL\omega_{\mathrm{sw}}}\varphi_k - \frac{P_k}{3v^0_{\mathrm{dc}_k}},$$

where lumped variables $v_{\mathrm{dc},k}$ and φ_k are defined as $v_{\mathrm{dc},k} = (1/3)\sum_j v^j_{\mathrm{dc},k}, \quad \varphi_k = (1/3)\sum_j \varphi^j_k$.

Ac-Side Dynamics: Each set of module-level three-phase H-bridges is modulated with the dVOC dynamics given by

$$\dot{V}_k = \mu V_k\left(\left(\frac{V_{\mathrm{g}}}{N}\right)^2 - V_k^2\right) - \frac{2\eta}{3V_k}(Q_k - Q^\star_k), \quad \text{(5a)} \qquad \dot{\theta}_k = \omega_k = \omega_0 - \frac{2\eta}{3V_k^2}(P_k - P^\star_k), \quad \text{(5b)}$$

where μ and η are control gains, and ω_0 is the nominal grid frequency. The peak voltage generated by each single phase inverter is denoted as V_k, and the three-phase waveforms are in the vector $v_k = [v^{\mathrm{a}}_k, v^{\mathrm{b}}_k, v^{\mathrm{c}}_k]^\top$. Active and reactive power delivered by the k-th module are represented as P_k and Q_k, respectively. Similarly, $P^\star_k$ and $Q^\star_k$ denote the corresponding references for active and reactive power, respectively. In subsequent analysis, we will show that $P^\star_k$ is generated by an upstream control loop whereas $Q^\star_k$ will be assumed constant. N series-connected sets of ac terminals with the aforementioned control give the following line filter dynamics:

$$\sum_{k=1}^{N} V_k\cos\delta_k = L_{\mathrm{f}}\frac{di_{\mathrm{d}}}{dt} - L_{\mathrm{f}}\omega i_{\mathrm{q}} + R_{\mathrm{f}}i_{\mathrm{d}} + V_g, \quad \sum_{k=1}^{N} V_k\sin\delta_k = L_{\mathrm{f}}\frac{di_{\mathrm{q}}}{dt} + L_{\mathrm{f}}\omega i_{\mathrm{d}} + R_{\mathrm{f}}i_{\mathrm{q}} \tag{6}$$

where $P_{\mathrm{in},k}$ is the PV-generated power and $P_{\mathrm{out},k}$ is power delivered to the QAB. Assuming the QAB circuitry is lossless, it follows that $P_{\mathrm{out},k}$ equals the ac side power, P_k, for the $k-$th module. The input power is expressed as $P_{\mathrm{in},k} = v_{\mathrm{pv},k}i_{\mathrm{pv},k}$ where the PV current $i_{\mathrm{pv},k}$ takes the form

PV Terminal Dynamics: Energy buffering between the PV panel and QAB stage is provided by the PV-side capacitance C_{pv}. The PV voltage dynamics can be expressed as

$$\frac{d}{dt}\left(\frac{1}{2}C_{\mathrm{pv}}v^2_{\mathrm{pv},k}\right) = P_{\mathrm{in},k} - P_{\mathrm{out},k}, \tag{7}$$

A small signal dynamic model is obtained by the addition of perturbations to $v_{\mathrm{pv},k}$, $P_{\mathrm{in},k}$, and $P_{\mathrm{out},k}$ in (7). This gives

$$V_{\mathrm{pv},k}C_{\mathrm{pv}}\frac{dv_{\mathrm{pv},k}}{dt} = f_{\mathrm{pv}}(v_{\mathrm{pv},k}, i_{\mathrm{pv},k}, r_{\mathrm{pv},k}) - p^\star_k. \tag{8}$$

We will simplify (8) by approximating the value of $f_{\mathrm{pv},k}(v_{\mathrm{pv},k}, i_{\mathrm{pv},k}, r_{\mathrm{pv},k})$ at distinct regions across the PV curve.

$$f_{\mathrm{pv},k}(\cdot) = \begin{cases} I_{\mathrm{pv},k}v_{\mathrm{pv},k}, & \text{when } v_{\mathrm{pv},k} < V_{\mathrm{mpp},k} - \dfrac{\varepsilon}{2} \\ -\dfrac{v^2_{\mathrm{pv},k}}{R_{\mathrm{mpp},k}}, & \text{when } V_{\mathrm{mpp},k} - \dfrac{\varepsilon}{2} < v_{\mathrm{pv},k} < V_{\mathrm{mpp},k} + \dfrac{\varepsilon}{2} \\ -\dfrac{V_{\mathrm{pv},k}}{r_{\mathrm{pv},k}}v_{\mathrm{pv},k}, & \text{when } v_{\mathrm{pv},k} > V_{\mathrm{mpp},k} + \dfrac{\varepsilon}{2} \end{cases}$$

The PV dc-link controller ensures the k-th PV voltage, $v_{\mathrm{pv},k}$, is regulated to follow the command $v^{\star}_{\mathrm{pv},k}$, which is produced by the MPPT. To this end, a PI controller processes the voltage error and generates the ac side power reference, $P^{\star}_{k}$. The PV dc-link controller is given by

$$P^{\star}_{k} = k_{\mathrm{p,pv}}(v_{\mathrm{pv},k} - v^{\star}_{\mathrm{pv},k}) + C_{\mathrm{pv}} k_{\mathrm{i,pv}} \int (v_{\mathrm{pv},k} - v^{\star}_{\mathrm{pv},k}) \mathrm{d}t. \tag{9}$$

MPPT Control: To evaluate MPPT performance we seek a simplified version of (8) and linearize the algebraic expression of the pv current around the MPP to obtain

$$i_{\mathrm{pv},k} = I_{\mathrm{mpp},k} - \frac{1}{R_{\mathrm{mpp},k}}(v_{\mathrm{pv},k} - V_{\mathrm{mpp},k}), \tag{10}$$

To track the MPP, we employ the integral control law that acts on the slope of the PV power-voltage curve as follows:

$$v^{\star}_{\mathrm{pv},k} = \gamma \int \frac{\partial (v_{\mathrm{pv},k} i_{\mathrm{pv},k})}{\partial v_{\mathrm{pv},k}} \mathrm{d}t \tag{11}$$

For each of the aforementioned subsystems, we now shift our focus to designing the controllers after application of singular perturbation theory. Our overall strategy is predicated on an intuition of how the various subsystems within each module interact and seeking a logical ordering of timescales over which they operate. Towards this objective, we first apply singular perturbation to each subsystem such that it is partitioned into fast and slow modes. This yields a form that is amenable to design such that we can obtain the preordained ordering and separation of timescales while also guaranteeing stability within and among subsystems. In the ensuing analysis we apply the aforementioned strategy and describe each subsystem sequentially from fastest to slowest.

QAB Dc-link Voltage Regulation:

State Equations: Dc link voltage control is achieved through the PI regulator in (4). To cast the subsystem in (3)–(4) into the singular perturbation framework, we define two new states as

$$e_{1,k} := n v_{\mathrm{pv},k} - v_{\mathrm{dc},k}, \quad e_{2,k} := C_{\mathrm{dc}} \int_{0}^{\tau} e_{1,k}\, \mathrm{d}\sigma + e_{2,k}(0),$$

where $\tau = t/C_{\mathrm{dc}}$ is the new time variable associated with the fast mode. Now (3) and (4) can be rewritten as

$$C_{\mathrm{dc}} \frac{de_{1,k}}{d\tau} = \frac{-v_{\mathrm{pv},k}}{nL\omega_{\mathrm{sw}}}(k_{\mathrm{p,dc}} e_{1,k} + k_{\mathrm{i,dc}} e_{2,k}) + \frac{P_k}{3v_{\mathrm{dc},k}{}^{0}}, \tag{12a}$$

$$\frac{de_{2,k}}{d\tau} = C_{\mathrm{dc}} e_{1,k}. \tag{12b}$$

From (12a), we set C_{dc} to zero, obtain the algebraic solution of $\bar{e}_{1,k}$, and substitute that into (12b) to obtain the reduced order model as follows:

$$\frac{d\bar{e}_{2,k}}{dt} = -\frac{k_{\mathrm{i,dc}}}{k_{\mathrm{p,dc}}} \bar{e}_{2,k} + \left(\frac{v_{\mathrm{pv},k}}{nL\omega_{\mathrm{sw}}}\right)^{-1} \frac{P}{3k_{\mathrm{p,dc}} v^{0}_{\mathrm{dc},k}} \tag{13}$$

The fast mode model is

$$\frac{d\widetilde{e}_{1,k}}{d\tau} = -\frac{v_{\mathrm{pv},k} k_{\mathrm{p,dc}}}{nC_{\mathrm{dc}} L\omega_{\mathrm{sw}}} \widetilde{e}_{1,k} =: -\omega^{f}_{\mathrm{QAB}} \widetilde{e}_{1,k}, \tag{14}$$

where $\widetilde{e}_{1,k}$ captures the error in excess of $\mathscr{O}(\varepsilon)$ in $e_{1,k} - \bar{e}_{1,k}$.

Stability and Control Parameter Selection: For stability, it is necessary to ensure $k_{\mathrm{p,dc}} \geq 0$ and $k_{\mathrm{i,dc}} \geq 0$. From (13), the effective bandwidth of the QAB loop is $\omega_{\mathrm{QAB}} = \frac{k_{\mathrm{i,dc}}}{k_{\mathrm{p,dc}}}$. This leads us to the first stability criteria as

$$\omega_{\mathrm{QAB}} \ll \omega^{f}_{\mathrm{QAB}} \ll \omega_{\mathrm{sw}}, \tag{15}$$

where ω_{QAB} corresponds to the slower acting integral control and ω^f_{QAB} captures the bandwidth of the fast mode model in (14). Appropriate substitutions into (15) give the following guideline for control gain selection:

$$\frac{k_{\mathrm{i,dc}}}{k_{\mathrm{p,dc}}} \ll \frac{v_{\mathrm{pv},k} k_{\mathrm{p,dc}}}{n C_{\mathrm{dc}} L \omega_{\mathrm{sw}}} \ll \omega_{\mathrm{sw}}. \tag{16}$$

DVOC-based Inverter Control:

State Equations: The nonlinear dVOC control law exhibits slower dynamics than the plant in (6). This follows from the observation that the small perturbation parameter $L_{\mathrm{f}}/R_{\mathrm{f}}$ gives fast line dynamics. Hence, we set $L_{\mathrm{f}}/R_{\mathrm{f}} = 0$ and obtain the following algebraic solution from (6):

$$i_{\mathrm{d}} = \frac{\sum_{k=1}^{N} V_k \cos(\delta_k - \phi_{\mathrm{f}}) - V_{\mathrm{g}} \cos(\phi_{\mathrm{f}})}{Z_{\mathrm{f}}}, \tag{17a}$$

$$i_{\mathrm{q}} = \frac{\sum_{k=1}^{N} V_k \sin(\delta_k - \phi_{\mathrm{f}}) + V_{\mathrm{g}} \sin(\phi_{\mathrm{f}})}{Z_{\mathrm{f}}}, \tag{17b}$$

where we recall that Z_{f} and ϕ_{f} denote the line impedance amplitude and angle, respectively. It follows that the i-th module delivers the active and reactive power

$$P_i = \sum_{k=1}^{N} \frac{3V_k V_i}{2Z_{\mathrm{f}}} \cos(\delta_k - \delta_i - \phi_{\mathrm{f}}) - \frac{3V_{\mathrm{g}} V_i}{2Z_{\mathrm{f}}} \cos(-\delta_i - \phi_{\mathrm{f}}), \tag{18a}$$

$$Q_i = -\sum_{k=1}^{N} \frac{3V_k V_i}{2Z_{\mathrm{f}}} \sin(\delta_k - \delta_i - \phi_{\mathrm{f}}) + \frac{3V_{\mathrm{g}} V_i}{2Z_{\mathrm{f}}} \sin(-\delta_i - \phi_{\mathrm{f}}). \tag{18b}$$

Insertion of (18a) into $\dot{\delta} = -(2\eta/(3V_k^2))(P_k - P_k^\star)$ gives the angle dynamics

$$\dot{\delta}_i = -\frac{2\eta}{3V_i^2} \left(\sum_{k=1}^{N} \frac{3V_k V_i}{2Z_{\mathrm{f}}} \cos(\delta_k - \delta_i - \phi_{\mathrm{f}}) \; - \frac{3V_{\mathrm{g}} V_i}{2Z_{\mathrm{f}}} \cos(-\delta_i - \phi_{\mathrm{f}}) - P_i^\star \right). \tag{19}$$

To obtain a small-signal model for the i-th inverter angle, we linearize (19) as

$$\dot{\widetilde{\delta}}_i = \frac{\eta}{V_i Z_{\mathrm{f}}} \left(\sum_{\substack{k=1 \\ k \neq i}}^{N} V_k \sin(\delta_i - \delta_k + \phi_{\mathrm{f}}) - V_{\mathrm{g}} \sin(\delta_i + \phi_{\mathrm{f}}) \right) \widetilde{\delta}_i - \frac{\eta}{V_i Z_{\mathrm{f}}} \sum_{\substack{k=1 \\ k \neq i}}^{N} V_k \sin(\delta_i - \delta_k + \phi_{\mathrm{f}}) \widetilde{\delta}_k,$$

where $\widetilde{\delta}_i$ represents a small-signal perturbation in δ_i. This is rewritten in matrix to obtain $\dot{\widetilde{\delta}} = (\eta/Z_{\mathrm{f}}) A \widetilde{\delta}$, where $\delta = [\delta_1, \delta_2, \ldots, \delta_N]^\top$ is the state vector and the state matrix A is

$$A = \begin{bmatrix} \sum_{\substack{k=1 \\ k \neq 1}}^{N} \xi_{1k} - \xi_1 & -\xi_{12} & \cdots & -\xi_{1N} \\ -\xi_{21} & \sum_{\substack{k=1 \\ k \neq 2}}^{N} \xi_{2k} - \xi_2 & \cdots & -\xi_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ -\xi_{N1} & -\xi_{N2} & \cdots & \sum_{\substack{k=1 \\ k \neq N}}^{N} \xi_{Nk} - \xi_N \end{bmatrix}. \tag{20}$$

We define ξ_{ik} and ξ_i in (20) as

$$\xi_{ik} := \frac{V_k}{V_i} \sin(\delta_i - \delta_k + \phi_{\mathrm{f}}), \quad \xi_i := \frac{V_{\mathrm{g}}}{V_i} \sin(\delta_i + \phi_{\mathrm{f}}). \tag{21}$$

The Gershgorin discs for A are defined as $\{z \in \mathbb{C} : |z - a_{ii}| \leq \sum_{\substack{j=1 \\ j \neq i}}^{N} |a_{ij}|\}, \quad i = 1, 2, \ldots N$. Every eigenvalue of A will be located within the union of the above discs, denoted as

$$G(A) := \bigcup_{i=1}^{N} \{z \in \mathbb{C} : |z - a_{ii}| \leq \sum_{\substack{j=1 \\ j \neq i}}^{N} |a_{ij}|\}.$$

If under all operating conditions, $G(A)$ is shown to lie entirely within the left-half plane (LHP), a sufficient condition of stability for the i-th module, where $i \in \{1,2,\dots N\}$, is

$$|\lambda_i - a_{ii}| \leq \sum_{\substack{j=1 \\ j\neq i}}^{N} |a_{ij}| \Rightarrow -\sum_{\substack{j=1 \\ k\neq i}}^{N} |a_{ij}| \leq \lambda_i - a_{ii} \leq \sum_{\substack{j=1 \\ k\neq i}}^{N} |a_{ij}|.$$

Assuming equal module voltages such that $V_j \approx V_k \approx V_{\rm g}/N$, we use ξ_{ij} and ξ_i from (21) to obtain the following stability criterion:

$$2\sum_{\substack{k=1 \\ k\neq i}}^{N} |\sin(\delta_i - \delta_k + \phi_{\rm f})| \leq N \sin(\delta_i + \phi_{\rm f}) \tag{22}$$

Stability and Control Parameter Selection: The dVOC controllers are simultaneously responsible for module-level power tracking and system-level synchronization. Assuming equal reactive power references such that $Q_i^\star = Q_j^\star, \forall\, i,j \in \{1,N\}$, it follows from (5a) that all module voltages are equal and $V_i = V_j \approx V_{\rm g}/N, \forall\, i,j \in \{1,N\}$. Furthermore, since the voltage dynamics are significantly faster than the angle dynamics, we can decouple the voltage dynamics from the angle dynamics to simplify (19) as

$$\dot{\delta}_i = -\frac{\eta}{Z_{\rm f}}\left(\sum_{k=1}^{N} \cos(\delta_k - \delta_i - \phi_{\rm f}) - N\cos(-\delta_i - \phi_{\rm f}) - P_i^\star\right). \tag{23}$$

Under small values of δ_i in (23), the effective bandwidth of the system is

$$\omega_{\rm dVOC} = \frac{\eta N}{Z_{\rm f}\sqrt{2}}. \tag{24}$$

Stability of (5a) necessitates $\mu, \eta > 0$ since V_k is positive. Moreover, since we need timescale separation between $\omega_{\rm dVOC}$ and $\omega_{\rm QAB}$, it implies

$$\omega_{\rm dVOC} \ll \omega_{\rm QAB} \rightarrow \frac{\eta N}{Z_{\rm f}\sqrt{2}} \ll \frac{k_{\rm i,dc}}{k_{\rm p,dc}}. \tag{25}$$

PV Dc-Link Control:

State Equations: The PI controller in (9) regulates $v_{{\rm pv},k}$. To cast (8)–(9) into the singular perturbation framework, we define two new states as

$$e_{1,k} = v_{{\rm pv},k} - v_{{\rm pv},k}^\star, \qquad e_{2,k} = C_{\rm pv}\int_0^\tau e_{1,k}\, d\sigma + e_{2,k}(0),$$

where $\tau = t/C_{\rm pv}$ is the new time variable for the fast mode. We follow similar analysis as the dc-link control for the QAB to arrive at the following design guidelines:

$$k_{\rm p,pv} \geq I_{\rm sc}, \tag{26a}$$

$$\max\left(\frac{1}{C_{\rm pv}}\frac{k_{\rm p,pv} - I_{{\rm pv},k}}{V_{{\rm pv},k}}, \frac{1}{C_{\rm pv}}\left(\frac{1}{r_{{\rm pv},k}} + \frac{k_{\rm p,pv}}{V_{{\rm pv},k}}\right)\right) \ll \omega_{\rm dVOC}, \tag{26b}$$

$$\max\left(\frac{k_{\rm i,pv}}{k_{\rm p,pv} - I_{{\rm pv},k}}, \frac{k_{\rm i,pv}}{k_{\rm p,pv}}\right) \ll \min\left(\frac{1}{C_{\rm pv}}\frac{k_{\rm p,pv} - I_{\rm pv}}{V_{{\rm pv},k}}, \frac{1}{C_{\rm pv}}\left(\frac{1}{r_{{\rm pv},k}} + \frac{k_{\rm p,pv}}{V_{{\rm pv},k}}\right)\right). \tag{27}$$

Maximum Power Point Tracking:

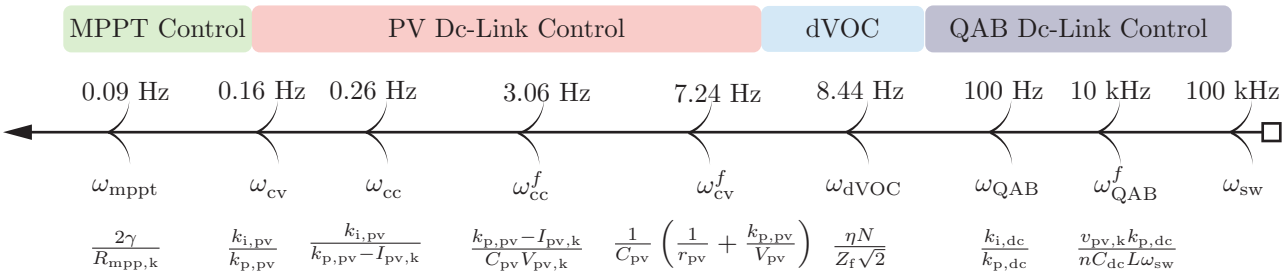


Figure 16: The various timescale-separated controllers are shown with their respective control bandwidths that are designed through singular perturbation approach.

State Equations: The MPPT controller in Fig. 15 uses $i_{\mathrm{pv},k}$ and $v_{\mathrm{pv},k}$ to determine the voltage reference $v^{\star}_{\mathrm{pv},k}$ for the PV dc-link regulator. Substitute the plant model in (10) into the MPPT integral control law in (11) to obtain

$$\dot{v}^{\star}_{\mathrm{pv},k}=\gamma\frac{\partial(v_{\mathrm{pv},k}i_{\mathrm{pv},k})}{\partial v_{\mathrm{pv},k}}=\gamma(v_{\mathrm{pv},k}\frac{\partial(i_{\mathrm{pv},k})}{\partial v_{\mathrm{pv},k}}+i_{\mathrm{pv},k})=-2\frac{\gamma}{R_{\mathrm{mpp},k}}v_{\mathrm{pv},k}+2\gamma I_{\mathrm{mpp},k}.$$

Stability and Equivalent Model: Fast inner control ensures $v_{\mathrm{pv},k}=v^{\star}_{\mathrm{pv},k}$ such that the MPPT law simplifies into

$$\dot{v}^{\star}_{\mathrm{pv},k}=-2\frac{\gamma}{R_{\mathrm{mpp},k}}v^{\star}_{\mathrm{pv},k}+2\gamma I_{\mathrm{mpp},k}.$$

The equivalent bandwidth of the MPPT loop becomes $\omega_{\mathrm{mppt}}=2\gamma/R_{\mathrm{mpp},k}$ and the corresponding stability condition that enforces timescale separation is

$$2\frac{\gamma}{R_{\mathrm{mpp},k}}\ll\min\left(\frac{k_{\mathrm{i,pv}}}{k_{\mathrm{p,pv}}-I_{\mathrm{pv}}},\frac{k_{\mathrm{i,pv}}}{k_{\mathrm{p,pv}}}\right). \tag{28}$$

7 Exprimental Results for Cascaded PV-Powered Setup

We demonstrate cascaded converter operation with fully functional decentralized controls on a system of three series-connected modules across the grid and an output filter. Module #1 was fed by a solar array simulator whereas modules #2 and #3 were powered by a fixed dc supply. All converter modules are rated for equal power delivery and employ identical controllers with the exception that modules #2 and #3 do not have MPPT and PV dc-link controllers due to their fixed dc inputs. To carry out decentralized control, each module in Fig. **??**(b) has its own control board that controls the QAB and three single-phase inverters. Each control board uses a TI-TMS280379D microcontroller. Given that the dVOC controller lies at the epicenter of several potentially competing requirements, we choose its parameters (i.e., μ and η) first among all the controllers. From there, all other control designs emanate outwardly from the dVOC subsystem such that the stability and timescale separation guidelines in the aforementioned section is followed. Table 3 lists the relevant system parameters and control gains that enforce timescale separation. Fig. 16 collects the relevant bandwidths corresponding to each of the subsystems in decreasing order of frequency.

Start-up Procedure: To begin, a current-limiting resistor was added in series with the converters. Next, the inverters were effectively bypassed by turning on the lower MOSFETs of each ac-side H-bridge. As seen on the left-hand side of Fig. 17(a), a current flows through the stack of bypassed converters that can be sensed by each module. This allows each inverter to synchronize its

Table 3: System parameters.

	Symbol	Description	Value	Units
Ac system	S_{rated}	module VA rating	3000	VA
	N	modules in series	3	
	V_{g}	rms line-neutral grid voltage	90	V
	ω_{nom}	rated frequency	60	Hz
	L_{f}	inductance	2.4	mH
	R_{f}	resistance	4.2	Ω
	μ	dVOC parameter I	1	$V^{-2}s^{-1}$
	η	dVOC parameter II	100	Ωs^{-1}
QAB dc-links	V_{dc}^{0}	nominal dc voltage	100	V
	ω_{sw}	switching frequency	100	kHz
	L	inductance	26	μH
	n	turns ratio	0.5	
	C_{pv}	input capacitance	660	μF
	C_{dc}	dc-link capacitance	200	μF
	$k_{\text{p,dc}}$	proportional gain	2.05	Ω^{-1}
	$k_{\text{i,dc}}$	integral gain	1290	$(\Omega\text{s})^{-1}$
MPPT & PV	V_{oc}	open- circuit voltage	200	V
	I_{sc}	short- circuit current	4.0	A
	V_{mpp}	MPP voltage	160	V
	I_{mpp}	MPP current	3.0	A
	$k_{\text{p,pv}}$	proportional gain	6	A
	$k_{\text{i,pv}}$	integral gain	6.53	As^{-1}
	γ	MPPT gain	0.01	V/V
Bandwidth	ω_{QAB}^{f}	QAB fast mode	10	kHz
	ω_{QAB}	QAB slow mode	100	Hz
	ω_{dVOC}	dVOC	8.44	Hz
	ω_{cc}^{f}	CCR-PV fast mode	3.06	Hz
	ω_{cv}^{f}	CVR-PV fast mode	7.24	Hz
	ω_{cc}	CCR-PV slow mode	0.26	Hz
	ω_{cv}	CVR-PV slow mode	0.16	Hz
	ω_{mppt}	MPPT control	0.09	Hz

dVOC-based controller and begin switching with zero power commands (i.e., $P_k^\star = 0, k \in \{1,2,3\}$). Thereafter, the dVOC modulates each inverter and power command tracking is eventually reached such that $P_k = 0, k \in \{1,2,3\}$. At this point, the modules have achieved communication-free synchronization as shown by the aligned voltage waveforms in Figure 17(b). The modest line current that remains is purely reactive and is due to small line voltage drops and mismatches between the grid voltage and commanded values.

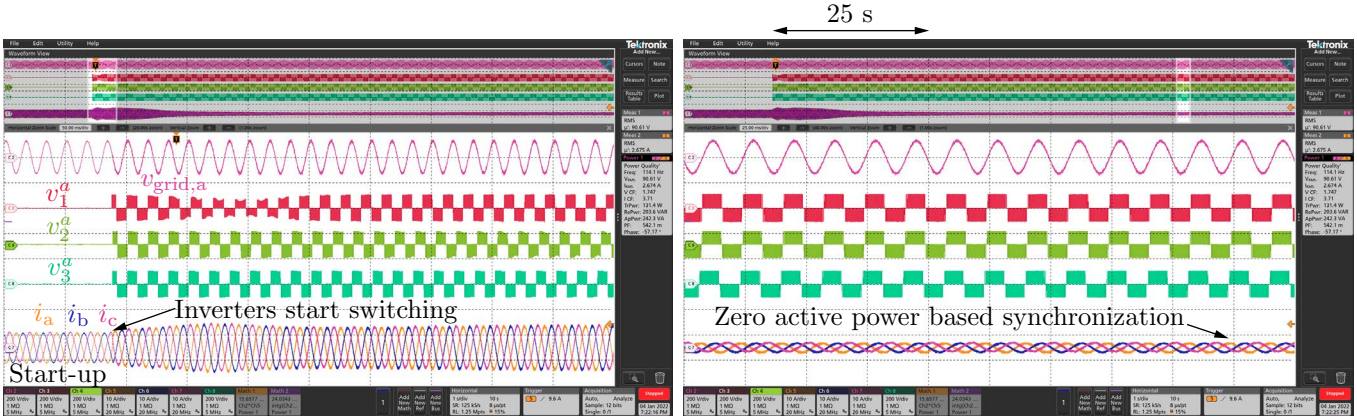
Nominal Operation: Power from modules #2 and #3 climb up to 200 W over one second after the modules have synchronized. As seen in Fig. 18(a), dc-side currents $i_{\text{pv},2}$ and $i_{\text{pv},3}$ increase to accommodate active power tracking such that $P_k = P_k^\star, k \in \{2,3\}$. Module #1 power reference, $P_1^\star$, originates from the upstream PV dc-link controller, which is in turn controlled by the MPPT control law. Power tracking in module #1 implies $P_1 = P_1^\star$ which ensures PV dc-link voltage regulation where $v_{\text{pv},1} = v_{\text{pv},1}^\star$. Thereafter, the MPPT controller continuously nudges $v_{\text{pv},1}^\star$ until the maximum power point is reached at $v_{\text{pv},1} = V_{\text{mpp}}$. While PV power ramps up, as depicted in Fig. 18(a), $i_{\text{pv},1}$ approaches I_{mpp} and output power becomes $P_1 \approx P_1^\star = P_{\text{mpp}}$. Zoomed in steady-state waveforms show a few ac cycles in Figure 18(b). Phase a line-neutral voltages for all three modules and the grid are plotted. Switched module voltages, $v_k^a, \forall k \in \{1,2,3\}$, appropriately lead the grid waveform to ensure $P_k = P_k^\star, k \in \{1,2,3\}$.

The power reference for module #1 oscillates around its MPP of 480 W while the reference for the other two modules are fixed at 200 W. This is reflected in the equal phase shifts of switched voltages v_2^a and v_3^a and the larger phase shift of v_1^a relative to the grid. All three modules have the same reactive power reference, $Q_1^\star = Q_2^\star = Q_3^\star = 0$. However, the dVOC droop characteristic does not guarantee perfect reactive power tracking since voltage is a local quantity. Hence, the waveforms in Fig.18(b) do imply some reactive power transfer.

To evaluate QAB dc-link voltage regulation, refer to Fig. 19(a) which shows module #1 input voltage, $v_{\text{pv},1}$, and its trajectory from V_{oc} to V_{mpp}. Correspondingly, the phase a floating dc link voltage, $v_{\text{dc},1}^a$, tracks $n\,v_{\text{pv},1}$. For the other two modules with fixed voltage inputs, the floating dc link voltages on phase a are held steady such that $v_{\text{dc},2}^a = v_{\text{dc},3}^a$. The floating dc link voltages on phases b and c are identical to the phase-a waveform for each respective module and are hence omitted. Inspection of the voltages in Fig. 19(b) reveals a second harmonic that is typical for single-phase power transfer. These pulsating components cancel once summed on the QAB primary input. However, the switching frequency harmonics of QAB and its multiples thereof still remain in the system and can be seen in Fig. 18(a) as the background high-frequency noise in $i_{\text{pv,k}}\ \forall\, k \in \{1,2,3\}$.

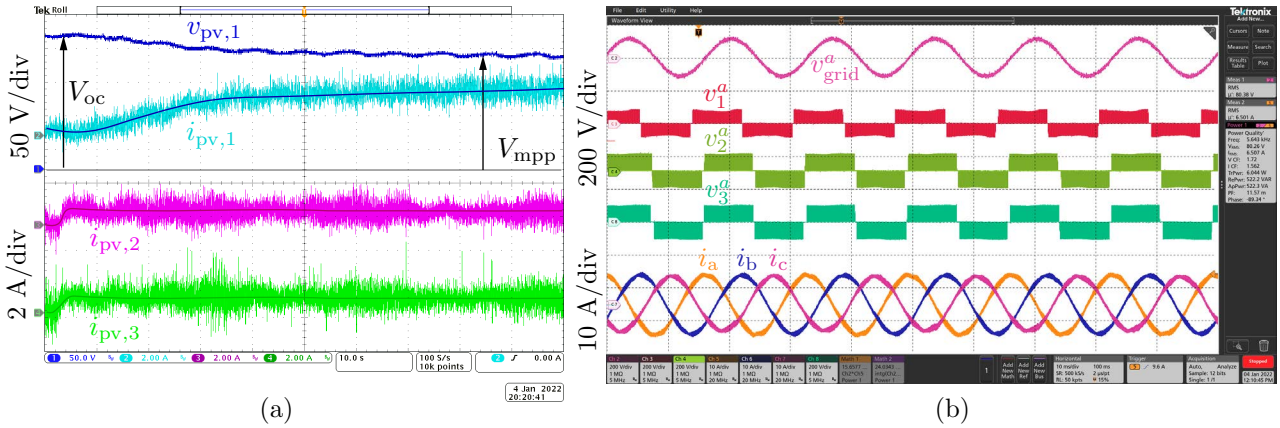
Response Under Dynamic Power-sharing: We now illustrate the ability of the proposed module-level control structure to preserve intended operation despite time-varying operating conditions in the remaining series-connected modules. Towards that end, we induce a $200\,\text{W} \rightarrow 300\,\text{W}$ power reference step change in modules #2 and #3, and observe the response of module #1. As shown in Fig. 20, module #1 is able to maintain MPPT operation and the overall system remains stable.

We next demonstrate the stability of the cascaded system for a step change in PV power of module #1. Fig. 22(a) and (c) shows the steady-state MPP operation at the two curves described in Table 4. In Fig. 22(b) we capture the transients when we suddenly switch from PV curve-A to PV curve-B whereas Fig. 22(d) shows repeated transitions between PV-curve A and B. Note that the fast transients in $v_{\text{pv},1}$ and $i_{\text{pv},1}$ are quickly damped out by the stable MPPT controller. Modules #2 and #3 continue to be regulated at $P_k = 200\,\text{W},\ k \in \{2,3\}$ and are able to maintain stable operation during the PV transients in module #1. Fig. 23(a) and (b) illustrates the corresponding steady-state ac-side waveforms corresponding to PV curve-A and PV curve-B, respectively. Higher power operation in Fig. 23(b) is characterized by larger ac-side currents and greater phase-shift between



(a) (b)

Figure 17: Startup transients show three series-connected modules synchronizing to the ac grid without external communication. The modules are synchronized with zero active power transfer to the grid after 25 seconds. A small reactive component remains due to a mismatch between the grid voltage and sum of commanded voltages.



(a) (b)

Figure 18: Experimental results show performance of subsystems within each module for three converters connected in series across a stiff grid. MPPT integral control action for module #1 occurs across the slowest timescale where it is evident in (a) that the operating point moves from open circuit to the MPP. Modules #2 and #3 show stable operation with constant dc power. In (b), we zoom in on a few ac cycles of the phase-a voltages produced by the modules and grid. Along with the regulated three-phase currents, these ac waveforms collectively show proper operation of the other controllers along with dVOC.

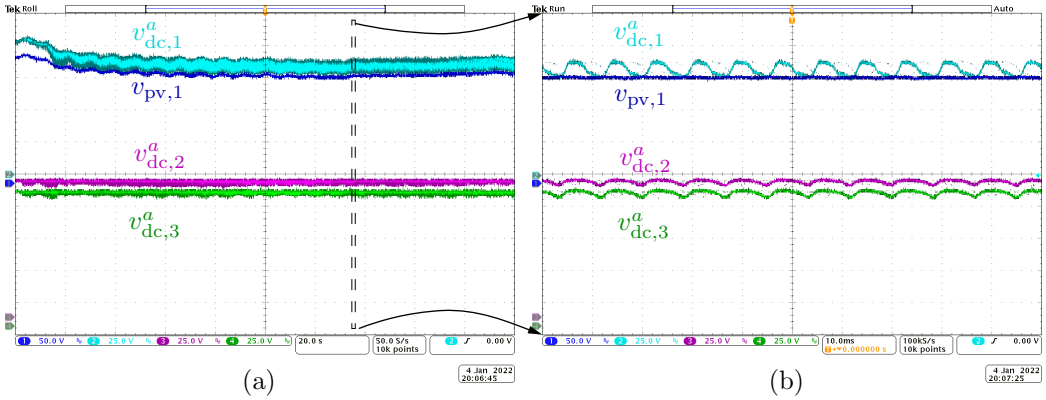


Figure 19: Experimental results in (a) illustrate regulation of phase-a QAB floating dc-link voltages in modules #1, #2, and #3. Module #1 input voltage shows a transition from the open circuit to MPP voltage. The second harmonic ripple in (b) is due to single-phase power delivery.

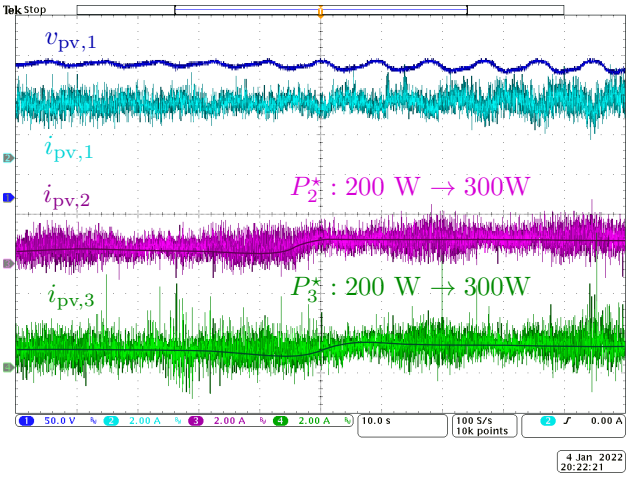


Figure 20: Experimental results for steady operation around the MPP for module #1 during a ramp change in $P^\star_2$ and $P^\star_3$.

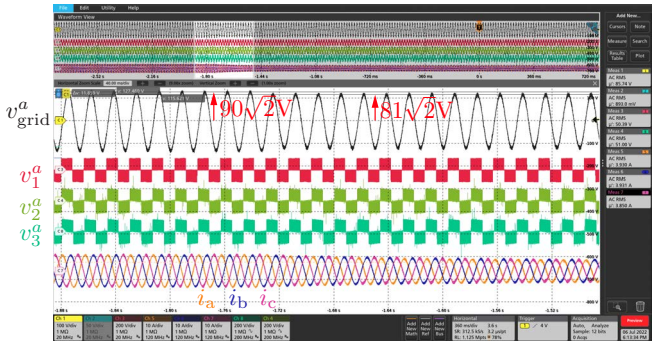


Figure 21: The series-connected converter set-up is shown to ride-through a 10% under-voltage condition. As the grid voltage reduces, the reactive power drops resulting in smaller ac-side currents.

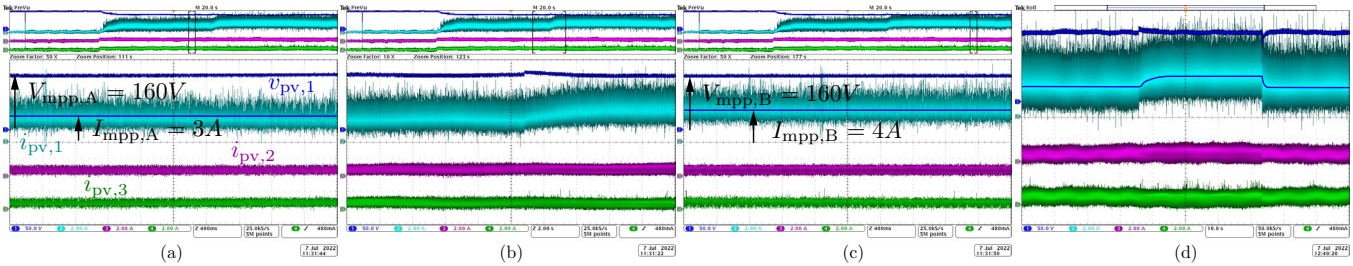


Figure 22: Experimental results show the robustness of the cascaded set-up when PV power is suddenly changed. Steady state operation at the two PV curve-A and PV curve-B appearing in Table 4 is shown in (a) and (c) respectively. In (d) we show the ability of system to undergo successive transitions between the two PV curves and we zoom on one such transition in (b).

Figure 23: The ac-side waveforms for the low insolation PV curve-A and high insolation PC curve-B is shown in (a) and (b) respectively. The different power level is reflected in the ac-side currents and phase-shift between phase-a grid voltage and corresponding ac-side voltage of module #1.

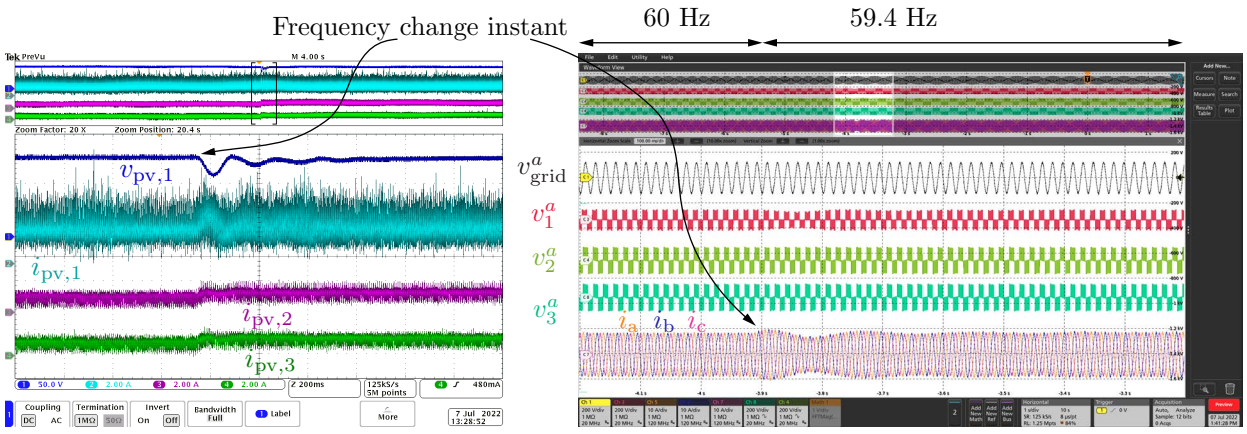
the switched-voltage v^a_1 and v^a_{grid} compared to low insolation operation in Fig. 23(a).

Table 4: PV curves

Curve	V_{mpp}	V_{oc}	I_{mpp}	I_{sc}	Comments
A	160 V	200V	3 A	5 A	lower insolation
B	160 V	200V	4 A	6 A	higher insolation

Nonideal Ac-Side Conditions: To validate grid-forming functionality, we study low-voltage and under-frequency ride-through performance of the cascaded connection. We also report the current and voltage total harmonic distortion (THD) of the two operating points shown in Table 4. When the grid voltage is reduced from the nominal value of 90 V to 81 V in RMS, the volt-Var droop causes each module to reduce its reactive power output. This is reflected in the lower ac-side currents as shown in Fig. 21.

The under-frequency response is shown in Fig. 24 where the grid-simulator suddenly changes its ac frequency from 60 Hz to 59.4 Hz. In Fig. 24(a), modules #2 and #3 operated from a fixed voltage source can be seen to increase their dc currents. This is due to their dVOC-based ac-side control that forces an increase in active power output to restore the system frequency. However, module #1 continues to operate at the fixed MPP, and only sees a brief transient during the frequency change that is stabilized by the PV controllers. These transients are reflected in their respective ac-side waveforms shown in Fig. 24(b) where we have zoomed in on the instant of



(a) (b)

Figure 24: Grid-forming operation is verified when the grid frequency is suddenly changed from 60 Hz to 59.4 Hz. Module #1 connected to the PV input continues to operate at MPP. Modules #2 and #3 with constant dc-input voltage, slightly increase their power output in accordance to their droop law.

frequency change.

The voltage THD was recorded as 0.554% and 0.858% at MPP curves A and B respectively. The current THD is calculated using specifications in IEEE standard 519-2014 as shown in Table 5. A Yokogawa WT5000 power analyzer was used to record these measurements. All THD measurements are well below the recommended standards.

Table 5: Current harmonics of ac-side output current as percentage

	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
IEEE 519-2014	4.0	2.0	1.5	0.6	0.3	5.0
Low Insolation (A)	0.95	0.2	0.24	0.28	0.07	1.29
High Insolation (B)	1.4	0.09	0.1	0.28	0.04	1.64

8 Medium-voltage prototype performance: NREL prototype

The experimental prototype of the dc-to-three-phase system is shown in Fig. 25. The prototype consists of 7 modules, each of which contains one primary board, three secondary boards, and planar magnetics. Each primary and secondary board contains a dedicated microcontroller. Each primary board contains a primary-side bridge of the QAB while each secondary contains a secondary-side bridge of the QAB and a H-bridge inverter.

Communication between the primary and secondaries of each module is achieved with optical cables. There are also additional communication channels between the primaries of each module achieved through BNC and LAN connections. The signaling includes:

1. synchronization pulses at $200\,\text{kHz}$ from the primary to each secondary in a module to help facilitate the phase-shift control of the module's QAB. This signal is communicated locally within one module.

2. synchronization pulses at $60\,\text{Hz}$ for setting power references for the secondaries and to facilitate synchronization with the grid. This signal is communicated globally amongst all modules.

3. synchronization pulses at $10\,\mathrm{kHz}$ to facilitate PWM interleaving of the series stacked H-bridge inverters. This signal is communicated globally amongst all modules.

4. Voltage references are sent from the primary to each secondary in a module to also help facilitate the phase-shift control of the module's QAB. This signal is communicated locally within one module via the Controller Area Network (CAN) communication protocol.

Tests have been successfully performed on up to four input parallel output series connected modules on this seven module prototype and operation has been validated. Fig. 26 shows ac voltages and currents generated for a three-phase resistive load by the system during steady-state operation. The system successfully delivers balanced three phase power to the load. It is also noted that the $10\,\mathrm{kHz}$ PWM interleaving successfully cancels switching ripple in the output current, generating high quality voltage and current waveforms.

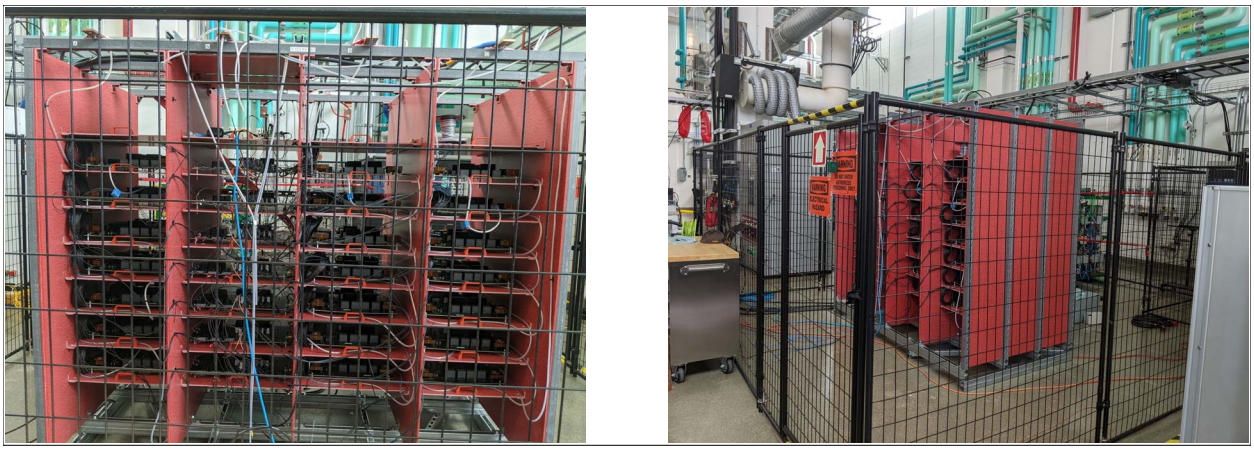


Figure 25: Fully assembled MV rack housing 7 modules consisting of primary, magnetics, and secondary boards.

9 Levelized Cost of Energy-Oriented System Optimization of the Novel Power Electronics Architecture

we summarize the achievements regarding LCOE optimization works accomplished in the project. First, the LCOE improvement approach used to make the design optimization tractable is explained. Based on the LCOE improvement approach that allows for evaluating the value of a new technology by comparing major differences while assuming other design components are the same (reducing the burden to estimate the LCOE of a new technology), the efficiency and cost models are developed. To model the key differences along with the new power electronics architecture that will impact the system LCOE, impacts of the modular power conversion on the system-level aspects, i.e., losses and costs are analyzed and factored into the system model. To derive the PV system design optimization with high computation efficiency with highly detailed system model parameters, the genetic algorithm has been employed. With the loss and cost models and seven design parameters, the genetic algorithm derived a set of design parameters to maximize the LCOE improvement that yields 5.5% less LCOE than a conventional 200 kW PV generation system with state-of-the-art practices. Below are the more details.

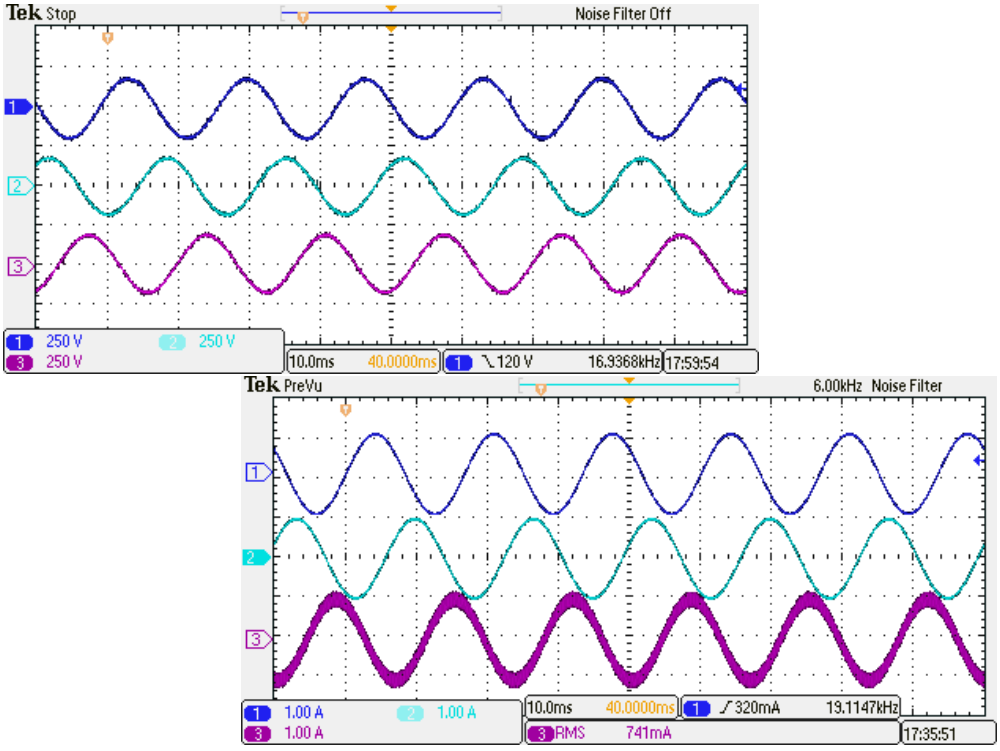


Figure 26: Experimental results for 4 series modules conducted at NREL with inverter modulation index set to 0.2. The Phase A, B, C voltages (Va, Vb, and Vc) are shown in (a). The Phase A, B, C currents (Ia, Ib, and Ic) are shown in (b)Proper phase interleaving is validated by the absence of switching ripple on the voltages and currents.

LCOE improvement approach: The project team used a LCOE *improvement* model that captures the key differences of a PV system with the C2 blocks from conventional approaches such as central inverters. Using the improvement model, one can compare the proposed direct medium-voltage-interfaced PV generation system to current state-of-the-art practices and quantify reductions in LCOE. We outlined the basis of our so-called *LCOE-improvement model* with the baseline LCOE of an established technology as:

$$\mathrm{LCOE} = \frac{C_0 + \sum_{t=1}^{t=T} \frac{C_t}{(1+i)^t}}{8760 \cdot P_{\text{rated}} \cdot \gamma \cdot \left(\sum_{t=1}^{t=T} (1-\delta)^{t-1}\right)} \tag{29}$$

where t is time in years, T is the lifetime of the PV system in years, C_0 is the initial investment cost, C_t is cost incurred at year t, i is the interest rate per period, δ is the PV module degradation factor, e.g., 0.8%/year, P_{rated} is the power plant capacity in watt, and $\gamma = c_t \cdot \eta_{PC}$ is the scaling factor, which is the ratio of actual electricity output over a year to the maximum possible output. c_t, capacity factor of a system, depends on geographical location (irradiance and temperature profile) and, in general, ranges from 0.1 to 0.4. η_{PC} is to represent power conversion efficiency from PV output to AC transmission to detail the inverter performance. To represent LCOE of a new system with key differences modeled with baseline values (with the bar in the equation), (29) can be modified as:

$$\mathrm{LCOE}_{\text{new}} = \frac{(\bar{C}_0 - \Delta C_0) + \sum_{t=1}^{t=T} \frac{C_t}{(1+i)^t}}{8760 \cdot P_{\text{rated}} (\bar{\gamma} + \Delta\gamma) \left(\sum_{t=1}^{t=T} (1-\delta)^{t-1}\right).} \tag{30}$$

where ΔC_0 and $\Delta\gamma$ are cost and efficiency improvements, respectively, of the proposed design. After neglecting second order terms, (30) can be approximated as the sum of two factors

$$\mathrm{LCOE}_{\mathrm{new}} \approx \overline{\mathrm{LCOE}} - \frac{\Delta C_0}{\bar{E}_{life}} - \overline{\mathrm{LCOE}}\frac{\Delta\gamma}{\gamma}. \tag{31}$$

Finally, we define the LCOE *improvement* factor as

$$\frac{\Delta\mathrm{LCOE}}{\overline{\mathrm{LCOE}}} \approx \frac{\Delta C_0}{\bar{E}_{\mathrm{life}}\overline{\mathrm{LCOE}}} + \frac{\Delta\gamma}{\bar{\gamma}} \tag{32}$$

where $\Delta\mathrm{LCOE} = \overline{\mathrm{LCOE}} - \mathrm{LCOE}_{\mathrm{new}}$. This improvement model simplifies burden in system modeling and significantly improves tractability of the problem since it allows us to isolate the factors which impact LCOE. Incorporating the loss (efficiency) and LCOE data of a baseline approach and improvement factors into (32), the potential improvement in LCOE of a new technology can be computed. More details of this work can be found in the previous reports submitted in BP1.

C2 System modeling: To capture the key differences in power conversion resulting from the C2 architecture and their resultant impacts on the system-level aspects including electrical balance of system (BOS) cost, the team constructed models for major inverter components, i.e., semiconductor switches and magnetics, and their effects on cost. The team modeled the power conversion loss and cost of semiconductor switches—incorporating effect of rated voltage and rated current capacity—and magnetic devices—incorporating effect of volume in different operating conditions. And then, we incorporated individual models into the system model to allow for comparing system-level efficiency and cost differences with the baseline system with conventional inverters in different design parameters including number of modules and the other design values. Finally, with the component and system-level modeling, LCOE improvement with different design parameters can be derived. Figure 27 shows a result obtained from the system model. As shown, the system LCOE improvement changes with design parameters varying in the design spaces, implying that a design optimization can derive the maximum improvement, balancing the cost and loss. In addition, one can get system-level understanding from the system model with parameter sweep, hinting optimal design direction from trade-offs, e.g., impact of number of modules on system performance and thus LCOE.

In addition to the modeling directly related to the power conversion architecture, the team also modeled the system-level impact from the C2 system. Savings in electrical balance of system (e-BOS) cost can be significant due to simplified interconnections, elimination of dc combiner boxes, and reduce wiring costs associated with medium-voltage cabling. Improved maintenance cost also offers lifetime cost reduction, and uninterruptible operation during block-level failures ensures continued energy harvest.

The team derived breakdown of e-BOS for a 200 kW PV system which is shown in Figure 28. As shown, components can be categorized into three types; Category A: wires including dc and ac cables that would be significantly changed in C^2 architecture, Category B: components for interconnection such as dc combiner boxes and ac panels that can be potentially removed by merging their functions into inverters, and Category C: others that may remain the same, regardless of architecture. It is noted that Category A accounts for 60%, Category B 7%, and Category C 33%, implying significant improvement opportunity in e-BOS with C^2 system.

To estimate savings from reduced wiring needs, a conventional 5 MW PV system was used as a baseline for a case study. This baseline system has 40 125 kW string inverters, each of which covers 13 to 15 strings with a dc combiner box. See details in the report of BP2Q4. In the proposed scenario, we envision i) C^2 modules replace dc combiner boxes, ii) replace lengthy

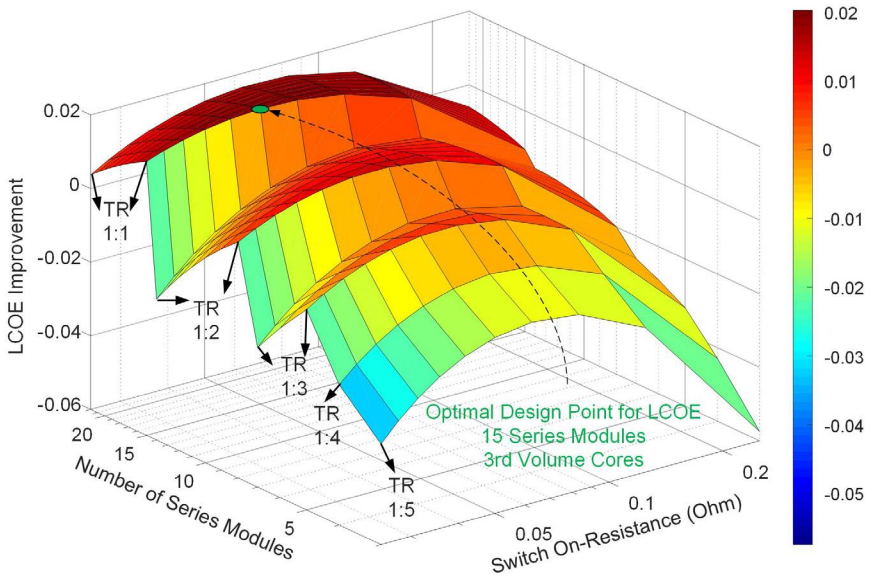


Figure 27: LCOE improvement with different number of modules and switch on-resistances at fixed core volume, $k_{\text{core}} = 3$.

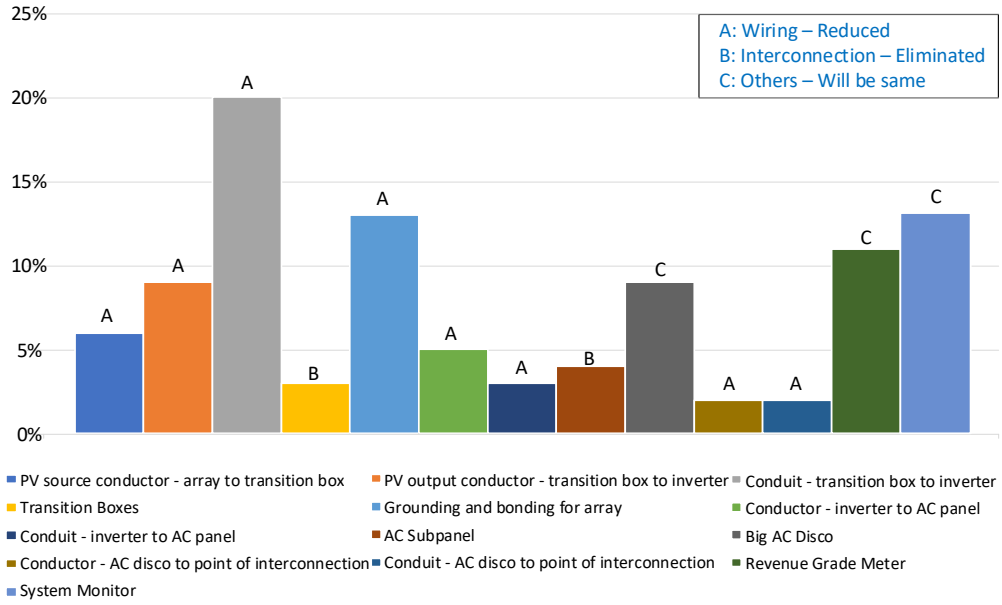


Figure 28: Electrical balance of system cost reduction breakdown for a 200 kW C^2 PV system.

2 kV dc wire runs with medium-voltage ac wires, and iii) remove ac panels as well as the step-up line transformer since medium voltage is provided directly. As illustrated in Fig. 29, 16 series-connected C^2 modules generate 13.8 kV without a bulky line transformer. Based on the envisioned physical configuration, the computed cost savings are in Figure 30. In summary, the e-BOS can be reduced to 69% of its original value. This follows from an approximately 40% reduction in wiring costs and elimination of Category B costs. Though the actual reduction would be different between particular systems, we programmed this estimate into the optimization framework for simplicity with the understanding that the baseline may represent many conventional system types. The team

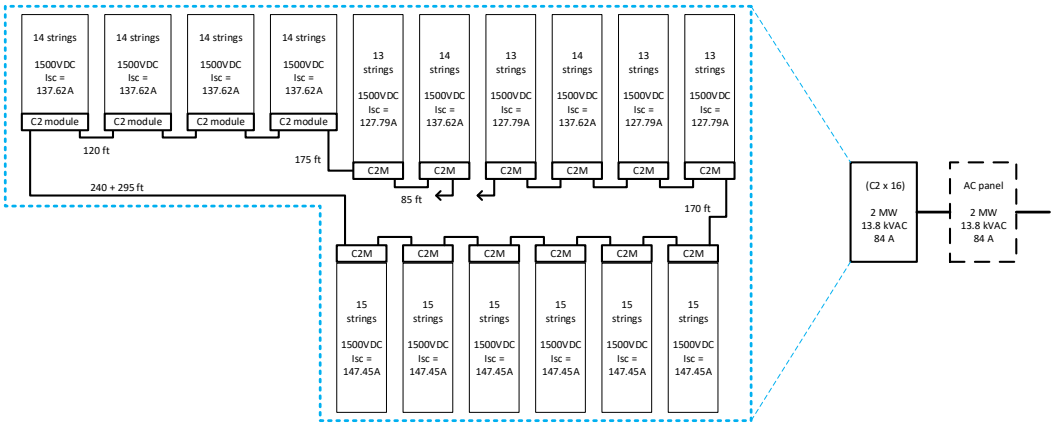


Figure 29: C^2 system that highly simplifies the collection system by eliminating dc combiner boxes and ac panels and having much simplier, and cost-saving direct dc-to-medium-voltage collection.

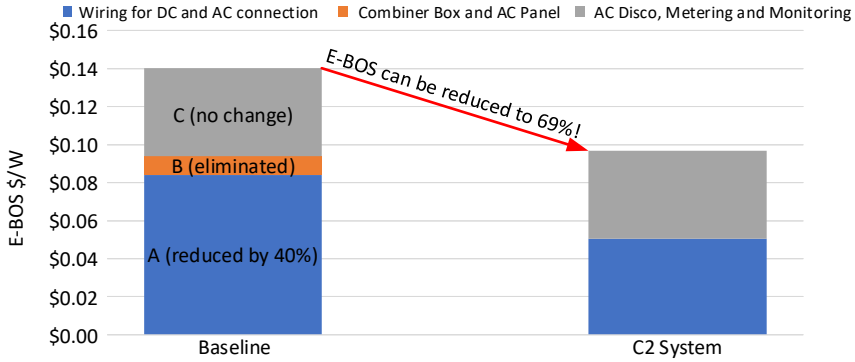


Figure 30: E-BOS reduction estimate. C^2 system is expected to reduce e-BOS cost to 69% comparing to the conventional configuration of the 2MW benchmark.

also evaluated the C^2 approach against other conventional such as string inverters. Among the configurations, we found the configuration in Fig. 29 is most beneficial in cost reduction.

LCOE-oriented design optimization framework: With the increasing number of design values to detail the system, the team developed a design optimization engine based on genetic algorithm to make the design optimization computationally efficient. Emulating the evolution process going through multiple generations (iterations), the design optimization can find an optimal design values with a reasonable computation requirement. Figure 31 summarizes the optimization process used in this project.

Design optimization and LCOE improvement with C2 architecture: With the efforts summarized above, the team estimated the potential LCOE improvement with the new modular power electronics architecture for a 200 kW PV farm. We ran the optimization engine with the latest models, and the results are tabulated in Table 6. The optimization engine implies the C^2 system can achieve 5.5% LCOE improvement with all models including eBOS improvement. Note that it is 2.5% higher than that without the cost. This is mainly due to e-BOS reductions and an optimized system rating. This LCOE improvement estimation underscores key advantages of the proposed architecture.

Discussion: We discuss about contributions of different system elements to the LCOE im-

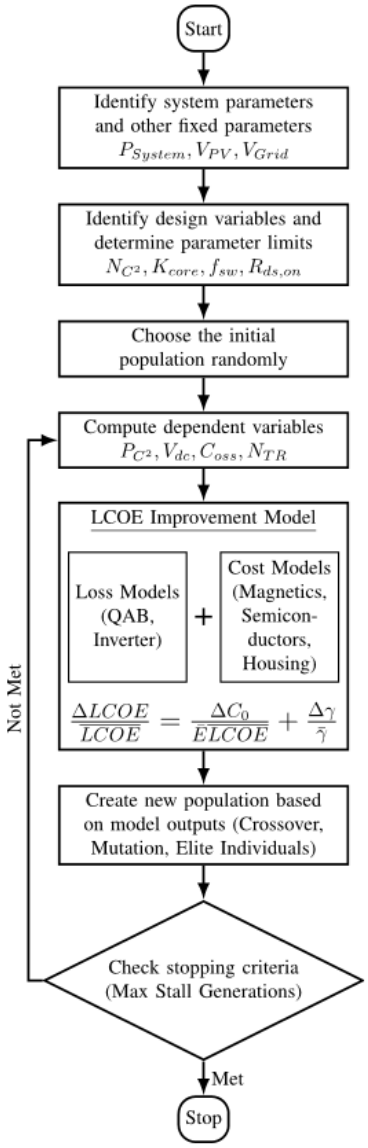


Figure 31: LCOE-oriented design optimization.

provement.

- Improvement in power conversion, direct-LVDC-to-MVAC, eliminating 50/60 Hz line-frequency transformer with high power density and high efficiency ferrite transformer and allowing use of low-voltage-rated semiconductor switches and reduced filter components, can lead to LCOE improvements. In a case study for 200 kW system, about 3% LCOE improvement was estimated.
- Improvement in system construction, eBOS cost specifically, can lead additional LCOE improvement with elimination of combiners and reduced wire costs from streamlined and higher voltage-rated wiring structure. In the case study, 69% improvement in eBOS was expected, leading to 2.5 % LCOE improvement.

Impact: The outcome of this task will provide a realistic picture of cost reductions for the envisioned application of utility-scale systems by comparing the resultant potential improvements

Table 6: Comparison of Optimal Design Parameters for LCOE improvement: before and after updates on e-BOS and loss model.

	Imp	N_{C^2}	V_{tr} [cm^3]	V_{ind} [cm^3]	$R_{ds,pri}$ [mΩ]	$R_{ds,sec}$ [mΩ]	$R_{ds,inv}$ [mΩ]	f_{dab} [kHz]	f_{inv} [kHz]	P_{sys} [kW]
w/o eBOS	2.97%	16	596	196	94	335	191	126	33	200
w/ eBOS	5.5%	15	881	484	31	179	54	123	47	520

to the current industry practices. Accordingly, these modeled cost reductions will be relevant to industry stakeholders in the utility-scale PV industry. These results will eventually be presented to industry stakeholders in BP3. To ensure that the proposed design framework and accompanying cost models are realistic, the team is soliciting input from an industry advisory board.

8. Significant Accomplishments and Conclusions: This project has produced a multitude of breakthrough innovations. One key innovation is the creation of the first-ever medium-voltage-rated PCB-based planar transformer with Kapton interlayer dielectrics. This innovation could change the landscape of magnetics design for medium voltage converters. We have also developed high performance power electronics hardware as well as novel decentralized control schemes that eliminate single points of failure and ensure resilient/scalable operation.

9. Path Forward: This project has paved the way for upcoming innovations by allowing our team to create the first prototype of the C2 architecture. In follow-on projects, we hope to develop more efficient incarnations of the medium-voltage magnetics with custom-designed cores as well as other types of advanced soft-switching circuits. On the controls side, we intend to develop future projects looking at strategies for other applications such as fast electric vehicle chargers, SSTs, wind systems, and industrial loads.

10. Products: Intellectual Property:

- Patent Application #17/839,924, “Planar Transformers With Interleaved Windings And High Voltage Isolation”

Journal Publications:

- R Mallik, B Majmunović, S Dutta, GS Seo, D Maksimović, B Johnson, ”Control Design of Series-connected PV-powered Grid-forming Converters via Singular Perturbation” in IEEE Transactions on Power Electronics, April 2023.
- B. Majmunovic, S. Mukherjee, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimovic, ”1 kV, 10 kW SiC-Based Quadruple Active Bridge DCX Stage for a DC to Three-Phase AC Module,” in IEEE Transactions on Power Electronics, vol. 37, no. 12, Dec. 2022.
- Y. Son, Satyaki Mukherjee, R. Mallik, B. Majmunovic, S. Dutta, B. Johnson, D. Maksimovic, and G.-S. Seo, ”Levelized-Cost-of-Electricity-Oriented Modular String Inverter Design Optimization for PV Generation System Using Geometric Programming,” IEEE Access, vol. 10. 2022.
- P. Achanta, B. Johnson, G.-S. Seo, and D. Maksimovic, “A multilevel DC to three-phase AC architecture for photovoltaic power plants,” in IEEE Transactions on Energy Conversion , vol. 34, no. 1, pp. 181-190, March 2019.

Conference Publications:

- R. Mallik, B. Majmunovic, S. Mukherjee, S. Dutta, G.-S. Seo, D. Maksimovic, and B. Johnson, ”Lyapunov based generalized dc side controllers for PV connected systems,” ECCE, Detroit MI, Oct. 9-13, 2022.
- S. Dutta, B. Majmunovic, S. Mukherjee, R. Mallik, G.-S. Seo, D. Maksimovic, Brian Johnson, ”Grid-connected Self-synchronizing Cascaded Inverters with Autonomous Power Sharing,” ECCE, Vancouver, Canada, Oct. 10-14, 2021.
- S. Mukherjee, B. Majmunovic, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson and D. Maksimović “A High-Frequency Planar Transformer with Medium-Voltage Isolation” APEC, 2021.
- S. Dutta, B. Majmunovic, S. Mukherjee, R. Mallik, G.-S. Seo, D. Maksimović, Brian Johnson, “A Novel Decentralized PWM Interleaving Technique for Ripple Minimization in Series-Stacked DC-DC Converters” in APEC, 2021.
- S. Dutta, M. Lu, R. Mallik, B. Majmunovic, S. Mukherjee, G.-S. Seo, D. Maksimović, and Brian Johnson “Decentralized Control of Cascaded H-bridge Inverters for Medium-Voltage Grid Integration” in COMPEL, 2020.
- K. Goodrick, G.-S. Seo, S. Mukherjee, J. Roy, R. Mallik, B. Majmunovic, S. Dutta, D. Maksimovic, and B. Johnson, “LCOE Design Optimization Using Genetic Algorithm with Improved Component Models for Medium-Voltage Transformerless PV Inverters” in Proc. Energy Conversion Conference and Expo, 2020.
- B. Majmunovic, S. Mukherjee, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, and D. Maksimovic, “Soft Switching Over the Entire Line Cycle in a Quadruple Active Bridge-Based DC to Three-Phase Quadruple Active Bridge-Based DC to Three-Phase AC Module” APEC, 2020.
- S. Dutta, R. Mallik, B. Majmunovic, S. Mukherjee, G.-S. Seo, D. Maksimovic, B. Johnson, “Decentralized carrier interleaving in cascaded multilevel DC-AC converters” in Proc. Workshop on Control and Modeling of Power Electronics, 2019.
- S. Mukherjee, Y. Gao, R. Ramos, V. Sankaranarayanan, B. Majmunovic, R. Mallik, S. Dutta, G.-S. Seo, B. Johnson, D. Maksimovic, “AC Resistance reduction using orthogonal airgaps in high frequency inductors” in Proc. Workshop on Control and Modeling of Power Electronics, 2019.
- R. Mallik, B. Majmunovic, S. Mukherjee, S. Dutta, G.-S. Seo, D. Maksimovic, B. Johnson, “Equivalent Circuit Models of Voltage-controlled Dual Active Bridge Converters” in Proc. Workshop on Control and Modeling of Power Electronics, 2019.
- B. Johnson, M. Lu, V. Purba, S. Dhople, “A Circuit-equivalent Model forCurrent-controlled Grid-tied Inverters” in Proc. Workshop on Control and Modeling of Power Electronics, 2019.
- M. Lu, S. Dhople, B. Johnson, “A grid-compatible virtual oscillator controller” in Proc. Energy Conversion Conference and Expo, 2019.
- G.-S. Seo, J. Roy, S. Mukherjee, R. Mallik, B. Majmunovic, S. Dutta, D. Maksimovic, B. Johnson, “Levelized-cost-of-electricity-driven design optimization for medium-voltage transformerless PV converters” in Proc. Energy Conversion Conference and Expo, 2019.

Publicity:

- (Web article) Clean Energy Institute, UW, “Professor Brian B. Johnson Leads Department of Energy-Funded Research to Halve Cost of Solar Power Electronics,” Link.
- (Web article) Department of Electrical and Computer Engineering, UW, “ECE Professor Brian Johnson leads Department of Energy-funded research,” Link.

11. Project Team and Roles: List all participants along with their individual roles and/or intellectual contribution (e.g., DOE personnel, students, collaborating organizations).

- Brian Johnson , Assistant Professor, University of Washington: Principal Investigator
- Dragan Maksimovic , Professor, CU Boulder: Co-Principal Investigator
- Gab-Su Seo , PhD, Senior Engineer, NREL: Co-Principal Investigator
- Soham Dutta , Graduate Research Assistant, University of Washington: Converter control.
- Rahul Mallik , Graduate Research Assistant, University of Washington: Modeling.
- Satyaki Mukherjee , Graduate Research Assistant, CU Boulder: Magnetics design.
- Branko Majmunovic, Graduate Research Assistant, CU Boulder: PCB and circuit design.
- John Fossum, Engineer, NREL: Medium-voltage test support including hi-pot test.
- Kurtis Buck, Engineer, NREL: Final multilevel prototype test support.
- Yeong Rack Son, Postdoctoral Researcher, NREL: LCOE optimizaiton.