A High-Power Density Segmented Traction Drive Inverter

Gui-Jia Su
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
sugj@ornl.gov

Jon Wilkins
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
wilkinsjp@ornl.gov

Lingxiao Xue
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
xuel@ornl.gov

Burak Ozpineci
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
burak@ornl.gov

Raj Sahu
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
rajsahuiitkgp@gmail.com

Emre Gurpinar
Buildings and Transportation Science Division
Oak Ridge National Laboratory
Oak Ridge, TN, USA
emre.gurpinar@ieee.org

***Abstract*— High power density is one of the requirements for traction drive inverters for meeting increasing demand for higher power and performance electrical vehicles (EV). This paper presents design and preliminary experimental results for a 100 kW high-power density inverter for EV traction drive applications. The inverter design was based on the segmented inverter topology that can significantly reduce the inverter DC filter capacitor and employs low-profile planar double-side-cooled SiC MOSFET-based power modules, compact mini-channel heat sinks with fin-profile optimized using genetic-algorithms, and high-ripple current capacitors. The design produced a compact inverter package with a total volume less than 1 litter, exceeding the power density goal of 100 kW/L. Preliminary experimental results are included to demonstrate the cooling and electrical performance.**

Keywords—high power density inverter, segmented traction drive, SiC MOSFET, genetic algorithms, mini-channel heat sink, double-side cooling.

I. INTRODUCTION

Demand for significantly faster acceleration and larger, more versatile electrical vehicles (EV) with performance matching or even exceeding the internal combustion engine-based vehicles are driving the need for higher-power traction drive systems at lower cost, weight, and volume. The United States Department of Energy (DOE) and its industrial partners have set the 2025 inverter power density target for the Electrification Program at 100 kW/L [1], more than seven times increase from the 2020 target of 13.4 kW/L or 87% volume reduction. All the major components of an inverter design must be minimized to meet the aggressive target [2].

With significantly reduced conduction and switching losses and increased operating junction temperatures, wide-bandgap (WBG) semiconductor switches provide a substantial reduction in the cooling system over the Silicon-based counterpart. Double-sided cooling approaches have been introduced to improve the package's thermal and electrical performances due to increased contact area on both sides of the dies, a more uniform temperature distribution within the structure, and smaller current loops. Double-side-cooled power modules thus have reduced peak temperatures of the dies, the overall package thermal resistance as well as lower package parasitic inductances [3]. Further shrinking the power modules will require heat sinks with high heat transfer coefficients of greater than 10000 W/m^2/°C to handle the increasing heat flux.

The DC bus filter capacitor is another bulky component: it makes up one-fifth of the volume with typical film capacitor materials in the standard 3-phase voltage source inverter. The segmented inverter topology was introduced in [4] to significantly reduce the DC bus capacitor requirements. On the other hand, ceramic capacitors offer higher ripple current handling capabilities and volumetric capacitance densities over the film-based counterpart and therefore present opportunities for down-sizing the inverter DC bus structure [5]. Concerns over the possible catastrophic failure modes and high cost with some of the ceramic materials must be addressed before their wide acceptance in EV applications.

This paper presents design and preliminary experimental results for a 100 kW high-power density traction drive inverter. The design is based on the segmented inverter topology to significantly reduce the DC bus capacitor, and employs low-profile planar double-side-cooled SiC MOSFET-based power modules, high thermal transfer performance and yet compact

heat sinks optimized using genetic-algorithms, and high-ripple current-capable capacitors. The end result is a compact inverter package with volume less than 1 litter, exceeding the power density goal of 100 kW/L. Preliminary experimental results are included to demonstrate the cooling and electrical performance.

II. Inverter Design

A. Inverter Configuration

Table I lists the inverter specifications. The inverter must produce an output power of 100 kW at a power factor of 0.7, i.e. 143 kVA. The coolant flow rate and maximum permissible pressure drop are also given in the table. The bus voltage is chosen at 800 V for better utilization of the SiC MOSFET's voltage capability as well as reducing the current requirements for the DC bus capacitor and current-carrying conductors in the inverter.

TABLE I. Inverter Specifications

Parameter	Value	Note
DC bus voltage (V)	800	
Power (kW)/(kVA)	100/143	at power factor of 0.7
Peak efficiency (%)	98	
Coolant flow rate (L/min)	10	Ethylene-glycol water 50/50 mixtur
Pressure drop (PSI)/(kPa)	2/13.79	

The inverter design was based on the segmented inverter topology because it can significantly reduce the inverter DC filter capacitor requirement [4]. Fig. 1 shows a block diagram of the three-phase segmented inverter. The drive topology segments the inverter phase-legs and motor stator windings into two groups to form two drive units. With interleaved pulse-width-modulation (PWM) between the two drives, the DC bus current ripple and thus the DC capacitance can be significantly reduced. Fig. 2 plots a comparison of normalized capacitor ripple current (a) and busbar current (b) vs. modulation index for the 3-phase and segmented inverters at various power factors. More than 50% reductions in the maximum ripple currents were possible with the segmented inverter. A maximum reduction of over 25% was also possible in the DC bus current. These reductions in currents translated to a smaller DC bus capacitor and busbars. Further, the DC link currents were inversely proportional to the DC bus voltage. For example, when the bus voltage was increased from 400 V to 800 V, the DC bus ripple currents were reduced by a factor of 2.

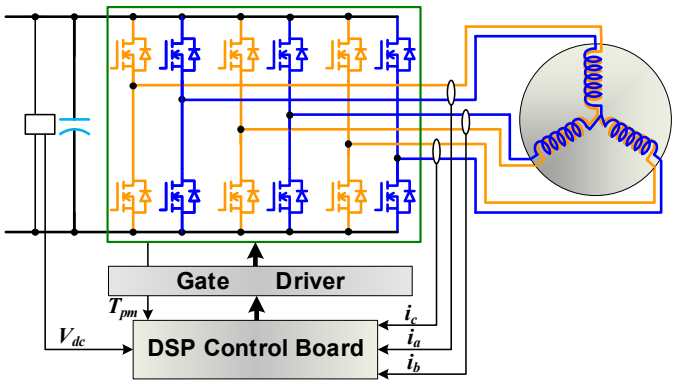


Fig. 1. Block diagram of a three-phase segmented traction inverter.

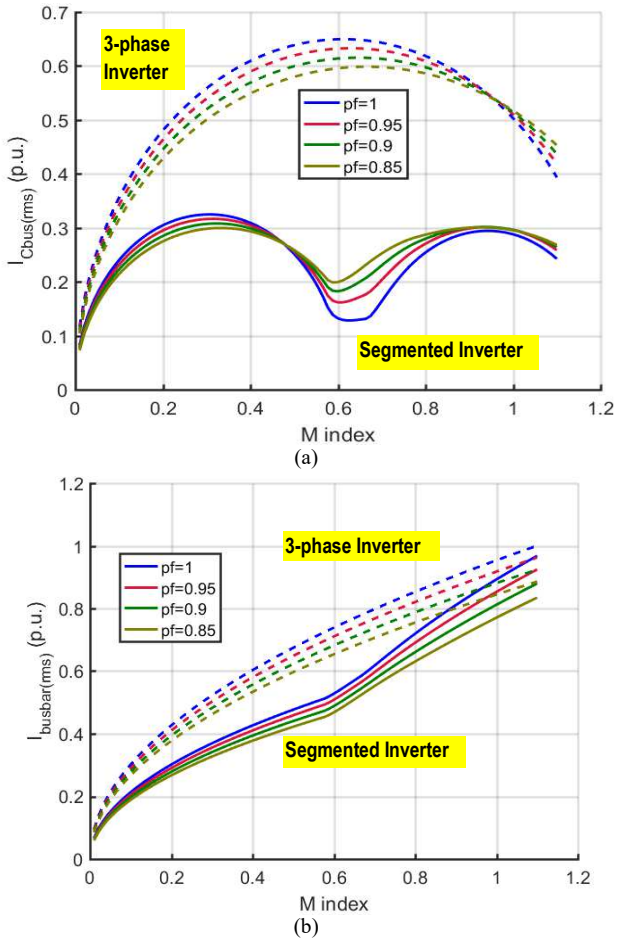


Fig. 2. Comparison of normalized capacitor ripple current (a) and busbar current (b) vs. modulation index for the 3-phase and segmented inverters at various power factors.

B. Heat Sink Optimazation Using Genetic Algorithms

Planar, double-side-cooled power modules were developed by our collaborators using Wolfspeed SiC MOSFET dies (CPM3-1200-0013A), silver-sintering die attachment, and interconnections made of low-temperature sintered porous silver posts [6, 7]. The compact package eliminates wire bonds in the power paths and offers the advantages of low profile, better heat extraction, and low package parasitic inductances. Fig. 3 shows a photo of the SiC MOSFET phase-leg module consisting two of SiC dies and a thermistor for monitoring the module temperature. The SiC dies have the following ratings: 1,200 V and 102 A at 100°C with on-resistance 13 mΩ at 25°C or 21 mΩ at 175°C [8].

Simulation studies were carried out in PLECS to determine the device losses for heat sink design. A PLECS loss model for the SiC MOSFET chips was derived from the datasheets and a packaged switch. Fig. 4 compares the losses per switch in the segmented inverter at output of 100 kW, switching frequency of 30 kHz, and power factors of 0.6 and 0.7 with three different space vector PWMs (SVPWMs): (a) bus-clamped SVPWM with MOSFET only in the third quadrant, (b) bus-clamped SVPWM with MOSFET plus body diode in the third quadrant, and (c) symmetrical SVPWM with MOSFET plus body diode in

the third quadrant. The results indicate (1) the bus-clamped SVPWM reduces switching loss significantly compared with the symmetrical SVPWM and (2) the diode conduction in the third quadrant depends on power factor and switching scheme. Therefore, the bus-clamped SVPWM was adopted in the designs to enhance the inverter efficiency.

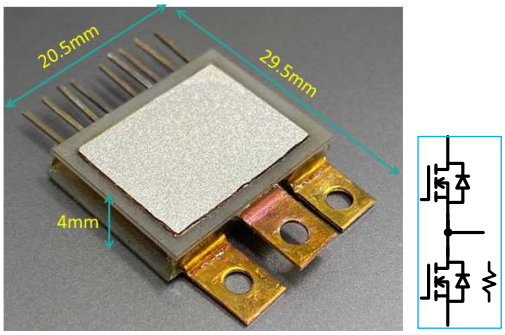


Fig. 3. Photo of the double-side-cooled SiC MOSFET power module.

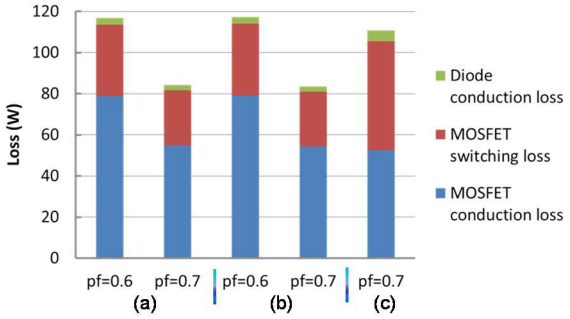


Fig. 4. Comparison of losses per switch at power factors 0.6 and 0.7 with three different SVPWMs.

Heat sinks for the double-side-cooled power module were designed using a genetic algorithm (GA)–based multi-objective heat sink optimization tool, which was implemented with Matlab in conjunction with the finite element analysis (FEA) software package COMSOL Multiphysics [9]. The design optimization method uses Fourier series to synthesize the heat sink fin geometry and an evolutionary optimization algorithm to optimize the parameters of the Fourier series for specified objectives.

Fig. 5 shows a cross-section of a liquid heat sink confined within a rectangular area spanned in horizontal direction by $0 \le x \le L_x$ and in vertical direction by $0 \le y \le L_y$ in the Cartesian coordinate system, where L_x and L_y are the maximum allowed horizontal and vertical dimensions, respectively. The area is divided into two parts, the fin domain and liquid domain, by a fin profile curve, Fp. For simplicity, the domains are assumed to have no holes and the curve can be mathematically defined using a 1D function with each point representing the height of the fin structure. Further let $Fp(x)$ be expressed using the summation of sinusoidal harmonics as

$$Fp_{(x)} = F_0 + \sum_{n=1}^{N} \left(F_n \cos\left(\frac{2\pi}{\lambda_x} nx + \phi_n\right)\right), \qquad (1)$$

where x varies between 0 and L_x, F_0 is a constant shift; λ_x is the wavelength, which is also equal to L_x; n is the harmonic order; F_n and ϕ_n are its amplitude and phase shift, respectively; and N is the total number of harmonics considered. The parameters of the Fourier series function are populated using GAs in Matlab and passed to COMSOL, where the 2D structure is extruded to a 3D heat sink, which is attached to the top of the power module with another copy on the bottom of the module for FEA thermal simulation. Thermal performance metrics including SiC junction temperatures, outlet coolant temperature, overall heat transfer coefficient and pressure drop are fed back to the evolutionary optimization process in Matlab. This evolution process repeats for many generations until satisfactory designs are found.

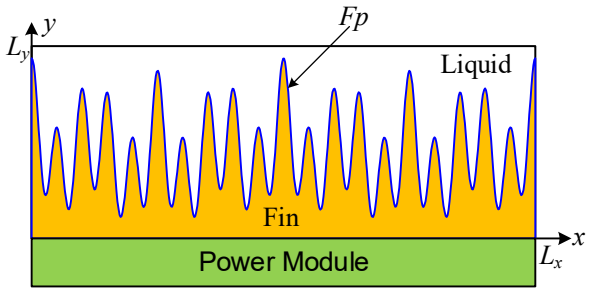


Fig. 5. Cross-section of a liquid heat sink and power module for the GA-based heat sink design optimization.

Fig. 6 shows a phase-leg module sandwiched between two heat sinks and plots the Pareto front and feasible designs for the GA-based heat sink design optimization. The optimization goal was to maximize the device-to-coolant convection coefficient and minimize the total volume of the heat sinks and power module under the following conditions: 150 W loss in each chip (leading to a heat flux in each device of 474 W/cm^2), 65°C coolant inlet temperature, 0.833 L/m flow rate (=10 L/m / 12), <10°C coolant temperature rise at the outlet, <2 psi (13.79 kPa) pressure drop, and <160°C maximum junction temperature.

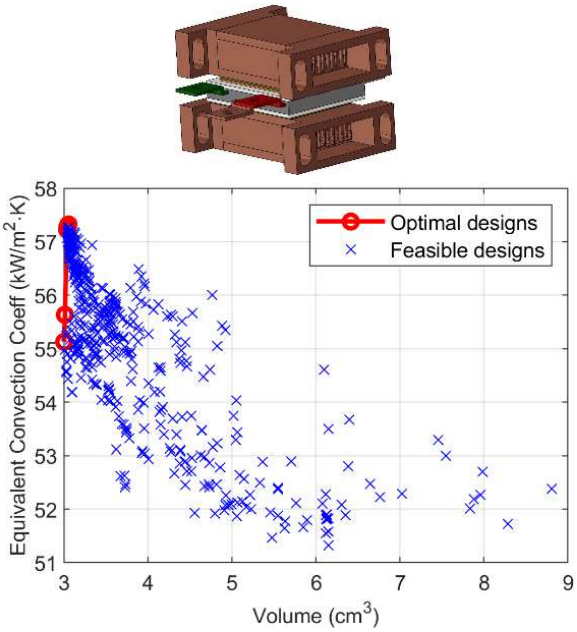
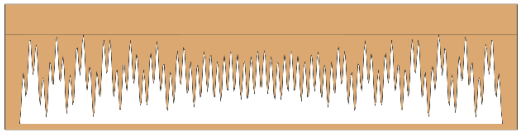
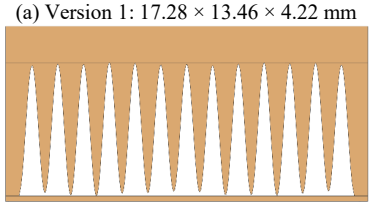


Fig. 6. (top) Double-side-cooled SiC power module and (bottom) feasible designs and Pareto-optimal front plot for the GA-based heat sink design optimization.

Fig. 7 shows the chosen optimal heat sink designs for two configurations. Version 1 design aligns the heat sink inlet and outlet with the power module gate leads and power tabs, respectively. Version 2 rotates the inlet and outlet by 90° and has a 54 % increase in volume compared with version 1. Unlike version 1, the second design, however, does not interfere with electrical connections between the power modules and gate drives or between the modules and inverter DC inputs and AC outputs. Therefore, version 2 was selected for the inverter prototype development. Fig. 8 shows FEA results for the surface temperature for the version 2 heat sink design. Thermal FEA results indicate: (1) the maximum junction temperatures for the two SiC dies were 153.3°C and 155.93°C, respectively; (2) the pressure drop was 749.27 Pa; and (3) the coolant maximum temperatures at the outlet were 74.89°C and 74.17°C, respectively.



(a) Version 1: 17.28 × 13.46 × 4.22 mm



(b) Version 2: 13.46 × 17.28 × 6.5 mm

Fig. 7. Optimal heat sink designs.

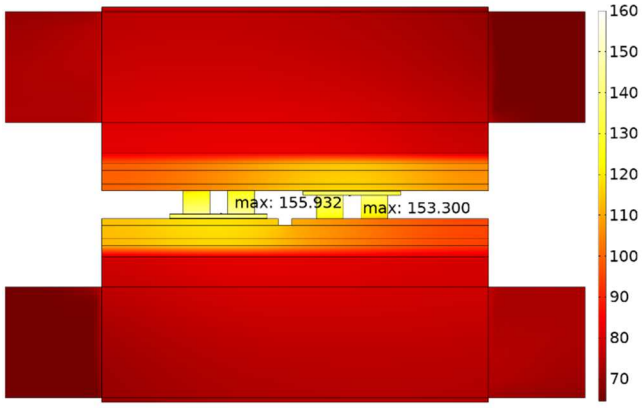


Fig. 8. FEA results for the version 2 heat sink design.

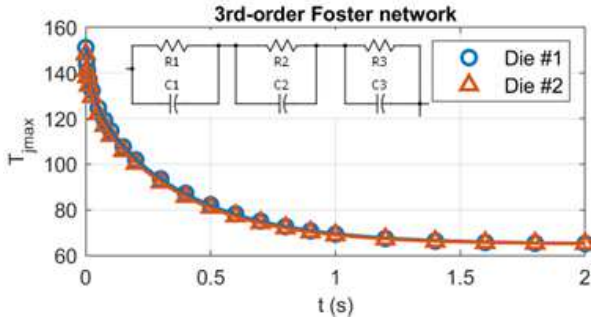


Fig. 9. Transient thermal impedance model.

A 3rd-order lumped thermal impedance model for the power module with the heat sinks was derived using transient-response FEA simulations and incorporated in a PLECS thermal model, as shown in Fig. 9, to investigate MOSFET junction temperature fluctuations of the two MOSFET dies in inverter switching operations. Fig. 10 plots simulation results for the symmetrical SVPWM (top) and bus-clamped SVPWM (bottom), at 100 kW, 30 kHz, and power factor of 0.7. The results indicate that the bus-clamped SVPWM gives more than 15°C reduction in the maximum junction temperature compared with the symmetrical SVPWM.

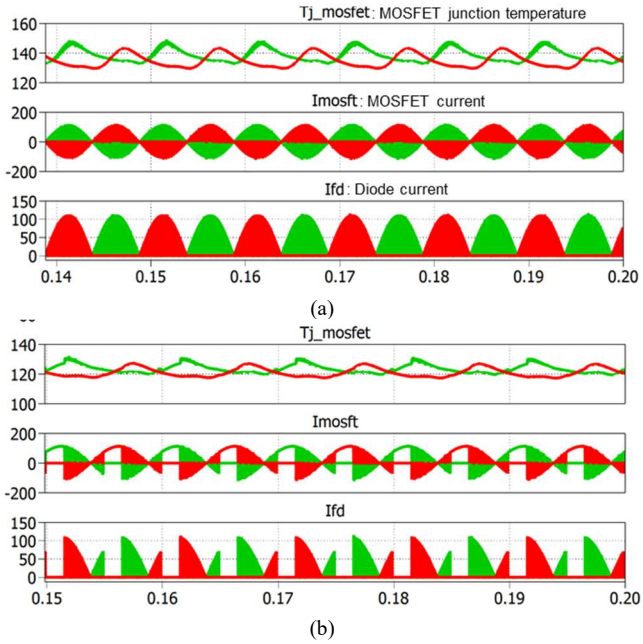


Fig. 10. Simulation results for MOSFET junction temperature fluctuations in inverter switching operations with (a) symmetrical SVPWM and (b) bus-clamped SVPWM. (Red for die #1 and green for die #2.)

C. *Manifold Design*

Two manifolds are needed to guide the coolant flowing into and out of the 12 heat sinks. FEA was used in the manifold design to ensure an even flow distribution to the heat sinks. Figs. 11 and 12 show flow simulation results for the cooling subsystem. A maximum deviation of less than 5 % from the average flow rate was calculated, indicating a relatively uniform flow distribution among the heat sinks.

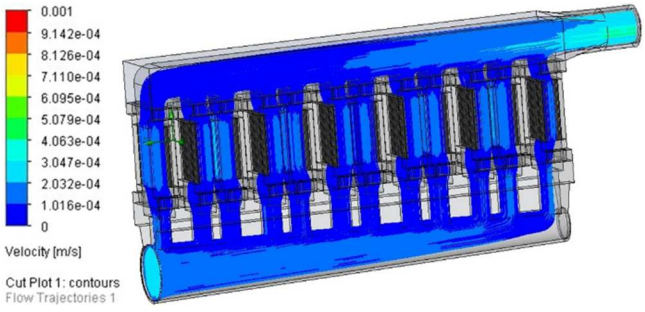


Fig. 11. Design for the inlet and outlet manifolds for ensuring an even flow distribution to the heat sinks.

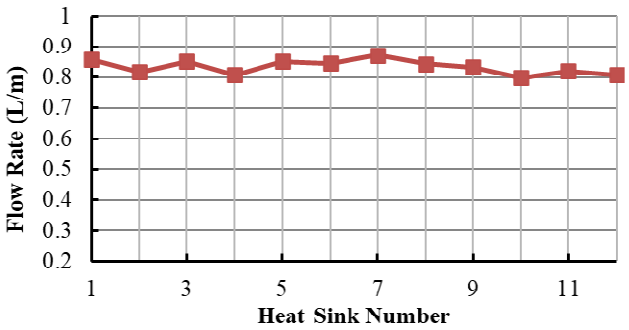


Fig. 12. Simulation results for the flow rate of each heat sink.

III. Prototype and Experimental Results

A. Prototype Construction

Fig. 13 shows a complete 100 kW inverter design using six of the power modules with their control pins directly soldered to the gate dive board and the power tabs attached to a DC bus capacitor board using short copper bus bars. TDK CeraLink capacitors were employed because of their high ripple current capability and operating temperature [10]. The inverter design has a volume of 0.98 L and meets the power density target (100 kW/L).

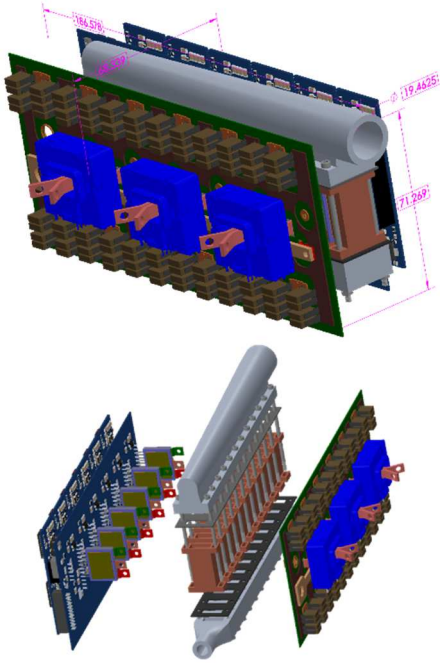


Fig. 13. 3D drawing for a 100 kW segmented inverter design (top), exploded view (bottom).

B. Cooling Subsystem Test

Before adding the gate drive and DC bus capacitor boards, the cooling subsystem consisting of the inlet and outlet manifolds and the 12 heat sinks was assembled and tested for leaks, and a pressure drop measurement was taken. Fig. 14 shows photos of the cooling subsystem test setup. Fig. 15 plots measured cooling subsystem pressure drops at various flow rates. At the rated flow rate of 10 L/min, the measured pressure drop was 1.5 psi (10.34 kPa), which is 25% lower than the maximum specification of 2 psi (13.79 kPa).

Fig. 14. Photos of cooling subsystem pressure test setup.

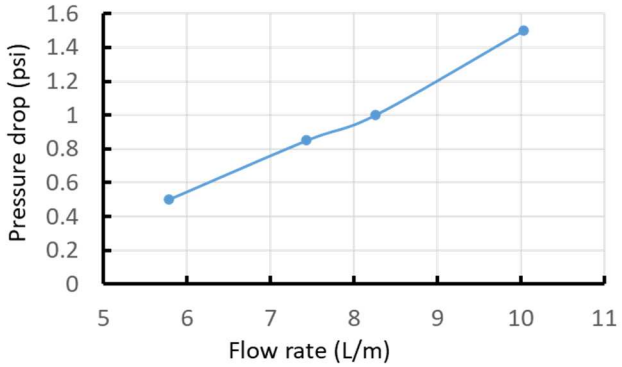
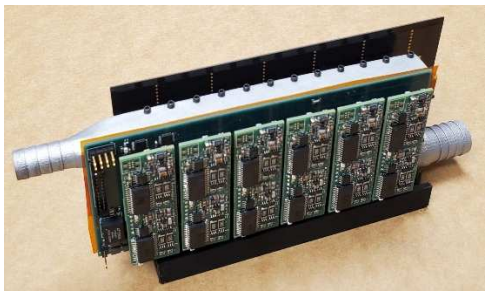


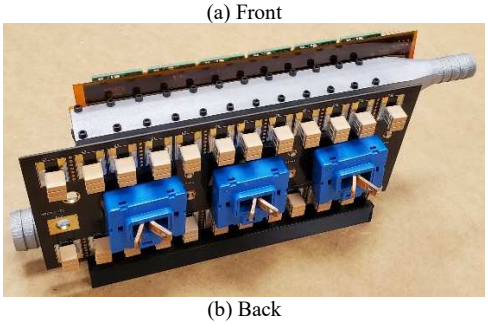
Fig. 15. Measured cooling subsystem pressure drop vs. flow rate.

C. Inverter Test

After the successful test of the cooling subsystem, the gate drive and DC bus capacitor boards were installed into the power modules to complete the 100 kW inverter assembly. The inlet and outlet manifolds were modified for more secure attachment of the cooling hoses. Fig. 16 shows photos of the assembled inverter prototype.



(a) Front



(b) Back

Fig. 16. Photos of the 100 kW inverter prototype.

The inverter was tested with a resistive load bank, and the test setup is shown in Fig. 17. Fig. 18 shows typical operating

waveforms for (from top to bottom) DC bus voltage, line-to-line voltage, and three-phase currents. Fig. 19 plots measured inverter efficiency vs. output power; the measured inverter efficiency is more than 99.2% over the tested load conditions.

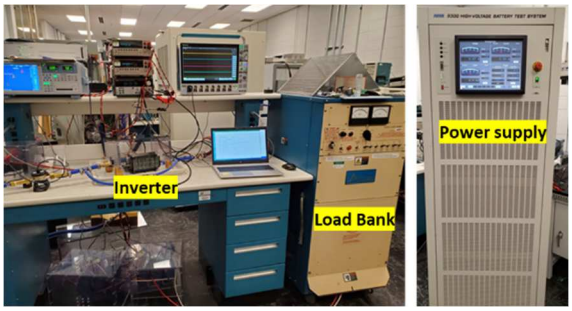


Fig. 17. Test setup for the 100 kW segmented inverter.

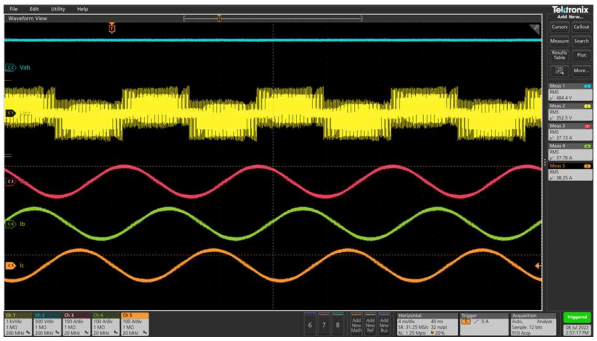


Fig. 18. Typical operating waveforms. From top to bottom: DC bus voltage, line-to-line voltage, and three-phase currents.

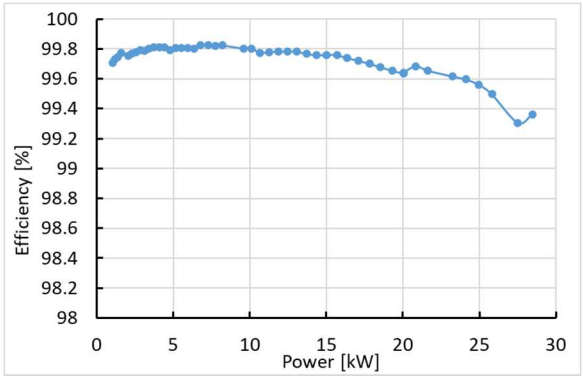


Fig. 19. Measured inverter efficiency vs. output power.

IV. Conclusions and Future Work

The combination of the segmented inverter topology, low-profile planar double-side-cooled SiC MOSFET power modules, optimized mini-channel heat sinks, and high-ripple current capacitor led to a compact traction inverter design with power density greater than 100 kW/L (140 kVA/L at power factor of 0.7). Preliminary test results with the 100 kW inverter prototype verified the design goal for thermal and electrical performances. Continuing validation test at various load condition is planned for future work.

Acknowledgment

This research used resources available at the Power Electronics and Electric Machinery Research Facility, a DOE EERE User Facility operated by the Oak Ridge National Laboratory (ORNL). This study is based upon the work supported by the U.S. Department of Energy (DOE), Vehicle Technologies Office (VTO). The authors would like to thank Mrs. Susan Rodgers, U.S. DOE Technology Development Manager for her support of this work. The authors also gratefully acknowledge Mr. Jonathan Willocks for his assistance in assembling the hardware, and Dr. Guo-Quan Lu, Dr. Khai D. T. Ngo, Dr. Rolando Burgos, Dr. Chao Ding, Mr. Zichen Zhang, Mr. Xingchen Zhao, and Mr. Tam Nguyen for providing the power modules and gate drivers and for their collaboration in demonstrating the traction inverter.

References

[1] U.S. DRIVE Partnership. *Electrical and Electronics Technical Team Roadmap*. U.S. DRIVE, U.S. Department of Energy, October 2017. Available at https://www.energy.gov/node/805366.

[2] I. Husain, B. Ozpineci, M. Islam, E. Gurpinar, G. Su, W. Yu, S. Chowdhury, L. Xue, D. Rahman, and R. Sahu, "Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles," in *Proceedings of the IEEE, vol. 109, no. 6*, pp. 1039-1059, June 2021, doi: 10.1109/JPROC.2020.3046112.

[3] H. Lee, V. Smet and R. Tummala, "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 239-255, March 2020, doi: 10.1109/JESTPE.2019.2951801.

[4] G. J. Su and L. Tang, "A Segmented Traction Drive System with a Small dc Bus Capacitor," 4th *IEEE Energy Conversion Congress and Exposition (ECCE 2012)*, pp. 2847–2853, September 16–20, 2012, Raleigh, North Carolina.

[5] S. Chowdhury, E. Gurpinar and B. Ozpineci, "Capacitor Technologies: Characterization, Selection, and Packaging for Next-Generation Power Electronics Applications," in *IEEE Transactions on Transportation Electrification*, vol. 8, no. 2, pp. 2710-2720, June 2022, doi: 10.1109/TTE.2021.3139806.

[6] C. Ding, H. Liu, K. D. T. Ngo, R. Burgos and G. -Q. Lu, "A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization," in *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11672-11680, Oct. 2021, doi: 10.1109/TPEL.2021.3070326.

[7] G.-Q. Lu, "Heterogeneous Integration Technologies for High-Temperature, High-Density, Low-Profile Power Modules of Wide Bandgap Devices in Electric-Drive Applications," Presentation at the 2021 DOE Vehicle Technologies Office Annual Merit Review Meeting. June 21-24, 2021.

[8] Wolfspeed bare die SiC MOSFET CPM3-1200-0013A datasheet. Available at https://www.wolfspeed.com/products/power/sic-bare-die-mosfets/1200v-bare-die-silicon-carbide-mosfets-gen3/cpm3-1200-0013a/.

[9] R. Sahu, E. Gurpinar and B. Ozpineci, "Fourier Analysis-Based Evolutionary Multi-Objective Multiphysics Optimization of Liquid-Cooled Heat Sinks," *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, 2020, pp. 4017-4023, doi: 10.1109/ECCE44975.2020.9235943.

[10] TDK CeraLink Capacitors, https://www.tdk-electronics.tdk.com/en/1054426/products/product-catalog/ceramic-capacitors/ceralink-capacitors.