ADVANCED FABRICATION TECHNOLOGIES FOR NANO-ELECTRONICS

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MAR 2 2 1996
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Three novel fabrication technologies are presented which greatly increase the tools available for the realization of nano-electronic devices. First, a sub-micron area post structure descending from a metallic airbridge allows gating of regions as small as 0.1 μm in diameter. This has enabled the study of such quantum phenomena as coupling of parallel quantum point contacts, and electron focusing around a tunable quantum antidot. We also describe two new techniques for backgating multiquantum well structures with submicron lateral resolution. These techniques enable separate ohmic contacts to individual quantum wells spaced as closely as 100 Å, and thus allow the fabrication of novel quantum tunneling devices. The first technique uses regrowth over a patterned ion-implanted substrate. The second involves a novel epoxy-bond-and-stop-etch (EBASE) processing scheme, whereby the original substrate is etched away and the backside then patterned using conventional methods.

SUB-MICRON AIRBRIDGE POST

The use of Schottky gates to modulate submicron areas is of considerable importance in such nanoelectronics research areas as coupled quantum point contacts, [1,2] lateral resonant tunneling through quantum antidot potentials both in the integral [3] and fractional [4-6] quantum Hall effect regimes, and the Aharanov-Bohm effect. [7] The observation of these phenomena requires that the electron phase coherence length, roughly the distance an electron travels before undergoing an inelastic scattering event, be longer than the device dimensions. To obtain these extraordinarily long phase coherence lengths, such structures are typically fabricated in the extremely high mobility two dimensional electron gases (2DEGs) formed in GaAs/AlGaAs heterostructures at low T. While the lateral geometry of nanoelectronic structures in this material can be defined by mesa etching down towards the 2DEG, this technique produces large numbers of electron traps at the etched surfaces and is difficult to control. Rather, it is far more advantageous to form the geometry by using surface Schottky gates to deplete those regions where the electrons are not wanted. [8] This has the additional advantage that the conducting width of the structure can be tuned with gate voltage, since the surface gates also deplete laterally from their edges up to a distance of a few microns. For example, it is this technique that allows the number of one-dimensional subbands in a quantum point contact to be controlled, [9] enabling observation of a conductance quantized in units of $2e^2/h$. However, because this technique

requires that the gate be connected to an external voltage source, those devices which require isolated sub-micron gate-depleted regions, such as the "hole" occurring in the middle of an Aharanov-Bohm ring, present a special challenge.

To meet this challenge, we have developed an integrated metallic air-bridge [10] and submicrometer gate post [2] for use in surface Schottky gates that can be independently biased. The air bridge and gate post are fabricated in a single step and are easily incorporated into existing processes. Previous work on sub-micron gating by Taylor et al. [11] and Simpson et al. [5] focused on the use of an interlevel dielectric to act as a spacer between multiple metal levels. However, the addition of a dielectric spacer adds two processing steps to the fabrication sequence and generally requires dry etching of the dielectric. Further, the plasma processing associated with both dielectric deposition and etching can have a significant deleterious impact on the device. [12] While in this work they used a first level metal disk to protect the semiconductor from plasma damage during the dry etching of the dielectric, since the contact hole must line up with the first level metal disk this method places stringent limitations on the minimum size which can be achieved.

By contrast, the airbridge-and-post process described here requires only one electron beam lithography step followed by a single metal evaporation and lift-off. The final structure leaves the semiconductor surface free of dielectric overlayers and does not involve a potentially damaging dry etch. Here we describe the use of our process to fabricate a pair of parallel quantum point contacts (QPCs) which exhibit coupling to one another. The structure consists of two outer gates of conventional first level metal separated by 1.6 μm, and between them a central gate composed of a 0.2 μm diameter post dropped from an airbridge. As will be shown, when subject to magnetic fields the structure can also be viewed as a quantum antidot potential within a narrow constriction.

The material used was an MBE-grown $Al_{0.3}Ga_{0.7}As$/GaAs heterostructure with the 2DEG located ~1200 Å beneath the surface. A 250 Å donor layer Si-doped to 1×10^{18} cm^{-3} was separated from the 2DEG by a 400 Å $Al_{0.3}Ga_{0.7}As$ spacer layer. The 2DEG has a density of 2.0×10^{11} cm^{-2} with a mobility of 10^6 cm^2/Vs, without illumination. Hall bars defined with optical lithography were fabricated by wet etching. Large area Au/Ge/Ni contacts and Cr/Au gate leads were optically defined and deposited by lift-off. The two outer first level gates of the device are then patterned by e-beam lithography and a Cr/Au liftoff.

TABLE 1. Exposures for airbridge/post definition.

Exposure Region	Dose (μC/cm^2)
2 μm wide lines on GaAs	320
2 μm wide bridges over GaAs	160
2 μm wide bridges over Au	140
Transition dose (line bridge)	250
0.2 μm square gate post	400*

*Results in 0.25 μm diameter post on GaAs.

After the first level gate metallization is complete, the airbridge formation is begun by spinning a bilayer resist profile of 600 nm of PMMA (496K) followed by 1200 nm of P(MMA-MAA) 9%. The P(MMA-MAA) layer is spun on in two coatings of equal thickness.

After each spin the sample is baked on a hot plate at 180°C for 15 minutes. The e-beam exposure of the airbridge structure requires a number of different doses for the different regions of the device, as listed in Table I. A high dose exposes both resist layers to define the large area support pillars and lines. Lower doses expose only the P(MMA-MAA) layer to define the actual bridge region, though because of differing electron backscatter rates this dose depends on whether the bridge crosses a GaAs surface or first level metal. A third, higher dose is used to define the sub-micron gate post. We also make use of a transition dose between the bridging region and the large support pillars. The e-beam lithography system was operated at 50 keV with a beam current of 2 nA. The airbridge is 2.0 μm wide and the contact hole is drawn as a 0.2 μm square hole in the center of the airbridge. After exposure, the sample is developed in MIBK:IPA (1:2) at room temperature for 3 minutes with light agitation. Figure 1 shows an example of the developed resist profile for a similar airbridge structure, clearly demonstrating the ability to selectively open holes to the substrate while maintaining a bridge above the bottom layer of resist. The P(MMA-MAA) layer shows excellent undercut, which allows a clean liftoff profile. Although it is possible to use a tri-level resist profile we have found that the bilayer resist is usually more than adequate for good liftoff. The bottom PMMA layer acts to guide the metal bridge over various topography, including etched facets and first level metal. We have found that the airbridge can span topography that is as tall as the bottom PMMA layer thickness.

Following the resist development, the sample is descummed and dipped in Buffered Oxide Etch (BOE) before loading into the evaporator. For this resist profile a Ti/Au (50/650 nm) metallization is defined by liftoff in acetone. We have previously reported on the fabrication of taller bridging structures with larger dimensions. [2] The process has a good amount of latitude and can be engineered for different applications. In the present application the airbridge is ~0.5 μm above the semiconductor surface and the gate post has
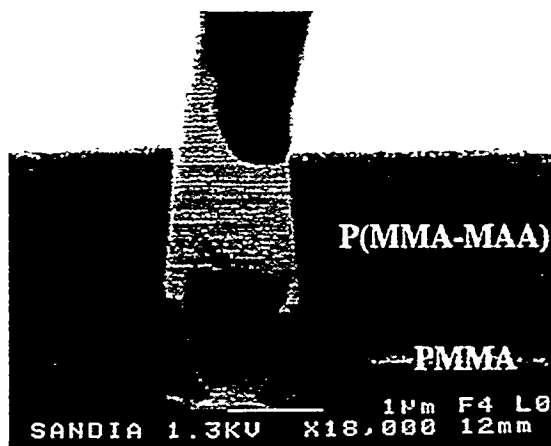

FIG. 1. Resist profile of the bi-layer resist after electron beam exposure and development in MIBK:IPA (1:2). The actual resist thicknesses shown are larger than those quoted in the text.
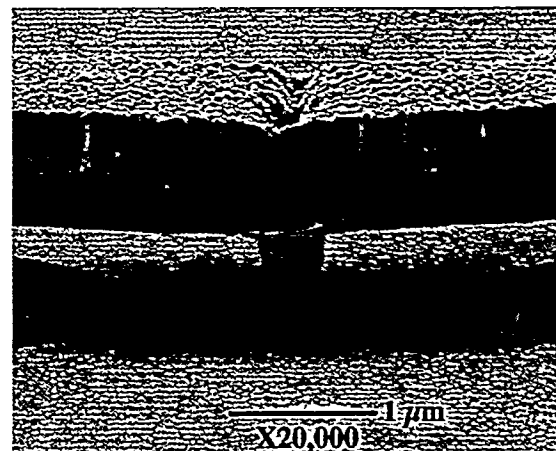
FIG. 2. Completed parallel quantum point contact structure. Side gates are first level metal and the center gate post and airbridge are second level metal. Exposure conditions are listed in Table 1.

a controllable minimum of ≥ 0.1 μm. If the airbridge is lowered so that it is closer to the substrate then it should be possible to fabricate gate posts with even smaller diameters. Figure 2 shows the completed structure with first level gates and the airbridge. Varying the dose from 380 to 440 μC/cm^2 increases the gate post diameter from 0.1 μm to 0.45 μm.

A similar airbridge approach, albeit for larger critical dimensions, has been previously reported [13] but this technique relies on the use of a complex development sequence for each layer of a tri-layer resist profile. Other techniques have required multiple e-beam exposures and metal evaporations. [14] Our technique uses a single exposure, a single development followed by a single metal evaporation and liftoff, with the advantage that the minimum feature size is not limited by alignment considerations.

The conductance through the parallel QPCs formed on either side of the gate post was measured at 0.1 K using standard low-frequency lock-in techniques. Depletion under the gates occurred at -0.25 V. The gap between either side gate and the center gate post is approximately 0.7 μm. Figure 3 shows the quantized conductance steps for two conditions: (a) all three gates swept together, and (b) with one QPC fully pinched off by a side and center voltage of -5.5 V
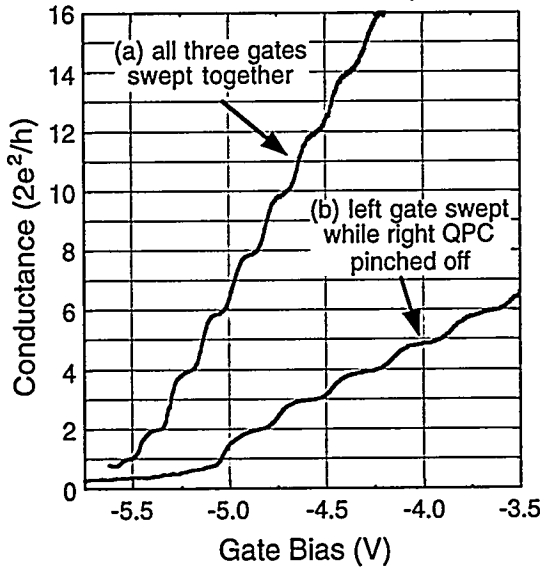

FIG. 3. Quantized conductance steps for the structure in Fig. 2. (a) All three gates swept together, yielding conductance steps of 4 e^2/h and exhibiting quantum coherence between the two QPCs. (b) Same structure with the right QPC fully pinched off and the left gate swept. The conductance steps are in units of 2 e^2/h.
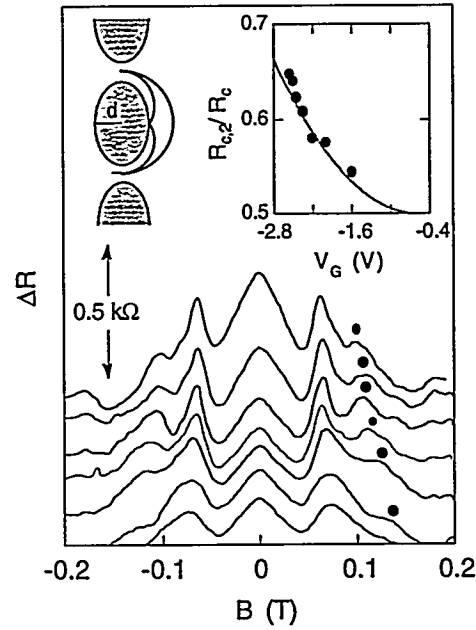
FIG. 4. Magnetoresistance of parallel QPCs with balanced electrical widths, at 0.3 K. Sidegate voltages were fixed at -0.7 V and -0.9 V, while center gate voltages were -1.6, -2.0, -2.2, -2.35, -2.45, -2.50, and -2.55 V. The primary focusing resistance peaks appear near ~0.07 Tesla and their positions change little with center gate bias. However, the positions of the secondary reflection focusing peaks (marked by dots) do change with center gate bias. Left inset: cyclotron orbits for primary and secondary peaks. Right inset: ratio of secondary to primary peak positions, discussed in Ref. 17.

and the other side gate swept. [When the opposite gate is measured in a similar manner, the data is virtually identical to (b).] No gate leakage was measured at any time during the measurements. With one QPC fully depleted, shown in (b), the conductance steps of the device were quantized in units of $2e^2/h$, obviously due to the other QPC. However, when both quantum point contacts were open, shown in (a), the conductance steps were quantized in units of $4e^2/h$. Steps of $4e^2/h$ were observed when all three gates were swept together, or when the center gate was swept with the side gates held at a constant bias. The locking of both QPCs together to produce conductance steps of $4e^2/h$ has been explained with a minimum energy argument by Smith et al. [1] When the two QPCs are within the electron phase coherence length, the QPCs form a coupled system and the sub-bands depopulate together. We note that the two QPCs pinched off at different biases (-5.5 and -5.0 V) when operated independently. SEM inspection of similar devices have shown excellent alignment of the center gate post in the middle of the two side gates, so we are forced to attribute this difference to random potential fluctuations in the channels.

The two QPCs in parallel can also be viewed as a narrow constriction with an antidot potential in the center. Thus the sample also exhibits electron focusing phenomena when a magnetic field B is applied. Earlier observations of magnetic focusing either used separated QPCs which could not be measured in parallel, [15] or occurred in large arrays of quantum dots in which the individual electron orbits were ensemble averaged [16] The structure in Fig. 2 allowed the first observation of focusing around a single antidot. [17]

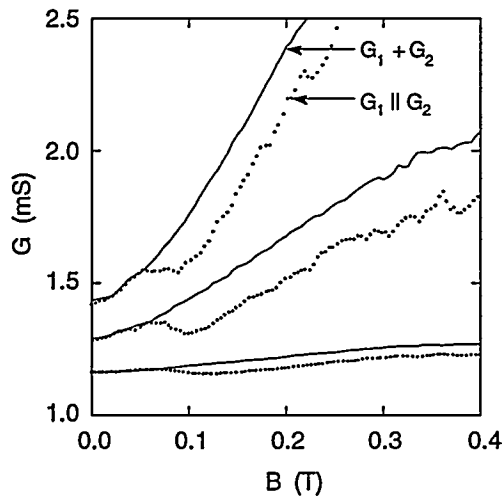Magnetic focusing in our structure occurs when the magnetic field B has a value such that an electron passing ballistically through one QPC is bent by B along a cyclotron orbit and focused back into the opposite QPC. As a result, the electron is localized around the antidot, and the resistance of the device increases. In Fig. 4 we show the $T = 0.3$ K magnetoresistance of the sample when the electrical widths of the two QPCs have been carefully balanced, and the bias on the central gate is stepped so as to vary the size of the antidot potential. A primary magnetic focusing peak is present at a nearly constant B of ~±0.07 T, in agreement with a simple calculation based on the geometry of the device. [17]   Also discernible is a secondary focusing peak, arising when the electron has a narrower cyclotron orbit and is specularly reflected in a single bounce off the antidot potential. (See sketch inset in Fig. 4.) The position of the secondary reflectance peak depends on the

FIG. 5. Low field magnetoconductance at three bias conditions of the two QPCs measured in parallel (dots), and the *sum* of the conductances of the two QPCs measured individually (solid line). Ohm's law is clearly violated.

size of the antidot and hence the bias of the central gate, while the position of the primary peak depends only on the QPC positions, which are relatively unchanged. The right inset plots the ratio of the cyclotron radii for the primary and secondary peaks as a function of gate voltage, along with a fit based on this model. [17]
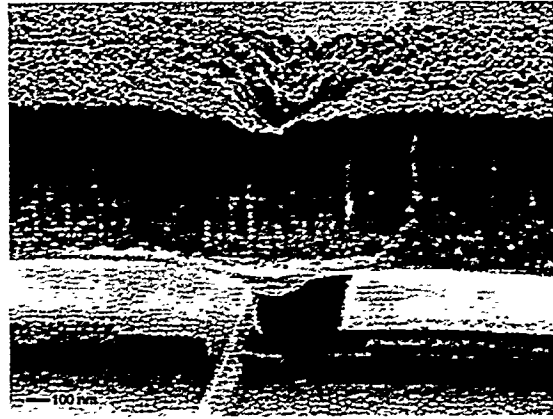

FIG. 6. Photo of Coulomb blockade device with a post/airbridge gate positioned over the quantum dot region. Biased positively, the post gate should deepen the dot potential and allow observation of the Coulomb blockade at higher temperatures.

We note that magnetic focusing in these structures produces a violation of Ohm's law: the conductance of the two QPCs measured in parallel *is not equal* to the sum of the conductances measured individually. In Fig. 5 is the magneto-conductance (MC) of an identical geometry structure fabricated in lower electron density material, for three bias conditions. [17] While the sum of the individual QPC MCs (lines) is fairly monotonic, the parallel MC (dots) displays the conductance dip corresponding to the focused orbit, and then follows the shape of the single QPC sum, though there is a constant conductance deficit that persists to higher B.

Although to date we have only performed electrical measurements on the coupled parallel QPC type of structure, we believe that the airbridge/gate post process will have great utility in future research on additional types of nanoelectronic structures. In Fig. 6 is shown a Coulomb blockade structure in which a submicron post-gate is positioned over the quantum-dot or island region of the device. Such a gate should allow the depth of the dot's confinement potential to be maintained with a positive post-gate voltage, while the dot is made narrower by negative side gate voltages. This should allow the energy level spacings to be made much larger, thus increasing the temperature at which the device can operate.

BACKGATING OF MULTIQUANTUM WELL STRUCTURES

The strong current interest in the behavior of double quantum well (DQW) structures was largely precipitated by two pioneering works. Boebinger et al. [18] demonstrated that at high magnetic field B such double 2DEG systems can form a correlated bilayer state, in which the positions of electrons in one QW are correlated with those in the other so as to minimize the total energy of the system. Palevski et al. [19] demonstrated that the coupling between a high mobility QW and a closely spaced low mobility QW could be controlled, yielding a switchable mobility edge and promising future device possibilities. While these experiments only used contacts to the two QWs in parallel, it was soon realized that the ability to make electrical contact to the individual QWs, even though they are spaced apart by a barrier whose width is only on the order of 100 Å, would enable a number of experiments which could much more effectively probe
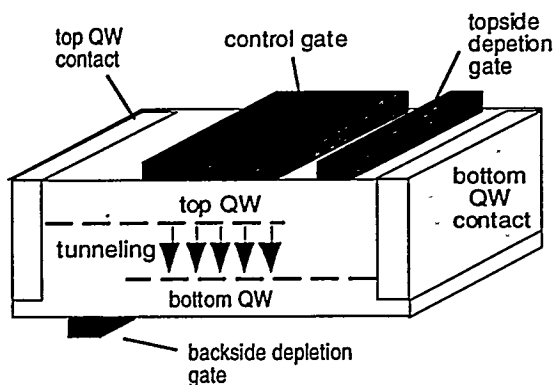
FIG. 7.   Sketch of the selective gate depletion method of making independent contacts to DQW structures. Geometry shown is for an interwell tunneling configuration.

both tunneling and Coulomb interactions between electrons in adjacent QWs. Ground breaking work in making independent contacts was performed by Eisentein et al., [20] who developed a selective backgating technique.   In the backgating scheme, each contact is comprised of two parts: a diffused metallic contact which reaches both of the QWs, and a gate which locally depletes electrons from the QW which one does *not* wish to contact. (See Fig. 7.)   Whereas a contact to the bottom QW uses a gate on the top surface, a contact to the top QW requires a backgate. (It is of course easy to extend this scheme to structures with more than two QWs by simply using both a top gate and a backgate for each contact.)   This technique allowed numerous other pioneering experiments on electron-electron interactions, including measurements of 2D-2D inter-QW tunneling as a function of gate bias, [21] in-plane magnetic fields, [22] and perpendicular magnetic fields, [23] and a measurement of Coulomb drag, [24] in which the "frictional" drag of a current flowing in one QW causes a voltage to be developed in the other QW.

In the implementation of Eisenstein et al., the backgates were simply patterned by conventional metallization and lift-off on the back surface of the substrate, after mechanically lapping it to a thickness of ~50 μm. This has the significant disadvantages of poor lateral resolution (on the order of the substrate thickness), and requires high operating biases (approaching 100 V) in order to fully deplete one of the quantum wells.   Further, handling of samples of such minimal thickness requires extreme care.   More recently, backgates have been fabricated by using a focused ion-beam to damage a conducting layer in the substrate before growth of the active layers. [25]   While submicron structures are possible, this technique requires expensive focused ion-beam equipment, available in only a few laboratories.   The same group has also fabricated backgate structures by using a shallow-angle etch to form the backgate pattern in a bulk doped layer, and then regrowing active layers upon the etched surface. [26]   This last technique requires regrowth on a non-planar structure, is limited in spatial resolution by the edges of the shallow angle etch, and is complicated by the fact that the material regrown on the relatively large etched facets is likely to have different doping efficiency, electron density, and mobility.

Described here are two novel techniques we have developed for submicron backgating of MQW structures.   In the first, backgates are ion-implanted through a SiN mask into a virgin undoped GaAs substrate. The active MQW layers are then regrown over the planar implanted substrate.   In the second technique, a novel wafer epoxy-bond-and-stop-etch (EBASE) method is used.   After processing of the front side, the wafer is epoxy-

bonded front-side down onto a new GaAs host substrate. The original substrate is then removed by mechanical lapping followed by a wet chemical etch down to a stop etch layer incorporated into the grown buffer. Backgates are then added to the exposed backside of the epitaxial layers, using conventional metallization and lift-off.

Laterally Patterned Ion-Implanted Backgates

In the ion-implanted backgate technique, the first step is to deposit 1 μm of SiN on clean epi-ready 3" GaAs substrates. Because the ion-implanted pattern will not be visible, it is necessary to place alignment marks in the substrate. This is done by patterning the SiN with photoresist, etching through the SiN with a Buffered Oxide Etch (BOE), and then using 1:1:8 $H_3PO_4{:}H_2O_2{:}H_2O$ to etch the alignment marks ~6000 Å into the GaAs. The wafer is than again coated with photoresist, which is exposed and developed with the backgate pattern. The SiN is again etched with BOE, opening windows in the SiN mask for the implant. The photoresist is then stripped in acetone, and the wafer is cleaned in an O_2 RF plasma at 850 mTorr for 30 minutes at 75 W. The resulting SiN-masked wafer is then given the following three ^{29}Si implants at a 7° tilt: 2×10^{13} cm^{-2} at 40 keV, 2×10^{13} cm^{-2} at 100 keV, and 8×10^{13} cm^{-2} at 200 keV. Secondary ion mass spectroscopy (SIMS) data shows that the implants result in a layer ~0.25 μm thick containing ~4×10^{18} cm^{-3} Si. The SiN is then removed using BOE. We note that, except for the relatively tiny alignment marks, at no point during the implant process do any organics come into contact with the substrate.

Because initial test wafers fabricated using this technique exhibited implanted backgates that had a tendency to leak to one another, two p-type blanket implants are performed at this point. The dose is kept sufficiently low that the Si-implant is only slightly compensated, yet high enough that $p\text{-}n$ junctions are formed, both beneath and at the edges of the backgates, for isolation. The implants used are both Be at 7° tilt: 7.5×10^{11} cm^{-2} at 40 keV, and 2.0×10^{12} cm^{-2} at 200 keV. This results in a layer ~0.8 μm thick containing ~3×10^{16} cm^{-3} Be.

The wafer is then given a rapid thermal anneal at 850 °C for 20 seconds to activate the implant, and is at this point ready to have the active layers regrown on it. Because of its superior regrowth capabilities, we use a metalorganic chemical vapor deposition (MOCVD) reactor which has recently shown record mobilities. [27] A typical layer structure contains two QWs separated by a ~100 Å barrier, and is as follows: 1500 Å GaAs buffer, an 8 period superlattice of 150 Å $Al_{0.45}Ga_{0.55}As$/ 600 Å GaAs, 1000 Å $Al_{0.3}Ga_{0.7}As$, 200 Å $Al_{0.3}Ga_{0.7}As$ doped 2×10^{18} cm^{-3}, a 500 Å $Al_{0.3}Ga_{0.7}As$ spacer layer, 150 Å wide GaAs bottom QW, a 100 Å $Al_{0.3}Ga_{0.7}As$ barrier, 150 Å wide GaAs top QW, a 500 Å $Al_{0.3}Ga_{0.7}As$ spacer layer, 200 Å $Al_{0.3}Ga_{0.7}As$ doped 2×10^{18} cm^{-3}, 500 Å $Al_{0.3}Ga_{0.7}As$, and a 30 Å GaAs cap layer. The high Al content in the superlattice buffer is found to be effective in preventing leakage between the backgates and the active QWs.

After regrowth, the wafer is cleaved into individual samples, which are then patterned into Hall bars using a conventional mesa etch, and aligning to the marks

previously etched into the substrate. Vias are then etched down to the implanted backgates, and Au/Ge/Ni contacts are evaporated both in the vias and on the arms of the Hall bar. The ohmic contacts are annealed at 420 °C for 90 seconds, and then top gates are deposited using standard metallization and lift-off.
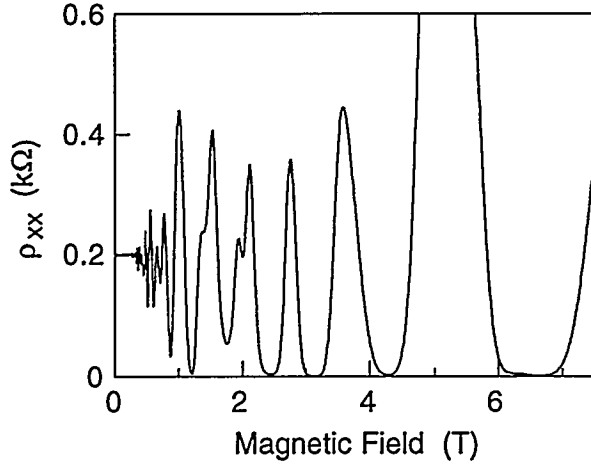

FIG. 8. Magnetoresistance of the DQW regrown by MOCVD over the implanted back gates. All gates were grounded. High quality of the quantum Hall effect states is apparent.
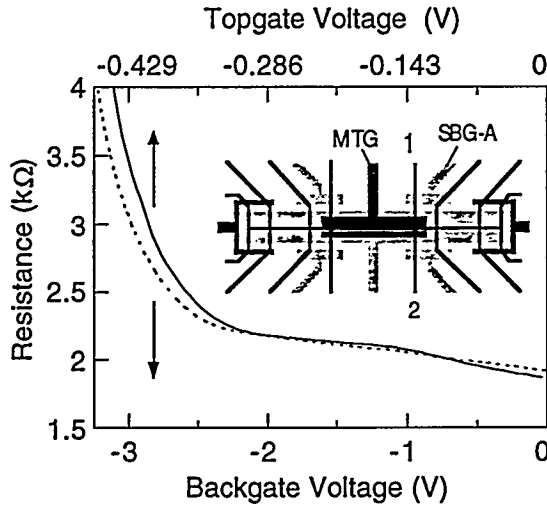

FIG. 9. Two-terminal resistance (contacts 1 & 2) as a function of gate bias for the main topgate (solid line), and a side backgate (dotted line). The two voltage scales differ by a factor of 7, the ratio of the gates' distance to the DQW layers. Inset: mesa (black lines), backgates (light gray), and topgates (dark gray).

The resulting back gated DQW samples are of excellent quality, with the implanted regions completely invisible under a microscope. The samples were measured at 0.3 K using standard low frequency lock-in techniques. With all gates unbiased, the sample whose growth structure is given above exhibited a total density of 3.2 x 10^{11} cm^{-2} and mobility of ~1.0 x 10^5 cm^2/Vs. In Fig. 8 we show the magnetoresistance of the sample to 7.5 Tesla, with all gates grounded. The high quality of the quantum Hall effect states is a good indication of the excellent quality of the MOCVD regrowth, and shows the dual period oscillations characteristic of DQWs. For this particular sample, a main backgate lay under the entire length of the Hall bar, and so four-terminal measurements of regions *not* over the backgate could not be performed. (See Fig. 9 inset.) However, for previously measured samples without the *p*-type implant the main backgate lay under only half the Hall bar. In those samples the density and mobility of regions regrown over the backgate were found to be identical to those regrown elsewhere, and of similarly good quality to the present sample.

In Fig. 9 we show the resistance between leads 1 and 2 (see inset) as a function of bias on

side backgate SBG-A, and also as a function of bias on the main topgate MTG, in each case with all other gates grounded. A plateau is seen at ~-2.2 V for the backgate, corresponding to the depletion of the bottom QW only. A similar plateau appears at a bias of -0.3 V on the topgate, corresponding to depletion of the top QW only. At a bias of -4 V for the backgate, and -0.6 V for the topgate, both QWs are depleted, causing the resistance to diverge. The other backgates exhibited almost identical behavior. We note that the shapes of the two curves are extremely similar, except for a factor of ~7 in gate voltage. (To emphasize this similarity the figure has both top and bottom axes, whose scales differ by a factor of 7.) This is almost identical to the 7.1 ratio of the distances of the top and backgates from the DQW electron layers, as expected.

The Epoxy-Bond-And-Stop-Etch (EBASE) Technique

We have also developed a different method for backgating MQW structures, which requires neither ion-implantation nor regrowth. This epoxy-bond-and-stop-etch (EBASE) technique enables the definition of mesas, Schottky gates, and ohmic contacts on the backside as well as the front, since the backside surface is made only a few 1000 Å away from the active layers. Essentially, the technique consists of processing the front side of the wafer, defining any mesas, ohmic contacts, and Schottky gates that are required. The sample is then epoxied front-side-down onto a host substrate to provide physical support. The original sacrificial substrate is then removed by mechanical lapping, followed by chemical etching to a stop-etch layer which has been incorporated into the grown buffer. The resulting exposed backside surface is on the order of 1 μm away from the active layers, and is free to be processed by conventional methods. Electrical contacts to the patterned front side are provided by etching via holes through to the front side ohmic metal and Schottky gates. The finished structure is robust against repeated cycling to liquid He temperatures, exhibiting no signs of cracking, stress, or flaking. The low T transport characteristics of samples fabricated in this manner are identical to those that have not undergone the wafer-bond-and-etch process, demonstrating that the process has no deleterious effects on sample quality.

Previous work done on flip-chip processing techniques has focused on either eutectic metal bonding, where the two surfaces become bonded by a heated metal layer diffusing simultaneously into the two substrates, [28] or by van der Waals forces created between the highly polished substrate surfaces. [29] The latter technique requires extensive and sophisticated processing in order to achieve the exceptionally clean and smooth surfaces needed, while the thermal annealing required in the former may damage such delicate structures as electron-beam defined gates. Further, it is not clear whether these techniques can be used on the highly non-planar surfaces presented by conventional mesas, contacts, and gate structures. By contrast, our EBASE technique can be used on surfaces with features up to a few microns in height, and requires no special cleaning procedures. We note that while recently Bhattacharya et al. [30] have used a similar technique in the fabrication of FETs, they did not report on the lateral extents of the bonded regions and whether the structures were tested at liquid He temperatures. To our knowledge, the

present paper reports the first use of this method in the selective gating of MQW structures.

The starting point in the fabrication sequence is the incorporation of the stop etch layer into the buffer of the MQW structure, grown either by MBE or MOCVD. We have found that the design of the buffer is important and must address two potential concerns. First, it must be possible to obtain a high selectivity of etch rates between the sacrificial GaAs substrate and the stop-etch layer. We use a citric acid selective etch buffered with H_2O_2 in the ratio 6.5:1 (citric:H_2O_2), which etches GaAs much faster than $Al_xGa_{1-x}As$. [31] While this etch solution in general shows a greater selectivity for higher Al content, we have found that a pure AlAs stop etch layer leaves a very rough surface after etching, presumably due to oxidation of the finished surface. On the other hand, $Al_{0.3}Ga_{0.7}As$ exhibits a selectivity over GaAs of only ~100, [31] which is somewhat low for our purposes. We have found that the higher aluminum content of a layer of $Al_{0.72}Ga_{0.28}As$ constitutes a reasonable compromise, exhibiting selectivities so high that they are difficult to measure, yet yielding an extremely smooth surface for patterning. The second concern is that the backside Schottky gates not leak through the buffer into the active layer. While the high Al content of the stop etch layer helps to prevent leakage, the growth of an $Al_xGa_{1-x}As$/ GaAs superlattice is found to further reduce the leakage current.

In this paper we focus on results from a high-quality DQW wafer grown by MOCVD. Details of the growth conditions have been given elsewhere. [32] A 1000 Å GaAs buffer layer is first grown, followed by a 1 μm thick $Al_{0.72}Ga_{0.28}As$ stop etch layer. Another 5000 Å of GaAs is then grown, followed by a 10-period superlattice of 100 Å $Al_{0.3}Ga_{0.7}As$ / 30 Å GaAs. At this point a standard DQW structure is grown, consisting of 2000 Å of $Al_{0.3}Ga_{0.7}As$, 200 Å of $Al_{0.3}Ga_{0.7}As$ doped n-type at 1×10^{18} cm^{-3}, a 500 Å $Al_{0.3}Ga_{0.7}As$ bottom spacer layer, the 150 Å GaAs bottom QW, a 100 Å $Al_{0.3}Ga_{0.7}As$ tunnel barrier, the 150 Å GaAs top QW, a 500 Å $Al_{0.3}Ga_{0.7}As$ top spacer layer, 200 Å of $Al_{0.3}Ga_{0.7}As$ doped n-type at 1×10^{18} cm^{-3}, and another 500 Å of $Al_{0.3}Ga_{0.7}As$. Finally, a 30 Å cap layer of GaAs doped n-type at 1×10^{18} cm^{-3} is grown.

The front side of the structure is then patterned using conventional methods. A Hall bar pattern is mesa-etched to a depth of 1500 Å, and Au/Ge/Ni contacts are evaporated on the ends of the Hall bar and annealed 90 seconds at 420 °C. Several front-side Schottky gates composed of 200 Å Ti / 2000 Å Au are then deposited by evaporation and lift-off.

After the front side processing is complete, the sample is ready to be epoxied to the host support substrate. It is important to use a host substrate whose lateral extent is smaller than that of the sacrificial substrate, so that the edge bead of epoxy which is squeezed out from the two substrates does not interfere with subsequent backside lithographic processing steps. Gatan Inc. Type G-1 epoxy, a low viscosity heat-cured epoxy commonly used for the preparation of transmission electron microscopy samples, is used to bond the samples. The epoxy and hardener is mixed following the manufacturers instructions, and is allowed to sit for 10 minutes so that any air bubbles present will dissipate. A dab of epoxy is then placed on the front side of the active wafer, and the host substrate is placed smooth-side down on the epoxy. Gentle downward pressure is applied
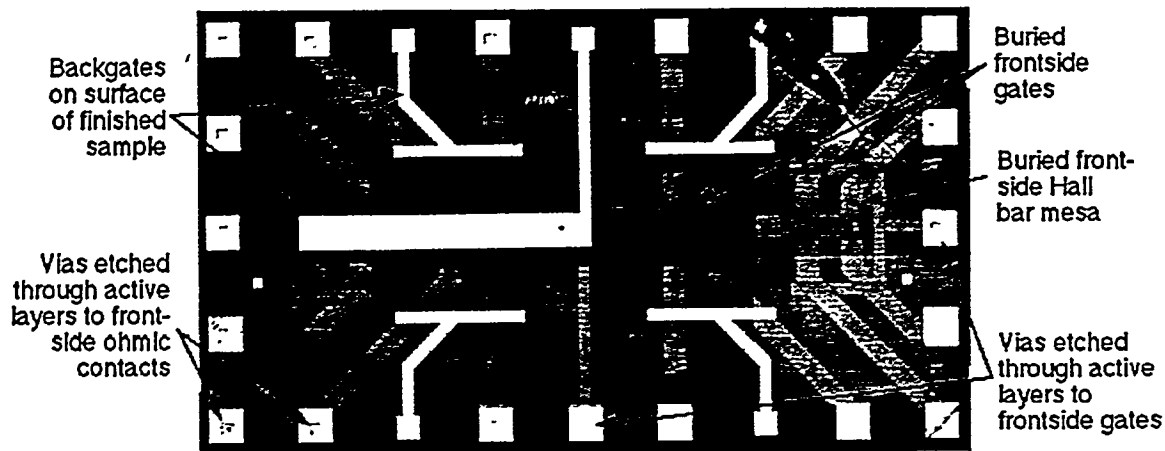
FIG. 10. Image of a completed 2 μm thick EBASE structure that has been patterned on both sides. The brightest regions are the backgates and metal pads over the via holes, both located on the now-exposed back surface. Also visible are the Hall bar mesa and front side gates, now buried under the 2 μm thick active layers. The image is a montage of several photos taken with infrared illumination.

to the host substrate while it is slid back and forth, forcing the layer of epoxy to become relatively thin, on the order of 2 μm. The sample is then baked on a 100 °C hotplate for ~30 minutes to cure the epoxy.

Once the epoxy has hardened, the original sacrificial substrate on which the active layers were grown is removed. Because of the relatively slow etch rate and poor uniformity of the selective citric acid etch, most of the substrate is first removed by mechanical lapping using a 3 μm Al_2O_3 grit, with the sample attached by wax to a glass puck. When only ~25 μm of the sacrificial substrate remains, the sample is removed from the lapping apparatus and cleaned. After attaching the host substrate side of the sample to a glass cover slip using wax, the sample is then placed in the citric acid selective etch to remove the remaining GaAs sacrificial substrate, which takes on the order of 1-2 hours. Because the etch is non-uniform, the surface appears very rough until the $Al_{0.72}Ga_{0.28}As$ stop etch layer is exposed, at which point it acquires a mirror finish.

At this point via holes are etched through the active layers to the (now buried) front side electrical contact pads for the gates and ohmics. On the same evaporation step, 200 Å Ti/ 2000 Å Au is deposited in the via holes, and also in the backside Schottky gate pattern. One mil Au wires are then attached to the contact pads using 50/50 In/Sn solder applied with a soldering iron at 200 °C. The sample is quite robust against the elevated temperatures of photoresist baking at 90 °C and the solder temperatures of 200 °C, with no deleterious effects observed. The effects of higher temperatures will be discussed below.

In Fig. 10 we show an image of the completed sample, before the Au lead wires have been attached. The sample was imaged with infrared, making the buried frontside patterns visible through the 2 μm thick active layers. The lightest regions are the backside gates and via metallization pads, residing on the exposed surface of the sample. The buried

Hall bar mesa pattern and frontside Schottky gates appear as light gray regions. While a lithography-related defect is visible in the upper right corner of the sample, we note that no cracking or peeling is present anywhere else. After repeated temperature cyclings to 0.3 K, the appearance of the structure and its low temperature electrical characteristics remained unchanged. The total lateral extent of the sample is ~ 8 mm x 4 mm, giving the single crystal active layer an aspect ratio of ~4000:1. Fig. 11 is a scanning electron micrograph of the edge of a similar sample after cleaving. Because the crystal planes of the active layers are not perfectly aligned with those of the host substrate, the cleaved edge of the active layers is rather rough. Nonetheless, the smooth surface of the stop etch layer is readily apparent, and the epoxy thickness is ~2 μm.

The sample's electrical characteristics were measured at 0.3 K in a top-loading pumped ^{3}He system using standard low frequency lock-in techniques. Fig. 12 shows the four terminal resistivity of a region over the main central backgate, as a function of backgate bias, with all other gates unbiased. The resistance increases as the bottom QW is depleted. At ~-3.4 V, the bottom QW is entirely depleted and a plateau is formed. At higher gate biases the top QW also begins to deplete, becoming completely depleted at ~ -7 V. In Fig. 13 we show the longitudinal resistivity as a function of B for several different backgate biases: (a) 0.0 V, (b) -1.0 V, (c) -2.0 V, and (d) -3.5 V. In (a) the 2D electron densities of the two QWs are equal to one another, at ~2.1 x 10^{11} cm^{-2} for each QW. (Each QW also has the same mobility, ~3.3 x 10^5 cm^2/Vs.) As a result, the Shubnikov-de Haas (SdH) oscillations from each well are identical, and so reinforce one another and do not exhibit beating. In (b) the densities of the two QWs are different, the top QW having been partially depleted, and a beating of the SdH oscillations at low B is readily apparent. In (c) the density difference has become even greater, causing the beating to become more rapid, and the minimum at Landau level filling factor v=2 near 8 Tesla to no longer reach zero. Finally, in (d) the bottom QW has been fully depleted, and only a single period of SdH oscillations from the top QW is apparent. Because the density in the top QW is still nearly 2.1 x 10^{11} cm^{-2}, the period of the SdH oscillations is nearly the

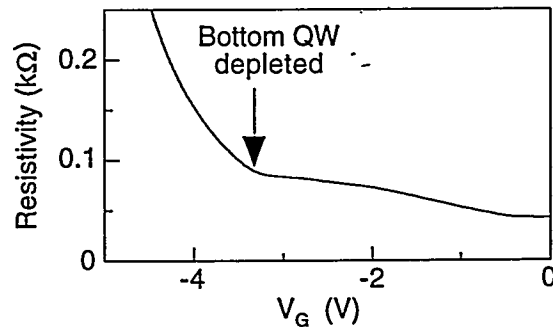FIG. 11. SEM of the edge of an EBASE sample.

FIG. 12. Four terminal resistance vs. backgate voltage for an EBASE sample. A clear plateau appears when the bottom QW becomes depleted.

same as in (a), only the oscillations are now due to the top QW only.

By performing Fourier transforms in $1/B$, the electron densities in each QW can be determined. In Fig. 14 we summarize the densities as a function of backgate bias. The total density depends nearly linearly on backgate voltage, while the top QW density remains relatively unchanged as long as some electrons remain in the bottom QW. We note that the effect of the backgate on the DQW is virtually identical to that of the top gate, except that

FIG. 13. Four terminal longitudinal resistivity as a function of B for four different backgate voltages. In (a) the two QWs have identical densities, producing "clean" quantum Hall effect oscillations without beating. In (b) and (c) the densities are imbalanced, producing substantial beating. In (d) the bottom QW is entirely depleted, and the oscillations, similar in appearance to (a), are from the top QW only.

the voltage scale is approximately a factor of 12 larger. This is in rough agreement with the factor of 14.6 greater distance of the backgate from the DQW layers.

We have tested the EBASE technique with active layers as thin as 2000 Å, also at lateral extents of 8 mm. Because, when defined by depletion, the lateral resolution of electrically conducting regions is limited to the distance between the gates and the active layers, this technique should allow submicron geometries to be defined by backgating, simultaneously with front-gating. Since the samples are clearly able to withstand temperatures of 200 °C, PMMA bake temperatures will not present a problem and electron-beam defined structures can be patterned on the backside. This should enable the construction of novel mesoscopic devices in MQW structures, such as Aharanov-Bohm interferometers in which the interference paths are the two QWs, [33] or novel quantum tunneling transistors. [34,35]

We have also attempted other processing steps on the EBASE sample backsides, including mesa etching and ohmic contact formation. On a sample which had no frontside processing, a Hall bar was mesa etched from the backside down to the epoxy, leaving it "freestanding", and Au/Ge/Ni contacts were evaporated over the ends of the Hall bar. At this point the Hall bar definition appeared excellent, with no cracking or peeling. The sample was then annealed at 400 °C for 60 seconds to drive the ohmic metallization into the electron layers. Some outgassing from the epoxy was observed during this process. After annealing, bands of discolored regions appeared throughout the 200 μm wide Hall bars. We believe that these are due to the active layer becoming locally unbonded from the epoxy. The sample was then measured at 0.3 K, and despite the local unbonding, was seen to have excellent electrical characteristics, nearly identical to Hall bars manufactured from the same wafer without the EBASE technique. We expect that with further work it should be possible to develop a process for making ohmic contacts without causing such unbonding, either by using ohmic contact metallizations such as Pd/Ge which do not require such high temperature anneals, or by using other epoxies.
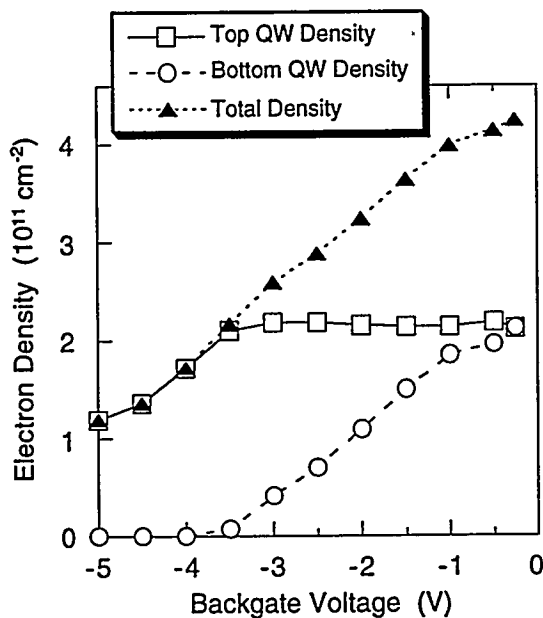

FIG. 14. Top QW density, bottom QW density, and total density in the EBASE sample as a function of backgate voltage. The top QW density remains constant as long as electrons remain in the bottom QW, while the total density is nearly linear with backgate bias.

In summary, we have presented three novel fabrication technologies for nano-electronic structures. First, we described a process for the fabrication of $\geq$ 0.1 μm diameter Schottky gate posts with integrated airbridges, for use in the construction of quantum interference devices, and quantum dot and antidot structures. Second, we described a simple and inexpensive method for backgating MQW structures by regrowing over patterned ion-implanted substrates. The method allows the use of low gate bias voltages, and should be amenable to submicron resolution. Finally, we introduced a novel EBASE process in which the patterned front side of a wafer is epoxied to a host substrate, and the original sacrificial substrate removed by etching to a stop-etch layer. The technique exposes a high quality backside surface, as close as a few 1000 Å to the active layers, for further processing by conventional methods including e-beam lithography. The EBASE samples are robust against temperature cycling up to +200 °C and down to 0.3 K. Initial results indicate that with some development the EBASE process will also be amenable to mesa etching and ohmic contact evaporation and annealing.

ACKNOWLEDGMENTS

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