Efficiency Optimization of Dual Active Bridge Converter Based on dV/dt Snubber Capacitors

Wei Xu, Adithyan Vetrivelan, Zhicheng Guo, Ruiyang Yu, Alex Q. Huang
Semiconductor Power Electronics Center (SPEC)
The University of Texas at Austin
Austin, Texas, USA
wei.xu@utexas.edu

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***Abstract*—This paper presents a lossless regenerative dV/dt snubber circuit for PWM converters to achieve high-efficiency high power-density without significant cost and reliability penalties. The dV/dt snubber employs lossless capacitors for each MOSFET device in a converter to provide an additional path to store the switching energy during turn-off transient and decrease the actual turn-off loss of the MOSFET channel. A novel mathematical turn-off loss model is built to separate the actual turn-off loss of the MOSFET channel and the recycling switching energy stored in the total equivalent output capacitance including Coss, the dV/dt snubber, and etc. Necessary snubber optimization strategy is proposed in order to balance the turn-off loss with ZVS operation range and deadtime conduction loss, and thereby achieving an optimal efficiency performance. To prove the validity and accuracy of the novel turn-off loss model and optimization strategy, the dV/dt snubber has been incorporated into a 1.3kV/200kW DC/DC and a 1kV/70kVA DC/AC PWM converters. Experimental results are given to demonstrate the validity of the proposed dV/dt snubber capacitors and optimization strategy.**

***Index Terms*—Snubber capacitors, optimization, DAB**

I. Introduction

The Dual Active Bridge (DAB), among many other isolated topologies, has an intrinsic ZVS turn-on capability as the transformer current is always lagging the primary side output voltage [1]. However, the turn-off loss is typically high and can become the dominant part at heavy load and high switching frequency [2]. To reduce the device switching loss, soft-switching techniques have been developed for PWM converters since the 1970s [3] [4]. Two main soft-switching techniques can be categorized: active soft-switching and passive soft-switching. The active soft-switching requires additional active devices and thus increase control complexity and decrease system reliability [5] [6] [7]. The passive soft-switching usually requires extra components, such as resistors, inductors, capacitors or diodes [8] [9]. The proposed dV/dt snubber in this paper is the simplest snubber circuit which only employs lossless capacitors for each MOSFET device.

In order to obtain the insight on how the snubber capacitors influence the turn-off loss, a novel turn-off loss model of the MOSFET channel during turn-off transient is developed and introduced. Analytical equations for the MOSFET channel current and voltage during turn-off transient is used to separate the actual switching loss of MOSFET channel and the recycling switching energy stored in the total equivalent output capacitors including the snubber capacitors. To prove the validity and accuracy of the novel turn-off loss model, numerical calculation and experimental results are demonstrated with a $1.3kV/200kW$ DAB under back-to-back DC/DC mode. A curve-fitting turn-off loss model as a function of V_{ds} and I_{ds} is developed based on the DC/DC experimental results.

Higher snubber capacitance will result in higher circulation current in a soft switching converter and longer deadtime requirement. Therefore, an optimization design based on the turn-off loss model and including ZVS range, deadtime calculation, and minimum circulation current is proposed to achieve maximum system efficiency. A $1kV/70kVar$ DAB with inductive load is demonstrated to verify the proposed optimization strategy under DC/AC mode. Finally, the proposed dV/dt snubber capacitors and optimization design can be used as a generalized method for DC/DC or DC/AC power electronic converters with ZVS or partial ZVS capability.

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II. Novel Turn-off Loss Model

During the turn-off transient of MOSFET, multiple capacitances influence the actual current flowing through the MOSFET channel such as the turning-off MOSFET/body diode output capacitance, the free-wheeling MOSFET/body diode output capacitance, the parasitic capacitance of magnetic components, and the dV/dt snubber capacitance across the MOSFET drain and source terminal. In order to obtain the insight on how the total equivalent capacitors influence the turn-off loss, a detailed turn-off transient analysis is needed.

A. Turn-off Transient Analysis

Fig. 1(a) shows the typical waveforms of MOSFET during turn-off. For simplicity, the drain voltage (v_{ds}) begins to increase linearly at time t_1, but the drain current (i_{ds}) remains constant at I_{DC}. Part of the current is used to charge the output capacitance (C_{gd} and C_{ds}), and part of them flows through the channel i_{ch}. The channel current is responsible for the turn-off loss. From time t_1 to t_2, the channel current is given by [10]:

$$i_{ch}(t) = g_m \cdot (V_{GP} - V_{TH}) \tag{1}$$

Where, V_{GP} is the plateau voltage, V_{TH} is the gate threshold voltage, g_m is the device transconductance. Between time

t_1 and t_2, a drain-to-gate current i_{GP} charges the gate-drain capacitance C_{gd} and the drain voltage increases at an almost fixed rate, the plateau voltage is given by:

$$V_{GP} = R_g \left\{ C_{GD,av} \frac{dv_{ds}(t)}{dt} \right\} + V_{GS,Low} \tag{2}$$

Where, R_g is the gate resistance, $V_{GS,Low}$ is the gate voltage at driver input which is either zero or a negative value during the turn-off, $C_{GD,av}$ is an assumed constant average value of the gate-drain capacitance (Miller capacitance). Between time t_1 and t_2, the channel is modeled as a gate-voltage controlled current source and the governing equation with $v_{ds}(t)$ as the dependent variable is:

$$C_{MOS} \frac{dv_{ds}(t)}{dt} + i_{ch}(t) = I_{DC} \tag{3}$$

Where, C_{MOS} is the total equivalent capacitance of the turning-off power MOSFET which is given by:

$$C_{MOS} = C_{oss,MOS} + C_{oss,D} + C_{mid} + C_{extn} \tag{4}$$

Where, $C_{oss,MOS}$ is the output capacitance of the turning-off MOSFET which typically equals to C_{gd}+C_{ds}, $C_{oss,D}$ is the free-wheeling MOSFET/body diode output capacitance, C_{mid} is the equivalent capacitance across the midpoint and DC+ of the circuit model which includes the parasitic capacitance of magnetic components in a practical design, C_{extn} is the snubber capacitance across the turning-off MOSFET. Substituting equations (1)-(4), the above equations can be solved as:

$$v_{ds}(t) = \frac{I_{DC} + g_m V_{TH}}{C_{MOS} + g_m R_g C_{GD,av}} t \tag{5}$$

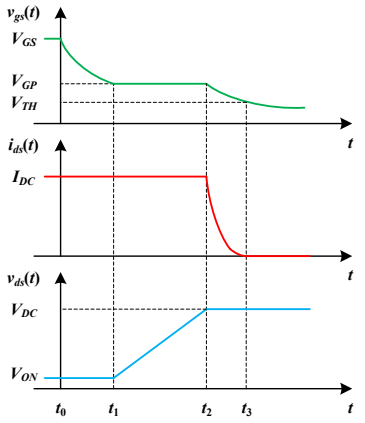
At time t_2, the load current begins to transfer from the MOSFET to the freewheeling diode. Between time t_2 and t_3, the drain source voltage remains constant at V_{DC} and the gate current discharges the gate-source capacitance, therefore, the channel current follows the gate voltage until it reached zero at time t_3 when V_{gs} reaches V_{TH}:

$$i_{ch}(t) = g_m \left[(V_{GP} - V_{GS,low}) e^{-\frac{t-t_2}{R_g C_{gs}}} - V_{TH} \right] \tag{6}$$

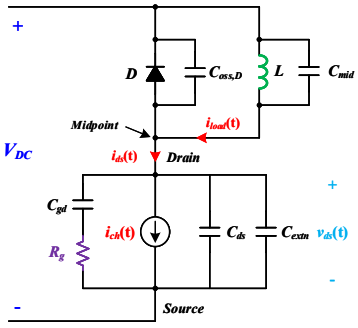
Where, C_{gs} is the gate-source capacitance. Therefore, the power loss dissipated in the MOSFET channel is:

$$P_{Loss}(t) = v_{ds}(t) \cdot i_{ch}(t) \tag{7}$$

Fig. 2 shows the turn-off waveforms and channel power losses with different snubber capacitances under $V_{DC} = 1200V$, $I_{DC} = 300A$. The average loss during one turn-off without snubber capacitors is $19.3mJ$. Contrarily, the average loss with 10nF snubber capacitors decreased by 61% to $7.5mJ$. With larger C_{extn}, the turn-off loss can be reduced to close to zero at the expense of much longer turn-off time. Due to the ZVS turn on capability of DAB, the energy stored in the snubber capacitors during turn off transient will be transferred to the load or source in the next switching cycle.



(a) Typical turn off waveforms



(b) Circuit model

Fig. 1. Switching off model of SiC MOSFET.

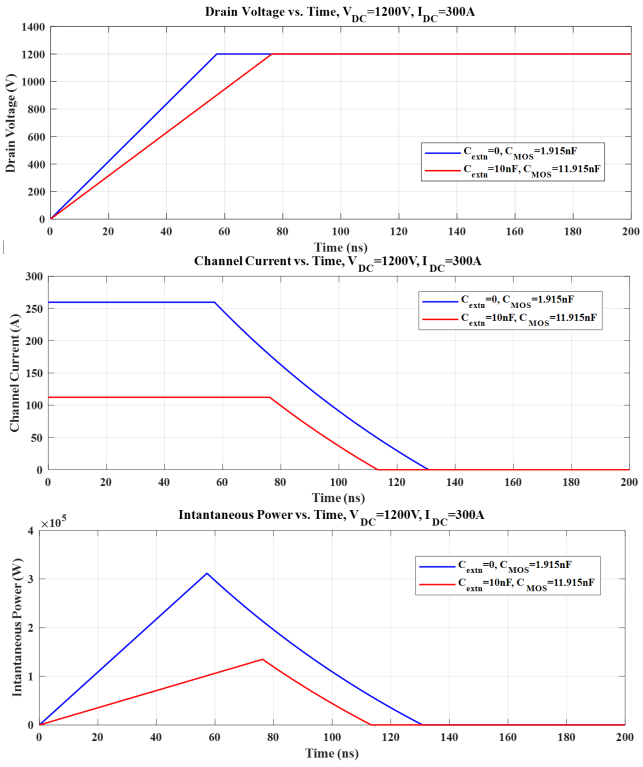


Fig. 2. Turn off waveforms and channel power losses.

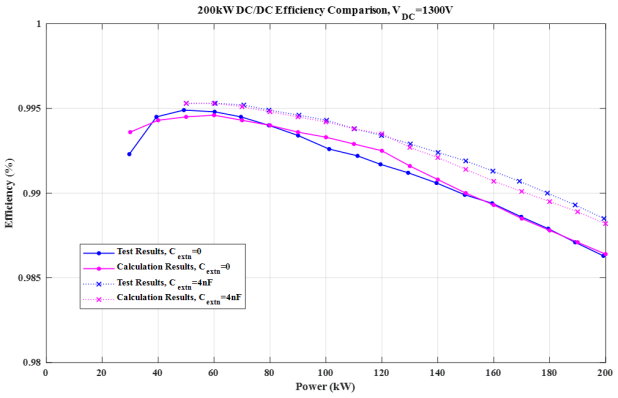


Fig. 3. 200kW DAB back-to-back DC/DC efficiency comparison.

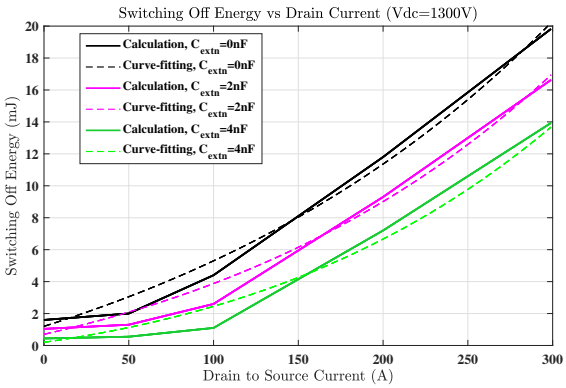


Fig. 4. 200kW DAB back-to-back DC/DC efficiency comparison.

B. DC/DC Experiment Verification

To verify the accuracy of the novel MOSFET channel loss model, a $1.3kV/200kW$ DAB back-to-back DC/DC test was performed. The switching frequency is fixed at $15kHz$. Only primary side MOSFET devices are paralleled with $4nF$ snubber capacitors in the test. Fig. 3 shows the 200kW back-to-back DC/DC efficiency comparison. Using the above MOSFET channel model, the calculated efficiency with C_{extn}=$4nF$ is around 0.16% higher than the calculated efficiency without snubber capacitors, while the test efficiency with C_{extn}=$4nF$ is around 0.2% higher than the test efficiency without snubber capacitors. This validates the accuracy of the proposed loss model, and they can be used for the turn-off loss estimation of SiC MOSFET power module application.

C. Curve-fitting Turn-off Loss Model

Using the proposed novel turn-off loss model, Fig. 4 shows the calculated turn-off energy loss of the $1700V$ SiC MOSFET versus the current. A curve fitting equation is further developed to allow the use of the equation for DAB optimization. The curve fitting result is given by:

$$E_{off}(V_{ds}, I_{ds}) = K_1 e^{K_2 I_{ds}} + K_3 + C_{MOS} K_4 (e^{K_5 I_{ds}} - 1) \quad (8)$$

Where, K_1 to K_5 are the curve fitting coefficients. For the $1700V$ SiC module, Table I lists the values of K_1 to K_5.

With larger CMOS, the turn-off loss can be reduced to close to zero at the expense of much longer turn-off time. The minimum $(dV/dt)_{min}$ occurs when the equation (6) equals to zero. Increasing C_{MOS} beyond this point is useless while making the ZVS turn-on harder and requires longer deadtime. $(dV/dt)_{max}$ corresponds to the case where no snubber C_{extn} across the drain and source terminal is used.

Between $(dV/dt)_{max}$ and $(dV/dt)_{min}$, the turn-off loss is getting lower and lower with increasing C_{MOS}. Although, higher C_{MOS} will result in lower turn-off loss, but more narrow ZVS range and higher body diode conduction loss due to deadtime. Therefore, C_{MOS} optimization is needed to achieve maximum system efficiency under full load range.

TABLE I
CURVE FITTING COEFFICIENTS OF THE TURN-OFF LOSS MODEL

Parameters	Value
K_1	8.6
K_2	0.0039
K_3	-7.4
K_4	-2.618×10^5
K_5	2.618×10^5

III. COMPREHENSIVE OPTIMIZATION STRATEGY

This paper selects dual phase shift (DPS) modulated single-stage DAB inverter as optimization objective. The ZVS conditions for DAB inverter are complicated due to the rectified sine wave voltage across the AC-link capacitors. Besides, one drawback of the DAB inverter is the high turn-off loss when the current and frequency are high [11]. The turn-off loss can become the dominant loss at heavy load. Additionally, many studies have reported that transformer circulation current is one major concern for the DAB [12] [13]. Therefore, in order to obtain high efficiency, a comprehensive optimization strategy including ZVS range, deadtime calculation, accurate turn-off loss estimation, and minimum circulation current is needed.

A. Accurate MOSFET Turn-off Loss

In a practical design, an additional snubber C_{extn} can be placed in parallel with the MOSFET to further reduce the turn-off loss. The proposed novel turn-off loss model as shown in equation (8) is adopted to estimate the turn-off loss.

For the adopted $1700V$ SiC module, Table I lists the values of K_1 to K_5. The curve of $C_{oss,D}$ and $C_{oss,MOS}$ versus drain source voltage are extracted from the test results [14]. C_{mid} typically includes the parasitic capacitance of the DAB inductor and the transformer. C_{mid} is the equivalent parasitic capacitance across the switch nodes of the half bridge must be charged from V_{DC} to $-V_{DC}$ (secondary AC side) or V_{DC} to 0 (primary DC side). The dual phase shift (DPS) modulation is adopted in the optimization strategy which means only DC side has zero-level voltage output. Therefore, there are totally two MOSFETs turning off at the same time in the AC side and one MOSFET in the DC side.

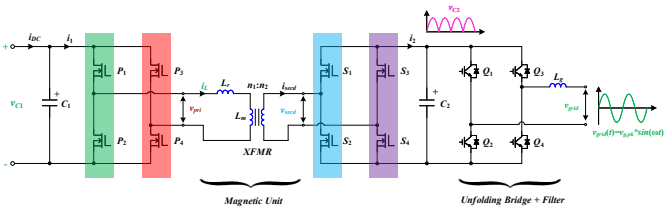


Fig. 5. Single-stage, bidirectional and isolated DAB inverter.

B. Transformer Circulation Current

Referring to Fig. 5, the DAB converter consists of the primary and secondary side full bridges connected with the MFT. The two full bridges produce phase shifted voltages v_{pri} and v_{secd}, resulting in an inductor current i_L. AC components of i_L and i_{secd} are rectified by the two active full bridges, leading to net DC currents i_1 and i_2 on both sides. Filter capacitors C_1 and C_2 absorb the high frequency components of i_1 and i_2. Rectified AC voltage $v_{C_2}(t)$ is connected to the grid through an unfolding bridge and line frequency reactor. The transformer turns ratio $n = n_1 : n_2$ is used in the analysis.

Typical waveforms of the DAB inverter with DPS modulation over one switching cycle are shown in Fig. 6. φ_1 is the phase shift between DC and AC side, φ_2 is the phase shift between the two half-bridge legs of the DC side. $P_{DAB} > 0$ means the power flows from the DC to the AC grid. Key equations of semiconductor devices, including I_1, I_2, I_3, $I_{P1,rms}$, and P_{DAB} under two different power flow directions are listed in the Appendix. To minimize the maximum turn-off current under heavy load (HL), the partial derivative of I_2 with respect to φ_1 and φ_2 under different power flow directions are given by equation (9)-(12). Definitions of variables a, b, c, M and K are listed in the Appendix.

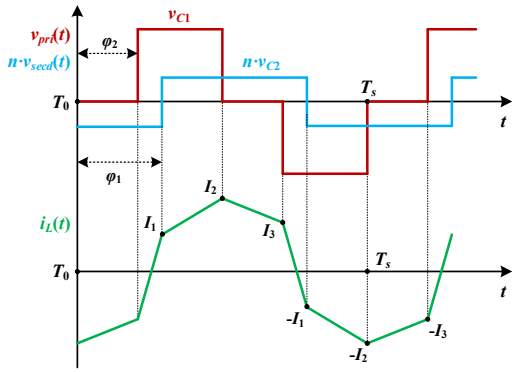
$$\frac{\partial I_2}{\partial \varphi_1} = 0|_{P_{DAB}>0} \Rightarrow \varphi_{1,HL} = \begin{cases} \frac{-b+\sqrt{b^2-4ac}}{2a} & 0 < M < 0.5 \\ \frac{-b-\sqrt{b^2-4ac}}{2a} & M \geq 0.5 \end{cases} \tag{9}$$

$$\varphi_{2,HL} = \frac{(4\varphi_1 - 1) + \sqrt{(4\varphi_1 - 1)^2 - 8(4\varphi_1^2 - 2\varphi_1 + K)}}{4} \tag{10}$$

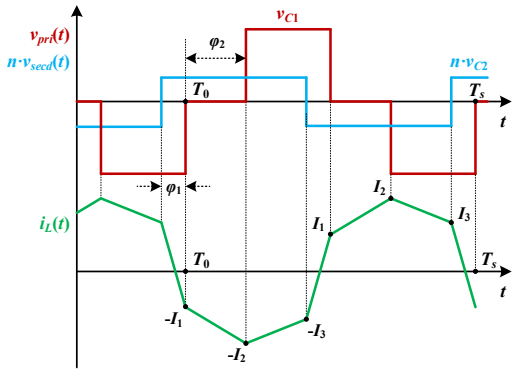
$$\frac{\partial I_2}{\partial \varphi_1} = 0|_{P_{DAB}<0} \Rightarrow \varphi_{1,HL} = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{11}$$

$$\varphi_{2,HL} = \begin{cases} \frac{(4\varphi_1+1)+\sqrt{(4\varphi_1+1)^2-8(4\varphi_1^2+2\varphi_1-K)}}{4} & 0 < M < 0.5 \\ \frac{(4\varphi_1+1)-\sqrt{(4\varphi_1+1)^2-8(4\varphi_1^2+2\varphi_1-K)}}{4} & M \geq 0.5 \end{cases} \tag{12}$$

To guarantee ZVS for all switches under light load (LL), the energy stored in the inductor L_r is required to discharge/charge the junction capacitance [15]. Therefore, the required ZVS constrains under different power flow directions are given by:



(a) $P_{DAB} > 0$, buck mode



(b) $P_{DAB} < 0$, buck mode

Fig. 6. Typical operating waveform of the DAB inverter with DPS.

$$\varphi_{1,LL}|_{P_{DAB}>0} = \frac{4L_\gamma f_s I_{ZVS} V_N + V_P^2 - V_N^2}{2V_P(V_P + V_N)} \tag{13}$$

$$\varphi_{2,LL} = \frac{(4\varphi_1 - 1) + \sqrt{(4\varphi_1 - 1)^2 - 8(4\varphi_1^2 - 2\varphi_1 + K)}}{4} \tag{14}$$

$$\varphi_{1,LL}|_{P_{DAB}<0} = \frac{4L_\gamma f_s I_{ZVS} V_N + V_P^2 - V_N^2}{2V_P(V_P + V_N)} \tag{15}$$

$$\varphi_{2,LL} = \frac{(4\varphi_1 + 1) + \sqrt{(4\varphi_1 + 1)^2 - 8(4\varphi_1^2 + 2\varphi_1 - K)}}{4} \tag{16}$$

C. ZVS Achievement and Deadtime Calculation

To achieve ZVS for all devices in a full bridge, a sufficient transformer current and deadtime are required to charge/discharge the four power MOSFETs equivalent capacitance C_{MOS}/Q_{MOS} the additional parasitic capacitance. By applying energy conservation equation to a full bridge converter before and after the ZVS transition, the required ZVS condition from energy point of view is given by:

$$\frac{1}{2}L_\gamma I_{ZVS}^2 \geq m\left[\int V_{ds} dQ_{oss,MOS} + \frac{1}{2}(C_{mid} + C_{extn})V_{ds}^2\right] \tag{17}$$

Where, $m = 2$ for primary DC side and $m = 4$ for secondary AC side MOSFETs. To avoid partial ZVS, a sufficient deadtime is required on the primary DC side:

$$\int_{t_{off}}^{t_{on}} i_L(t_{off})dt \geq Q_{equiv} \tag{18}$$

$$Q_{equiv} = 2\left[Q_{oss,MOS}(V_{dc}) + (C_{mid} + C_{extn})V_{dc}\right] \tag{19}$$

Where, $i_L(t_{off})$ is the primary side current during the deadtime interval $DT_{pri} = t_{on} - t_{off}$, Q_{equiv} is the equivalent output charge of the total equivalent capacitance C_{MOS}. A minimum deadtime $DT_{min} = 500ns$ is used in the optimization algorithm to avoid the half bridge short circuit and a maximum deadtime $DT_{max} = 2us$ is used to allow partial ZVS turn on under light load condition.

Similarly, required deadtime to charge/discharge the total equivalent output capacitance of secondary side is given by:

$$\int_{t_{off}}^{t_{on}} i_L(t_{off})\frac{n_1}{n_2}dt \geq Q_{equiv}(v_{C_2}) \tag{20}$$

Where, n_1 and n_2 are the transformer winding turns of the primary and secondary side, respectively. Since the secondary side is a rectified sine waveform, the voltage dependence of the charge must be included in the optimization. The above equations can be utilized to find the minimum required dead time to achieve ZVS while minimizing the circulation current.

D. Comprehensive Optimization Strategy

Minimizing the DAB circulation current must be satisfied while meeting the ZVS condition. The turn-off loss reduction from the external snubber capacitance C_{extn} has to be traded off with the deadtime diode conduction loss. Therefore, the external C_{extn} on both the primary and secondary side could be one optimization target based on this algorithm.

Moreover, typical input voltage range V_{in}=900V, 950V ..., 1300V and load conditions P_{DAB}=P_{rated}*(10%, 20% ..., 100%) are adopted in the optimization model in order to achieve the highest California Energy Commission (CEC) efficiency. The flow chart of the proposed comprehensive optimization strategy is shown in Fig. 7.

Fig. 8 shows the external total equivalent capacitance C_{extn} optimization results. The optimal capacitance for primary and secondary side power stage is $C_{extn,pri}$=8.7nF and $C_{extn,secd}$=4.6nF, respectively.

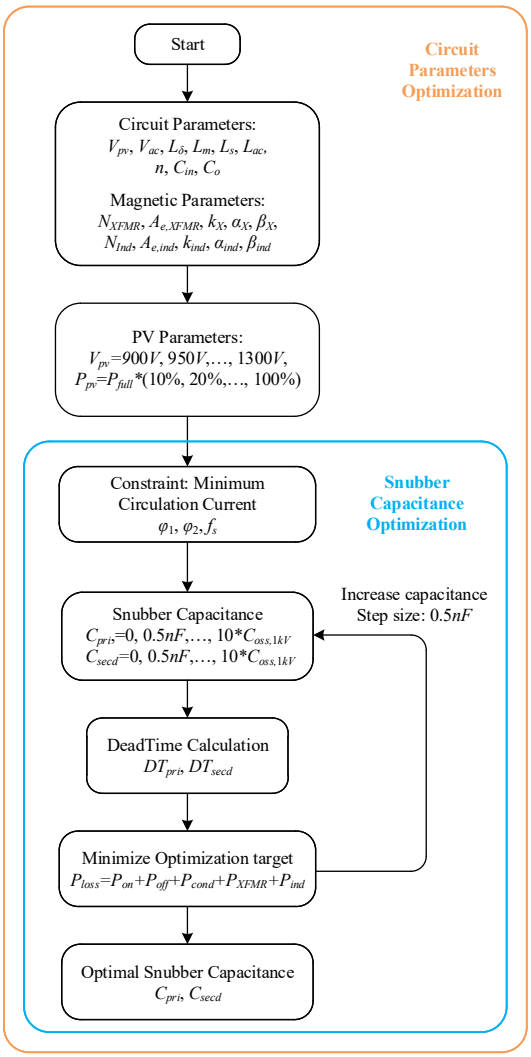


Fig. 7. Flow chart of the comprehensive optimization strategy.

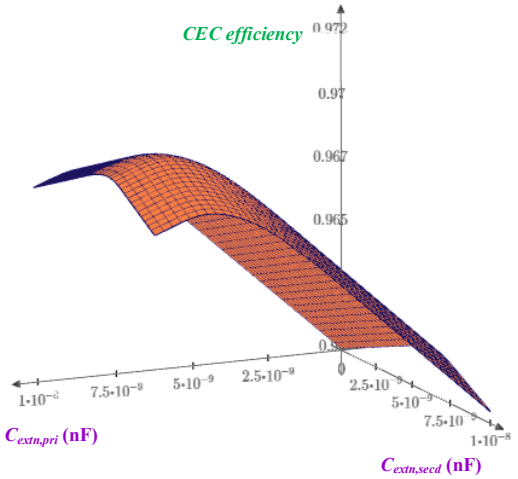


Fig. 8. C_{extn} optimization results for the DAB inverter.

IV. Experimental Verification

In order to justify the proposed turn-off loss model and optimization strategy, necessary experiments based on a $1kV/70kVar$ DAB inverter with inductive load are performed.

A. DC/AC Inductive Load Test

Fig. 9 shows the developed prototype of the SiC DAB inverter. The DC side voltage is $1000V$. Dual phase shift is used in this inductive load test. In addition to the phase shift, the switching frequency is fixed $25kHz$. The maximum tested efficiency is 97.5% at $70kVar$ as shown in Fig. 11. Some

key waveforms are shown in Fig. 10(a) and the zoomed in waveforms over few switching cycles is shown in Fig. 10(c). The THD of inductive load current as shown in Fig. 10(a) is 4.5%. The voltage overshoot across the drain source terminal is around $150V$ under this condition. The HIOKI power analyzer PW6001 with $1500V$ voltage range and 500A/±0.02% high-accuracy sensors CT6875 is used in the high power test.

B. C_{extn} Optimization Verification

Fig. 11 shows the efficiency comparison with different snubber capacitance C_{extn}. The maximum efficiency of the DAB inverter without the proposed dV/dt snubber capacitors is 97.16%. The maximum efficiency increased by 0.33% to 97.49% when employing a snubber $C_{extn,secd}$=$4nF$ and $C_{extn,pri}$=$8nF$ across primary and secondary side MOSFETs respectively. The maximum efficiency decreased to 97.4% when the snubber is increased to $C_{extn,secd}$=$8nF$ and $C_{extn,pri}$=$16nF$. Between no snubber case and $C_{extn,secd}$=$4nF$ case, the system maximum efficiency increases with the snubber capacitance.

Fig. 12 shows the maximum efficiency and CEC efficiency curves with different snubber capacitance $C_{extn,secd}$. The optimal snubber capacitance with the highest CEC efficiency occurs around $C_{extn,secd}$=$4nF$ which verified the validity of the proposed optimization strategy discussed in section III.

V. Conclusion

This paper primarily introduces a dV/dt snubber that employs lossless capacitors across MOSFET drain source terminal in a converter to decrease the actual turn-off loss of the MOSFET. A novel turn-off loss model for accurate loss estimation is proposed and experimentally verified with a $1.3kV/200kW$ back-to-back DC/DC test. In order to improve the DAB inverter power conversion efficiency, a comprehensive optimization strategy based on the proposed novel turn-off loss model and including ZVS range, deadtime calculation, and minimum circulation current is proposed. A $1kV/70kVar$ DC/AC inductive load test is performed to verify the validity and accuracy of the proposed novel turn-off loss model and optimization strategy. Maximum efficiency 97.5% is achieved in the inductive load mode while the efficiency under real power mode is expected to be higher than 98%. The proposed dV/dt snubber analysis and implementation in this paper could provide some guidance on the real power electronics hardware design using MOSFET.

Appendix

Some key parameters of the SiC devices, including I_1, I_2, I_3, $I_{P1,rms}$, and P_{DAB} for DAB inverter under different power flow directions are listed below.

A. DAB parameters definition for $P_{DAB} > 0$

$$I_1 = \frac{v_{c1}(4\varphi_1 - 2\varphi_2 - 1) + v_{c2}}{4L_\gamma f_s} \tag{21}$$

$$I_2 = \frac{v_{c1}(1 - 2\varphi_2) - v_{c2}(1 - 4\varphi_1)}{4L_\gamma f_s} \tag{22}$$

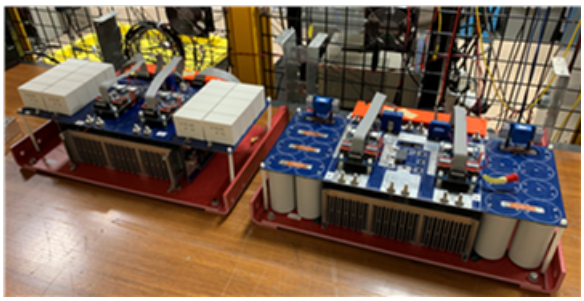
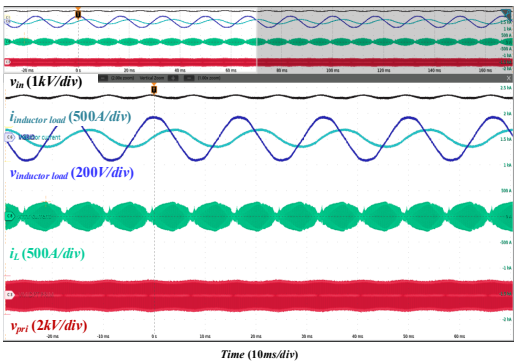
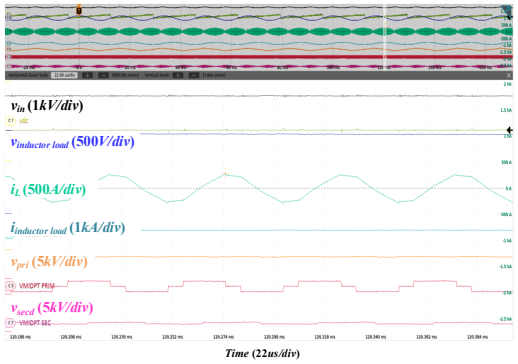


Fig. 9. Single-stage DAB inverter. Transformer is not shown here.



(a) Key waveforms under $70kVar$



(b) Zoomed-in waveforms under $70kVar$

Fig. 10. $1kV/70kVar$ DC/AC inductive load experimental results.

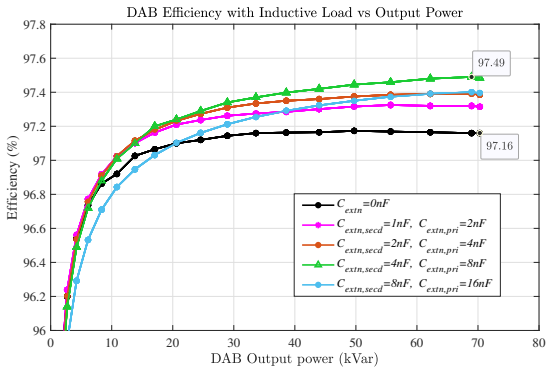


Fig. 11. DAB efficiency comparison with C_{extn}.

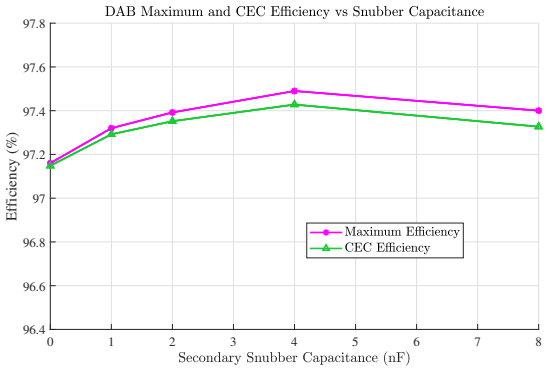


Fig. 12. DAB efficiency comparison with C_{extn}.

$$I_3 = \frac{v_{c1}(1-2\varphi_2) - v_{c2}(1-4\varphi_1+4\varphi_2)}{4L_\gamma f_s} \tag{23}$$

$$P_{DAB} = \frac{v_{c1}v_{c2}(4\varphi_1^2 - 4\varphi_1\varphi_2 + 2\varphi_2^2 - 2\varphi_1 + \varphi_2)}{-2L_\gamma f_s} \tag{24}$$

B. DAB parameters definition for $P_{DAB} < 0$

$$I_1 = \frac{v_{c1}(1-2\varphi_2) - v_{c2}(1+4\varphi_1)}{4L_\gamma f_s} \tag{25}$$

$$I_2 = \frac{v_{c1}(1-2\varphi_2) - v_{c2}(4\varphi_1-4\varphi_2+1)}{4L_\gamma f_s} \tag{26}$$

$$I_3 = \frac{v_{c1}(-4\varphi_1+2\varphi_2-1) + v_{c2}}{4L_\gamma f_s} \tag{27}$$

$$P_{DAB} = \frac{v_{c1}v_{c2}(4\varphi_1^2 - 4\varphi_1\varphi_2 + 2\varphi_2^2 + 2\varphi_1 - \varphi_2)}{2L_\gamma f_s} \tag{28}$$

To minimize the maximum turn-off current, some key variables, including a, b, c, M and K under different power flow directions are listed below.

$$M = \frac{V_{c2}}{V_{c1}} \tag{29}$$

$$K = \frac{2L_\gamma f_s P_{DAB}}{V_{c1}V_{c2}} \tag{30}$$

$$a = 16\left[V_{c1}^2 + (V_{c1} - 2V_{c2})^2\right] \tag{31}$$

$$b = 8\left[V_{c1}^2 + (V_{c1} - 2V_{c2})^2\right] \times sgn(P_{DAB}) \tag{32}$$

$$c = \begin{cases} (8K-1)(V_{c1}-2V_{c2})^2 + V_{c1}^2 & P_{DAB} > 0 \\ (V_{c1}-2V_{c2})^2 - (8K+1)V_{c1}^2 & P_{DAB} < 0 \end{cases} \tag{33}$$

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REFERENCES

[1] A. Rodríguez, A. Vázquez, D. G. Lamar, M. M. Hernando and J. Sebastián, "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 790-804, Feb. 2015, doi: 10.1109/TPEL.2014.2309853.

[2] W. Xu, R. y. Yu, Z. Guo and A. Q. Huang, "Design of 1500V/200kW 99.6% Efficiency Dual Active Bridge Converters Based on 1700V SiC Power MOSFET Module," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 6000-6007, doi: 10.1109/ECCE44975.2020.9235903.

[3] F. Z. Peng, Gui-Jia Su and L. M. Tolbert, "A passive soft-switching snubber for PWM inverters," 2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289), Cairns, QLD, Australia, 2002, pp. 129-134 vol.1, doi: 10.1109/PSEC.2002.1023858.

[4] M. Mohammadi, E. Adib and M. R. Yazdani, "Family of Soft-Switching Single-Switch PWM Converters With Lossless Passive Snubber," in IEEE Transactions on Industrial Electronics, vol. 62, no. 6, pp. 3473-3481, June 2015, doi: 10.1109/TIE.2014.2371436.

[5] P. J. M. Menegaz, J. L. F. Vieira and D. S. L. Simonetti, "A magnetically coupled regenerative turn-on and turn-off snubber configuration," in IEEE Transactions on Industrial Electronics, vol. 47, no. 4, pp. 722-728, Aug. 2000, doi: 10.1109/41.857951.

[6] D. M. Divan, "Static Power Conversion Method and Apparatus Having Essentially Zero Switching Losses and Clamped Voltage Levels,"U.S. Pat. 4,864,483, Sept. 5, 1989.

[7] J. Bauman and M. Kazerani, "A Novel Capacitor-Switched Regenerative Snubber for DC/DC Boost Converters," in IEEE Transactions on Industrial Electronics, vol. 58, no. 2, pp. 514-523, Feb. 2011, doi: 10.1109/TIE.2010.2046576.

[8] S. J. Finney, B. W. Williams and T. C. Green, "RCD snubber revisited," in IEEE Transactions on Industry Applications, vol. 32, no. 1, pp. 155-160, Jan.-Feb. 1996, doi: 10.1109/28.485827.

[9] K. Fujiwara and H. Nomura, "A novel lossless passive snubber for soft-switching boost-type converters," in IEEE Transactions on Power Electronics, vol. 14, no. 6, pp. 1065-1069, Nov. 1999, doi: 10.1109/63.803400.

[10] B. Jayant Baliga, "Fundamentals of Power Semiconductor Devices", 2nd ed., Raleigh, NC, 2008, pp. 446-449.

[11] S. Sen, L. Zhang, T. Chen, J. Zhang and A. Q. Huang, "Three-phase Medium Voltage DC Fast Charger based on Single-stage Soft-switching Topology," 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, USA, 2018, pp. 1123-1128, doi: 10.1109/ITEC.2018.8450169.

[12] H. Shi, H. Wen, J. Chen, Y. Hu, L. Jiang and G. Chen, "Minimum-Reactive-Power Scheme of Dual-Active-Bridge DC–DC Converter with Three-Level Modulated Phase-Shift Control," in IEEE Transactions on Industry Applications, vol. 53, no. 6, pp. 5573-5586, Nov.-Dec. 2017, doi: 10.1109/TIA.2017.2729417.

[13] H. Bai and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge DC–DC Converters Using Novel Dual-Phase-Shift Control," in IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2905-2914, Nov. 2008, doi: 10.1109/TPEL.2008.2005103.

[14] W. Xu et al., "Hardware Design and Demonstration of a 100kW, 99% Efficiency Dual Active Half Bridge Converter Based on 1700V SiC Power MOSFET," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 2020, pp. 1367-1373, doi: 10.1109/APEC39645.2020.9124401.

[15] Qi Tian, "Modeling and Control of Single-stage Isolated AC/DC Converter," Ph.D. dissertation, Dept. ECE, NC State Univ., Raleigh, North Carolina, 2016.