# Design of 1500V/200kW 99.6% Efficiency Dual Active Bridge Converters Based on 1700V SiC Power MOSFET Module

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***Abstract*—High efficiency, high density and galvanically isolated power converters are attractive for medium voltage high power applications. This paper presents a 1.5kV/200kW bidirectional Dual Active Bridge (DAB) converter using a newly developed 1.7kV SiC MOSFET module. The intended application is megawatt scale solid state transformer (SST) and 1500V PV inverter application using modular architecture. One novel model to estimate the turn-off loss using snubber capacitors is proposed and experimentally verified. An optimized PCB-based busbar design is introduced to reduce the voltage overshoot across the SiC device, making the design suitable for 1.5kVdc applications. The mechanism of how the optimized PCB-based busbar can reduce the voltage overshoot is quantitatively interpreted and experimentally verified. The DAB converter achieved an efficiency of 98.85% at 200kW and a maximum of 99.53% at 60kW. The maximum efficiency for series-resonant mode is 99.6% at 85kW and 99.3% at 200kW. The power density is 26W/inch3 (1.6MW/m3) which is much higher than traditional industry products.**

***Keywords— Dual Active Bridge (DAB), Snubber Capacitors, PCB-based Busbar, Series Resonant, SiC MOSFET, Modular Converter, Bidirectional DC-DC***

## I. INTRODUCTION

Despite the advancement in SiC devices over the last few years, one hindrance to its wide adoption is its high cost. For 1500Vdc applications, such as utility scale PV inverter and solid state transformer (SST), using higher voltage rated SiC power devices or three level topologies is an expensive option. The proposed novel hardware design in this paper focuses on using newly developed $1700V$ SiC MOSFET module in $1500V$ applications. In using these devices in $1500V$ applications, the stray inductance of the commutation loop can cause significant voltage overshoot across the device [1-3], and therefore must be carefully designed and minimized.

Many studies have demonstrated the PCB-based busbar design in high power applications [4-6]. In general, a low stray loop inductance could reduce the voltage overshoot during turn off transient [4]. Several papers have discussed how the stray loop inductance affects the turn-on and turn-off losses [7-8]. However, quantitative analysis and overshoot prediction of the PCB-based busbar design and high frequency decoupling capacitors design have never been discussed in detail. Since voltage stress during the turn-off is very critical to the device reliability, especially in over current or short circuit condition, it is necessary to predict the overvoltage spike using the compact PCB-based busbar design. Meanwhile, in terms of system reliability, partial discharge becomes increasingly important in medium voltage applications [9]. Therefore, optimized PCB-based busbar design with low voltage overshoot and high PDIV (Partial Discharge Inception Voltage) is one of the research focuses.

The Dual Active Bridge (DAB), among many other isolated topologies, has an intrinsic ZVS turn-on capability as the transformer current is always lagging the primary side output voltage [10]. However, the turn-off loss is typically high since and can become the dominant part at heavy load and higher switching frequency. An external paralleled capacitor across the drain and source terminal, widely known as the $dV/dt$ snubber capacitor, can be used to decrease the turn-off loss. While many studies have reported the measured switching losses [11-12], a quantitative analysis of how the snubber capacitors influence the MOSFET channel loss have never been considered in detail.

In order to evaluate the feasibility of using $1700V$ SiC devices for $1500V$ applications, the mechanism of how the optimized PCB-based busbar reduces the voltage overshoot is needed. This paper proposes a quantitative voltage spike prediction model based on the extracted parameters in the optimized PCB-based busbar. For simplicity, lossless MOSFET channel model is adopted to replicate the turn off voltage oscillation which could guide the practical PCB copper trace layout and parameters design. $1kV/255A$ double pulse tests are performed to verify the feasibility of the proposed voltage overshoot model.

This paper also proposes an analytic model for estimating the turn-off loss reduction using snubber capacitors. An analytical equation for the MOSFET channel resistance during turn-off transient is proposed to separate the actual switching loss on MOSFET channel and the recyclable switching energy stored in the snubber capacitors. To prove the proposed turn-off loss model, numerical calculation and experimental results are demonstrated with a $1.3kV/200kW$ DAB back-to-back DC/DC test.

In addition, to achieve commercial readiness design, the concept of impedance tank is introduced in the DAB converter. The proposed power module could meet the requirements of "plug and play" using a compact power stage and magnetic tray design. By only changing the impedance tank located inside the magnetic tray, 1.3$kV$/200$kW$ DAB back-to-back DC/DC tests with both non-resonant and series-resonant modes are demonstrated and compared.

Finally, this proposed power module design can be used as a building block for medium voltage utility scale power electronic systems with input parallel and output series configuration.

## II. Lossless Snubber Capacitors

### A. New MOSFET Turn-off Loss Model

One of the main drawbacks of a non-resonant DAB converter is the high turn-off current introduced by its trapezoidal transformer current waveform. Fig. 1 shows a typical power loss distribution results of a 1.5$kV$/150$kW$ DAB DC/DC converter. The turn-off loss contributes 45% of the total power loss.

A capacitive snubber across the drain and source terminal can be used to decrease the turn-off loss at heavy load. In order to obtain the insight on how the external paralleled capacitors influence the turn-off loss, a turn-off loss model of the MOSFET channel during turn off transient is developed and introduced. Fig. 2(a) shows the typical waveforms for power MOSFET during turn-off. For simplicity, the drain voltage ($v_{ds}$) begins to increase linearly at time $t_1$, but the drain current ($i_{ds}$) remains constant. Part of the current is used to charge the output capacitance ($C_{gd}$ and $C_{ds}$), and part of them will flow through the channel $i_{ch}$. The channel current is responsible for the turn-off loss. From time $t_1$ to $t_2$, the channel current is given by [13]:

$$i_{ch}(t) = g_m \cdot (V_{GP} - V_{TH}) \quad (1)$$

Where, $V_{GP}$ is the plateau voltage, $V_{TH}$ is the gate threshold voltage, $g_m$ is the device transconductance. Between time $t_1$ and $t_2$, a drain-to-gate current $i_{GP}$ charges the gate-drain capacitance $C_{gd}$ and the drain voltage increases at an almost fixed rate, the plateau voltage is given by:

$$V_{GP} = R_g \cdot i_{GP} + V_{GS,Low} = R_g \left\{ C_{GD,av} \frac{dv_{ds}(t)}{dt} \right\} + V_{GS,Low} \quad (2)$$

Where, $R_g$ is the gate resistance of the driver circuit, $V_{GS,Low}$ is the gate voltage at driver input which is either zero or a negative value during the turn off, $C_{GD,av}$ is an assumed constant average value of the gate-drain capacitance (Miller capacitance) during the turn off.

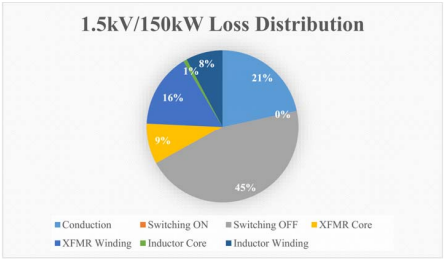



Fig. 1. Power loss distribution @ 1.5$kV$/150$kW$ operation

Fig. 2(b) shows the circuit model during turn off transient, the channel is modeled as a gate-voltage controlled current source. Between time $t_1$ and $t_2$, the governing differential equation with $v_{ds}(t)$ as the dependent variable is:

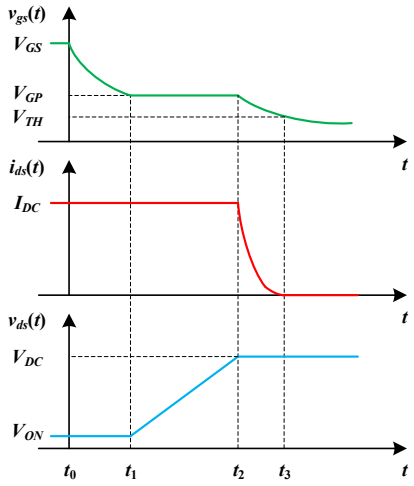
$$C_{MOS} \frac{dv_{ds}(t)}{dt} + i_{ch}(t) = I_{DC} \quad (3)$$

Where, $I_{DC}$ is the load instantaneous current at turn-off, $C_{MOS}$ is the total equivalent capacitance of the turning-off power MOSFET which is given by:

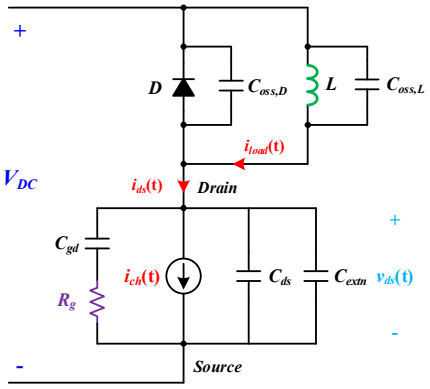
$$C_{MOS} = C_{oss,MOS} + C_{oss,D} + C_{mag} + C_{extn} \quad (4)$$

Where, $C_{oss,MOS}$ is the $C_{oss}$ of the turning-off MOSFET which typically equals to $C_{ds}$+$C_{gd}$, $C_{oss,D}$ is the free-wheeling MOSFET/body diode output capacitance, $C_{mag}$ is the parasitic capacitance of transformer or inductor winding, $C_{extn}$ is the external parallel capacitance across the drain and source terminal. Substituting equations (1-4), the above differential equation can be solved as:

$$v_{ds}(t) = \frac{I_{DC} + g_m V_{TH}}{C_{MOS} + g_m R_g C_{GD,av}} t \quad (5)$$




(a) Typical turn off waveforms




(b) Circuit model

Fig. 2. Switching off model of SiC MOSFET

At time $t_2$, the load current begins to transfer from the MOSFET to the freewheeling diode. Between time $t_2$ and $t_3$, the drain source voltage remains constant at $V_{DC}$ and the gate current discharges both the gate-source capacitance, therefore, the channel current follows the gate voltage until it reached zero at time $t_3$ when $V_{gs}$ reaches $V_{TH}$:

$$i_{ch}(t) = g_m\left[\left(V_{GP} - V_{GS,Low}\right)\cdot e^{\frac{t-t_2}{R_g C_{gs}}} + V_{GS,Low} - V_{TH}\right] \quad (6)$$

Where, $C_{gs}$ is the gate-source capacitance. Therefore, the instantaneous power loss dissipated in the MOSFET channel is due to the channel current:

$$P_{Loss}(t) = v_{ds}(t)\cdot i_{ch}(t) \quad (7)$$

Fig. 3 shows the turn off waveforms and instantaneous power curves with different snubber capacitances under $V_{DC}$=1200$V$, $I_{DC}$=300$A$ during turn off transient. All parameters about SiC MOSFET in above equations are extracted from experimental test and Wolfspeed's preliminary datasheet. The snubber capacitors reduced the maximum instantaneous power loss in the MOSFET substantially hence the turn-off energy is substantially reduced. With larger $C_{extn}$, the turn-off loss can be reduced to close to zero at the expense of much longer turn-off time due to the slow $dV/dt$.

Under $V_{DC}$=1200$V$, $I_{DC}$=300$A$ condition, the average loss in the MOSFET without snubber capacitors is 19.3$mJ$. Contrarily, the MOSFET loss with 10$nF$ snubber capacitors decreased by 61% to 7.5$mJ$. Due to the ZVS turn on capability of DAB, the energy stored in the snubber capacitors during turn off transient will be transferred to the load or source in the next switching cycle.

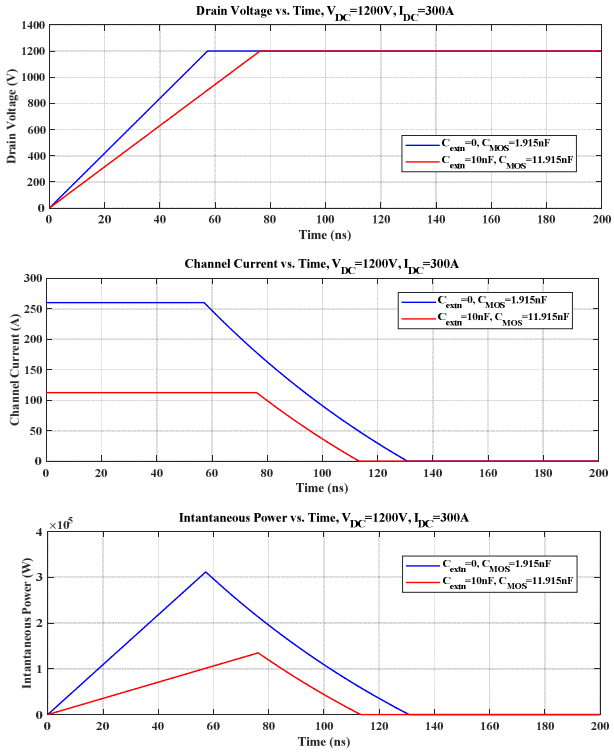



Fig. 3. Turn off waveforms and instantaneous power loss

## B. Optimal Snubber Selection

According to the equation (1) and (2), the MOSFET channel current is given by:

$$i_{ch}(t) = g_m\left[R_g\left\{C_{GD,av}\frac{dv_{ds}(t)}{dt}\right\} + V_{GS,Low} - V_{TH}\right] \quad (8)$$

If the channel current is reduced to zero, there is no turn-off loss. For one specific power MOSFET, gate resistance $R_g$ and system parameters, and the total equivalent capacitance $C_{MOS}$ is fixed. Therefore, the minimum $(dV/dt)_{\min}$ with snubber capacitors occurs when the equation (8) equals to zero which means the gate plateau voltage cannot be observed ($V_{GP}$=$V_{TH}$). Keep increasing the snubber capacitance beyond this point is useless while making the ZVS turn on harder. $(dV/dt)_{\max}$ corresponds to the case where no external snubber is used.

Between $(dV/dt)_{\max}$ and $(dV/dt)_{\min}$, the turn-off loss is getting lower and lower. However, high $C_{extn}$ will result in higher circulation current in a soft switching converter and longer deadtime requirement. Therefore, additional optimization is needed to consider both the turn-off loss and the conduction loss. Fig. 4 shows a typical $dV/dt$ optimization example using Wolfspeed's half bridge module HT-3234-R-VB under $V_{DC}$=1300$V$, $I_{DC}$=200$A$. The optimized snubber capacitance is around 8$nF$ where partial ZVS is achieved and the total device loss (including conduction loss) is minimized.

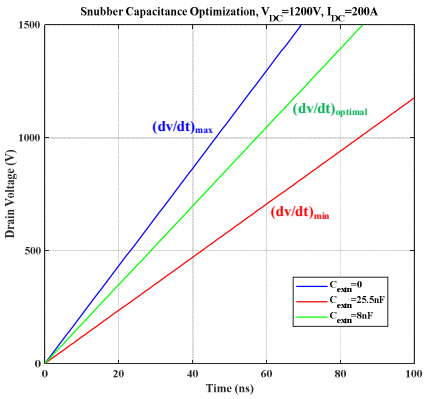



Fig. 4. 1200/200A snubber capacitance optimization

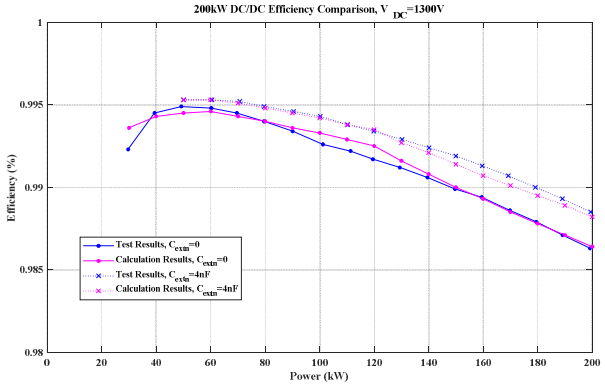



Fig. 5. 200kW DAB back-to-back DC/DC efficiency comparison

### C. Experiment Verification

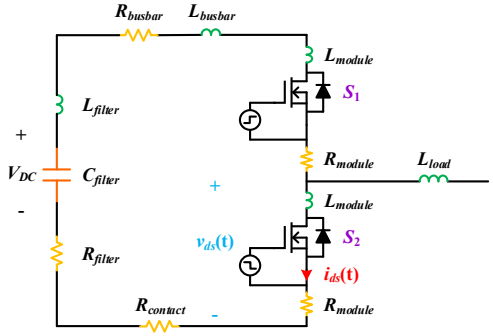
To verify the accuracy of the new MOSFET channel loss model, a 1.3$kV$/200$kW$ DAB back-to-back DC/DC test was performed. The switching frequency is fixed at 15$kHz$. Only primary side MOSFET devices are paralleled with 4$nF$ snubber capacitors in the test. Fig. 5 shows the 200$kW$ back-to-back DC/DC efficiency comparison. Using the above MOSFET channel model, the calculated efficiency with $C_{extn}$=4$nF$ is around 0.16% higher than the calculated efficiency without snubber capacitors, while the test efficiency with $C_{extn}$=4$nF$ is around 0.2% higher than the test efficiency without snubber capacitors. This indirectly validates the proposed loss model and snubber selection procedure and they can be used for future high power SiC MOSFET power module application.

## III. Optimized PCB-based Busbar

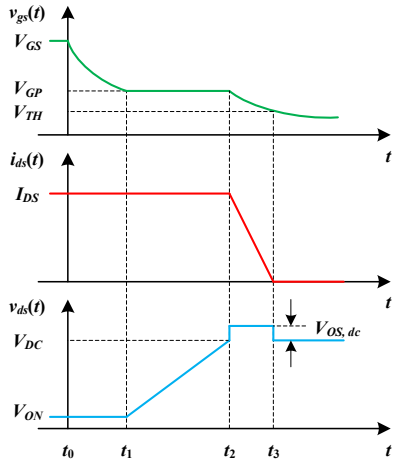
In section II, loop inductance and resistance during turn off transient were neglected for simplicity. However, to evaluate the feasibility of using 1700$V$ SiC devices for a 1500$V$ application, the mechanism of the optimized PCB-based busbar reduces the voltage overshoot should be given.

### A. Traditional PCB Busbar

Fig. 6(a) shows a typical circuit model of the half bridge MOSFET module. $L_{filter}$ and $R_{filter}$ are the equivalent *ESL* and *ESR* of the DC filter capacitors, $L_{busbar}$ and $R_{busbar}$ are the equivalent stray inductance and resistance of the PCB busbar, $L_{module}$ and $R_{module}$ are the extracted stray inductance and resistance inside Wolfspeed's module HT-3234-R-VB, $R_{contact}$ is the contact resistance between SiC module and busbar terminal. Fig. 6(b) shows the turn off waveforms of the bottom device $S_2$. Similar to the turn off transient in section II, the load current begins to transfer from the power MOSFET to the freewheeling diode at time $t_2$. Due to the loop inductance $L_{loop}$, there is an voltage overshoot across the drain and source terminal of the device $S_2$. Between time $t_2$ and $t_3$, the differential equation with $v_{ds}(t)$ as the dependent variable is shown in equation (9).




(a) Circuit model




(b) Theoretical turn off waveforms

Fig. 6. Circuit analysis for traditional PCB busbar

For simplicity, assuming there is no power loss dissipation in the MOSFET, the equation could be simplified as:

$$L_{loop}C_{ds}\frac{d^2v_{ds}(t)}{dt^2} + R_{loop}C_{ds}\frac{dv_{ds}(t)}{dt} + v_{ds}(t) - V_{DC} = 0 \quad (10)$$

$$L_{loop} = L_{filter} + L_{busbar} + L_{module} \approx 57nH \quad (11)$$

$$R_{loop} = R_{filter} + R_{busbar} + R_{contact} + R_{module} \approx 0.27\Omega \quad (12)$$

Where $C_{ds}$ is the equivalent capacitance across the drain and source terminal of the device $S_2$. Using the initial condition at time $t_2$, the equation (10) can be solved as (13) and (14).

$$V_{OS,dc} = L_{loop}\frac{di_{ds}(t)}{dt} = L_{loop}\frac{I_{ds}}{t_3 - t_2} \approx 285V \quad (14)$$

Where, $V_{OS,ds}$ is the DC average value of the overvoltage shoot across the drain and source terminal, $t_{CNS}$ is a calculated value when the initial condition $v_{ds}(t_2)$=$V_{DC}$, $t_1$, $t_2$, and $t_3$ are the calculated values from the model in the section II. Table I shows the stray parameters values of the circuit model.

TABLE I. Parasitic Parameters of Traditional Busbar

| Location | Symbol | Value |
|---|---|---|
| ***DC filter*** | $L_{filter}$ | 35$nH$ |
| | $R_{filter}$ | 12$m\Omega$ |
| ***Busbar*** | $L_{busbar}$ | 15$nH$ |
| | $R_{busbar}$ | 2.1$m\Omega$ |
| | $R_{contact}$ | 0.25$\Omega$ |
| ***SiC module*** | $L_{module}$ | 7$nH$ |
| | $R_{module}$ | 5$m\Omega$ |
| | $C_{ds}$ | 1.4$nF$ |
| | $C_{pk}$ | 2$nF$ |

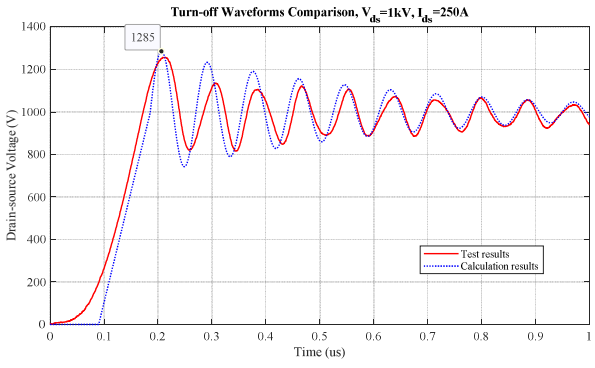



Fig. 7. Turn-off waveforms comparison for traditional PCB busbar

$$L_{loop}C_{ds}\frac{d^2v_{ds}(t)}{dt^2}+L_{loop}\frac{d}{dt}\left(\frac{v_{ds}(t)}{R_{MOS}(t)}\right)+R_{loop}C_{ds}\frac{dv_{ds}(t)}{dt}+\frac{R_{loop}+R_{MOS}(t)}{R_{MOS}(t)}v_{ds}(t)=V_{DC} \quad (9)$$

$$v_{ds}(t)=V_{DC}+\frac{V_{OS,dc}}{2}\cdot e^{\frac{t-t_2-t_{CNS}}{2}\left(-\frac{\sqrt{C_{ds}R_{loop}^2-4\cdot L_{loop}}}{\sqrt{C_{ds}}\cdot L_{loop}}-\frac{R_{loop}}{L_{loop}}\right)}+\frac{V_{OS,dc}}{2}\cdot e^{\frac{t-t_2-t_{CNS}}{2}\left(\frac{\sqrt{C_{ds}R_{loop}^2-4\cdot L_{loop}}}{\sqrt{C_{ds}}\cdot L_{loop}}-\frac{R_{loop}}{L_{loop}}\right)} \quad (13)$$

$$v_{ds}(t)=v_{dc}(t)+\frac{V_{OS,dc1}}{2}\cdot e^{\frac{t-t_2}{2}\left(-\frac{\sqrt{C_{ds}R_{loop1}^2-4\cdot L_{loop1}}}{\sqrt{C_{ds}}\cdot L_{loop1}}-\frac{R_{loop1}}{L_{loop1}}\right)}+\frac{V_{OS,dc1}}{2}\cdot e^{\frac{t-t_2}{2}\left(\frac{\sqrt{C_{ds}R_{loop1}^2-4\cdot L_{loop1}}}{\sqrt{C_{ds}}\cdot L_{loop1}}-\frac{R_{loop1}}{L_{loop1}}\right)} \quad (15)$$

$$v_{dc}(t)=V_{DC}+\frac{V_{OS,dc2}}{2}\cdot e^{\frac{t-t_2-t_{CNS2}}{2}\left(-\frac{\sqrt{C_{ds}R_{loop2}^2-4\cdot L_{loop2}}}{\sqrt{C_{ds}}\cdot L_{loop2}}-\frac{R_{loop2}}{L_{loop2}}\right)}+\frac{V_{OS,dc2}}{2}\cdot e^{\frac{t-t_2-t_{CNS2}}{2}\left(\frac{\sqrt{C_{ds}R_{loop2}^2-4\cdot L_{loop2}}}{\sqrt{C_{ds}}\cdot L_{loop2}}-\frac{R_{loop2}}{L_{loop2}}\right)} \quad (19)$$

Fig. 7 shows the theoretical $v_{ds}(t)$ calculated from equation (13) using the parameters in Table I and the actual double pulse test result under $1kV/255A$. The maximum overshoot value calculated from the above circuit model is $1285V$ which is close to the actual test value $1274V$.

### B. Optimized PCB Busbar

To further reduce the overshoot across the drain and source terminal, an optimized PCB-based busbar and high frequency decoupling capacitors are used. Fig. 8 shows the 3D model of Wolfspeed's half bridge module HT-3234-R-VB. The AC terminal is in the middle of the DC+ and DC- terminals. The internal SiC dies are also distributed in the same structure. This allows the possibility to drastically reduce the commutation loop's size assuming an appropriate layout. Fig. 9 shows the optimized PCB-based busbar layout. To reduce commutation length, the middle terminal of the mid-point is eliminated (see Fig. 8) and high frequency decoupling capacitors are placed there instead to fully utilize the effective area on the top of the SiC module. A sandwich structure of PCB copper trace is adopted to get a higher parasitic capacitance between DC links.

TABLE II. PARASITIC PARAMETERS OF PCB BUSBAR

| Location | Symbol | Value |
|---|---|---|
| ***DC filter*** | $L_{filter}$ | $35nH$ |
| | $R_{filter}$ | $12m\Omega$ |
| ***Busbar*** | $L_{busbar1}$ | $5nH$ |
| | $R_{busbar1}$ | $0.5m\Omega$ |
| | $R_{contact1}$ | $0.1\Omega$ |
| | $L_{busbar2}$ | $10nH$ |
| | $R_{busbar2}$ | $0.5m\Omega$ |
| | $R_{contact2}$ | $0.15\Omega$ |
| ***Decoupling*** | $L_{decouple}$ | $1nH$ |
| | $R_{decouple}$ | $0.05m\Omega$ |
| | $C_{decouple}$ | $90nF$ |
| ***SiC module*** | $L_{module}$ | $7nH$ |
| | $R_{module}$ | $5m\Omega$ |
| | $C_{ds}$ | $1.4nF$ |
| | $C_{pk1}$ | $0.5nF$ |

Compared to the traditional busbar design discussed, two different and more compact commutation loops are introduced. Fig. 10 shows the circuit model of the optimized PCB-based busbar operating under buck mode. $L_{decouple}$ and $R_{decouple}$ are the equivalent *ESL* and *ESR* of the high frequency decoupling capacitors. Since the decoupling capacitors are placed between the filter capacitors and the SiC module, $L_{busbar}$, $R_{busbar}$ and $R_{contact}$ are automatically separated into different segments inside the corresponding small loops. Table II shows the stray parameters values of the circuit model shown in the Fig. 10.

To simplify the analysis how the decoupling capacitors reducing the voltage spike across SiC device, assuming the voltage across the decoupling capacitors $v_{dc}(t)$ keep constant is appropriate since the resonant frequency in loop 1 is much higher than that in loop 2. Using the equation (7), the theoretical voltage across the drain and source terminal of device $S_2$ is shown in equation (15) – (18).

$$L_{loop1}=L_{decouple}+L_{busbar1}+L_{module}\approx 13nH \quad (16)$$

$$R_{loop1}=R_{decouple}+R_{busbar1}+R_{contact1}+R_{module}\approx 0.1\Omega \quad (17)$$

$$V_{OS,dc1}=L_{loop1}\frac{di_{ds}(t)}{dt}=L_{loop1}\frac{I_{ds}}{t_3-t_2}\approx 25V \quad (18)$$

Where, $V_{OS,ds1}$ is the high frequency component peak value of the overvoltage shoot across the drain and source terminal of the device $S_2$, $t_{CNS}$ is the calculated value when the initial condition $v_{ds}(t_2)=V_{DC}$, $t_1$, $t_2$, and $t_3$ are the calculated time constants from the model in the section II. Table II shows the parameters values of the circuit model shown in the Fig. 10. Part of the values in table II are extracted from the ANSYS/Q3D simulation. Using the equation (10), the voltage across the decoupling capacitors can be solved as equation (19) – (22).

$$L_{loop2}=L_{decouple}+L_{busbar2}+L_{filter}\approx 36nH \quad (20)$$

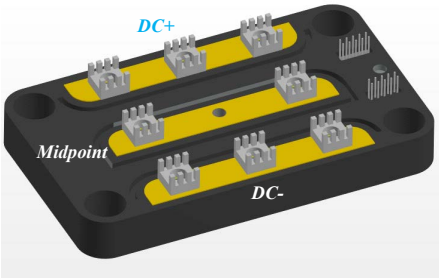



Fig. 8. Wolfspeed's HT-3234-R-VB & Connectors

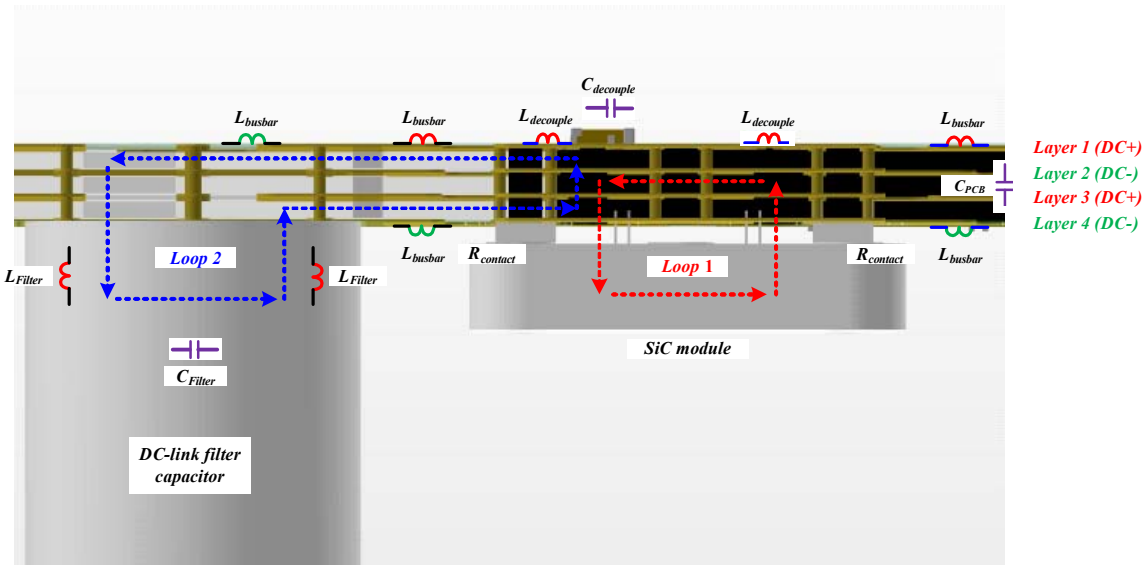



Fig. 9. Optimized PCB-based busbar layout

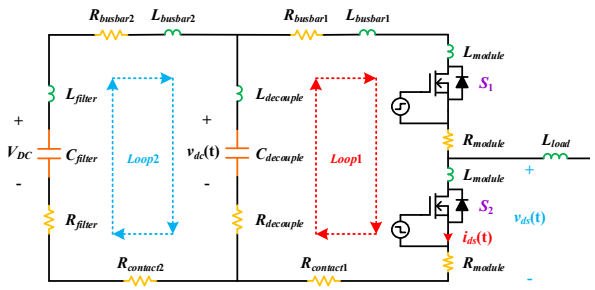



Fig. 10. Circuit model of the optimized PCB-based busbar

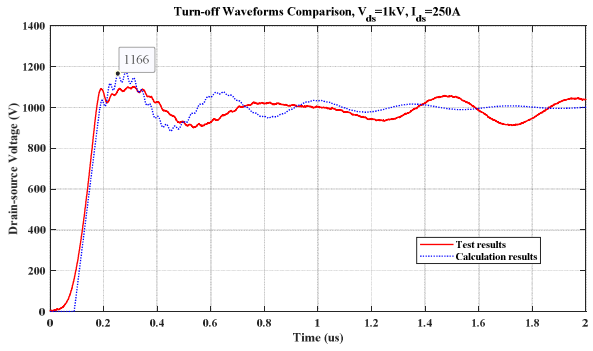



Fig. 11. Turn-off waveforms comparison for optimized PCB busbar

$$R_{loop2} = R_{decouple} + R_{busbar2} + R_{contact2} + R_{filter} \approx 0.16\Omega \quad (21)$$

$$V_{OS,dc2} = L_{loop2}\frac{di_{ds}(t)}{dt} = L_{loop1}\frac{I_{ds}}{t_3 - t_2} \approx 150V \quad (22)$$

Where $t_{CNS2}$ is the calculated coefficient when the initial condition $v_{ds}(t_2)=V_{DC}$. Fig. 10 shows the theoretical $v_{ds}(t)$ calculated from equation (15) and the actual test results under $1kV/255A$. The maximum overshoot value calculated from the above circuit model is $1166V$ which is close to the actual test value $1108V$. Compare the test results in the Fig. 7 and Fig. 10, the maximum overshoot is only $108V$ with optimized PCB-based busbar which is 39% of that with traditional busbar. Therefore, the optimized PCB busbar significantly reduced the overshoot voltage across the devices, and this validates the proposed voltage overshoot prediction can be used for the $1700V$ SiC module in $1500V$ applications.

## IV. Prototype and Experiment Results

### A. Commercial Level Design

In order to achieve commercial readiness design, the concept of impedance tank is introduced in the DAB converter. By only changing the impedance tank located inside the magnetic tray, the power module could meet the requirements of "plug and play" for industry application. Fig. 12 shows the prototype pictures of the proposed DAB converter. The impedance tank shown in the Fig. 12(c) could be single inductor or inductor capacitor in series.

### B. Experiment Results

Series resonant DAB as shown in the Fig. 12(c) could achieve lower turn-off current with higher RMS value of the transmission power. The turn-off current of series resonant DAB is much lower than that of non-resonant DAB and the rms value of transformer current of series resonant DAB is higher than that of non-resonant DAB with the same phase shift angle which means series resonant DAB could get the same transmission power with a smaller phase shift angle.

Fig. 13 shows the experimental efficiency results between the non-resonant and series-resonant DAB modes with input voltage equals to $1300V$. The switching frequency is fixed at $15kHz$. The maximum efficiency points are 99.53% at $60kW$ for non-resonant mode and 99.6% at $90kW$ for series resonant mode. The temperature rises on the PCB surface, transformer core &

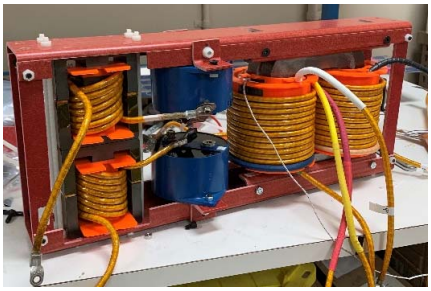
winding and external inductors are 25°*C*, 29°*C* and 36°*C*, respectively.

## V. Conclusions

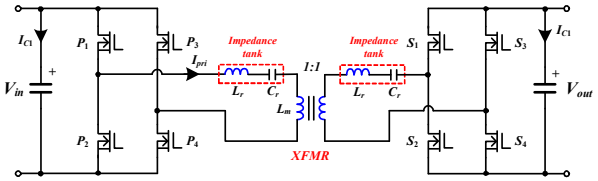
This paper proposes a novel quantitative model to estimate the turn-off loss using lossless snubber capacitors. Analytic equations for the MOSFET channel current and the drain voltage during turn off transient are derived in order to separate the actual switching loss on MOSFET channel and the recyclable switching energy stored in the lossless snubber capacitors. A 1.3*kV*/200*kW* DC/DC back-to-back experiment is performed to verify the feasibility and accuracy of the proposed MOSFET turn-off loss model. The experiment results validate the proposed MOSFET loss model and optimization procedure.

This paper also proposes a quantitative model for predicting the voltage spike value during turn-off transient. The mechanism of how the optimized PCB-based busbar and decoupling capacitors reduce the voltage overshoot are interpreted. Based on some test data and ANSYS/Q3D extracted parameters, the quantitative model successfully replicates the voltage oscillation across the drain and source terminals. 1*kV*/255*A* double pulse tests are performed to verify the feasibility of the proposed voltage overshoot model. The tolerance is in the range of +/-60*V* which is around 6% of the actual operation DC link voltage. In order to better estimate the voltage overshoot, more tests and analysis are needed in the future.

(a) Power stage



(b) Magnetic tray

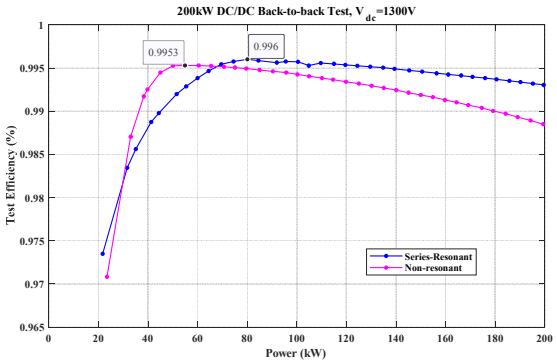



(c) DAB converter with impedance tank

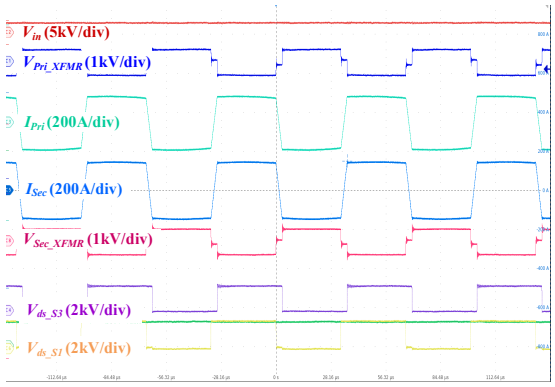
Fig. 12. Prototype pictures of the proposed DAB converter

To achieve the commercial readiness, the concept of impedance tank is used in the hardware design. By only changing the mechanical parts on the magnetic tray, 1.3*kV*/200*kW* DAB back-to-back DC/DC tests with both non-resonant and series-resonant modes are demonstrated and compared. The non-resonant DAB converter achieved an efficiency of 98.85% at 200*kW* and a maximum of 99.53% at 60*kW*. The maximum efficiency for series-resonant mode is 99.6% at 85*kW* and 99.3% at 200*kW*.

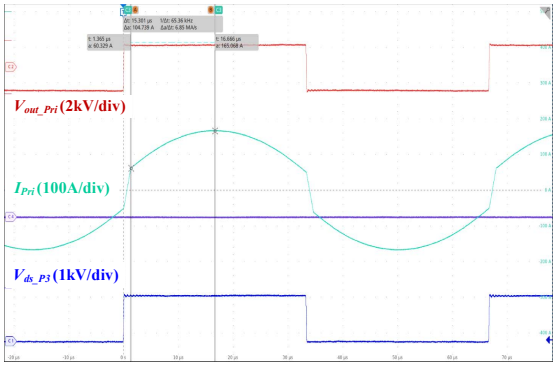
The power density is 26*W*/*inch*$^3$ (1.6*MW*/m$^3$) which is much higher than traditional industry products and potential as a building block for medium voltage utility scale power electronic systems with input parallel and output series configuration.




(a) Efficiency comparison




(b) Non-resonant mode




(c) Series-resonant mode

Fig. 13. Experimental test results

The series resonant mode has achieved better efficiency than traditional non-resonant mode, more analysis and optimization on the resonant mode for both DC/DC and DC/AC operation could be an interesting research work.

PCB thermal test results showed adding more thinner layers would not have a detrimental effect, thus more layers can be used to get higher parasitic capacitance and achieve a lower voltage overshoot or remove the DC link snubber capacitors. The input-parallel-output-series (IPOS) configuration could be used to expand both voltage and power ratings for three phase medium voltage high power applications. Further study would be needed to address input current sharing issues and output multilevel voltage balancing control.

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