Hardware Design and Demonstration of a 100kW, 99% Efficiency Dual Active Half Bridge Converter Based on 1700V SiC Power MOSFET

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***Abstract*—High efficiency, high density and galvanically isolated power converters are attractive for numerous medium voltage high power applications. This paper presents a 1.5kVdc, 100kW bidirectional Dual Active Half Bridge (DAHB) using newly developed 1.7kV SiC MOSFET modules. The DAHB achieved an efficiency of 98.6% at full load of 100kW and a maximum of 99% at 45kW, operating as an isolated DC/DC converter. The converter also achieved an efficiency of 97.8% operating as an isolated DC/AC inverter. An optimized PCB-based busbar design has significantly reduced the voltage overshoot across the device, making the design suitable for 1500Vdc input application such as 1500V PV inverters. Typical partial discharge inception voltage (PDIV) of the optimized PCB busbar is 1.7kVpeak with total charge <10pC. The power density of the DAHB converter is 1.8MVA/m^3 which is much higher than traditional two-stage industry products. The DAHB converter can be used as a building block for a 4.16kV/1MVA utility scale PV systems with input parallel and output series configuration.**

Keywords—Dual Active Half Bridge (DAHB), Bidirectional DC-DC, Single Stage DC-AC, PCB-based Busbar, Modular Converter, SiC MOSFET, PV Inverter

I. INTRODUCTION

Fig. 1 shows the architecture of conventional utility scale PV power plants. Typically, PV power plant consists of PV panels, a central solar inverter and a bulky line frequency transformer. The solar inverter consist of a single or two-stage energy conversion circuit with or without galvanically isolation and is tasked with the responsibilities of MPPT and producing a steady AC voltage at the output. However, with respect to efficiency, reliability and power density, single stage solutions are increasingly preferred [1, 2]. In the future, SiC based PV inverters, coupled with advanced topology and control, can offer substantial levelized cost of energy (LCOE) reduction in PV farms. One of such topologies is to use a single stage isolated DC/AC inverter and connect the PV directly to the medium voltage grid without the line frequency transformer. This approach is the motivation of the presented work aimed at developing a 1500Vdc to 4160V medium voltage PV inverter.

Fig. 1. Typical utility scale solar power plant architecture

Despite the advancement in SiC devices over the years, one hindrance is still its high cost. For 1500Vdc PV applications, using higher voltage rated SiC power devices or three level topologies is an expensive option. The proposed converter will therefore focus on using newly developed 1700V SiC MOSFET module in 1500V PV applications. In using these devices in 1500V applications, the stray inductance of the commutation loop can cause significant voltage overshoot across the devices especially during cold start-up [3]. [4] presents a PCB busbar design based on a SiC half bridge module HT-3231-R from Wolfspeed. The PCB busbar significantly increased the power density compared to traditional laminated copper busbar. However, the copper trace design does not completely overlap the current path inside the SiC module, and therefore, cannot fully exploit the symmetric packaging advantage of HT-3231-R. Meanwhile, in terms of system reliability, partial discharge becomes increasingly important in medium voltage applications [5]. Therefore, low stray inductance PCB-based busbar design with high Partial Discharge Inception Voltage (PDIV) is one of the research focuses.

The well-known Dual Active Half Bridge (DAHB) has low component count and an intrinsic soft turn-on capability as the transformer current is always lagging the primary side half bridge output voltage [6]. For DC/AC operation, accurate C_{oss}/Q_{oss} extraction is necessary in order to achieve ZVS turn on over the full voltage range. The turn off loss is dominant when operating at heavy power load or high turn-off current condition. Lossless snubber capacitors across each device are proposed as a possible solution to increase the efficiency at heavy load. All these hardware design advantages make the DAHB modular converter feasible for high power applications. The input parallel output series configuration could easily scale the DAHB modular converter to medium voltage applications.

The objective of this paper is to develop a 1.5kV/100kW DAHB modular converter with high efficiency, high power density and high reliability. C_{oss}/Q_{oss} data of the 1.7kV SiC MOSFET module must be extracted to achieve ZVS turn on

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over full voltage range. Lossless snubber capacitors need to be analyzed and implemented to achieve high efficiency at heavy load. Secondly, in order to realize 1.5kV field applications especially for the cold start-up situation, an optimized PCB-based busbar design could significantly decrease the voltage spike across the devices. Furthermore, a 100kW transformer with high power density and high PDIV is designed to achieve output cascaded medium voltage applications. Finally, this paper provides experimental results to prove the feasibility of the 1.5kV/100kW DAHB modular converter.

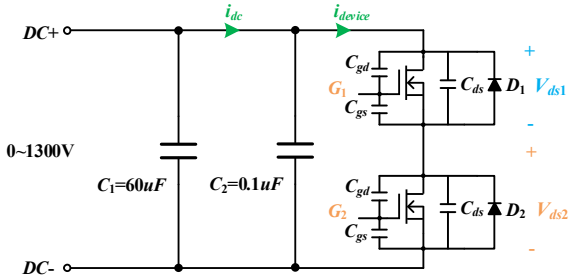
II. SiC Power Module C_{OSS}/Q_{OSS} Extraction

Fig. 2 shows the C_{oss}/Q_{oss} test circuit and typical waveforms. According to the typical waveforms, the top device and bottom devices are switched on and off at fixed frequency and both C_{oss1} and C_{oss2} are charged only one time by i_{device} within one switching cycle. Assuming the output charge of each device S_1 and S_2 are equal and the average charge of capacitors C_1 and C_2 equal to zero, the total equivalent output charge of SiC MOSFET power module can be derived as [7]:

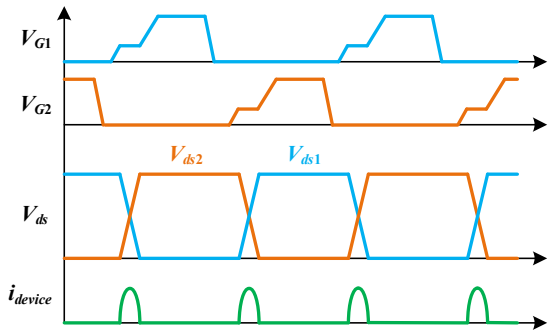
$$Q_{oss}|_{V_{ds}} = I_{device\_avg}/2f_s \tag{1}$$

Where V_{ds} is the voltage across the drain source terminal, I_{device_avg} is the mean value of i_{device} shown in the Fig. 2(a), and f_s is the switching frequency which is 20kHz in the test.

In order to get detailed Q_{oss} data, ranging from 0V to the maximum operating voltage, the curve fitting method proposed in [8] is used to express the equivalent capacitance:



(a) Q_{oss} test circuit



(b) Typical theretical waveforms

Fig. 2. C_{oss}/Q_{oss} extraction test circuit and theretical waveforms

$$C_{oss}(V_{ds}) = \frac{k}{\sqrt{V_{ds}+V_{bi}}} + C_{pk} \tag{2}$$

Where V_{ds} is the voltage across the drain source terminal, V_{bi} is the built-in potential of the SiC PN junction, C_{pk} is the parasitic capacitance, such as package and test setup related, k is determined by the dimension of the die, dielectric constant of SiC, doping concentration and the elementary charge.

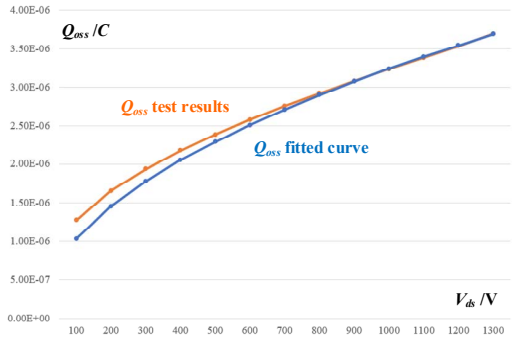
The equivalent output charge Q_{oss} can be computed as the integral of the output capacitance:

$$\begin{aligned} Q_{oss}(V_{dc}) &= \int_0^{V_{dc}} \left(\frac{k}{\sqrt{V_{ds}+V_{bi}}} + C_{pk} \right) dV_{ds} \\ &= 2k\left(\sqrt{V_{dc}+V_{bi}} - \sqrt{V_{bi}}\right) + C_{pk}V_{dc} \end{aligned} \tag{3}$$

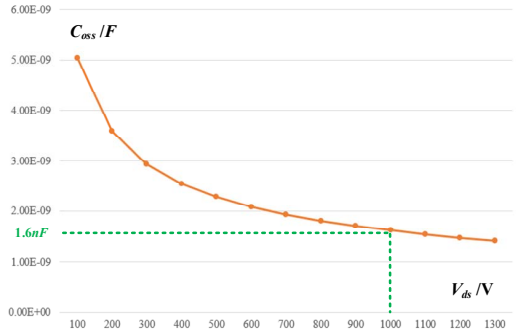
The Q_{oss} test results and the corresponding Q_{oss} using curve fitting are presented in Fig. 3(a) and the relative output capacitance model is shown in Fig. 3(b). The derived model fit well to the C_{oss} value of 1.44nF @1kV provided by Wolfspeed's datasheet.

III. Lossless Snubber Capacitors

Fig. 4(a) shows the equivalent capacitor model including the external lossless snubber capacitor of the MOSFET power device. The paralleled snubber capacitor provides a low impedance current path compared to the MOSFET channel when switching off the device. The switching energy stored in



(a) Output charge Q_{oss}



(b) Output capacitance C_{oss}

Fig. 3. Measured C_{oss}/Q_{oss} of Wolfspeed 1700V SiC MOSFET module

this capacitor is released to the load or source again when the load current in the next switching period meets the minimum ZVS turn on condition.

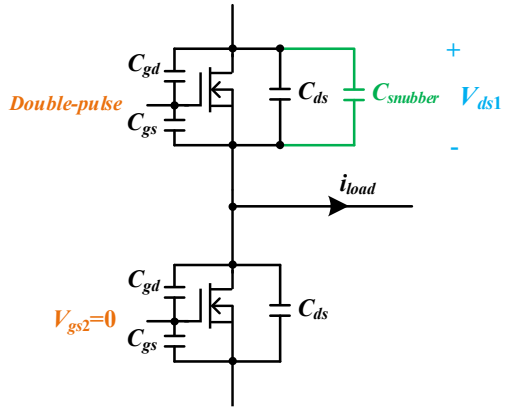
According to the definition of instantaneous switching off energy, the E_{off} in each switching period can de derived as:

$$E_{off} = \frac{1}{2} V_{ds} i_{load} t_{off} - \int V_{ds} dQ_{oss} \quad (4)$$

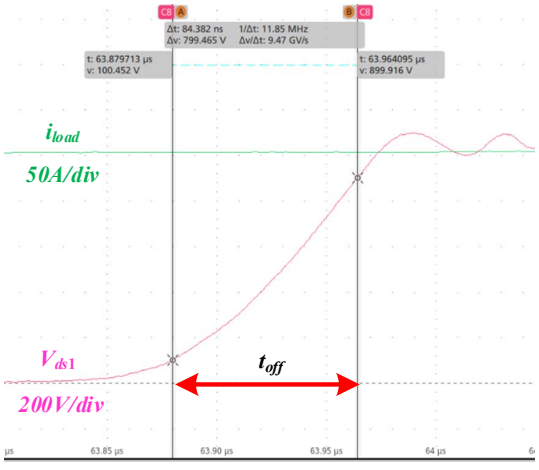
When considering the external snubber capacitors, the equation can be re-written as:

$$E_{off} = \frac{1}{2} V_{ds} i_{load} t_{off} - \int V_{ds} dQ_{oss} - \frac{1}{2} C_{snubber} V_{ds}^2 \quad (5)$$

The results between different cases based on a 1kV/250A double pulse test are compared in Table I. The corresponding test circuit and items definition in the hard switching turn off period are shown in Fig. 4. The test results suggest lossless snubber capacitors can significantly reduce the turn off loss which is a dominant part at heavy power load operation mode.



(a) Turn off switching loss test circuit



(b) Typical test waveforms

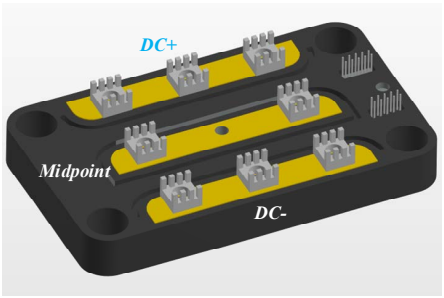
Fig. 4. Turn off switching loss test circuit and wavefroms

TABLE I. SWITCHING OFF LOSS TEST RESULTS

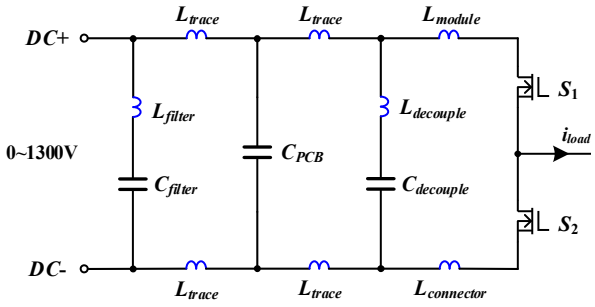
Condition	Different Test Cases		
	No snubber	*Snubber case* 1	*Snubber case* 2
$C_{snubber}$ / nF	0	4	16
t_{off} / ns	84.4	88.24	104.7
i_{load} / A	253	253	253
E_{off} / mJ	9.6	7.9	4.0
p.u.	100%	84%	42%

IV. OPTIMIZED PCB-BASED BUSBAR DESIGN

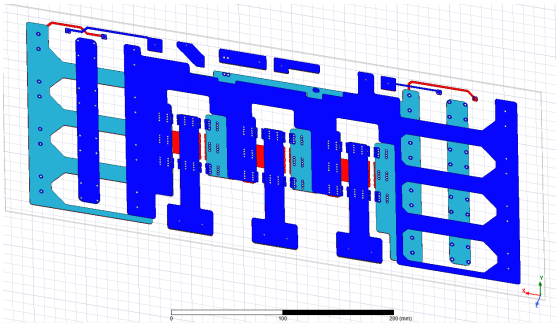
Fig. 5 shows the 3D model of Wolfspeed's half bridge module HT-3234-R-VB with connectors. The AC terminal is in the middle of the *DC*+ and *DC*- terminals. The internal SiC dies are also distributed in the same structure. This allows the possibility to drastically reduce the commutation loop's size and inductance assuming an appropriate layout.



(a) Wolfspeed's HT-3234-R-VB & Connectors



(b) Parasitic parameters circuit model



(c) ANSYS/Q3D simulation model

Fig. 5. Optimized PCB-based busbar equivalent model

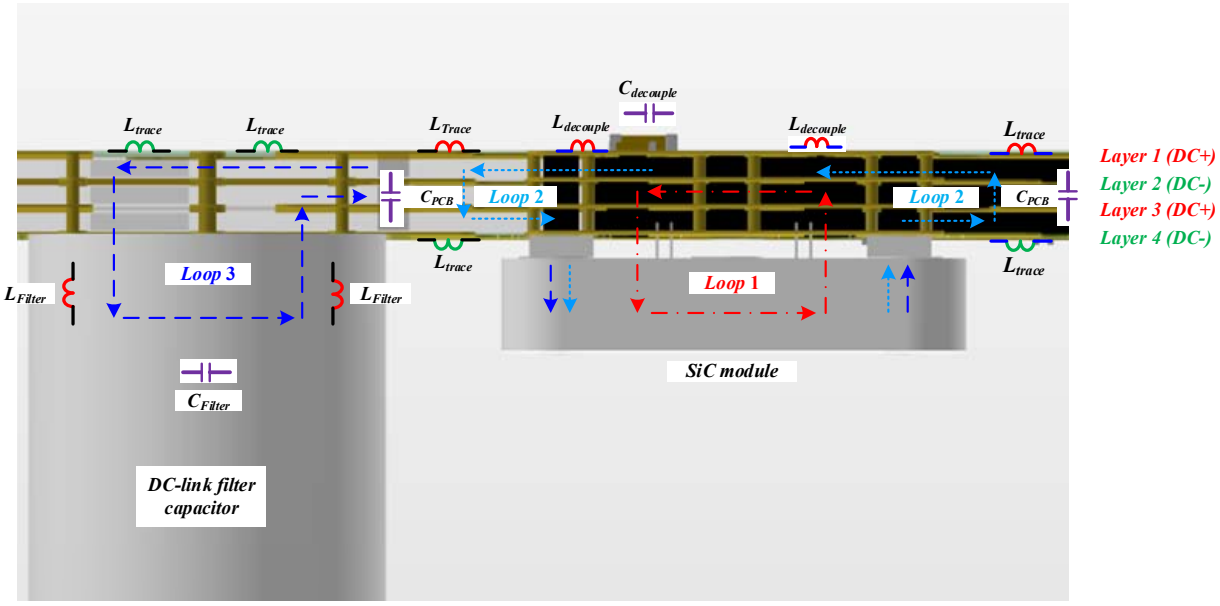


Fig. 6. Optimized PCB layout based on equivalent circuit model

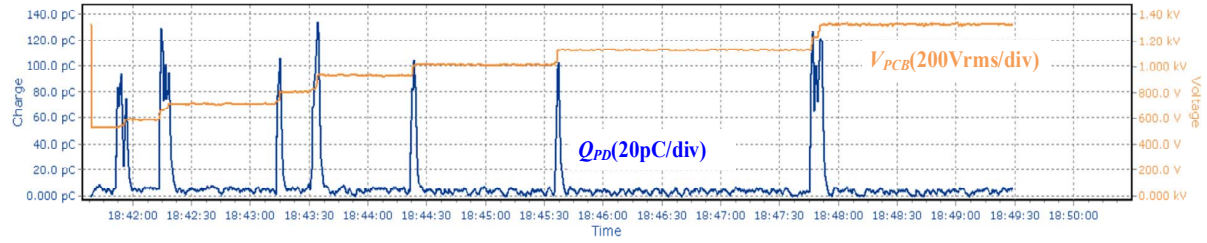


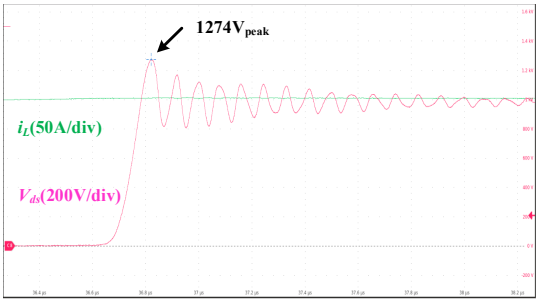
Fig. 7. Partial discharge test results of optimized PCB

The equivalent loop inductance is affected by four different major inductances in the design – the internal module structure (L_{module}), the PCB trace (L_{PCB}), the high-frequency decoupling ceramic capacitors ($L_{decouple}$), and DC-link filter capacitors (L_{filter}). The latter three branches can, in turn, effect the sharing of high frequency switching current and ultimately determine the final voltage spike across the module die. The equivalent circuits are shown in Fig. 5(b). The parameter C_{PCB} is the parasitic capacitance between the positive and negative busbar which are laid out using a sandwich structure. $C_{decouple}$ is the high voltage ceramic capacitors (3640 packaging size) which are put very close to the *DC*+ and *DC*- terminals on PCB. C_{filter} is the DC-link film capacitors which are used to limit the voltage ripple. L_{module} is the internal parasitic inductance from the datasheet.

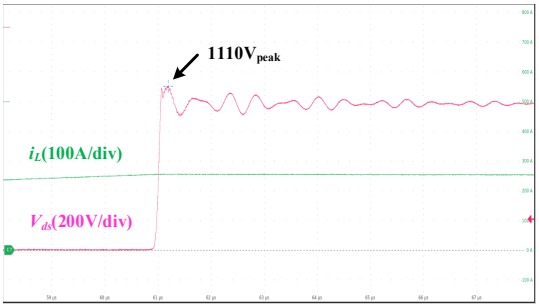
Using the ANSYS/Q3D simulation model shown in Fig. 5(c), Table II lists all parameters' simulation results related to the equivalent circuit model. Fig. 6 shows the actual PCB layout based on the hybrid equivalent circuit. To reduce commutation length, the middle terminal of the mid-point is eliminated (see Fig. 4(a)) and high frequency decoupling capacitors are placed there instead to fully utilize the effective area on the top of the power module. Fig. 7 shows the dynamic partial discharge which proved the reliability for the 1.7kV peak application.

TABLE II. PCB PARASITIC PARAMETERS SIMULATION RESULTS

Location	Parasitic Parameters		
	Inductance	***Capacitance***	***Resistance***
Decoupling capacitors	$L_{connector}$	$C_{connector}$	$R_{connector}$
	$0.3nH$	N.A.	$0.04m\Omega$
	$L_{decouple}$	$C_{decouple}$	$R_{decouple}$
	$0.9nH$	$90nF$	$0.05m\Omega$
PCB busbar	L_{trace}	C_{PCB}	R_{PCB}
	N.A.	$2.6nF$	N.A.
DC filter	L_{filter}	C_{filter}	R_{filter}
	$15nH$	$50uF$	$2.1m\Omega$
SiC module	L_{module}	C_{module}	R_{module}
	$7nH$	$2pF$	$2.5m\Omega$

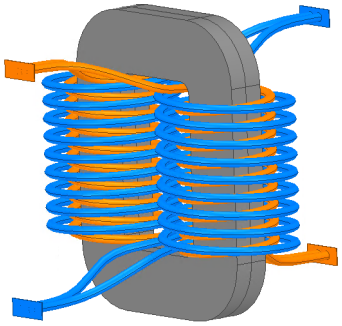


(a) Without decoupling capacitors



(b) With 90nF decoupling capacitors

Fig. 8. Double pusle test results of optimized PCB



(a) Parallel-concentric winding structure

(b) 100kW transformer with L_r/L_m=0.052%

Fig. 9. Fabricated 100 kW medium frequency transformer

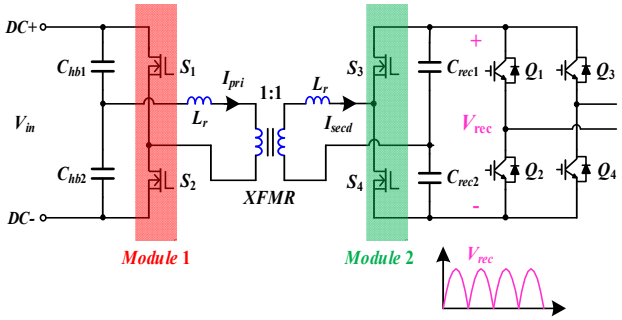
To verify the inhibition effect of the optimized PCB on the voltage overshoot, a double pulse test was performed at 1kV/255A. Fig. 8 shows the test results in which the maximum overshoot is 274V without decoupling capacitors and 110V with only 90nF decoupling capacitors. The optimized PCB busbar significantly reduced the overshoot voltage across devices.

V. Medium Frequency Transformer Design

TABLE III. Transformer Parameters

Item	Symbol	Value
Magnetizing inductance	L_m	4.2mH
Leakage inductance	L_δ	2.2uH
Turns ratio	N_p:N_s	9:9
DC insulation voltage	V_{PD_dc}	10kV
AC insulation voltage	V_{PD_ac}	4.3$kVrms$

Fig. 9 shows a 100kW medium frequency transformer (MFT) with a low loss magnetic core (FINEMET® FT-3TL). The parallel-concentric winding structure of the MFT increases the current carrying capability and reduces the leakage inductance to 2.2uH. To meet the insulation requirement for medium voltage applications, 10kVdc voltage and 4.3kVrms have been tested with total partial discharge < 50pC. Table III summarizes the parameters of the 100kW transformer.



(a) Dual active half bridge modular converter

(b) 100kW preliminary prototype

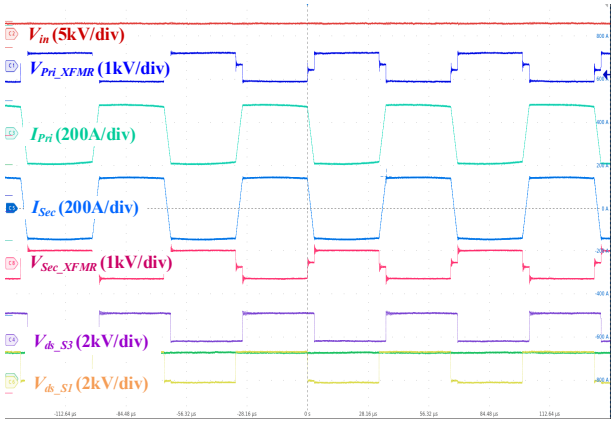
Fig. 10. Bidirectional isolated DAHB modular converter

VI. Circuit Configuration of The DAHB Modular Converter

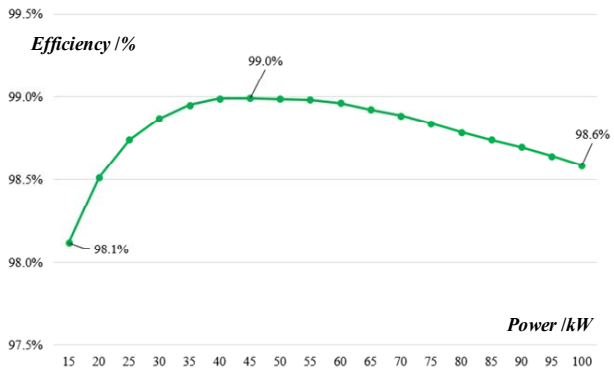
TABLE IV. DAHB Experimental Parameters

Item	Symbol	Value
Input voltage	V_{in}	800-1300V
Rated power	P_{rated}	100kW
Switching frequency	f_s	15-50kHz
Input capacitance	$C_{hb1,2}$	250uF
Output capacitance	$C_{rec1,2}$	10uF
External inductor	L_r	12.5uH
Dead time	T_d	700ns

Fig. 10 shows the circuit configuration and preliminary prototype of the DAHB modular converter. Wolfspeed's half bridge module HT-3234-R-VB has an ultra-low on resistance of 2.5$m\Omega$ @ 25°C and 5.25$m\Omega$ @ 175°C respectively. Low stray inductance (7nH), internal symmetric packaging and an external optimized PCB-based busbar design are conducive to achieve high efficiency and density. Related experimental parameters of the DAHB converter are tabulated in Table IV.



(a) Typical DC/DC test waveforms



(b) DC/DC efficiency curve, V_{in}=1300V

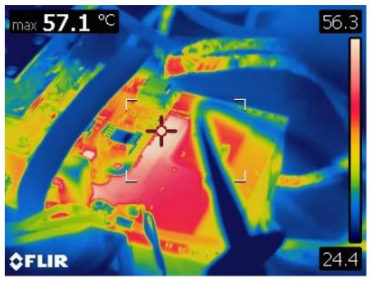
Fig. 11. 100kW DAHB modular converter DC/DC experiment

VII. Experimental Results

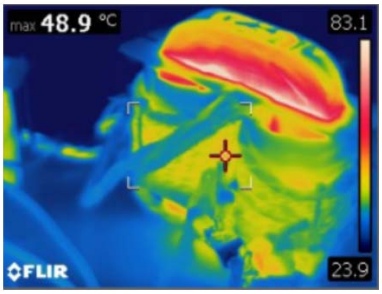
To verify the high efficiency and thermal capability of the 1300Vdc, 100kW bidirectional isolated DAHB modular converter using 1.7kV 400A all-silicon carbide half-bridge module, a DC/DC back-to-back recycling power test and DC/AC test with resistive load are conducted.

A. DC/DC back-to-back recycling test

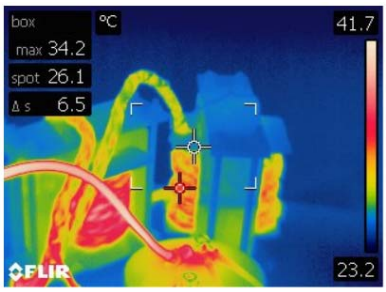
Fig. 12 shows the DC/DC experimental waveforms and efficiency curve with input voltage equals to 1300V. For DC/DC operation, the switching frequency is fixed at 15kHz. The maximum efficiency point is 99% at 45kW in a wide range from 10kW to 100kW. Thermal test results at rated 100 kW power are shown in the Fig. 13. The temperature rise on the PCB surface, transformer core & winding and external inductors are 32°C, 59°C and 17°C respectively at an ambient temperature of 25°C.



(a) Optimized PCB surface

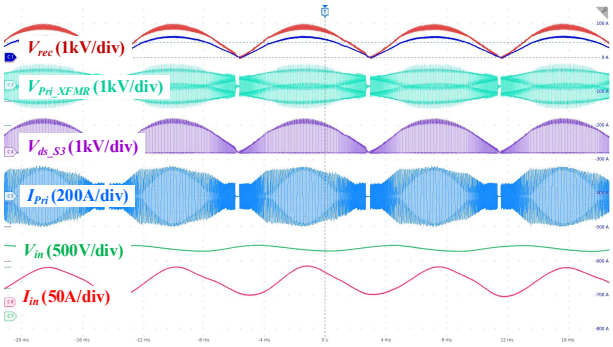


(b) Transformer core and winding

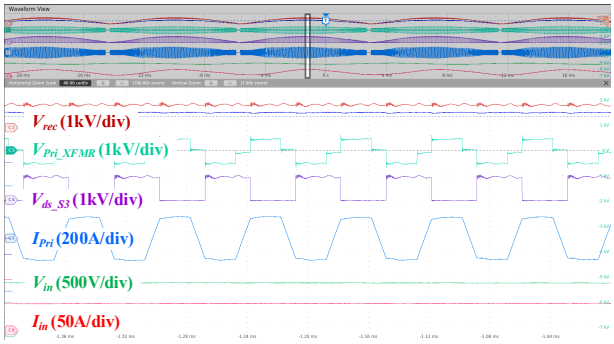


(b) External inductor

Fig. 12. 100kW DAHB modular converter thermal test results



(a) Typical DC/AC test waveforms



(b) Zoom in of typical DC/AC test waveforms

Fig. 13. 50kW DAHB modular converter DC/AC experiment

B. *DC/AC operation with load resistor*

Fig. 13 shows the DC/AC typical experimental waveforms. Note that with the limitation of the high-power load bank used, the maximum power that was tested now is 50kW and the maximum efficiency point is 97.8% at 35kW. For DC/AC operation, the switching frequency ranges from 15kHz to 50kHz. To achieve more efficient operation especially during zero current crossing, the maximum switching frequency was set to be 50kHz.

VIII. CONCLUSIONS

This paper highlights the design optimizations and complexities and demonstrates the feasibility of a 1.5kVdc, 100kW, variable frequency bidirectional isolated dual active half bridge modular converter using 1.7kV silicon carbide MOSFET module. The maximum efficiency point in DC/DC operation mode is 99% at 45kW and 98.6% at 100kW. The maximum achieved conversion efficiency for DC/AC operation mode is 97.8% at 35kW and 97.6% at 50kW. All power losses are measured by HOIKI PW6001 power analyzer excluding the gate driver and controller losses.

To achieve ZVS turn on over the full voltage range, especially for DC/AC operation mode, dynamic C_{oss}/Q_{oss} data was extracted and verified for the newly developed 1700V SiC MOSFET module. Lossless snubber capacitors were shown to be effective in increasing the efficiency for heavy load conditions but has a tradeoff with ZVS boundary at light loads. An optimized PCB-based busbar design has significantly reduced the voltage overshoot across devices. Typical partial discharge inception voltage (PDIV) of the optimized PCB busbar is 1.7kV peak with total partial discharge <10pC. Full power thermal testing has verified the long term operating reliability of the DAHB modular converter.

To meet the requirement of medium voltage applications, a 100kW medium frequency transformer (MFT) with a low loss magnetic core (FINEMET® FT-3TL) was also designed. The parallel-concentric winding structure of the MFT increases PDIV to 4.3kVrms with a total partial discharge <50pC and a significantly reduced leakage inductance.

The input-parallel-output-series (IPOS) configuration could be used to expand both voltage and power ratings for three phase medium voltage high power applications. Further study would be needed to address input current sharing issues and output multilevel voltage balancing control.

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REFERENCES

[1] S.B. Kjaer, J.K. Pedersen, F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," IEEE Transactions on Industry Applications, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005.

[2] Yang Chen, K.M. Smedley, "A cost-effective single-stage inverter with maximum power point tracking", IEEE Transactions on Power Electronics, vol. 19, no. 5, pp. 1289-1294, Sept. 2004.

[3] Liu Li, Yang Yin-tang, Chai Chang-chun, "Temperature dependence of breakdown in anisotropic 6H-SiC MOSFET", 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, Dec. 2008

[4] Bryce Aberg, Radha Sree Krishna Moorthy, et al., "Estimation and Minimization of Power Loop Inductance in 135 kW SiC Traction Inverter," IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1772-1777, March 2018.

[5] Yue Xu, et al., "Medium-Voltage SiC-based Converter Laminated Bus Insulation Design and Assessment," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7. No. 3, Sept. 2019.

[6] Alberto Rodríguez, et al., "Different Purpose Design Strategies and Techniques to Improve the Performance of a Dual Active Bridge With Phase-Shift Control," IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 790-804, Feb. 2015.

[7] Xiaoqing Song, A.Q. Huang, Mengjia Lee, Gangyao Wang, "A dynamic measurement method for parasitic capacitances of high voltage SiC MOSFETs," Energy Conversion Congress and Exposition (ECCE), pp. 935-941, Sept. 2015.

[8] Li Wang, Qianlai Zhu, Wensong Yu, Alex Q. Huang, "A Study of Dynamic High Voltage Output Charge Measurement for 15 kV SiC MOSFET", 2016 Energy Conversion Congress and Exposition (ECCE), Sept. 2016.