March 1996 • NREL/TP-413-20809

Light-Trapped, Interconnected, Silicon-Film™ Modules

Annual Subcontract Report 18 November 1994 - 18 November 1995

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D. H. Ford
AstroPower, Inc.
Newark, Delaware

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
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NREL technical monitor: H.S. Ullal

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1 INTRODUCTION

1.1 Project Overview

AstroPower is developing a module manufacturing technology based on a film-silicon technology. AstroPower, as a Technology Partner in the Thin-Film Partnership, will employ its Silicon-Film™ technology toward the development of an advanced thin-silicon-based, 400 watt, 4 ft x 8 ft (2.97 m^2) photovoltaic panel product for use in power applications. This module will combine the design and process features of the most advanced thin-silicon solar cells with light trapping. These solar cells will be integrated into a low-cost interconnected array.

This advanced product includes the following features:

- silicon layer grown on a low-cost substrate,
- a 50-micron thick silicon layer with greater than 100 micron diffusion lengths,
- light trapping due to back-surface reflection,
- back surface passivation,
- 900 cm^2 interconnected sub-module.

The 50-micron thick silicon layer achieves high solar cell performance and can lead to a sub-module conversion efficiency as high as 19%. These performance design features, combined with low-cost manufacturing using relatively low-cost capital equipment, continuous processing and a low-cost substrate, will lead to a panel cost of less than $1.00/watt.

The three year project involves five tasks and builds on present processes and capabilities. Tasks I and II are intended to increase module efficiency by optimizing the sub-module and sub-element material properties and structure. Tasks III and IV are intended to reduce the cost of module integration by improving the module fabrication processes and module efficiency, and understanding encapsulation and reliability issues. Task V is intended to improve the technical base supporting the manufacturability of the near-term product by developing prototype manufacturing processes. During the first year of the program, our efforts were focused on Tasks I and II.

1.2 Technical Approach

The solar cell sub-element device structure (Figure 1b) consists of a thin (35–50 μm) polycrystalline silicon layer which is grown on a low-cost substrate material. The thin layer/low-cost substrate approach results in lower cost by minimizing the use of relatively expensive silicon feedstock material. Diffusion lengths equivalent to twice the device thickness are required to assure high carrier collection throughout the bulk of the base layer, enabling the use of imperfect materials and increased doping levels for improved solar cell voltage and fill factor.

Thin films grown on an insulating substrate allow the fabrication of large-area, series-interconnected sub-modules (see Figure 1a) [1]. The sub-module design incorporates a method of partitioning the thin-film photovoltaic layer into sub-elements and reconnecting them as a series connected array. The sub-module design also incorporates conductivity enhancement to minimize the power loss associated with lateral current flow through the thin base layer.

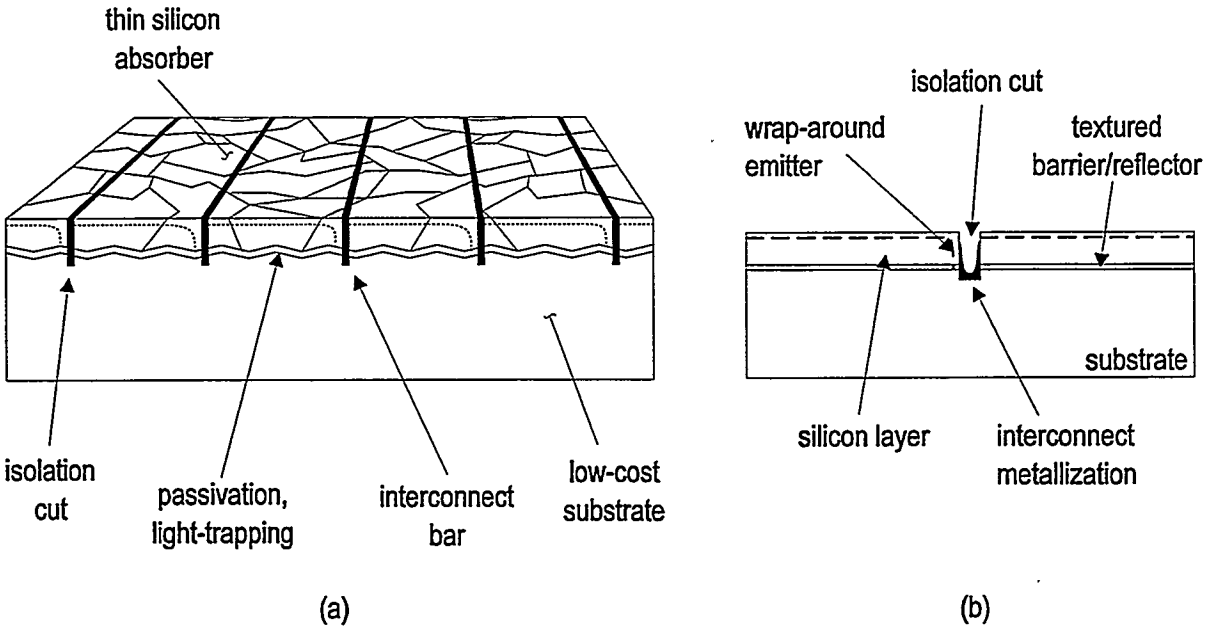


Figure 1. *(a) Solar cell sub-module device structure and (b) sub-element device structures.*

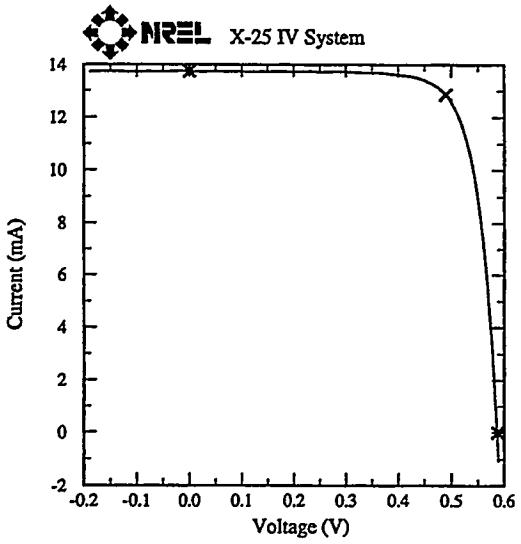
The solar cell device structure incorporates light trapping and back-surface passivation to improve energy conversion efficiency. Light trapping is achieved by using a diffuse reflector located at the back surface of the thin film, resulting in enhanced optical absorption of weakly absorbed light and improved current generation. Electrical passivation of the back surface is achieved by developing the barrier layer to minimize surface recombination velocity at the barrier/silicon interface. Back-surface passivation results in improved voltage and fill factor by minimizing the reverse saturation current.

Research and development efforts of the first year of the program focused on the first two tasks of the workplan: design of the sub-element and sub-module structures and development of key processes to improve conversion efficiency.

1.3 Key Results of First Year Program

The key results of the first year of this program are:

- a confirmed 12.2% efficient, thin solar cell fabricated on a low-cost substrate,
- demonstration of films grown on barrier-coated substrates which, after being subjected to a phosphorous gettering process, exhibited diffusion lengths greater than 250 μm,
- development of a new, low-cost substrate and barrier coating which supports the growth of thin film of silicon,
- demonstration of optical confinement in 60-μm thick films with 80 μm diffusion lengths.



Sample D-1#5	Jan. 25, 1996
ASTM E 892-87 Global	Area = 0.457 cm^2
V_{oc} = 0.587 V	V_{max} = 0.489 V
I_{sc} = 13.74 mA	I_{max} = 12.86 mA
J_{sc} = 30.09 mA/cm^2	P_{max} = 6.298 mW
Fill Factor = 78.1%	Eff = 13.8 %

Figure 2. *I-V characteristic of a thin-layer solar cell fabricated on a new barrier-coated substrate.*

A new barrier-coated substrate has been pivotal to the first year program. It has enabled, for the first time, diffusion lengths greater than the thickness of the device to be measured in low-cost films of silicon. This has led to a solar cell efficiency of 12.2% (confirmed at NREL; J_{sc} = 27.9 mA/cm^2, V_{oc} = 578 mV, FF = 75.5%, see Figure 2). This is the first efficiency greater than 12% achieved with a polycrystalline silicon grown by a low-cost process on a barrier-coated substrate. The following section summarizes the key results of the first year of this program.

2 TECHNICAL PROGRESS OF THE FIRST YEAR PROGRAM

2.1 New Barrier-Coated Substrate

Ceramic Substrates. Before the start of the program, ceramic materials were used as the substrate for thin layer growth. The barrier layer was developed primarily to prevent impurity

contamination of the silicon layer [2]. The contamination problem restricted silicon layer quality; minority carrier diffusion lengths were typically less than 10 μm, conversion efficiency was typically less than 7%. Up to the beginning of the program, efforts to develop the barrier were largely unsuccessful.

New Substrate and Barrier Layer. A new, low-cost substrate and barrier were developed during the first year of the program. Based on our experience with previous substrate materials, including steel [3], ceramic [4], and graphite cloth [5], a new substrate material was identified. The new substrate material has sufficient mechanical strength to support the silicon layer and has a well matched thermal coefficient of expansion. A barrier layer was then developed specifically for this substrate, which was successful in preventing chemical impurity contamination of the layer of silicon. This allowed good-quality silicon layers to be grown and conversion efficiencies exceeding 13% to be achieved.

2.2 Film Growth Development

Growth on New Barrier-Coated Substrate. Development of the silicon deposition process has proceeded with the new barrier-coated substrate. Our efforts were focused on increasing the grain size and reducing layer thickness to below 100 μm. Optimization of the growth conditions led to a significant increases in grain size. Layers as thin as 60 μm, with grains as large as 1 mm were achieved [6]. Figure 3 shows the typical cross-sectional morphology of these films.

Figure 3. *Cross-sectional morphology illustrating grain size and film thickness of silicon layers grown on the new barrier-coated substrate.*

Capping Layers. Capping layers were also evaluated. These layers were deposited over the precursor material before the growth process. The resulting films exhibited grain sizes approaching 400 μm. The capping layers were determined to be unnecessary.

Minority Carrier Diffusion Length. Silicon layers grown on the new barrier-coated substrate show remarkably improved minority carrier diffusion length. Films grown on barrier-

coated ceramic substrates typically exhibit diffusion lengths of less than 10 μm, and generally do not respond to post-growth treatments such as gettering or hydrogenation. Impurity contamination is reduced with the new barrier layer and substrate, resulting in diffusion lengths ranging between 20–40 μm in as-grown films. This represents a moderate improvement compared to films grown on ceramic substrates. However, external gettering with phosphorous has resulted in a further improvement in diffusion length.

The gettering process employed has been developed specifically for Product I wafers where bulk lifetime improvements have been demonstrated [7]. The process is carried out in a standard solid-state diffusion tube, in a $POCl_3/O_2$ ambient, at 890°C for 4 hours. Aluminum as an additional gettering agent was used on the front surface of some samples. After gettering, the heavily doped phosphorous region or aluminum-silicon alloyed region at the front surface is removed by etching in a 95:5::HNO_3:HF solution. Subsequently, solar cells are fabricated for testing and analysis.

The minority carrier diffusion length of the base layer is inferred from internal quantum efficiency (IQE) measurements in the wavelength range of 750 to 950 nm. The average diffusion length of devices processed with phosphorous gettering is greater than 100 μm with and without the aluminum layer on the front surface [8]. Recently, several devices have exhibited diffusion lengths greater than 250 μm (see Figure 4) without aluminum.

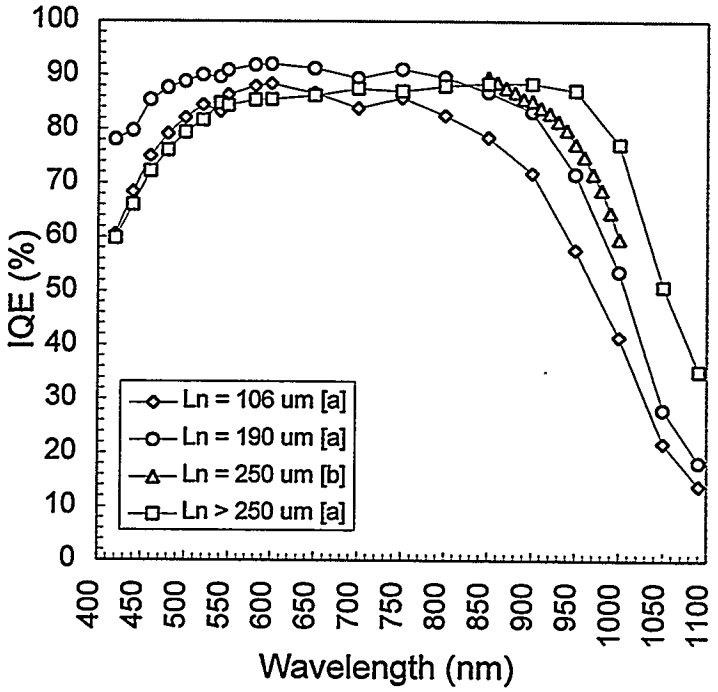


Figure 4. *IQE response of several solar cell devices ([a] Tested at AstroPower, [b] Tested at Georgia Institute of Technology).*

Local, Growth-Related Defects. Solar cell devices fabricated from material grown on the new barrier-coated substrate initially exhibited poor open-circuit voltage and poor fill factor. Figure 5 shows the I-V characteristics of two devices with this behavior: (1) the best solar cell of that lot (10.4 % efficient) and (2) a device with extremely poor open circuit voltage and fill factor. PC-1D modeling was used to analyze the I-V characteristics and determine the cause of poor I-V performance. Important material and solar cell parameters, such as base doping level, emitter sheet resistivity and minority carrier diffusion length were measured independently and used in the model. Series resistance, shunt conductance and J_{02} saturation current density were extracted by obtaining a close fit of the model I-V curve to the actual data. Figure 5 also shows the best fit obtained by PC-1D for each device. The extracted parameters are shown in Table 1.

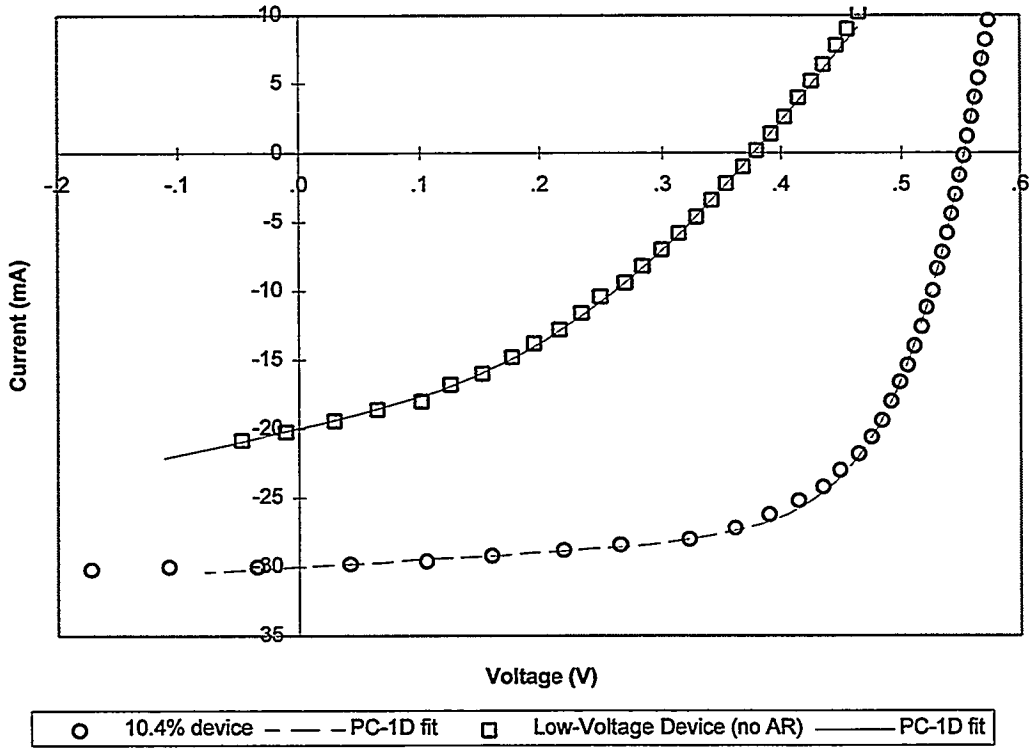


Figure 5. *Actual and modeled I-V characteristics of 0.5 cm^2 solar cell devices exhibiting poor open circuit voltage and poor fill factor.*

Table 1. *Extracted parameters for PC-1D model fit to recently fabricated solar cell devices.*

Cell ID	Voc (V)	Jsc (mA/cm2)	FF (%)	Series Resistance	Shunt Conductance	J_{02}
'10.4% Cell'	.552	29.9	63.2	1.0 $\Omega.cm^2$	5 mS	0.4 $\mu A/cm^2$
'Low-Voltage Cell	.455	19.8	30.5	7.0 $\Omega.cm^2$	20 mS	10 $\mu A/cm^2$

Gray I-V data were obtained on the '10.4 % cell' to independently determine the value of the J_{02} saturation current density. Open circuit voltage is plotted against short circuit current for various incident optical intensities in Figure 6. The linear portion of the plot near one-sun

conditions is described by a slope of n=1.94 and an intercept of 0.9 $\mu A/cm^2$, very close to the value extracted by the PC-1D modeling. From the plot of Figure 6, it is clear that, at one-sun operating conditions, the I-V characteristics, particularly open circuit voltage and fill factor, are dominated by a J_{02}-like saturation current density.

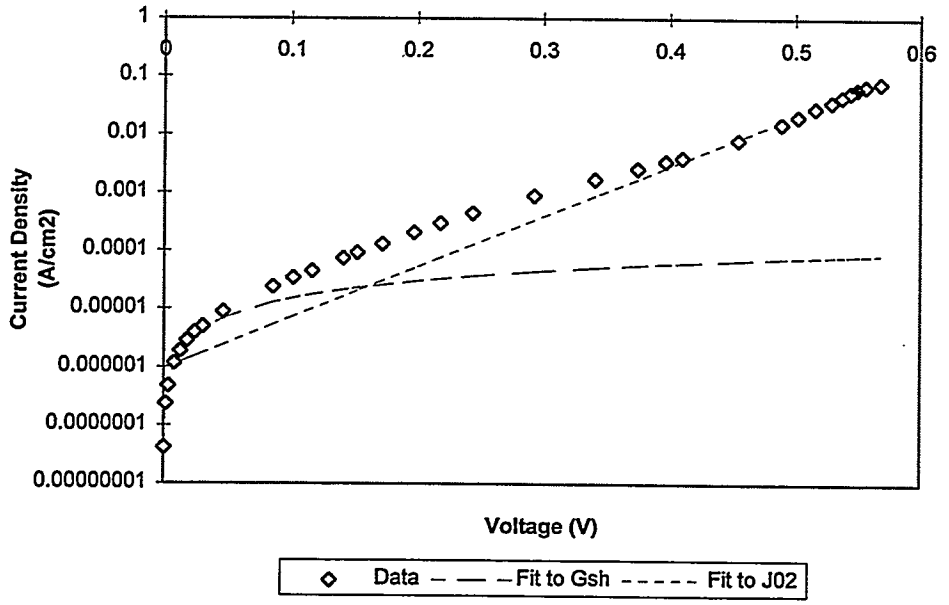


Figure 6. *Gray I-V data of the '10.4% Cell' with best fit lines to G_{sh} and J_{02}. The one-sun V_{oc}-I_{sc} pair is marked by a '+' symbol.*

A localized defect was suspected as the cause of the poor solar cell performance described above. The 'low-voltage cell' characterized in Figure 5 was cut into eight smaller section and each section was tested individually. A composite of the eight I-V characteristics is shown in Figure 7. Table 2 summarizes the key data points along these I-V curves and compares them with data taken before the device was cut.

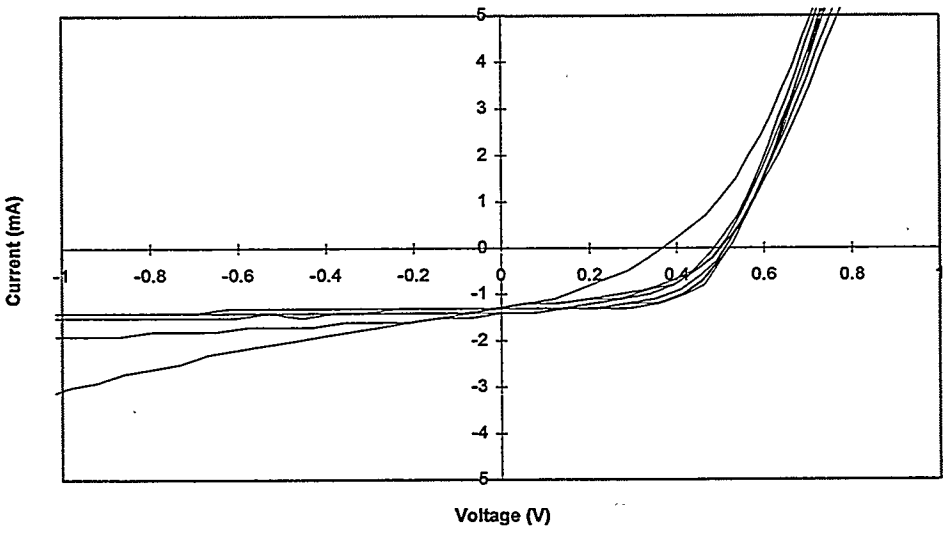


Figure 7. *Composite of eight I-V curves representing the response of eight sections of the 'low-voltage cell'.*

Table 2. *Key I-V parameters of the curves presented in Figure 7.*

Cell ID	Voc (mV)	Jsc (mA/cm^2)	FF (%)
segment 1	495	17.0	52.8
segment 2	503	17.4	47.9
segment 3	511	18.9	55.9
segment 4	515	18.2	59.7
segment 5	372	18.2	32.5
segment 6	519	18.7	60.1
segment 7	489	19.8	43.7
segment 8	523	18.4	62.6
'Low-Voltage Cell' whole	504	18.4	51.7

It is clear that a few segments limit the overall performance of the solar cell, in this case segment 5 and segment 7. Therefore, we concluded that a localized defect due to the growth process was limiting voltage and fill factor in solar cell devices. A post-growth heat treatment was incorporated into the processing, effectively solving this problem. This process removes the local shunt-like defect, greatly improving solar cell performance, especially open circuit voltage and fill factor.

2.3 Sub-Element Design Issues

The material development efforts led to improved material quality. Therefore an effort was undertaken to design a solar cell geometry and contact pattern specifically for thin layers.

Since the substrate and barrier are electrically insulating, special consideration to current conduction through the base layer is required. In this structure, electrical contact to the base layer is not possible through the substrate, and therefore, it is made on the top surface along the perimeter of the active device area. Current must flow laterally through the relatively thin base layer (50–100 μm thick) to reach the base contact. This introduces a potentially high series resistance and potentially poor fill factor. Figure 8 shows a schematic of the contact scheme used for device fabrication.

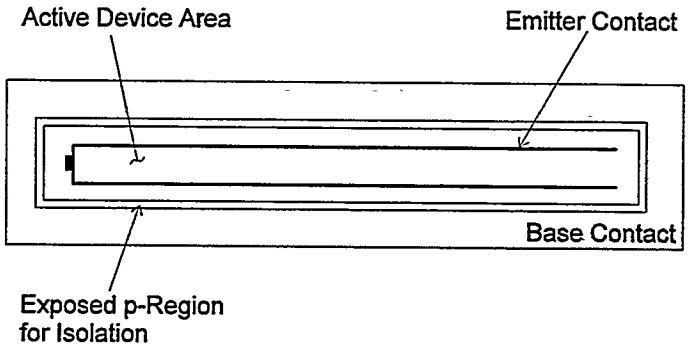


Figure 8. *Solar cell geometry and contact pattern currently used for device fabrication.*

A spreadsheet model was developed which considers solar cell designs based on base electrical contacts located on the top surface. The model incorporates the power loss to resistive effects and shading due to the emitter grid structure. Typical input parameters to the model are listed in Table 3.

Table 3. *Key Process Parameter Variables:*

Variable Name	Description	Typical Value	Units
A	cell area	1.0	cm^2
L	length of cell (long dimension)	1–10	cm
J_{mp}	max. power current density	2.50E-02	A/cm^2
V_{mp}	max. power voltage	0.55	V
t_b	thickness of base	1.00E-02	cm
ρ_b	resistivity of base	1	ohm-cm
t_e	thickness of emitter	5.00E-05	cm
ρ_e	resistivity of emitter	0.0025	ohm-cm
t_g	thickness of gridlines	1.00E-03	cm
ρ_g	resistivity of gridlines	1.00E-06	ohm-cm
N	number of gridlines	1–10	
w_g	width of gridline	7.50E-03	cm
w_b	width of busline	5.00E-03	cm

Equations developed to model resistive and optical losses are shown below.

Base layer resistive losses:

$$P_{loss} = \frac{1}{24} J_{mp}^2 \frac{\rho_b}{t_b} \frac{A^3}{L^4} \left(2L^2 - A\right)$$

Emitter layer resistive losses:

$$P_{loss} = \frac{1}{12} \frac{A^3}{N^2 L^2} J_{mp}^2 \frac{\rho_e}{t_e}$$

Gridlines resistive losses:

$$P_{loss} = \frac{LA^2}{N} J_{mp}^2 \frac{\rho_g}{w_g t_g}$$

Shading losses:

$$P_{loss} = \left(Lw_g N + \frac{A}{L} w_b \right) J_{mp} V_{mp}$$

The model can be used to determine the optimum length and width aspect ratio and the optimum number of emitter gridlines for any size of solar cell. Figure 9 shows the predicted power loss as a percentage of total power available for a 1.0 cm^2 solar cell. A photolithographic mask set was constructed with final dimensions of 0.27 cm by 2.1 cm (0.57 cm^2) and included two gridlines for the emitter and a contact pad for testing. Predicted total resistive and optical loss for this mask set is about 4.0%.

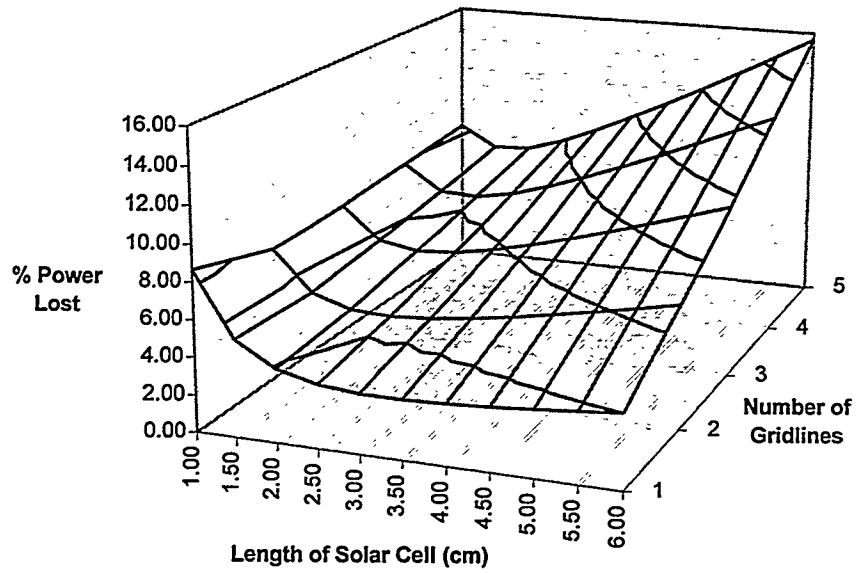


Figure 9. *Illustration of modeling results used to design a new photolithographic mask set. Percentage of power lost is predicted given the length and number of emitter gridlines for a total solar cell area of, in this case, 1.0 cm^2.*

2.4 Sub-Element Process Development

A solar cell fabrication sequence was developed specifically for the thin-film material. The process is very similar to standard high-efficiency polycrystalline silicon solar cell processes, including phosphorous gettering, emitter etchback after diffusion, emitter passivation by PECVD oxide deposition, evaporated contacts, and double layer anti-reflection coating. The baseline fabrication sequence is outlined in Table 4.

Table 4. *Solar Cell Fabrication Process*

Process Step	Process Details
Sample clean:	-Chemical polish (90:10::HNO_3:HF) ~ 10–15 min. -Organics etch (1:1::H_2SO_4:H_2O_2) 10 min. -Heavy metals etch (1:1::HCl:H_2O_2) 10 min. -Oxide strip (20:1::H_2O:HF) until hydrophobic *each step followed by DI water rinse
Getter:	-Steam clean tube with DI water; clean boat in 20:1::H_2O:HF -Push samples (890°C) flowing N_2 ~7–8 min. -Purge with N_2 15 min. -Getter for 2 hours @ 7:5::O_2:$POCl_3$ -Cool to <800°C in O_2, then pull ~7–8 min.
Sample clean:	-Repeat clean as above
Phosphorous Diffusion:	-Steam clean tube with DI water; clean boat in 20:1::H_2O:HF -Push samples (850°C) flowing N_2 ~7–8 min. -Purge with N_2 15 min. -Pre-deposition 7 min. @ 2:1::O_2:$POCl_3$ -Purge with N_2 15 min. -Oxidation in O_2 50 min. -Switch from O_2 to forming gas (5% H_2/balance N_2), 15 min. -Turn furnace off, continuing to flow forming gas, anneal samples until furnace temperature is ≤ 300°C (several hours).
H+:	-Oxide strip (20:1::H_2O:HF), brief DI water rinse -RF hydrogenation 40 min. (300°C)
Damage etchback:	-Oxide strip, DI water rinse -Etchback (1000:100:1::HNO_3:H_2O:HF) for 1 min. intervals checking sheet resistivity to final sheet resistivity of 60–70Ω/sq. (~ 2–3 min.), DI water rinse
Emitter Isolation	-Photolithography to define active device area -Plasma etch isolate (~ 5–10 min.) -Remove photoresist in acetone followed by methanol, DI water rinse
Emitter passivation:	-Oxide strip, DI rinse -Deposit 100Å CVD oxide n=1.47 (300°C) -CVD oxide anneal, 30 min. in forming gas (400°C)
Base Contact	-Photolithography to define base contact -Evaporate 5000Å aluminum, liftoff in acetone, followed by methanol, DI water rinse -Alloy contacts 1 min. (525°C)
Emitter Contact	-Photolithography to define emitter contact with overlap on base contact -Evaporate Ti/Pd/Ag (500/500/500Å) -Liftoff in acetone, followed by methanol, DI rinse
Silver Plate Up and Sinter	-Ag plate contacts to 10 μm thickness -Sinter contacts 1 min. (425°C)
Anti-Reflection Coating	-Deposit MgF/ZnS double layer AR coating

These processes were developed over a series of four device fabrication runs. Several options were identified for the optimization of the solar cell fabrication process: thermal vs. PECVD oxide passivation for the emitter, optimized base doping level, hydrogen ion implantation and improved base contact firing sequence. Figure 10 shows the progress made in best solar cell efficiency during the course of the first year of the program. The key developments responsible for efficiency improvement are indicated on the chart.

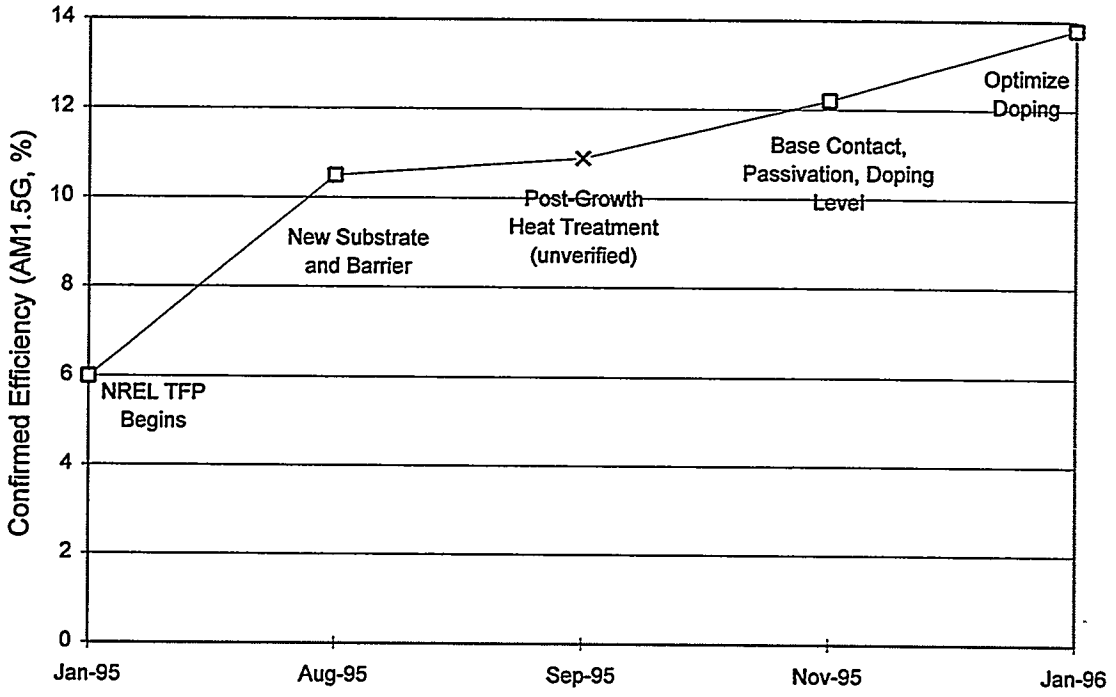


Figure 10. *Progress of best efficiency solar cells during the first year and the key process developments responsible for efficiency improvement (verified at NREL unless noted).*

Run #1. The base line process described in [1] was used initially with provision made for the top-side base contact. A baseline highest efficiency of 10.5% (AM1.5G, NREL) was established.

Run #2. From the post-fabrication analysis of the devices of Run #1, it became apparent that a local shunt-like mechanism was severely limiting device performance. Although short circuit current was reasonably high (average of > 19 mA/cm^2, no AR), open circuit voltage and fill factor were lower than expected, as described in Section 2.2 This analysis led to the use of a post-growth heat treatment step. Voltage and fill factor improved substantially. The limiting factor for voltage became the saturation current density due to low base doping level (~ 1–5x10^{15} cm^{-3}), and the limit to fill factor became series resistance.

The highest efficiency achieved in this run was 10.9 % (AM1.5G, unverified).

Run #3. Several changes were made to the process to improve open circuit voltage and short circuit current. Base doping level was increased by a factor of 10. The target doping level was $2x10^{16}$ cm^{-3}. Doping levels between $1.4x10^{16}$ and $1.8x10^{16}$ cm^{-3} were achieved. Open circuit voltage improved substantially.

The doping level was also increased to lower the sheet resistivity of the base layer, which, as determined by the model developed during the first year program, was the largest contributor to the series resistance. This resulted in a dramatic improvement in fill factor.

PECVD and thermal oxidation were compared to determine how to improve the emitter surface passivation and gain a better short-wavelength quantum efficiency. However, the response was not improved for either method of passivation.

The highest efficiency achieved in this run was 12.2 % (AM1.5G, NREL).

Run #4. This run repeated Run #3 in most respects, however, the amount of dopant added to the precursor material was lowered by 20% in an effort to further improve short circuit current density. Also, a plasma-enhanced hydrogen implantation step was added to improve device performance. The net effect of these two processes was a drop in average short-circuit current by about 1 mA/cm^2. This is most likely due to a reduction in short-wavelength quantum efficiency response caused by the hydrogen implantation sequence.

The highest efficiency achieved in this run was 13.8 % (AM1.5G, NREL).

Table 5 shows improvements in average figures for these four device fabrication runs. Figures 11–13 show the improvements in the key I-V characteristics for the four device fabrication runs described above.

Table 5. *Average values of open circuit voltage, short circuit current and fill factor for four fabrication runs performed during the first year program.*

	Run #1	Run #2	Run #3	Run #4
Open Circuit Voltage	454	479	566	559
Short Circuit Current	19.4	17.8	19.6	18.5
Fill Factor	42.5	51.2	66.3	68.1

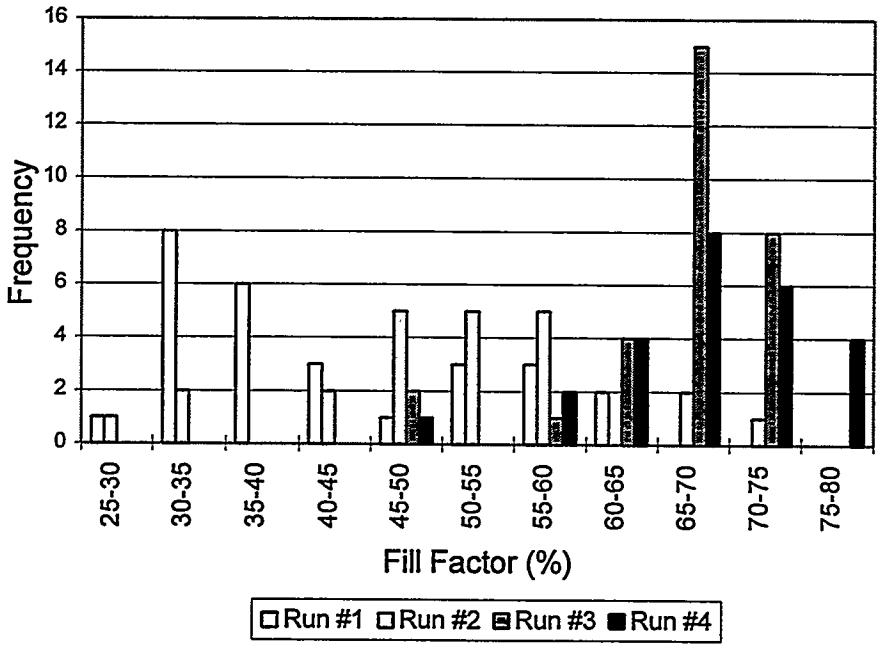


Figure 11. *Histogram of fill factor for four device fabrication runs performed during the first year program.*

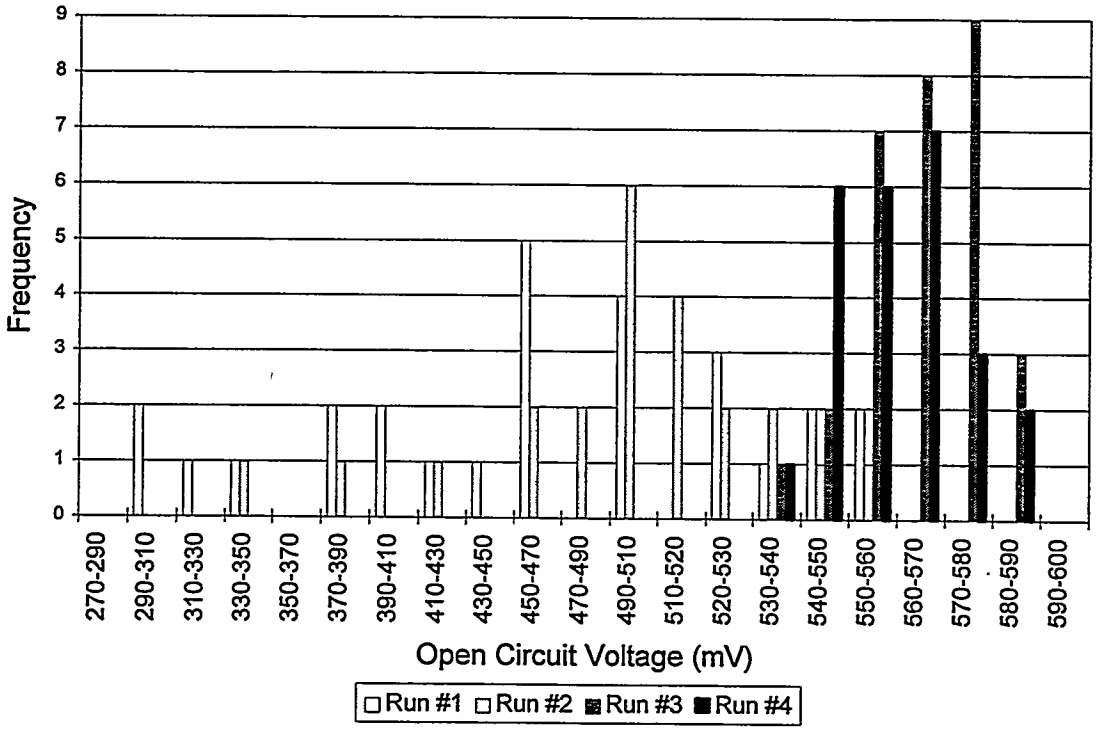


Figure 12. *Histogram of open circuit voltage for four device fabrication runs performed during the first year program.*

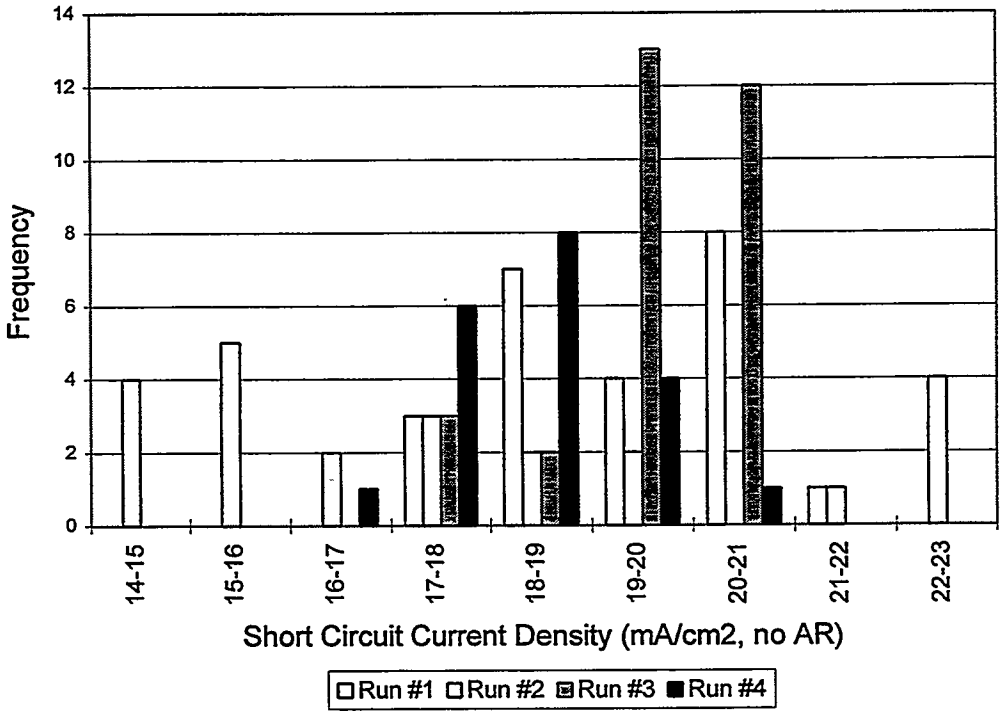


Figure 13. *Histogram of short circuit current before AR coating for four device fabrication runs performed during the first year program.*

2.5 Other Sub-Element Fabrication Results

Light-Trapping. The measured effective diffusion lengths in several small-area test devices approached half the device thickness. Diffusion lengths of this size prompted a more detailed investigation of light trapping properties.

Rand and Basore (3) have presented a quantitative technique for characterizing the light trapping effectiveness of thin photovoltaic layers with reflecting back surfaces. The reflectance and spectral response of weakly absorbed, near-bandgap light can be analyzed to determine the reflectance of the back surface and the effective optical path length of near-bandgap light. The reflectance, external quantum efficiency, and internal quantum efficiency of a small-area (approx. 0.2 cm^2) test device (60 μm thick) fabricated from a thin film of silicon grown on the new substrate material is shown in Figure 14.

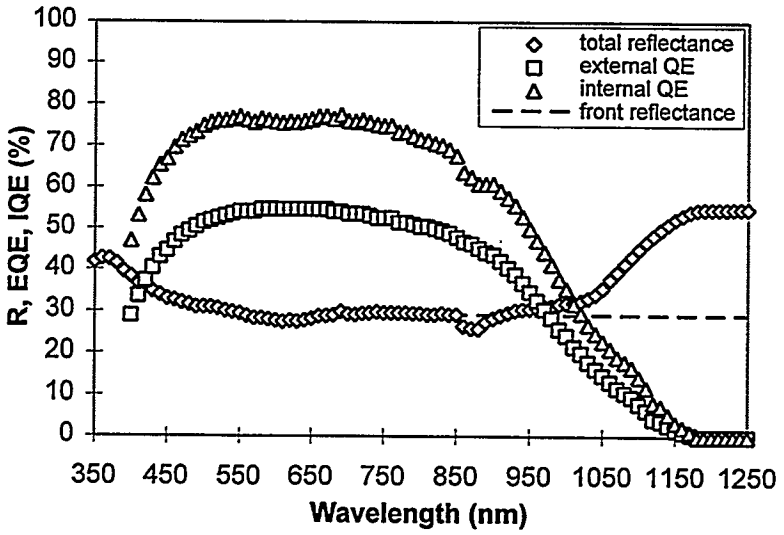


Figure 14. *Reflectance, external quantum efficiency, and internal quantum efficiency of a small area test device. The boost in reflectance above 1050 nm is due to reflection from the barrier layer. Front reflectance for sub-bandgap light is estimated from data in the 750–850 nm range.*

Analysis of these data by examination of inverse internal quantum efficiency versus inverse absorption is shown in Figure 15. From the inverse slope of a best fit line for short wavelength light (750 to 980 nm), a diffusion length of 82 μm is calculated. From the inverse slope of the best fit line for long wavelength light (1050 to 1100 nm), an effective optical thickness of 570 μm and corresponding effective optical path length, Z, of approximately 20 is calculated. Furthermore, the reflectivity of the barrier layer to weakly absorbed light is calculated to be 29% or greater.

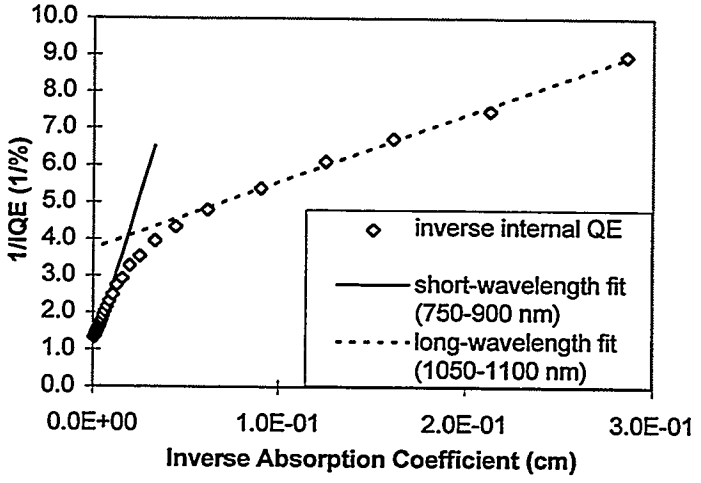


Figure 15. *Inverse internal quantum efficiency versus inverse absorption coefficient. The internal quantum efficiency is calculated from the estimated front reflectance of Figure 14.*

The sample under study had a textured front surface and was randomly textured at the barrier. This texturing led to a significant portion of the light being internally reflected at oblique angles to produce an optical path length much greater than the device thickness. A combination of a relatively low back surface reflection (≤ 29%) and low back-surface passivation lowered the overall collection efficiency of near-bandgap light to 28%.

2.6 Module Manufacturing Technology

Module Fabrication Technology. AstroPower has in place a module manufacturing facility with a capacity greater than 4 MW/year. Modules are fabricated with single crystal silicon and Silicon-Film™ Product I solar cells. Module power levels range from 80 to 120 watts for the different products.

The technology used in module fabrication is the same for both single crystal and Product I, and follows the conventional industry standards. . Solar cells are tabbed with solder coated copper strapping. Soldering is done in automated stringing equipment. Strings of solar cells are laminated to a tempered glass superstrate with EVA. A tedlar back sheet is included in the lamination. The leads are brought out through the tedlar backing and a junction box is attached. Aluminum framing is used to protect the edges.

The existing Silicon-Film™ module product uses solar cells that are 240 cm^2 in size. Prototype modules have been fabricated with solar cells 700 cm^2 in size. This was accomplished by a straight-forward extension of the existing tabbing technology. Such technology will be used to fabricate modules for this program.

Commercial-Scale Substrates. A prototype manufacturing process for the production of nominally 15 cm-wide barrier-coated substrates has been designed. The design includes the capability for fabricating the base substrate and the means to incorporate the requirements for a metallurgical barrier, and the light-trapping and back-surface passivation features. The design of the contact scheme will depend on the details of the device structure, several components of which are presently under active development. This has not been completed. Some of the preparation processes under active development are accomplished during substrate fabrication, others during subsequent processing. The prototype process design includes these. The process development approach, and accordingly the prototype process design, has been to divide the requirements between the substrate and barrier layer, with the substrate providing the mechanical strength, thermal expansion matching properties and electrical conductivity; and the barrier layer providing good conditions for film growth, a high degree of diffuse reflectivity, and good passivation at the back surface.

The process for fabricating 15 cm-wide substrates has already been demonstrated, employing a modified version of the manufacturing method presently being utilized for a fabrication step of the Silicon-Film™ Product I wafers. The process has been modified to yield an in-situ layer that, in combination with a second layer, provides for the metallurgical requirements, and accomplishes a degree of light-trapping as well.

Key Elements Of Commercial-Scale Silicon-Film™ Sub-Module. A prototype manufacturing process for the production of the key active elements on the nominally 15 cm-wide Silicon-Film™ substrates developed in Subtask 5.1 has been designed. The design includes the capability for depositing, growing and preparing 50-micron thick films of silicon. There are several processes under active development for preparing the silicon layers, all of which have demonstrated the capability to achieve the production rates required for low-cost manufacturing. A detailed design of the prototype manufacturing process will await the selection from those methods presently under examination. Critical to the selection will be the best practical device performance.

3 SUMMARY AND SECOND-YEAR OBJECTIVES

The first-year program was very successful, and all technical milestones and deliverables were completed. A new barrier-coated substrate has enabled, for the first time, the growth of high-quality thin-layer polycrystalline silicon to be grown on a low-cost substrate. High diffusion lengths have been measured after external phosphorous gettering. This has led to a confirmed 12.2% efficiency for a 0.57 cm^2, thin-layer solar cell grown on a low-cost substrate.

The second-year program will focus on the development of the substrate for light-trapping and passivation properties. Although light-trapping has been observed in silicon layers grown on the new barrier-coated substrate, it has not been optimized for such. Conversion efficiencies exceeding 15% are expected as the properties of the substrate is further developed. A second area of focus will be the development of the basic fabrication technologies related to the formation of the monolithically integrated sub-module. This includes techniques for sub-element isolation, interconnection, and conductivity enhancement. Finally, manufacturing technologies will be adopted or developed for key fabrication processes.

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R.B. Hall, J.A. Rand, J.E. Cotter, D.H. Ford

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AstroPower, Inc.
Solar Park
Newark, Delaware 19716-2000

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13. ABSTRACT *(Maximum 200 words)*

This report describes the first year of work performed by AstroPower, Inc., of Newark, Delaware, under the Thin-Film PV Partnership Program. The work led to the development of a new barrier-coated substrate that has enabled high-quality thin-layer polycrystalline silicon to be grown on a low-cost substrate. High diffusion lengths were measured after external phosphorous gettering. This led to a confirmed 12.2% efficiency for a 0.57cm^2, thin-layer solar cell grown on a low-cost substrate.

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